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(54) **Title**: POWER SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURE WITH CHARGE TRAPPING MATERIAL IN THE GATE DIELECTRIC

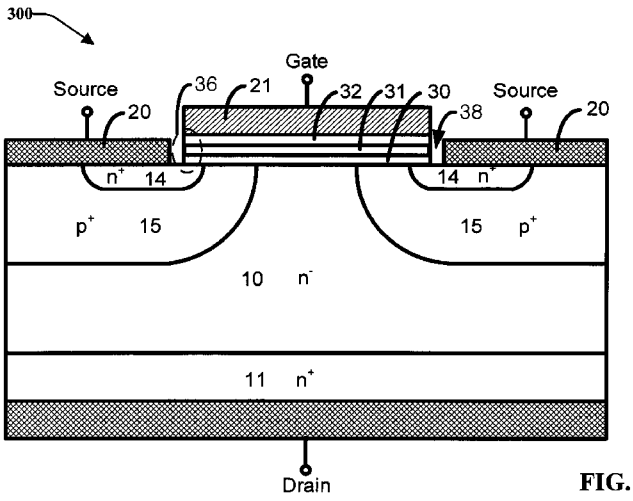

FIG. 3

(57) **Abstract**: The subject disclosure presents power semiconductor devices, and methods for manufacture thereof, with improved ruggedness. In an aspect, the power semiconductor devices are power field effect transistors (FETs) having enhanced suppression of the activation of the parasitic bipolar junction transistor (BJT) and a normal threshold value. The devices comprise a doped source (14) of a first conductivity type, a doped body (15) of a second conductivity type, a source electrode (20) short-connecting the doped body (15) and the doped source (14), a doped drift region (10) of the first conductivity type, a first layer (30) of a gate dielectric region (36) covering the surface of the doped drift region (10), and forming channel from the doped source (14) to the doped drift region (10), a second layer (31) of the gate dielectric region (36) over the first layer (30), a third layer (32) of the gate dielectric region (36) over the second layer (31), and a gate electrode (21) over the third layer (32).

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POWER SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURE WITH CHARGE TRAPPING MATERIAL IN THE GATE DIELECTRIC

PRIORITY CLAIM

[0001] This application claims priority to U.S. Provisional Patent Application Serial No. 61/457,067 filed on December 20, 2010, entitled "POWER SEMICONDUCTOR FIELD EFFECT TRANSISTOR STRUCTURES WITH CHARGE TRAPPING MATERIAL IN THE GATE DIELECTRIC." The entirety of the aforementioned application is incorporated by reference herein.

TECHNICAL FIELD

[0002] This disclosure relates generally to power device structures, e.g., to power field effect transistor (FET) structures with heavily doped body and charge trapping material in the gate dielectric.

BACKGROUND

[0003] Field effect transistors, such as n-channel power metal-oxide-semiconductor field effect transistors (MOSFETs), are generally desired to have low conduction and switching losses in many power applications. Field effect transistors should also be rugged enough to prevent the parasitic bipolar junction transistor from turning on under high current conditions, such as unclamped inductive switching (UIS). The failure of MOSFETs during UIS is due to activation of the parasitic NPN bipolar transistor in breakdown mode.

[0004] The parasitic NPN bipolar junction transistor (BJT) in the power MOSFET is composed of the n+-source, p-body and n--drift, and these three regions also act as the emitter, base and collector of the parasitic bipolar junction transistor, respectively. The p-body is connected to the source electrode through a p+ region, and the n+-source/p-body junction is shorted at the source electrode of the device. The n+-source/p-body junction will not be forward biased at the static on-state or off-state of the power MOSFET. However, under transient conditions such as avalanche operation of the power MOSFET, reverse recovering of the body diode and fast rising of drain-to-source voltage, current will flow through the p-body

to the source electrode. This will cause a potential drop across the resistance of the p-body. If the current flow is large enough and the potential drop is significantly high enough, the n+-source/p-body junction will be forward biased, and the parasitic bipolar junction transistor will be activated. The activation of the parasitic bipolar junction transistor will cause a second-breakdown behavior of the power MOSFET, and thermal runaway can also result.

[0005] The above-described deficiencies of conventional field effect transistors are merely intended to provide an overview of some of problems of current technology, and are not intended to be exhaustive. Other problems with the state of the art, and corresponding benefits of some of the various non-limiting embodiments described herein, may become further apparent upon review of the following detailed description.

SUMMARY

[0006] The following presents a simplified summary to provide a basic understanding of some aspects described herein. This summary is not an extensive overview of the disclosed subject matter. It is not intended to identify key or critical elements of the disclosed subject matter, or delineate the scope of the subject disclosure. Its sole purpose is to present some concepts of the disclosed subject matter in a simplified form as a prelude to the more detailed description presented later.

[0007] To correct for the above noted deficiencies of conventional field effect transistors, provided are field effect transistors, and methods for manufacturing field effect transistors, with heavily doped body (p+-body) and normal threshold voltage. In an aspect, provided is a power semiconductor field effect transistor structure comprising a doped body of a second conductivity type, a source electrode short-connecting the body and the doped source, a doped drift region of the first conductivity type, a first layer of a gate dielectric region covering the surface of the doped body and forming channel from the doped source to the doped drift region, a second layer of the gate dielectric region on top of the first layer, a third layer of the gate dielectric region on top of the second layer, and a gate electrode on top of the third layer. In an aspect, the doped source and the doped body are formed by high dose ion-implantation and annealing. Further, in an aspect, the doped body forms direct contact to the source electrode, and the second layer of the gate dielectric is a charge trapping material.

[0008] In another embodiment, provided is a method for fabricating a power semiconductor field effect transistor structure comprising: forming a doped drift region of a first conductivity type, forming a gate stack over the doped drift region, including, forming a first gate dielectric layer, forming a second gate dielectric layer on top of the first gate dielectric layer, forming a third gate dielectric layer on top of the second gate dielectric layer, deposing a gate electrode on the third gate dielectric layer, and patterning the gate electrode and the gate dielectric layers, forming a doped body of a second conductivity type in the doped drift region, forming a doped source of the first conductivity type in the doped body, wherein the first gate dielectric layer covers a surface of the body and forms a channel from the doped source to the doped drift region, forming a contact hole adjacent to the gate stack, and forming a source electrode above the doped source and the doped body, wherein source electrode short connects the doped body and the doped source. In an aspect, the forming the doped source includes forming the doped source by high dose ion-implantation and annealing, and the forming the doped body includes forming the doped body by high dose ion-implantation and annealing. In addition, in an aspect, the second gate dielectric layer is a charge trapping material.

[0009] The following description and the annexed drawings set forth in detail certain illustrative aspects of the disclosed subject matter. These aspects are indicative, however, of but a few of the various ways in which the principles of the various embodiments may be employed. The disclosed subject matter is intended to include all such aspects and their equivalents. Other advantages and distinctive features of the disclosed subject matter will become apparent from the following detailed description of the various embodiments when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Non-limiting and non-exhaustive embodiments of the subject disclosure are described with reference to the following figures, wherein like reference numerals refer to like parts throughout the various views unless otherwise specified.

[0011] FIG. 1 presents a cross-sectional view of a prior art structure of a commonly used power metal-oxide-semiconductor field effect transistor (MOSFET).

[0012] FIG. 2 presents a cross-sectional view of prior art structure of a power n-channel

power MOSFET with an optimized doping profile of the p-body.

[0013] FIG. 3 presents a cross-sectional view of a field effect transistor embodied as a power MOSFET in accordance with an embodiment.

[0014] FIG. 4 presents a cross-sectional view of the formation of the drift region accordance with an embodiment.

[0015] FIG. 5 presents a cross-sectional view of the formation of the charge trapping layers in accordance with an embodiment.

[0016] FIG. 6 presents a cross-sectional view of the formation of the gate electrode accordance with an embodiment.

[0017] FIG. 7 presents a cross-sectional view of the formation of the doped body in accordance with an embodiment.

[0018] FIG. 8 presents a cross-sectional view of the formation of the doped source in accordance with an embodiment.

[0019] FIG. 9 presents a cross-sectional view of the formation of the contact hole in accordance with an embodiment.

[0020] FIG. 10 presents a cross-sectional view of the formation of the source electrode in accordance with an embodiment.

[0021] FIG. 11 presents a cross-sectional view of a field effect transistor embodied as an IGBT in accordance with an embodiment.

[0022] FIG. 12 presents a cross-sectional view of an insulated-gate bipolar transistor (IGBT) in accordance with an embodiment.

[0023] FIG. 13 presents a non-limiting flow diagram of a method for fabricating an FET in accordance with an embodiment.

[0024] FIG. 14 presents a non-limiting flow diagram of a method for fabricating an FET in accordance with another embodiment.

[0025] FIG. 15 presents a graph depicting the experimental transfer characteristics of a power MOSFET in accordance with an embodiment.

[0026] FIG. 16 presents a graph depicting the experimental I_{DS}-V_{DS} characteristics of the power MOSFET with a programmed threshold voltage as shown previously in FIG. 15.

DETAILED DESCRIPTION

[0027] Various aspects or features of this disclosure are described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In this specification, numerous specific details are set forth in order to provide a thorough understanding of the subject disclosure. It should be understood, however, that the certain aspects of disclosure may be practiced without these specific details, or with other methods, components, materials, *etc.* In other instances, well-known structures and devices are shown in block diagram form to facilitate describing the subject disclosure.

[0028] By way of introduction, the subject matter disclosed herein relates to a power field effect transistor (FET) with a heavily doped (between $1x10^{18}cm^{-3}$ and $1x10^{20}cm^{-3}$) body (p+-body) and a normal threshold voltage. Embodiments of the subject application thus provide a FET with a heavily doped body (p+-body) and a charge trapping material in the gate dielectric. In order to avoid activation of the parasitic bipolar junction transistor, as discussed in the background, in various embodiments, the resistance of the p-body is reduced by heavy doping. However, the doping concentration of the p-body also determines the threshold voltage of the device. As a result, when the p-body is heavily doped, the power MOSFET may have too high of a threshold voltage, and thus various embodiments described herein address these and other issues.

[0029] With the subject embodiments of a FET, the base resistance of the parasitic bipolar junction transistor (BJT) is significantly reduced because of the high doping concentration (between $1x10^{18}cm^{-3}$ and $1x10^{20}cm^{-3}$) of the p+-body. The high doping concentration of the p+-body also causes a positive shift of the threshold voltage of the power FET. However, the positive shift of the threshold voltage is compensated by the positive fixed charges created in the charge trapping material of the gate dielectric. As a result of the compensation, the threshold voltage of the FET device is kept at a normal value. The normal value is typically between 1 V and 3 V for devices with a breakdown voltage below 100 V, and between 2 V and 4 V for devices with a breakdown voltage above 100 V. Moreover, the p+-body can form ohmic contact directly with the source electrode. The fabrication process of the subject FET is thus simplified in comparison to conventional FET's which require a p+ region for connection to the source electrode.

[0030] The various embodiments of the subject FET improve ruggedness due to the suppression of the activation of the parasitic bipolar junction transistor under transient conditions. Moreover, the threshold voltage of the subject FET device can be programmed to a target value by controlling the amount of trapped positive fixed charges. The characteristic of programmable threshold voltage can be applied to insulated-gate bipolar transistors (IGBTs) to be used in power module applications. In an IGBT module, different IGBTs are connected in parallel. In order to obtain a uniform current distribution in the module at the on-state, the threshold voltage of different IGBTs should be kept the same. However, this goal can be challenging due to process variations. With the subject FETs, the threshold voltage of different IGBTs can be programmed to have the same value. Accordingly, the subject FETs can include IGBTs with an electrically programmable threshold voltage.

[0031] The subject FETs will now be described with reference to the drawings. Although the subject FETs are illustrated as an n-channel power metal-oxide-semiconductor field effect transistor (MOSFET), it is noted that the disclosure is equally applicable to p-channel power MOSFETs and other power field effect transistors such as an IGBT.

[0032] With reference initially to FIG. 1, presented is a prior art structure of a conventional power MOSFET 100. Device 100 comprises a doped n^- drift region 10 on an n^+ substrate 11. Device 100 further includes a gate dielectric layer 34 above the n^- drift region 10 and a gate 21 above the gate dielectric. The gate dielectric 34 is a single layer of insulator, typically silicon oxide. Device 100 further comprises a p-body 12 below the gate 21 and a source electrode 20. The p-body 12 is generally formed by ion-implantation and annealing. The typical peak doping concentration of the p-body 12 of the commonly used power MOSFET is from $1x10^{16}cm^{-3}$ to $1x10^{18}cm^{-3}$. The p-body 12 is connected to the source electrode 20 through the heavily doped p^+ region 13. The p-body 12 further comprises an n^+ source 14. The parasitic NPN bipolar junction transistor (BJT) in the power MOSFET device 100 is composed of the n+ source 14, the p-body 12 and the n^- drift region 10, and these three regions also act as the emitter, base and collector of the parasitic bipolar junction transistor, respectively. The p-body is connected to the source electrode

through the p+ region 13, and the n+ source/p-body junction is shorted at the source electrode 20 of the device 100.

[0033] The n+-source/p-body junction of device 100 will not be forward biased at the static on-state or off-state. However, under transient conditions such as avalanche operation of the power MOSFET device 100, reverse recovering of the body diode and fast rising of drain-to-source voltage, current will flow through the p-body 12 to the source electrode 20. This will cause a potential drop across the resistance of the p-body 12. If the current flow is large enough and the potential drop is significantly high enough, the n+-source/p-body junction will be forward biased, and the parasitic bipolar junction transistor will be activated. The activation of the parasitic bipolar junction transistor will cause a second-breakdown behavior of the power MOSFET device 100, as well as thermal runaway.

[0034] FIG. 2 presents another prior art structure of a power MOSFET device 200 with similar features 11, 10, 34, 21, 12, 13, and 20 and with an improved, e.g., optimized, doping profile of the p-body 12. In device 200, silicon oxide spacers 35 and the poly-silicon gate 21 were used as a self-aligning mask for high dose (between $1x10^{14}/cm^2$ and $1x10^{16}/cm^2$ boron ion-implantation. As a result, the p-body 12 is heavily doped at the region 17 under the n+ source 14. However, the doping concentration of p-body region 12 which is close to the channel is the same as that of device in FIG.1. The doping optimization of the p-body of device 200 results in heavily doping of the part of the p-body 12 which is farther away from the channel. However, the p-body region which is close to the channel still has low doping, otherwise, the threshold voltage of the device 200 would be affected. Because of this limitation, the part of the p-body which is closed to the channel is not heavily doped, leaving that part of the parasitic bipolar junction transistor still susceptible to turn-on during the transient conditions.

[0035] Turning now to FIG. 3, presented is a cross-section of an FET 300 embodied in a power MOSFET in accordance with an embodiment of the subject disclosure. Device 300 comprises a doped source of a first conductivity type (n^+ source 14), a doped body of a second conductivity type (p^+ body 15), a source electrode short-connecting the body and the source, and a doped drift region (n^- drift region 10) of the first conductivity type. In an aspect, the doped source is an n^+ source 14 and is heavily doped, the doped body is a p^+

body 15 and is heavily doped, and the doped drift region is an n^- drift region 10 and is lightly doped. For example, in a dose of the ion-implantation for the p^+ body 15 is from $1x10^{14}/cm^2$ to $1x10^{16}/cm^2$ with a peak doping concentration of the p+ body 15 from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$. In another example, the dose of the ion-implantation for the n+-source 14 can be from about$1x10^{14}/cm^2$ to $1x10^{16}/cm^2$. The doping concentration for the n^- drift region 10 depends on the voltage rating of the power MOSFET. Still in yet another example, the doping concentration for the n^- drift region 10 is between $1x10^{14}cm^{-3}$ and $1x10^{17}cm^{-3}$As seen in FIG. 3, the n^- drift region 10 is located adjacent to and below the p^+ body 15, and the n^+ source 14 is located within the upper surface of the p^+ body 15. In particular, the source 14 is located adjacent to a bottom surface of the source, a bottom surface of contact hole 38, which separates the source from the gate stack and is adjacent to the gate stack, and adjacent to a bottom surface of the gate dielectric region 36.

[0036] Device 300 further includes a gate dielectric region 36 above the n^- drift region 10 and a gate 21 above the gate dielectric region 36. Gate dielectric region 36 comprises of a charge trapping material 31 embedded in the gate dielectric of the power MOSFET device 300. In an aspect, gate dielectric region 36 comprises multiple layers. In an aspect, a first layer 30 of the gate dielectric region 36 is positioned above a surface of the n+ source 14, the p^+ body 15 and the n^- drift region 10. For example, the first layer of a gate dielectric region 36 can cover the surface of the p^+ body 15 and the surface of the n^- drift region 10, and form a channel from the source 14 to the drift region 10. In an aspect, the first layer 30 comprises silicon oxide. The first layer may have a thickness from about 0.2nm to about 20 nm. In another aspect, the first layer 30 may have a thickness from about 0.5 to about 15 nm. Still in yet another aspect, the first layer 30 may have a thickness from about 1nm to 10nm.

[0037] The second layer 31 of the gate dielectric region 36 includes a charge trapping material 31. In an aspect, the charge trapping material 31 includes at least one of silicon nitride, silicon nanocrystal, or a combination of both silicon nitride and silicon nanocrystal. However, it should be appreciated that any type of charge trapping material can be employed. The second layer 31 enables an amount of fixed charge to be located therein. Further, since the amount of the fixed charge can be exactly controlled, the threshold

voltage of the device is electrically programmable. In an aspect, the thickness of the charge trapping material 31 is from about 0.2 to about 200nm. In another aspect, the thickness of the charge trapping material is from about 0.5nm to about 150nm. In yet another aspect, the thickness of the charge trapping material is from 1nm to 100nm. Still in yet another aspect, the thickness of the charge trapping material is from about 10nm to about 50nm.

[0038] The third layer 32 of the gate dielectric region 36 can include at least one of silicon oxide or aluminum oxide. In an aspect, the thickness of the third layer 32 of the gate dielectric is from about 1nm to about 250nm. In yet another aspect, the thickness of the third layer is from about 5nm to about 225nm. In yet another aspect, the thickness of the third layer is from about 10nm to about 200nm. Still, in yet another aspect, the thickness of the third layer is from about 50nm to about 150nm.

[0039] In an embodiment, the peak doping concentration of the p^+-body 15 is from is greater than than$1x10^{18}cm^{-3}$ and from about $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$. The p^+-body 15 is directly connected to the source electrode 20. In an aspect, the source electrode 20 is aluminum. In another aspect, the source electrode can comprise of any metal, including but not limited to tungsten, copper, titanium nitride, titanium silicide, cobalt silicide and nickel silicide. A thickness of the source electrode 20 may be from about 0.1μm to about 20μm. In an embodiment, the gate electrode 21 is at least one of poly-silicon, metal or metal silicide. In an aspect, the thickness of the gate electrode 21 is from about 10nm to about 2000nm.

[0040] FIGs. 4 - 11 present the fabrication process of an FET device (such as device 300) embodied in a power MOSFET in accordance with an embodiment of the subject disclosure. As mentioned supra, in a conventional power MOSFETs, the doping concentration of the p-body is limited by the threshold voltage requirement. To increase the p-body doping can reduce the base resistance, but it can result in too high of the threshold voltage. The following fabrication process presents a simplified process for creating a power FET with an optimized doping profile for suppressing the activation of the parasitic BJT and for creating a power FET with a programmable V_{TH}.

[0041] With reference to FIG. 4, depicted is a device 400 with formation of a lightly doped (between $1x10^{14}cm^{-3}$ to $1x10^{17}cm^{-3}$) n^- drift region 10 on an n+ substrate 11. In an aspect, the n^- drift region 10 is formed by epitaxial growth on the n+ substrate 11. For

example, the process of forming a power FET in accordance with the subject disclosure can begin with growing the n^- drift region 10 (an N epitaxial layer) with a resistivity ranging from 0.10 to 10 ohm-cm on top of an n+ substrate 11. In an aspect, the substrate has a resistivity of 0.001 to 0.010 ohm-cm. In an embodiment, the thickness and the resistivity of the n^- epitaxial layer 10 can depend on the device requirements for the on-resistance and breakdown voltage. In an embodiment, the thickness of the n^- epitaxial layer 10 is about two to six microns.

[0042] FIG. 5 shows a device 500 with the formation of the gate dielectric region 36 layers. According to an aspect, the first layer 30 of the gate dielectric region 36 is silicon oxide and having a thickness from about 1nm to about 10nm. In an aspect, the first layer 30 of the gate dielectric region 36 is formed by dry oxidation of the silicon surface. For example, forming the first gate dielectric layer 30 can comprise of oxidizing the surface, via dry oxidation, of the n^- drift region 10. According to another aspect, the first layer 30 of the gate dielectric region 36 comprises of native oxide on the silicon surface of the n^- drift region 10.

[0043] The second layer 31 of the gate dielectric region 36 is formed over of the first layer 30 of the gate dielectric region 36. The second layer 31 of the gate dielectric region 36 comprises a charge trapping material 31. In an aspect, the typical thickness of the charge trapping material 31 is from about 1nm to about 100nm. In an aspect, the charge trapping material 31 is silicon nitride which is formed by chemical vapor deposition. For example, forming the second gate dielectric layer 31 can include depositing silicon nitride on the first get dielectric layer 30. According to another aspect, the charge trapping material 31 is silicon nanocrystal which is formed by chemical vapor deposition. For example, forming the second gate dielectric layer 31 can include depositing silicon nanocrystal on top of the first gate dielectric layer 30. According to another aspect, the charge trapping material 31 is a combination of silicon nitride and silicon nanocrystal, where both of these materials are formed by chemical vapor deposition. Still in yet another aspect, the charge trapping material 31 is silicon nanocrystal which is formed by silicon ion-implantation after the formation of the third layer of the gate dielectric. According to a further aspect, the charge

trapping material 31 is a combination of silicon nitride formed by chemical vapor deposition and silicon nanocrystal formed by ion-implantation.

[0044] The third layer 32 of the gate dielectric region 36 is formed over of the charge trapping material 31. According to an aspect, the third layer 32 of the gate dielectric region 36 is silicon oxide which is formed by oxidizing the charge trapping material 31. For example, forming the third gate dielectric layer 32 can comprise of oxidizing the second gate dielectric material 31. In another aspect, the third layer 32 of the gate dielectric region 36 is silicon oxide which is formed by chemical vapor deposition. For example, forming the third gate dielectric layer 32 can comprise of depositing silicon oxide over the second gate dielectric layer 31. In yet another aspect, the third layer 32 of the gate dielectric region is aluminum oxide which is formed by atomic layer deposition. In an embodiment, the thickness of the third layer 32 of the gate dielectric region 36 is from about 10nm to about 200nm.

[0045] FIG. 6 shows a device 600 with the formation of poly-silicon of the gate electrode 21. In an aspect, the poly-silicon 21 is formed by chemical vapor deposition. For example, a poly-silicon layer 21 can be deposited over the third gate electrode layer 32. In an aspect, the thickness of the poly-silicon of the gate electrode 21 is from 10nm to 2000nm. According to another aspect the poly-silicon of the gate electrode 21 can be transferred to metal or metal silicide after the formation of the p^+ body 15 and n^+ source 14. For example, after the formation of the as shown in FIG.s 9 and 8, the poly-silicon gate electrode can be silicided after the formation of the p^+ body 15 and n^+ source 14.

[0046] FIG. 7 shows the formation of the gate stack of a device 700. According to an embodiment, the poly-silicon of the gate electrode 21 and the gate dielectric region 36 comprising of layers 30, 31 and 32, are patterned by anisotropic etching to form a gate stack. The gate stack is formed such that it is centered over the upper surface of the n^- drift region 10 and over a portion of a surface of the p^+ body 15 adjacent to the n^- drift region 10. In an aspect, the etching can include reactive ion etching.

[0047] FIG. 8 shows the formation of the p^+ body 15 of device 800. According to an aspect, the p+ body 15 is formed by high dose ion-implantation and annealing. In an aspect, the dose of the ion-implantation is from $1x10^{14}/cm^2$ to $1x10^{16}/cm^2$. In an aspect, the

annealing is carried out at a temperature between 800 degree C and 1200 degree C for a duration between 1 second and 10 hours, such that the p+ body 15 reaches a depth between 0.3μm and 3μm. A peak doping concentration of the p+ body 15 can be from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$. The p+ body 15 comprises of a region of an upper surface of the n^- drift region 10 and located under a portion of the gate stack.

[0048] FIG. 9 shows the formation of a n^+ source 14 of device 900. In an aspect, the n+ source 14 is formed by high dose ion-implantation and annealing. The dose of the ion-implantation for the n+-source 14 can be from about$1x10^{14}/cm^2$ to $1x10^{16}/cm^2$. n+-source 14 comprises of a region of an upper surface of p+ body 15 and located under a portion of the gate stack. In an aspect, annealing is carried out at a temperature between 800 degree C and 1100 degree C for a duration between 1 second and 100 minutes, such that the n+-source 14 reaches a depth between 0.01μm and 0.5μm.

[0049] FIG. 10 shows the formation of a contact hole in device 1000. According to an embodiment, the contact hole is formed by silicon oxide 33 deposition and patterning. For example, a silicon oxide layer 33 can be deposited over the gate stack. In an aspect, a thickness of the deposited silicon oxide 33 is from about 100nm to about 1000nm. Then, following the formation of the source electrodes 20 as shown in FIG. 11, the silicon oxide layer 33 can be patterned via etching, such as reactive ion etching, in order to form contact holes 38, (depicted in FIG. 3, device 300).

[0050] FIG. 11 shows the formation of a source electrode 20 of device 1100. In an aspect, the source electrode is formed by aluminum deposition and patterning. For example, aluminum can be deposited over a surface of the p+ body, the n+-source 14, and a portion of the silicon oxide layer 33. In an aspect, the thickness of the deposited aluminum 20 may be from about 0.1μm to 20μm. Then, the aluminum layer and/or the silicon oxide layer can be patterned via etching, such as reactive ion etching to form device 300, pictured in FIG. 3.

[0051] It should be appreciated that the fabrication steps of the subject FET device embodied in an IGBT is the same as that for a subject FET device embodied in a power MOSFET except the formation of the n^- drift region 10. For the power MOSFET, the n^- drift region 10 is formed by epitaxial growth on the n^+ substrate 11. However, for the IGBT

device, the n^- drift region 10 is formed by epitaxial growth on the p+ substrate 16 or thinning down of an n^- doped substrate wafer.

[0052] FIG. 12 presents a cross-section of an FET device 1200 embodied in an IGBT in accordance with an embodiment of the subject disclosure. The device 1200 structure is similar to the power MOSFET device 300 structure shown in FIG.3. However, with device 1200, the substrate of the IGBT is a p+ substrate 16. The p+ base (i.e. p+ body) 15 of device 1200 is heavily doped, and charge trapping material 31 is embedded in the gate dielectric region 36 of the IGBT device 1200. The doping concentration for the n^- drift region 10 depends on the voltage rating of the IGBT. Still in yet another example, the doping concentration for the n^- drift region 10 is between $1x10^{12}cm^{-3}$ and $1x10^{15}cm^{-3}$. In an aspect, the first layer 30 of the gate dielectric region 36 is silicon oxide, and having a thickness from about 1nm to about10nm. The second layer 31 of the gate dielectric region 36 comprises a charge trapping material 31. In an aspect, the charge trapping material 31 is at least one of silicon nitride, silicon nanocrystal or a combination of both materials. Further, in an aspect, a thickness of the charge trapping material 31 is from about 1nm to about 100nm.

[0053] Further, in an aspect, the third layer 32 of the gate dielectric region 36 is silicon oxide or aluminum oxide. A thickness of the third layer 32 of the gate dielectric region is may be from about 10nm to 200nm. In an embodiment, the peak doping concentration of the p+ base (i.e. p+ body) 15 is from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$. The p+ base (i.e. p+ body) 15 is directly connected to the metal of the emitter (source) electrode 20. In an aspect, the metal of the emitter (source) electrode (20) is aluminum. A thickness of the aluminum 20 can be from about 0.1μm to about 20μm. The gate electrode 21 of the subject device 1200 can be poly-silicon, metal or metal silicide. In an aspect, a thickness of the poly-silicon of the gate electrode 21 is from about 10nm to about 2000nm.

[0054] According to the present embodiments, planar power field effect transistors are shown from FIG. 3 to FIG. 12. However, it should be appreciated that the gate stack, including the charge trapping material 31 in the gate dielectric region 36 and heavily doped p^+ body 15, can also be embodied in trench gate power field effect transistors.

[0055] FIGs. 13-14 illustrate methodologies in accordance with certain aspects of this disclosure. While, for purposes of simplicity of explanation, the methodologies are shown and described as a series of acts, it is to be understood and appreciated that this disclosure is not limited by the order of acts, as some acts may occur in different orders and/or concurrently with other acts from that shown and described herein. For example, those skilled in the art will understand and appreciate that methodologies can alternatively be represented as a series of interrelated states or events, such as in a state diagram. Moreover, not all illustrated acts may be required to implement methodologies in accordance with certain aspects of this disclosure. Additionally, it is to be further appreciated that the methodology disclosed hereinafter and throughout this disclosure is capable of being stored on an article of manufacture to facilitate transporting and transferring such methodologies to computers.

[0056] Turning now to FIG. 13, presented is a high level flow diagram of a process 1300 for fabricating an FET in accordance with an embodiment of the subject disclosure. At reference numeral 1302, a doped drift region of a first conductivity type is formed. In an aspect, the doped drift region is formed by epitaxial growth of an n^--drift region on an n^+ substrate. At 1304, a gate stack is formed over the doped drift region. Forming the gate stack includes forming a first gate dielectric layer at 1306, forming a second gate dielectric layer over the first layer at 1308, forming a third gate dielectric layer over of the second gate dielectric layer at 1310, deposing a gate electrode over the third gate dielectric layer at 1312, and then patterning the gate electrode and the gate dielectric layers at 1314.

[0057] After the formation of the gate stack, at 1316, a doped body of a second conductivity type is formed in the doped drift region. In an aspect, the doped body is a p^+ body formed by high dose ion-implantation and annealing. At 1318, a doped source of the first conductivity type is formed in the doped body, wherein the first gate dielectric layer covers a surface of the body and forms a channel from the doped source to the doped drift region. In an aspect, the doped source in an n^+ source formed by high dose ion-implantation and annealing. Then, at 1320, a contact hole is formed adjacent to the gate stack. The contact hole can be formed by depositing a dielectric layer and patterning the dielectric layer. Further, at 1322, a source electrode is formed above the doped source and the doped

body, wherein source electrode short connects the doped body and the doped source. In an aspect, the source electrode is formed by depositing a metal layer and patterning.

[0058] Turning now to FIG. 14, presented is a high level flow diagram of a process 1400 for fabricating a FET in accordance with an embodiment of the subject disclosure. At reference numeral 1402, a doped drift region of a first conductivity type is formed. In an aspect, the doped drift region is formed by epitaxial growth of an n^--drift region on an n^+ substrate. At 1404, a gate stack is formed over the doped drift region. Forming the gate stack includes forming a first gate dielectric layer at 1406, forming a second gate dielectric layer over of the first layer at 1408, forming a third gate dielectric layer over of the second gate dielectric layer at 1410, deposing a gate electrode over the third gate dielectric layer at 1412, and then patterning the gate electrode and the gate dielectric layers at 1414. After the formation of the gate stack, at 1416, ions are implanted into an upper portion of the doped drift region and under a portion of the gate stack at doping concentration from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$ to form a doped body of a second conductivity type at 1418.

[0059] FIG. 15 presents a graph 1500 depicting an exemplary non-limiting set of sample results illustrating one or more aspects of the various embodiments described herein. The experimental transfer characteristics of a power MOSFET in accordance with an embodiment is shown in the figure. Using the techniques described herein, the doping concentration of the p-body is increased by an order of magnitude compared to that of the conventional power MOSFET, and the threshold voltage of the novel device was programmed to the same 1 V as that of the conventional device by applying -25 V to the gate of the device for 15 ms, as shown in the figure. Due to the heavily doped p-body 15, the parasitic BJT activation in the novel device is suppressed.

[0060] FIG. 16 presents a graph 1600 depicting the I_{DS}-V_{DS} characteristics of the power MOSFET with a programmed threshold voltage of 1 V as shown previously in FIG. 15.

[0061] Unclamped inductive switching (UIS) measurement was used to evaluate the ruggedness of a subject device as characterized in FIG. 15 and FIG. 16. In the measurement, the device under test (DUT) was connected in series with an inductor (400 μH) along with a DC power supply (30 V) at room temperature. A single voltage pulse (0 V to 20 V) was

applied to the gate of the DUT, and the width of the pulse was increased until the failure of the DUT was observed at high I_{DS} and high V_{DS}. As a result, the avalanche energy absorption of the novel device at UIS is about 5.2 times that of the conventional power MOSFET. The above results have been accepted for publication on IEEE Electron Device Letters.

[0062] The resultant power devices formed herein are useful in any electronic device. For example, the resultant power devices are useful in computers, appliances, industrial equipment, hand-held devices, telecommunications equipment, medical equipment, research and development equipment, transportation vehicles, radar/satellite devices, and the like. Hand-held devices, and particularly hand-held electronic devices, achieve improvements in portability due to the small size and lightweight of the memory devices. Examples of hand-held devices include cell phones and other two way communication devices, personal data assistants, Palm Pilots, pagers, notebook computers, remote controls, recorders (video and audio), radios, small televisions and web viewers, cameras, and the like.

[0063] What has been described above includes examples of the subject invention. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the subject invention, but one of ordinary skill in the art may recognize that many further combinations and permutations of the subject invention are possible. Accordingly, the subject invention is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims. Furthermore, to the extent that the term "includes" and "involves" are used in either the detailed description or the claims, such terms are intended to be inclusive in a manner similar to the term "comprising" as "comprising" is interpreted when employed as a transitional word in a claim.

[0064] Reference throughout this specification to "one embodiment," or "an embodiment," means that a particular feature, structure, or characteristic described in connection with the embodiment is included in at least one embodiment. Thus, the appearances of the phrase "in one embodiment," or "in an embodiment," in various places throughout this specification are not necessarily all referring to the same embodiment. Furthermore, the particular features, structures, or characteristics may be combined in any suitable manner in one or more embodiments.

[0065] The word "exemplary" and/or "demonstrative" is used herein to mean serving as an example, instance, or illustration. For the avoidance of doubt, the subject matter disclosed herein is not limited by such examples. In addition, any aspect or design described herein as "exemplary" and/or "demonstrative" is not necessarily to be construed as preferred or advantageous over other aspects or designs, nor is it meant to preclude equivalent exemplary structures and techniques known to those of ordinary skill in the art. Furthermore, to the extent that the terms "includes," "has," "contains," and other similar words are used in either the detailed description or the claims, such terms are intended to be inclusive - in a manner similar to the term "comprising" as an open transition word - without precluding any additional or other elements.

CLAIMS

What is claimed is:

1. A power semiconductor field effect transistor structure comprising:

a doped source (14) of a first conductivity type;

a doped body (15) of a second conductivity type;

a source electrode (20) short-connecting the body and the doped source;

a doped drift region (10) of the first conductivity type;

a first layer (30) of a gate dielectric region (38) covering the surface of the doped body (15) and forming a channel from the doped source (14) to the doped drift region (10);

a second layer (31) of the gate dielectric region (36) over the first layer;

a third layer (32) of the gate dielectric region (36) over the second layer; and

a gate electrode (21) over the third layer.

2. The semiconductor structure of claim 1, wherein the doped source (14) is formed by high dose ion-implantation and annealing.

3. The semiconductor structure of claim 1, wherein the doped body (15) is formed by high dose ion-implantation and annealing.

4. The semiconductor structure of claim 1, wherein the source electrode (20) is a metal.

5. The semiconductor structure of claim 1, wherein the doped body (15) forms direct contact to the source electrode (20).

6. The semiconductor structure of claim 1, wherein the gate electrode (21) is at least one of poly-silicon, metal or metal silicide.

7. The semiconductor structure of claim 1, wherein the doped drift region (10) is formed by epitaxial growth on a doped substrate (11) or by thinning down of a doped substrate wafer.

8. The semiconductor structure of claim 1, wherein the doped body (15) comprises silicon, and the first layer (30) of the gate dielectric region (36) is native silicon oxide of the surface of the silicon or silicon oxide formed by thermal oxidation of the surface of the body (15).

9. The semiconductor structure of claim 1, wherein the second layer (31) of the gate dielectric region (36) is a charge trapping material.

10. The semiconductor structure of claim 1, wherein the second layer (31) of the gate dielectric region (36) is at least one of silicon nitride or silicon nanocrystal.

11. The semiconductor structure of claim 9, wherein the charge trapping material is formed by chemical vapor deposition after the formation of the first layer (30).

12. The semiconductor structure of claim 9, wherein the charge trapping material is formed by ion-implantation after the formation of the third layer (32).

13. The semiconductor structure of claim 1, wherein the third layer (32) is silicon oxide formed by oxidizing the second layer (31) or by chemical vapor deposition.

14. The semiconductor structure of claim 1, wherein the third layer (32) is aluminum oxide formed by atomic layer deposition.

15. The semiconductor structure of claim 1, wherein the structure is embodied in a power metal-oxide-semiconductor field effect transistor (MOSFET).

16. The semiconductor structure of claim 1, wherein the structure is embodied in an insulated-gate bipolar transistor (IGBT).

17. A method for fabricating a power semiconductor field effect transistor structure comprising:

forming a doped drift region (10) of a first conductivity type;

forming a gate stack over the doped drift region, including,

forming a first gate dielectric layer (30);

forming a second gate dielectric layer (31) over the first gate dielectric layer (30);

forming a third gate dielectric (32) over the second gate dielectric layer (31);

deposing a gate electrode (21) over the third gate dielectric layer (32); and

patterning the gate electrode (21) and the gate dielectric layers (30, 31, 32);

forming a doped body (15) of a second conductivity type in the doped drift region (10);

forming a doped source (14) of the first conductivity type in the doped body (15),

wherein the first gate dielectric layer (30) covers a surface of the doped body (15) and forms a channel from the doped source (14) to the doped drift region (10);

forming a contact hole (38) adjacent to the gate stack; and

forming a source electrode (20) above the doped source (14) and the doped body (15),

wherein the source electrode (20) short connects the doped body (15) and the doped source (14).

18. The method of claim 17, wherein the forming the doped source (14) includes forming the doped source by high dose ion-implantation and annealing.

19. The method of claim 17, wherein the forming the doped body (15) includes forming the doped body by high dose ion-implantation and annealing.

20. The method of claim 17, wherein the source electrode (20) is a metal.

21. The method of claim 17, wherein the doped body (15) forms direct contact to the source electrode (20).

22. The method of claim 17, wherein the gate electrode (21) is at least one of poly-silicon, metal or metal silicide.

23. The method of claim 17, wherein the forming the doped drift region (10) includes forming the doped drift region by epitaxial growth on a doped substrate (11) or by thinning down a doped substrate wafer.

24. The method of claim 17, wherein the doped body (15) comprises silicon, and the first gate dielectric layer (30) of the gate dielectric region (36) is native silicon oxide of the surface of the silicon, or wherein the forming the first gate dielectric layer includes oxidizing the surface of the doped body (15) by thermal oxidation to form silicon oxide.

25. The method of claim 17, wherein the second gate dielectric layer (31) is a charge trapping material.

26. The method of claim 17, wherein the second gate dielectric layer (31) is at least one of silicon nitride or silicon nanocrystal.

27. The method of claim 25, wherein the forming the second gate dielectric layer (31) includes forming the charge trapping material by chemical vapor deposition after the formation of the first gate dielectric layer (30).

28. The method of claim 25, wherein the forming the second gate dielectric (31) layer includes forming the second gate dielectric layer (31) by ion-implantation after the forming of the third gate dielectric layer (32).

29. The method of claim 17, wherein the third gate dielectric layer (32) is silicon oxide formed by oxidizing the second gate dielectric layer (31) or by chemical vapor deposition.

30. The method of claim 17, wherein the third gate dielectric layer (32) is aluminum oxide formed by atomic layer deposition.

31. The method of claim 17, wherein the structure is embodied in a power metal-oxide-semiconductor field effect transistor (MOSFET).

32. The method of claim 17, wherein the structure is embodied in an insulated-gate bipolar transistor (IGBT).

33. A method for fabricating a power semiconductor field effect transistor structure comprising:

forming a doped drift region (10) of a first conductivity type;

forming a gate stack over the doped drift region, including,

forming a first gate dielectric layer (30);

forming a second gate dielectric layer (31) over the first gate dielectric layer (30);

forming a third gate dielectric layer (32) over the second gate dielectric layer (31);

deposing a gate electrode (21) over the third gate dielectric layer (32); and

patterning the gate electrode (21) and the gate dielectric layers (30, 31, 32);

implanting ions into an upper portion of the doped drift region 10 and under a portion of the gate stack at doping concentration from $1x10^{18}cm^{-3}$ to $1x10^{20}cm^{-3}$; and

forming a doped body (15) of a second conductivity type.

34. The method of claim 33, further comprising:

forming a doped source (14) of the first conductivity type in the doped body (15), wherein the first gate dielectric layer (30) covers a surface of the doped body (30) and forms a channel from the doped source (14) to the doped drift region (10);

forming a contact hole (38) adjacent to the gate stack; and

forming a source electrode (20) above the doped source (14) and the doped body (15), wherein the source electrode (20) short connects the doped body (15) and the doped source (14).

35. The method of claim 34, wherein the forming the doped source (14) includes forming the doped source by high dose ion-implantation and annealing.

36. The method of claim 33, wherein the forming the doped body (15) includes performing an annealing process following the implanting the ions.

37. The method of claim 33, wherein the second gate dielectric layer (31) is a charge trapping material.

38. The method of claim 33, wherein the second gate dielectric layer (31) is at least one of silicon nitride or silicon nanocrystal.

39. The method of claim 38, wherein the forming the second gate dielectric layer (31) includes forming the charge trapping material by chemical vapor deposition after the formation of the first gate dielectric layer (30).

40. The method of claim 33, wherein the forming the second gate dielectric layer (31) includes forming the second gate dielectric layer by ion-implantation after the forming of the third gate dielectric layer (32).

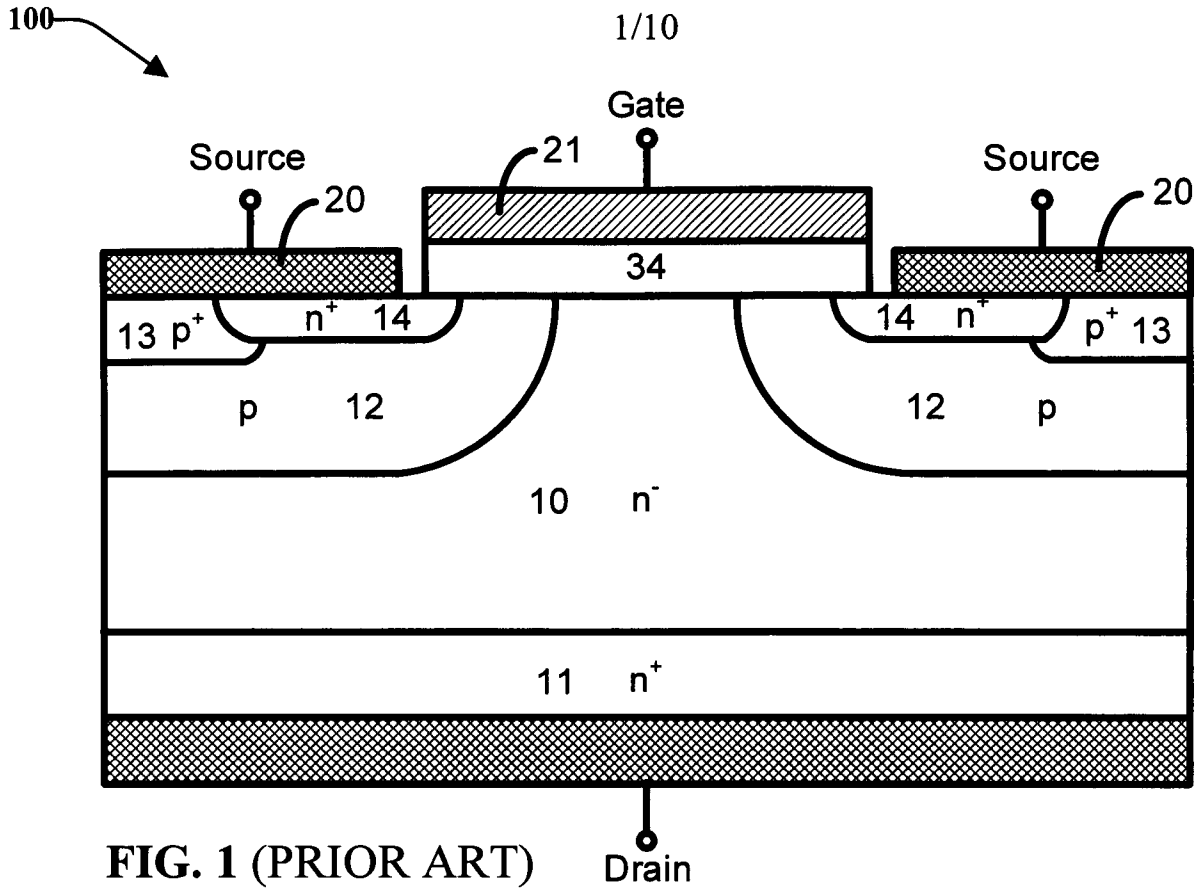

FIG. 1 (PRIOR ART)

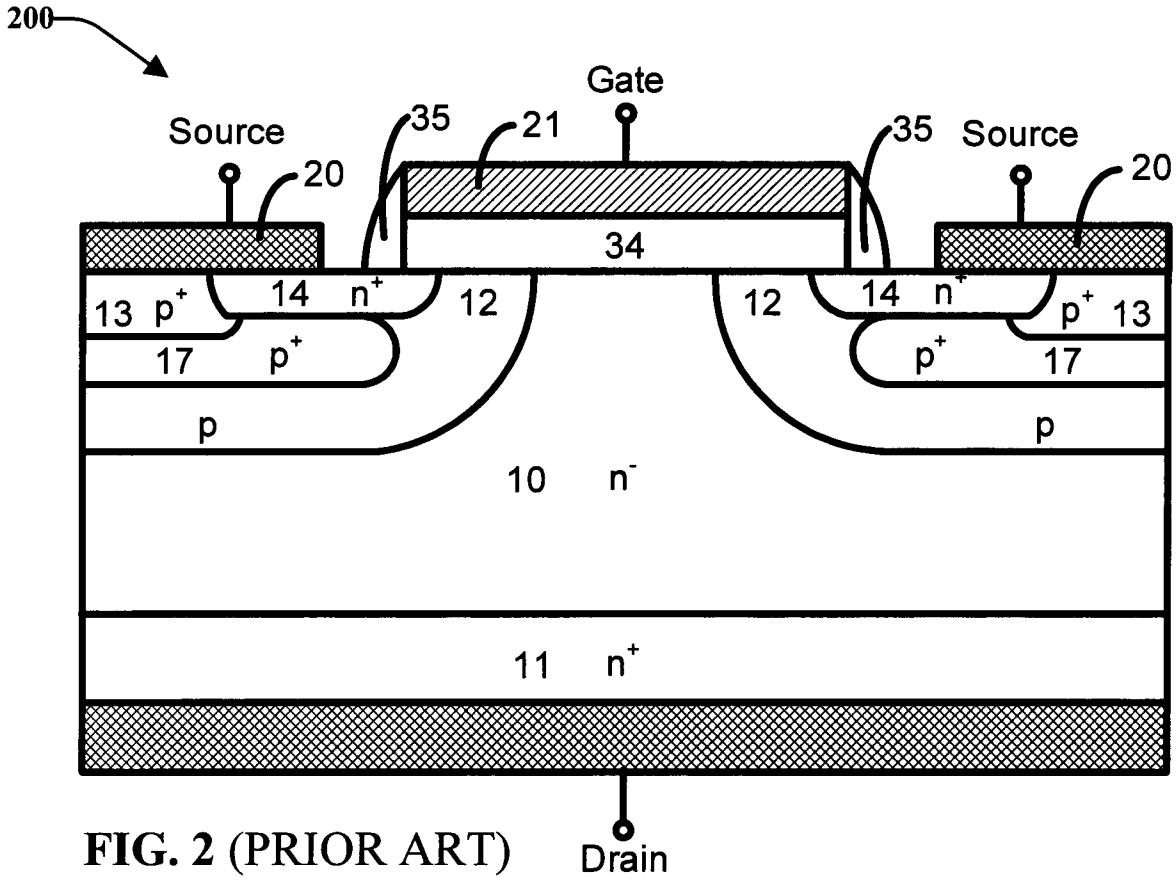

FIG. 2 (PRIOR ART)

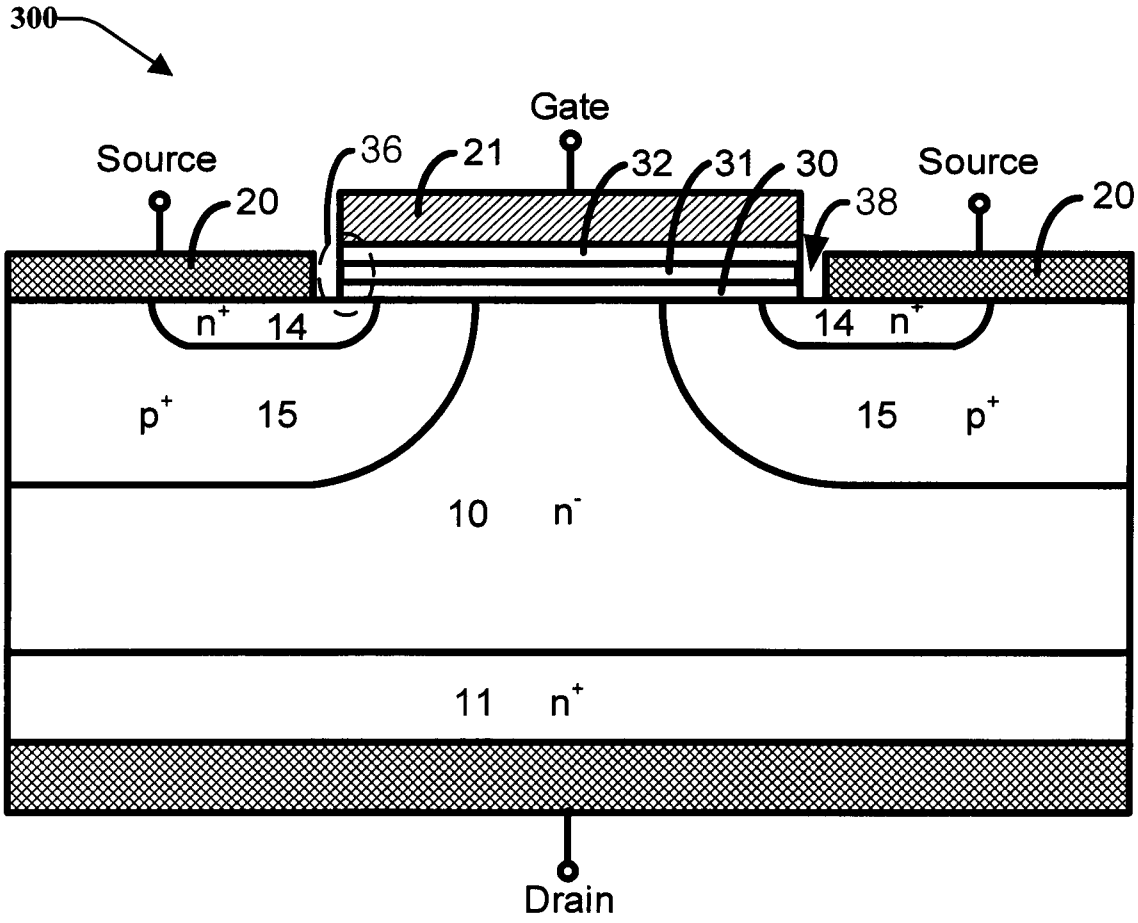
300
Gate
Source
36
21
32
31
30
Source
20
38
20
n+
14
14
n+
p+
15
15
p+
10
n-
11
n+
Drain

FIG. 3

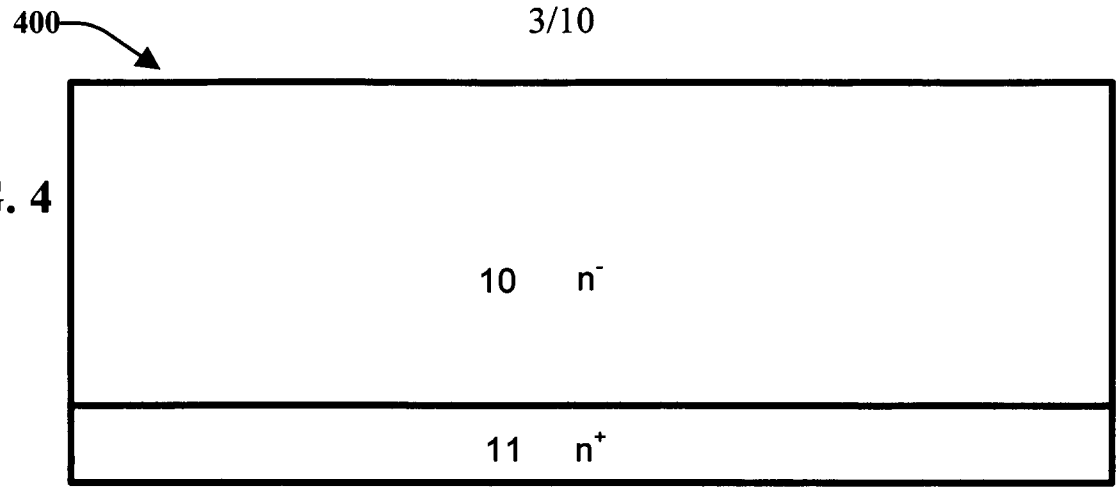

FIG. 4

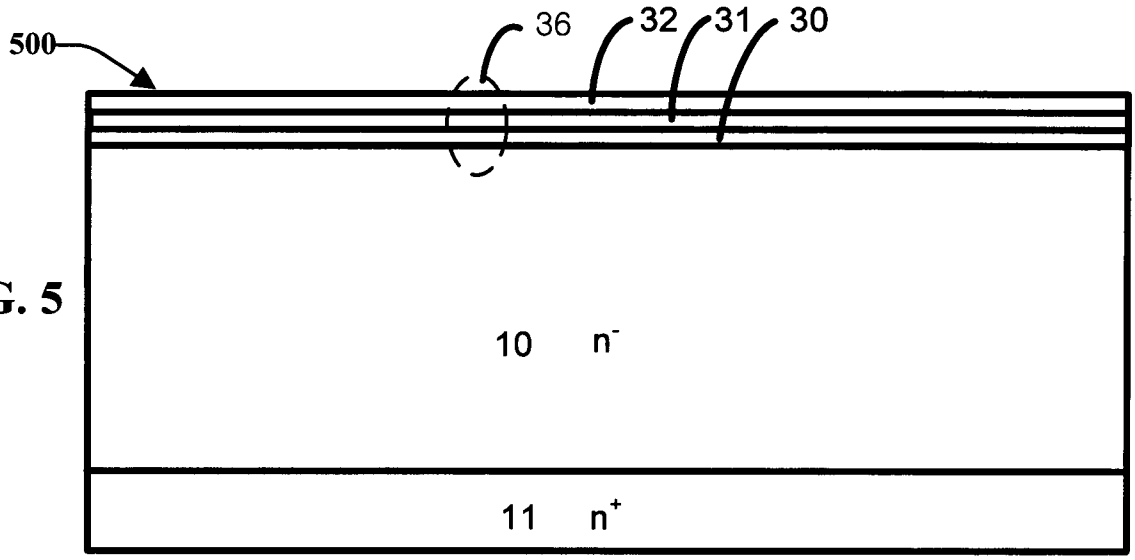

FIG. 5

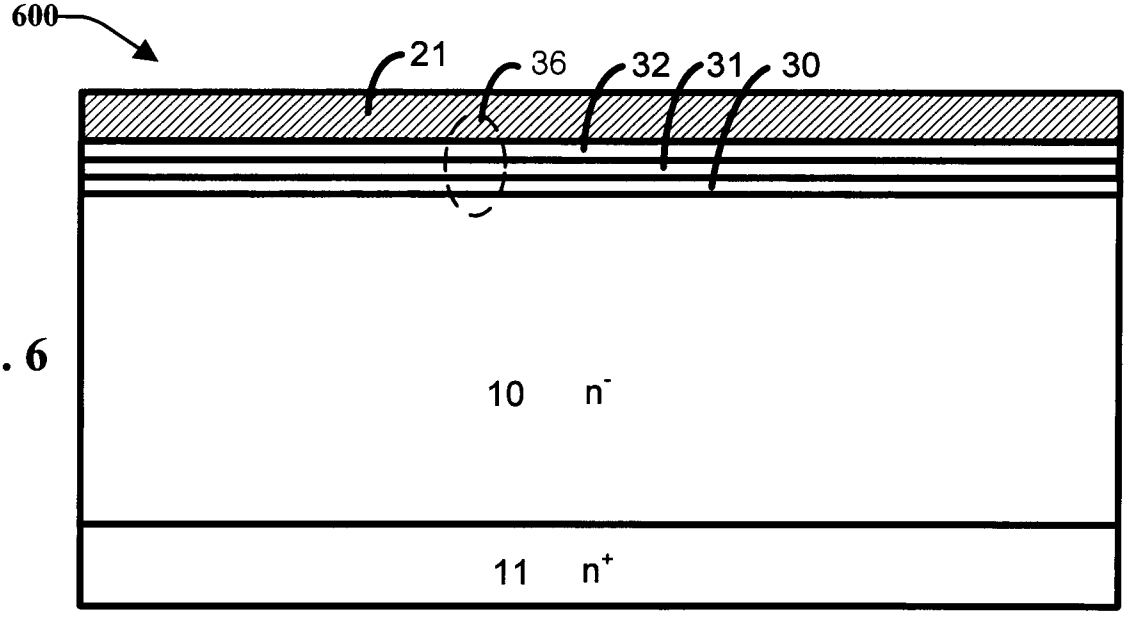

FIG. 6

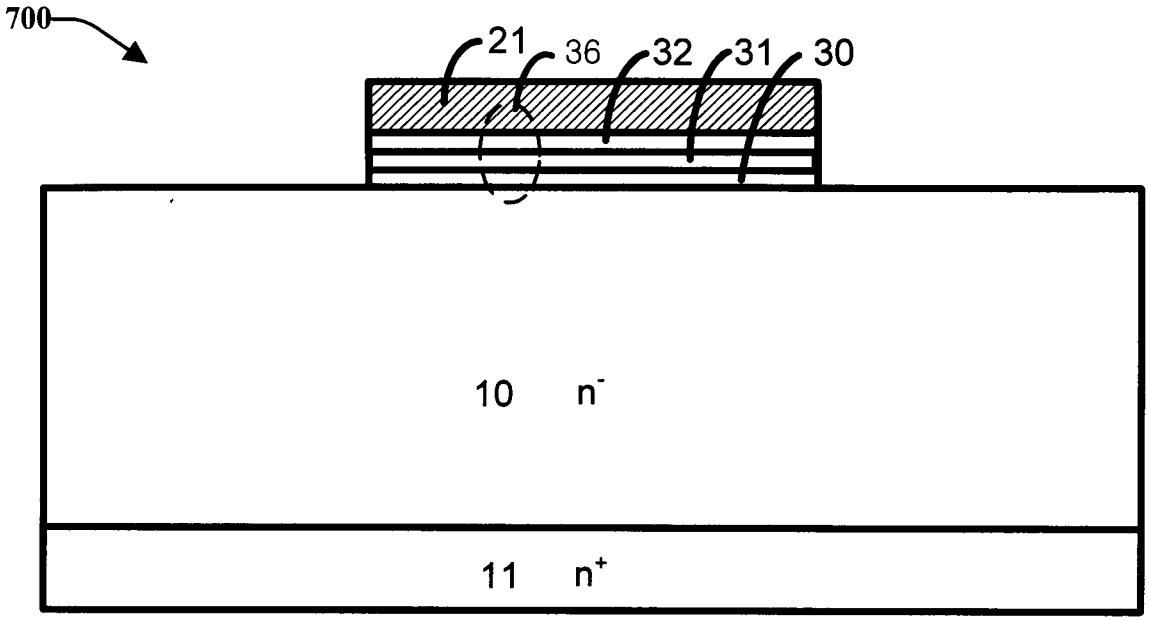

FIG. 7

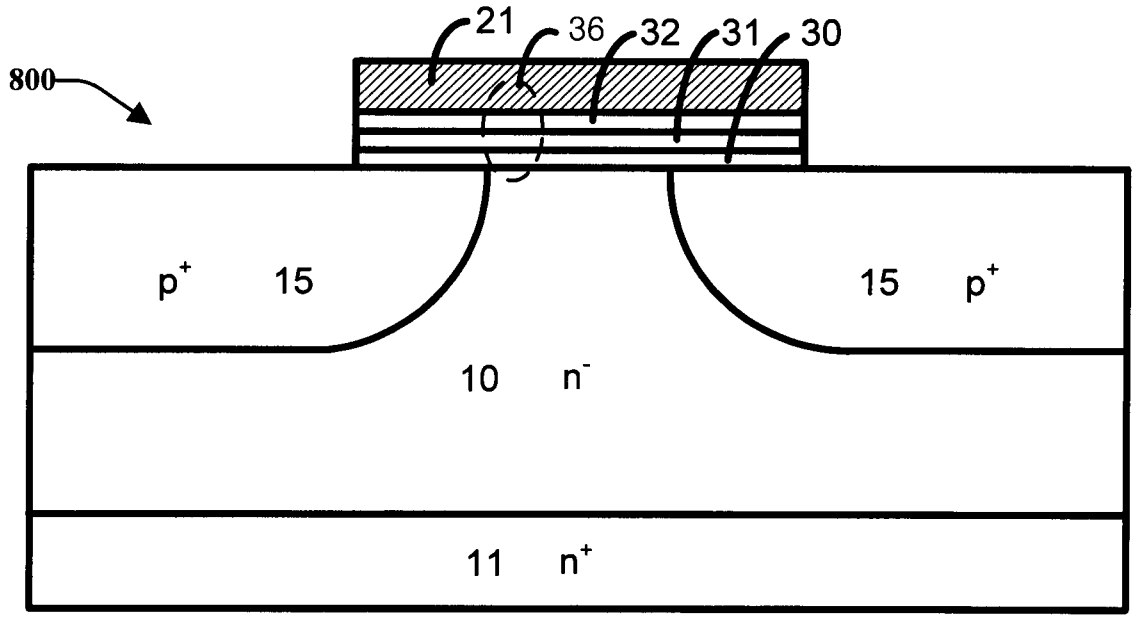

FIG. 8

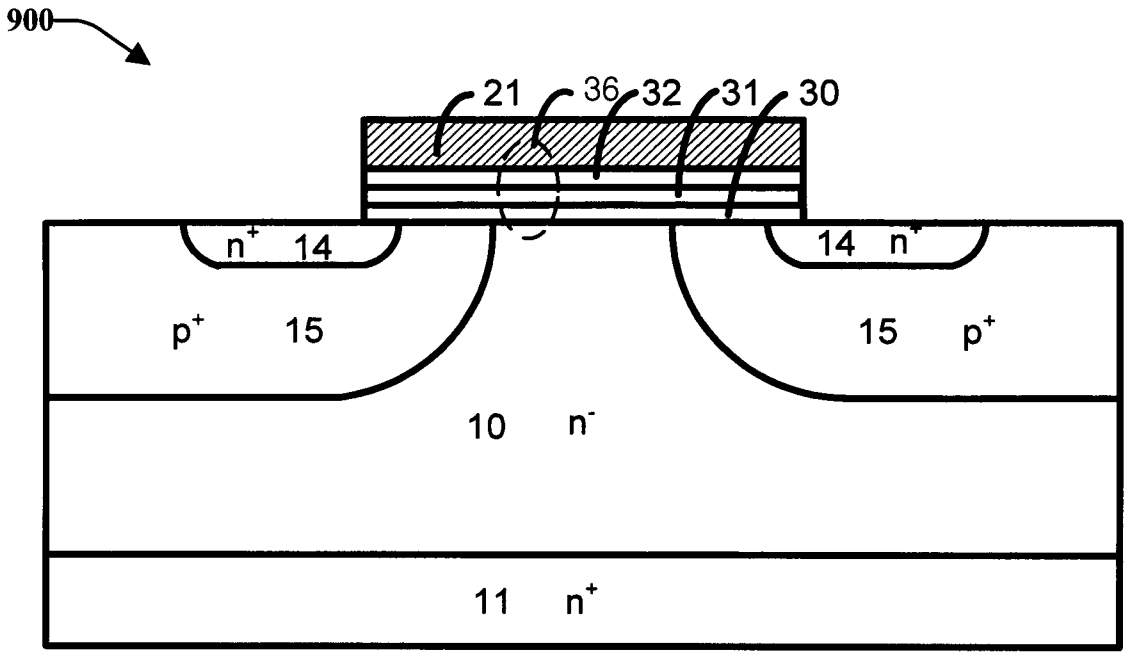
900
21
36
32
31
30
n+ 14
14 n+
p+ 15
15 p+
10 n-
11 n+

FIG. 9

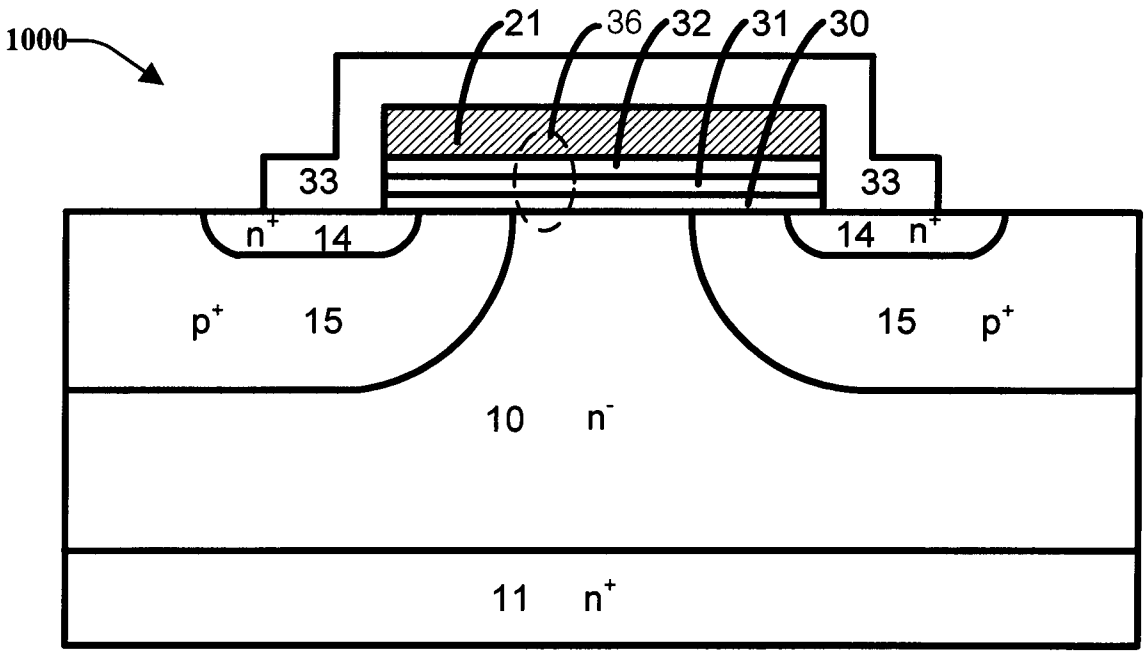
1000
21
36
32
31
30
33
33
n+ 14
14 n+
p+ 15
15 p+
10 n-
11 n+

FIG. 10

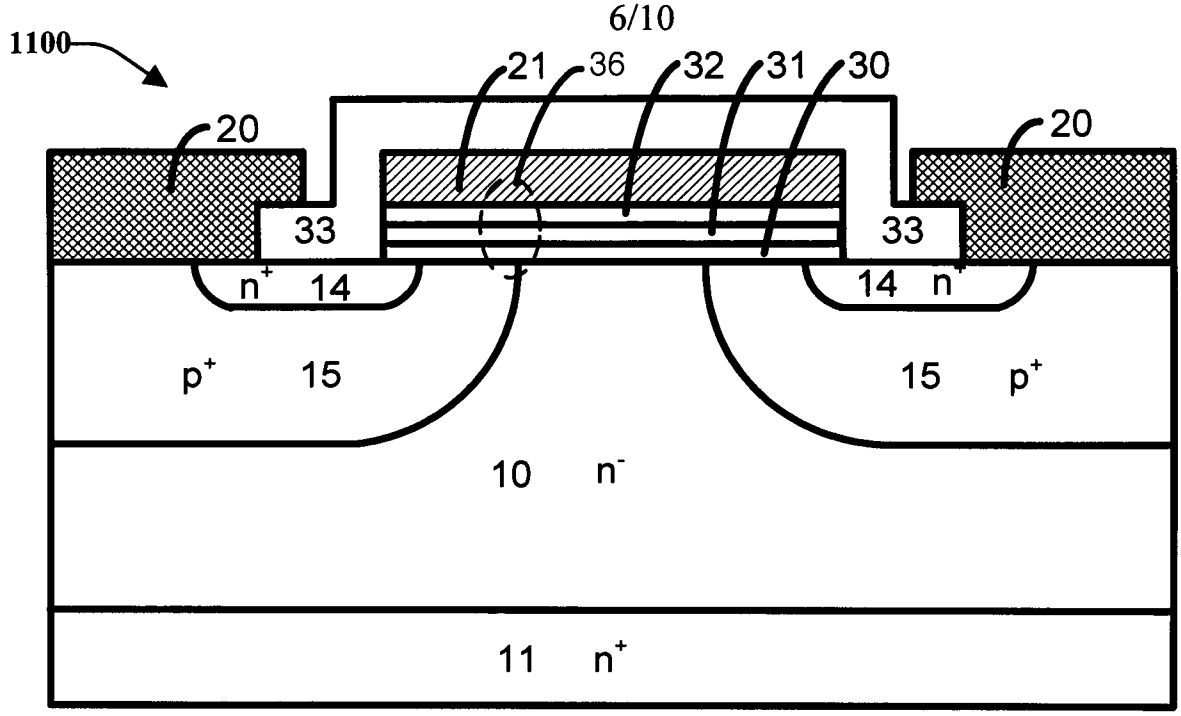
1100
21
36
32
31
30
20
20
33
33
n+
14
14
n+
p+
15
15
p+
10
n-
11
n+

FIG. 11

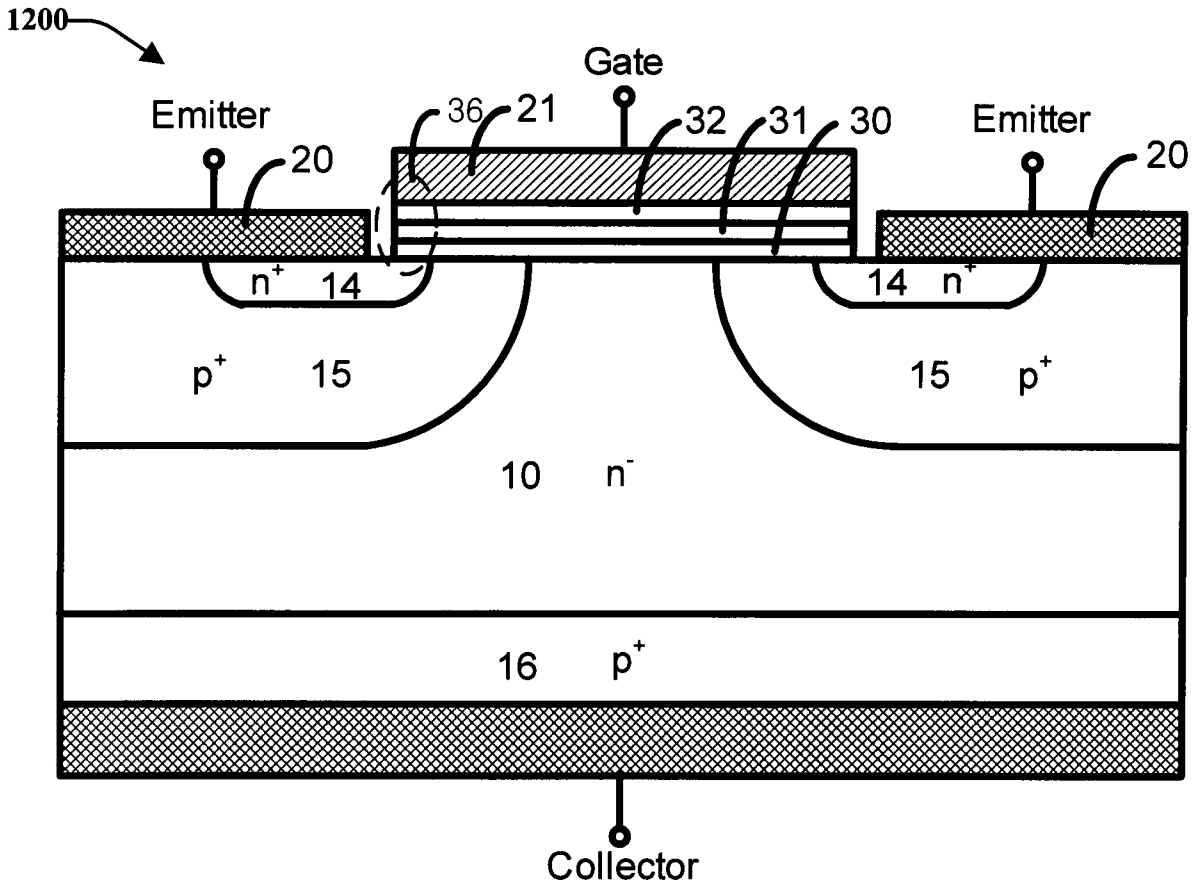
1200
Gate
Emitter
Emitter
36
21
32
31
30
20
20
n+
14
14
n+
p+
15
15
p+
10
n-
16
p+
Collector

FIG. 12

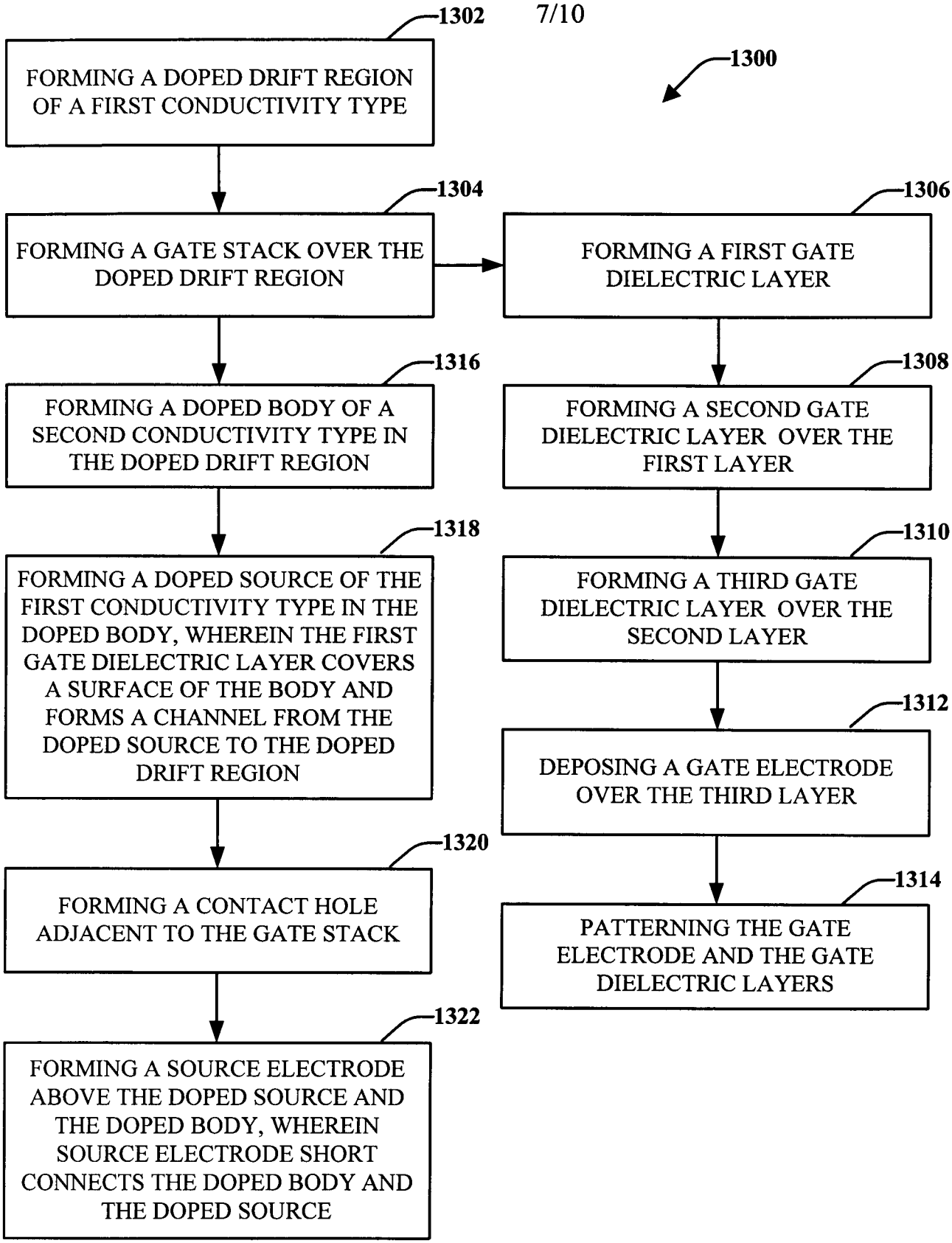
1300
1302
FORMING A DOPED DRIFT REGION OF A FIRST CONDUCTIVITY TYPE
1304
FORMING A GATE STACK OVER THE DOPED DRIFT REGION
1306
FORMING A FIRST GATE DIELECTRIC LAYER
1316
FORMING A DOPED BODY OF A SECOND CONDUCTIVITY TYPE IN THE DOPED DRIFT REGION
1308
FORMING A SECOND GATE DIELECTRIC LAYER OVER THE FIRST LAYER
1318
FORMING A DOPED SOURCE OF THE FIRST CONDUCTIVITY TYPE IN THE DOPED BODY, WHEREIN THE FIRST GATE DIELECTRIC LAYER COVERS A SURFACE OF THE BODY AND FORMS A CHANNEL FROM THE DOPED SOURCE TO THE DOPED DRIFT REGION
1310
FORMING A THIRD GATE DIELECTRIC LAYER OVER THE SECOND LAYER
1312
DEPOSING A GATE ELECTRODE OVER THE THIRD LAYER
1320
FORMING A CONTACT HOLE ADJACENT TO THE GATE STACK
1314
PATTERNING THE GATE ELECTRODE AND THE GATE DIELECTRIC LAYERS
1322
FORMING A SOURCE ELECTRODE ABOVE THE DOPED SOURCE AND THE DOPED BODY, WHEREIN SOURCE ELECTRODE SHORT CONNECTS THE DOPED BODY AND THE DOPED SOURCE

FIG. 13

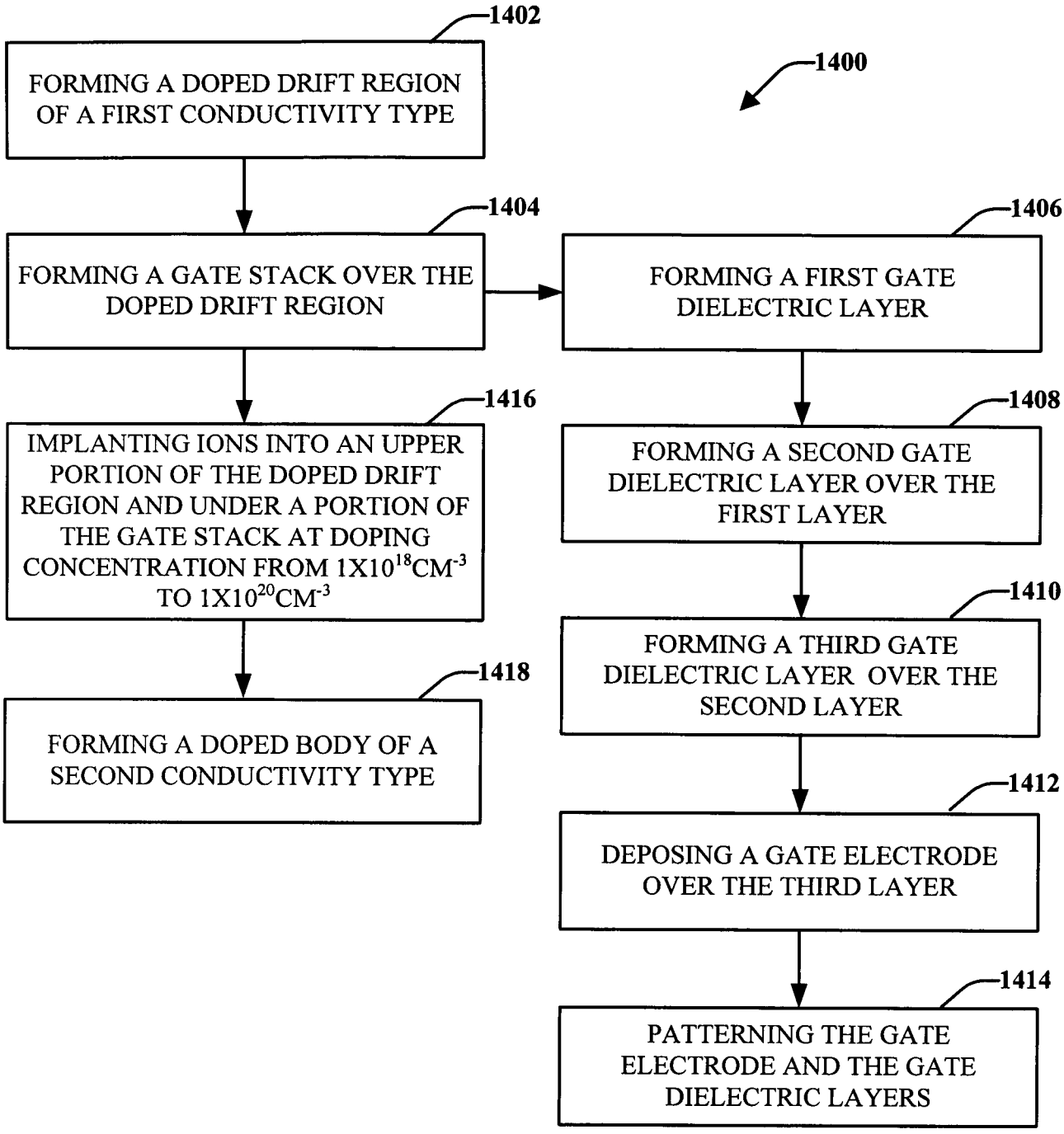
1400
1402
FORMING A DOPED DRIFT REGION OF A FIRST CONDUCTIVITY TYPE
1404
FORMING A GATE STACK OVER THE DOPED DRIFT REGION
1406
FORMING A FIRST GATE DIELECTRIC LAYER
1408
FORMING A SECOND GATE DIELECTRIC LAYER OVER THE FIRST LAYER
1410
FORMING A THIRD GATE DIELECTRIC LAYER OVER THE SECOND LAYER
1412
DEPOSING A GATE ELECTRODE OVER THE THIRD LAYER
1414
PATTERNING THE GATE ELECTRODE AND THE GATE DIELECTRIC LAYERS
1416
IMPLANTING IONS INTO AN UPPER PORTION OF THE DOPED DRIFT REGION AND UNDER A PORTION OF THE GATE STACK AT DOPING CONCENTRATION FROM 1X10^{18}CM^{-3} TO 1X10^{20}CM^{-3}
1418
FORMING A DOPED BODY OF A SECOND CONDUCTIVITY TYPE

FIG. 14

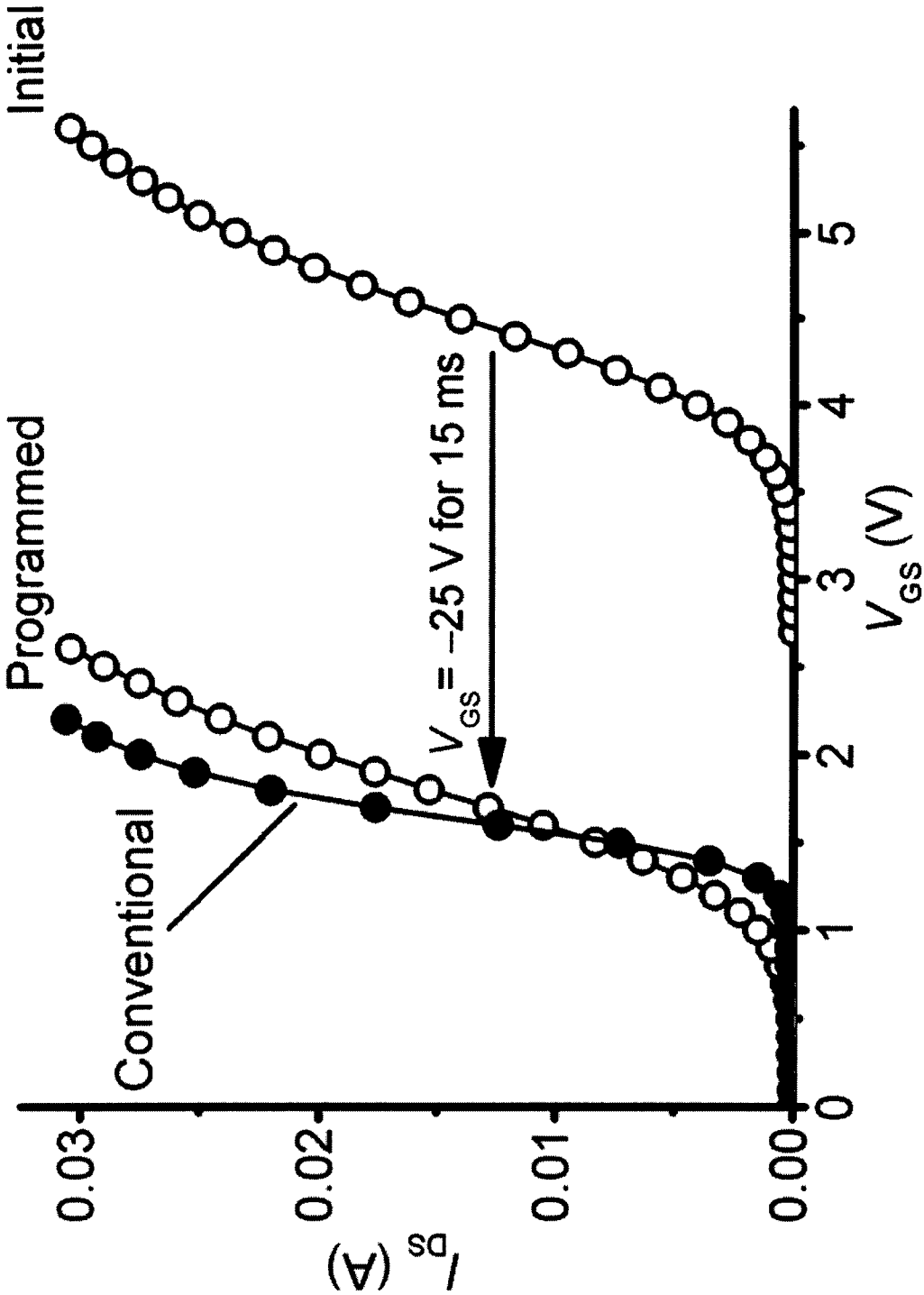
1500
Initial
Programmed
Conventional
V_{GS} = −25 V for 15 ms
I_{DS} (A)
0.03
0.02
0.01
0.00
0
1
2
3
4
5
V_{GS} (V)

FIG. 15

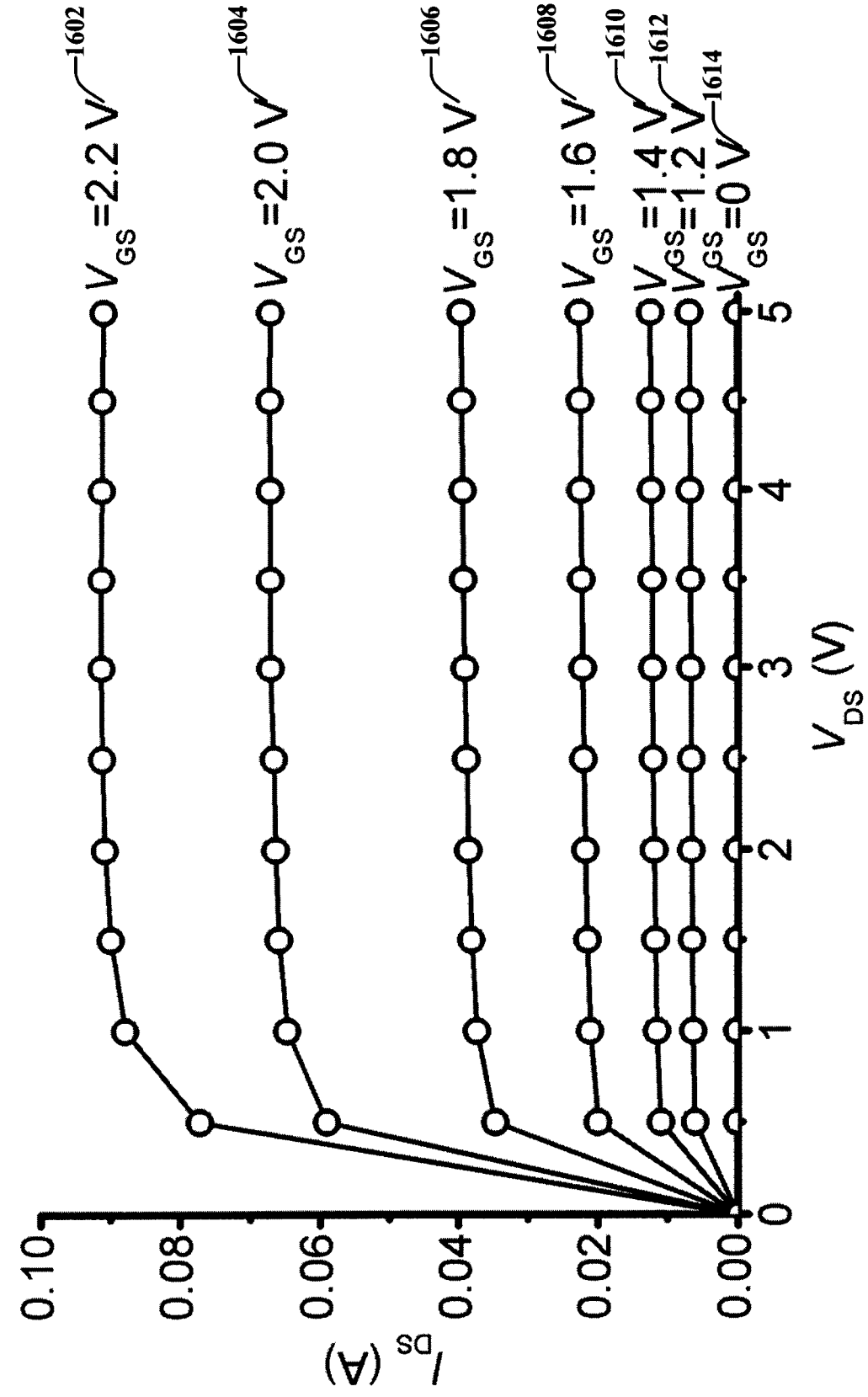
1600
1602
1604
1606
1608
1610
1612
1614
V_{GS} =2.2 V
V_{GS} =2.0 V
V_{GS} =1.8 V
V_{GS} =1.6 V
V_{GS} =1.4 V
V_{GS} =1.2 V
V_{GS} =0 V
I_{DS} (A)
0.10
0.08
0.06
0.04
0.02
0.00
0
1
2
3
4
5
V_{DS} (V)

FIG. 16

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2011/002140

A. CLASSIFICATION OF SUBJECT MATTER

See extra sheet

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC: H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNPAT,CNKI,DWPI,EPODOC: power, MOSFET, IGBT, gate, dielectric, insulat+, trap+, nitride, oxide, ruggedness, UIS, stacked, nanocrystal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	CN1478302A (CREE INC) 25 Feb. 2004 (25.02.2004) page 23, line 1 to page 28, line 14, figs. 6,8A-8H	1-40
X	CN1527369A (DENSO CORP) 08 Sep. 2004 (08.09.2004) page 14, line 7 to page 26, line 13 figs. 2,6-11C	1-40
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☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
09 Mar. 2012 (09.03.2012)	**29 Mar. 2012 (29.03.2012)**
Name and mailing address of the ISA/CN The State Intellectual Property Office, the P.R.China 6 Xitucheng Rd., Jimen Bridge, Haidian District, Beijing, China 100088 Facsimile No. 86-10-62019451	Authorized officer CHE,Xiaolu Telephone No. (86-10)62411843

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