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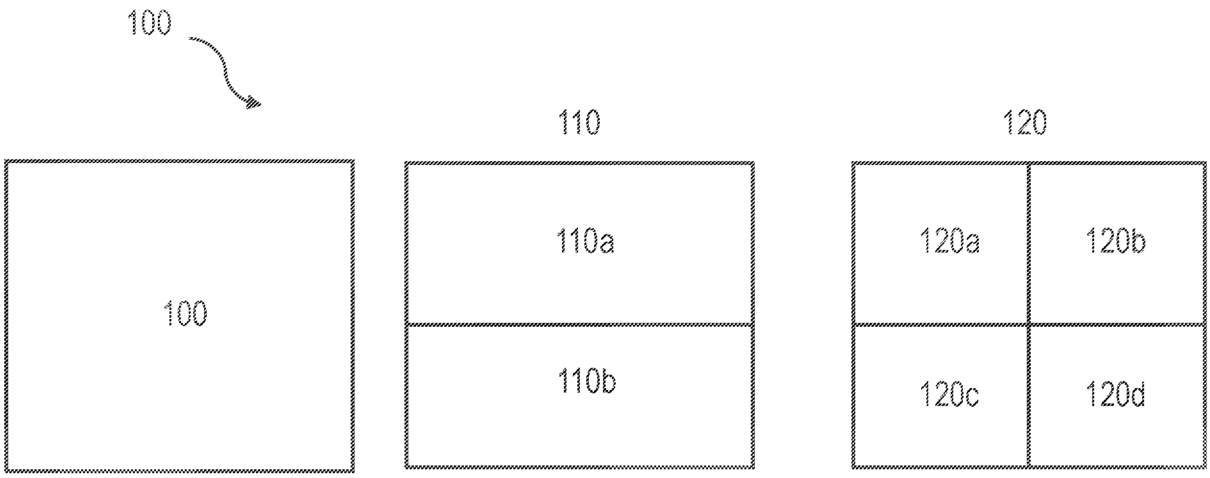

FIG. 1

(57) **Abstract:** A decoder comprising circuitry configured to receive a bitstream, partition the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions, determine a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function a line segment slope angle, determine a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector, and decode the current block using the first motion vector and the second motion vector.

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METHODS AND SYSTEMS OF ADAPTIVE GEOMETRIC PARTITIONING

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of priority of U.S. Provisional Application Serial No. 63/072,065, filed on August 28, 2020, and entitled "METHODS AND SYSTEMS OF ADAPTIVE GEOMETRIC PARTITIONING," which is incorporated by reference herein in its entirety.

FIELD OF THE INVENTION

The present invention generally relates to the field of video compression. In particular, the present invention is directed to methods and systems of adaptive geometric partitioning.

BACKGROUND

A video codec can include an electronic circuit or software that compresses or decompresses digital video. It can convert uncompressed video to a compressed format or vice versa. In the context of video compression, a device that compresses video (and/or performs some function thereof) can typically be called an encoder, and a device that decompresses video (and/or performs some function thereof) can be called a decoder.

A format of the compressed data can conform to a standard video compression specification. The compression can be lossy in that the compressed video lacks some information present in the original video. A consequence of this can include that decompressed video can have lower quality than the original uncompressed video because there is insufficient information to accurately reconstruct the original video.

There can be complex relationships between the video quality, the amount of data used to represent the video (e.g., determined by the bit rate), the complexity of the encoding and decoding algorithms, sensitivity to data losses and errors, ease of editing, random access, end-to-end delay (e.g., latency), and the like.

Motion compensation can include an approach to predict a video frame or a portion thereof given a reference frame, such as previous and/or future frames, by accounting for motion of the camera and/or objects in the video. It can be employed in the encoding and decoding of video data for video compression, for example in the encoding and decoding using the Motion Picture Experts Group (MPEG)'s advanced video coding (AVC) standard (also referred to as H.264). Motion compensation can describe a picture in terms of the transformation of a reference picture to the current picture. The reference picture can be previous in time when compared to the current picture, from the future when compared to the current picture. When images can be accurately synthesized from previously transmitted and/or stored images, compression efficiency can be improved.

SUMMARY OF THE DISCLOSURE

In an aspect, a decoder comprising circuitry configured to receive a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary non-parallel to and intersecting the at least a first partition boundary, partition the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions, determine a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function a line segment slope angle, determine a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector, and decode the current block using the first motion vector and the second motion vector, wherein decoding further comprises smoothing the first predictor and the second predictor across the at least a first partition boundary, and adding residual pixel values to the first predictor and the second predictor.

In another aspect, a method includes receiving, by a decoder, a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary non-parallel to and intersecting the at least a first partition boundary, partitioning, by the decoder, the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions, determining, by the decoder, a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function a line segment slope angle, determining, by the decoder, a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector, and decoding, by the decoder, the current block using the first motion vector and the second motion vector, wherein decoding further comprises smoothing the first predictor and the second predictor across the at least a first partition boundary, and adding residual pixel values to the first predictor and the second predictor

In an embodiment, a decoder may include circuitry configured to receive a bitstream, select a current block, determine, from the bitstream, a number of geometric partitioning modes applicable to the current block, identify a geometric partition of the current block as a function of the number of geometric partitioning modes and decode the current block as a function of the geometric partition.

In an embodiment, a method includes receiving, at a decoder, a bitstream, selecting, by the decoder, a current block, determining, by the decoder and from the bitstream, a number of geometric partitioning modes applicable to the current block, identifying, by the decoder, a geometric partition of the current block as a function of the number of geometric partitioning modes, and decoding, by the decoder, the current block as a function of the geometric partition.

The details of one or more variations of the subject matter described herein are set forth in the accompanying drawings and the description below. Other features and advantages of the subject matter described herein will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

For the purpose of illustrating the invention, the drawings show aspects of one or more embodiments of the invention. However, it should be understood that the present invention is not limited to the precise arrangements and instrumentalities shown in the drawings, wherein:

FIG. 1 is a block diagram illustrating an exemplary embodiment of block partitioning;

FIG. 2 is an illustration of an exemplary embodiment of geometric partitioning;

FIG. 3 is an illustration of an exemplary embodiment of geometric partitioning;

FIG. 4 is an illustration of an exemplary embodiment of a set of available angles for geometric partitioning;

FIG. 5 is an illustration of an exemplary embodiment of a set of available angles for geometric partitioning;

FIG. 6 is an illustration of an exemplary embodiment of a set of available angles for geometric partitioning;

FIG. 7 is an illustration of an exemplary embodiment of a set of available angles for geometric partitioning;

FIG. 8 is a process flow diagram illustrating an example process of adaptive geometric partitioning;

FIG. 9 is a system block diagram illustrating an example decoder capable of decoding a bit stream according to some implementations of the current subject matter;

FIG. 10 is a system block diagram illustrating an example video encoder according to some implementations of the current subject matter; and

FIG. 11 is a block diagram of a computing system that can be used to implement any one or more of the methodologies disclosed herein and any one or more portions thereof.

The drawings are not necessarily to scale and may be illustrated by phantom lines, diagrammatic representations, and fragmentary views. In certain instances, details that are not necessary for an understanding of the embodiments or that render other details difficult to perceive may have been omitted. Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Some implementations of the current subject matter include performing inter prediction with regions that have been partitioned with a geometric partitioning mode, as selected from an adaptive number of possible geometric partitioning modes, in which a rectangular block may be divided into two or more non-rectangular regions. Performing inter prediction with non-rectangular blocks that have been partitioned with geometric partitioning an adaptive number of regions may allow partitioning to more closely follow object boundaries, resulting in lower motion compensation prediction error, smaller residuals, and thus improved compression efficiency. During inter prediction, motion compensation may be performed using motion vectors predicted for blocks (e.g., coding units, prediction units, and the like) determined according to a geometric partitioning mode. Motion vectors may be predicted using advanced motion vector prediction (AMVP) and/or via merge mode, where the motion vector is selected from a list of motion vector candidates without encoding a motion vector difference.

The current subject matter may be applied to relatively larger blocks, such as blocks with a size of 128 x 128 or 64 x 64, for example. In some implementations, the geometric partitioning may involve partitioning a current block into an adaptive number of regions, such as two or more regions for a given current block, and a motion information can be determined for each region.

Motion compensation may include an approach to predict a video frame or a portion thereof given the previous and/or future frames by accounting for motion of the camera and/or objects in the video. Motion compensation may be employed in encoding and decoding of video data for video compression, for example in the encoding and decoding using the Motion Picture Experts Group (MPEG)-2 (also referred to as advanced video coding (AVC)) standard. Motion compensation may describe a picture in terms of the transformation of a reference picture to a current picture. A reference picture may be previous in time or from the future when compared to a current picture. When images can be accurately synthesized from previously transmitted and/or stored images, compression efficiency may be improved.

Block partitioning may refer to a method in video coding to find regions of similar motion. Some form of block partitioning may be found in video codec standards including MPEG-2, H.264 (also referred to as AVC or MPEG-4 Part 10), and H.265 (also referred to as High Efficiency Video Coding (HEVC)). In example block partitioning approaches, non-overlapping blocks of a video frame may be partitioned into rectangular sub-blocks to find block partitions that contain pixels with similar motion. This approach can work well when all pixels of a block partition have similar motion. Motion of pixels in a block may be determined relative to previously coded frames.

Referring now to FIG. 1, a diagram illustrating an exemplary embodiment of block partitioning of pixels is presented. An initial rectangular picture or block 100, which may itself be a sub-block (e.g., a node within a coding tree), can be partitioned into rectangular sub-blocks. For example, at 110, block 100 is partitioned into two rectangular sub-blocks 110a and 110b. Sub-blocks 110a and 110b may then be processed separately. As another example, at 120, block 100 may be partitioned into four rectangular sub-blocks 120a, 120b, 120c, and 120d. Sub-blocks may themselves be further divided until it is determined that the pixels within the sub-blocks share the same motion, a minimum block size is reached, or another criteria. When pixels in a sub-block have similar motion, a motion vector may describe the motion of all pixels in that region.

Still referring to FIG. 1, some approaches to video coding can include geometric partitioning, which may be a form of partitioning in which a rectangular block (e.g., as illustrated in FIG. 1) is further divided by a straight line segment into two regions that may be non-rectangular. FIG. 2 illustrates various exemplary geometric partitions that may be formed according to geometric partitioning modes; each geometric partition may be defined by intersecting a block using a line segment. Where a geometric partition divides a block into more than two regions, two or more line segments as described in this disclosure may by used to define the geometric partition; line segments may be specified as overlapping or non-overlapping.

As a further non-limiting example, FIG. 3 is a diagram illustrating an example of geometric partitioning. An exemplary rectangular block 300, which may be described as having a width of M pixels and a height of N pixels, denoted as MxN pixels, may be divided along a straight line segment P_1P_2 304 into two regions, a first region 308 and a second region 312. In an embodiment, and without limitation, rectangular block 300 may have a width of M pixels and a heigh of N pixels comprising a 64 x 64 width and height. In another embodiment, and without limitation, rectangular block 300 may have a width of M pixels and a height of N pixels comprising a 128 x 128 width and height. When pixels in first region 308 have similar motion, a motion vector may describe the motion of all pixels in that region. Motion vector may be used to compress first region 308. Similarly, when pixels in second region 312 have similar motion, an associated motion vector may describe the motion of pixels in the second region 312. Such a geometric partition may be signaled to the receiver (e.g., decoder) by encoding positions P_1 and P_2 (or representations of positions P_1 and P_2) in the video bitstream.

In an embodiment, and still referring to FIG. 3, geometric inter prediction and/or geometric partitioning may be signaled in terms of an angle, denoted in FIG. 3 as a, from the horizontal and displacement b from a point situated at a geometric reference of block, where displacement may be interpreted as any possible form of distance or norm, including without limitation the Euclidean definition of a length of a line segment orthogonal to the line segment forming the partition and terminating at the point at the geometric reference. As used in this disclosure a “geometric reference” is reference point and/or origination point of displacement b that exists within current block. In an embodiment, and without limitation, geometric reference may denote a geometric center, such as but not limited to a central location and/or point of current block For example, and without limitation, geometric inter prediction and/or geometric partitioning may be signaled in terms of an angle, denoted in FIG. 3 as a, from the horizontal and displacement *b* from a point situated at a geometric center of block, where displacement may be interpreted as any possible form of distance or norm, including without limitation the Euclidean definition of a length of a line segment orthogonal to the line segment forming the partition and terminating at the point at the geometric center.

With continued reference to FIG. 3, geometric partitions may have possible modes specified according to potential positions, defined by *b*, and potential angles, defined by *a*, of line segment slopes used to perform such partitions. A number of possible modes may be specified and/or signaled by specifying and/or signaling how many possible values of *a* and/or *b* are available for use in specifying each line segment. As a non-limiting example, possible values for line segment slope angle *a* may be a range of quantized angles of between 0 and 360 degrees with 11.25 degrees of separation, which gives total 32 angles. Further continuing the example, parameter *b* representing a separation line displacement relatively to the geometric reference of the block may have different values; values *a* and *b* may be stored in a table of size 140x(3+5)/8=140 bytes.

Referring now to FIG. 4, a number of possible modes may be signaled and/or specified by defining a range and/or set of possible values for *a*, given a fixed set of possible values for *b*. For instance, and without limitation, a first set of possible modes may be defined by a first set of 32 values for *a*, depicted in FIG. 4 as angles from a horizontal line of rays 0-31, may be combined with a set of possible values of *b*, such as 5, for a total of 140 modes. A second set of modes, which may be smaller, may include specified by a second, potentially smaller, set of possible values of *a* as shown in FIG. 5, which may be derived in a non-limiting example, by removal of angles as defined in larger set; for instance, and without limitation, angles defined by rays 3, 5, 11, 13, 19, 27, and 29 from FIG. 4 may be eliminated from second set of possible angles, resulting in 24 possible angles depicted as a non-limiting example as defined by rays 0 through 23, which in a non-limiting example may be combined with 5 possible values of *b* for a total of 82 possible modes.

As a further non-limiting example, and as depicted for instance in FIG. 6, a third set of modes, which may be smaller, may include specified by a second, potentially smaller, set of possible values of *a*, which may be derived in a non-limiting example, by removal of angles as defined in larger set; for instance, and without limitation, angles defined by rays 5, 7, 17, and 19 from the set of rays as depicted in FIG. 5, may be eliminated from third set of possible angles, resulting in 20 possible angles depicted as a non-limiting example as defined by rays 0 through 19, which in a non-limiting example may be combined with 5 possible values of *b* for a total of 64 possible modes.

Referring now to FIG. 7, and in a further non-limiting example, a fourth set of modes, which may be smaller, may include specified by a second, potentially smaller, set of possible values of *a* , which may be derived in a non-limiting example, by removal of angles as defined in larger set; for instance, and without limitation, angles defined by rays 1, 9, 11, and 19 as depicted in FIG. 6 may be eliminated from fourth set of possible angles, resulting in 16 possible angles, which in a non-limiting example may be combined with 5 possible values of *b* for a total of 50 possible modes.

Although examples described above refer to varying the number of geometric modes by varying the number of angles *a* that may be used, numbers of modes may alternatively be specified by varying the number of values for *b*, either keeping values for *a* fixed, or in combination with variations in sets of possible values for *a*.

Referring now to FIG. 8, an exemplary embodiment of a method 800 of adaptive geometric partitioning is illustrated. At step 805, a bitstream is received, for instance and without limitation at a decoder. Bitstream includes any of the bitstream as described above, in reference to FIGS. 1-7. Bitstream includes a current picture, the current picture includes a current block of pixels with multiple geometric partition boundaries. Current picture includes any of the current picture as described above, in reference to FIGS. 1-7. Bitstream includes at least a first partition boundary partitioning the block into first and second non-rectangular regions. First partition boundary includes any of the first partition boundary as described above, in reference to FIGS. 1-7. Bitstream includes a second partition boundary that is non-parallel to and intersecting the at least a first partition boundary. Second partition boundary includes any of the second partition boundary as described above. In reference to FIGS. 1-7.

Still referring to FIG. 8, at step 810, decoder partitions the second non-rectangular region of the current block. Partition includes any of the partition as described above, in reference to FIGS. 1-7. Decoder partitions the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions. Geometric partitioning mode includes any of the geometric partitioning mode as described above, in reference to FIGS. 1-7. Decoder may determine the geometric partitioning mode as a function of receiving, in the bitstream, a signal identifying the number of partitioning modes, such as an integer value; determination may be performed as a function of the signal. Determining the number of partitioning modes may include receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes, where a label is defined as a datum used to identify a stored number of partitioning modes; as a non-limiting example, a label may include one or more bits in a field corresponding to a signaled number of modes in a sequence parameter set (SPS), picture parameter set (PPS) or the like, such as 2-bitfield corresponding to 4 possible numbers of modes or the like. As a non-limiting example, a label may be used to retrieve a number of modes from a lookup table.

Still referring to FIG. 8, numbers of modes may be identified and/or defined in any manner as disclosed above. For instance, and without limitation, a number of geometric partitioning modes may correspond to a distribution of line segment slope angles. A number of modes may be selected from a plurality of possible mode quantities, which may include at least four distinct possible mode quantities, for instance as described above. As a non-limiting example, a plurality of possible mode quantities may include a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140. Additionally or alternatively, geometric partition may be signaled in bitstream, for instance and without limitation in an SPS or a PPS, including without limitation communication of angle a and/or displacement b as described above, and/or one or more labels, as described above, suitable for looking up such angle and/or displacement, or the like

Still referring to FIG. 8, at step 815, determines a first predictor for use on a first side of the at least a first partition boundary using a first motion vector. First predictor includes any of the first predictor as described above, in reference to FIGS. 1-7. First motion vector includes any of the first motion vector as described above, in reference to FIGS. 1-7. First motion vector extends from the first partition boundary to the second partition boundary as a function of a line segment slope angle. Line segment slope angle includes any of the line segment slope angle as described above, in reference to FIGS. 1-7.

Still referring to FIG. 8, at step 820, method 800 includes determining a second predictor as a function of a second motion vector. Second predictor includes any of the second predictor as described above, in reference to FIGS. 1-7. Second motion vector includes any of the second motion vector as described above, in reference to FIGS. 1-7. Second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector. Geometric reference includes any of the geometric reference as described above, in reference to FIGS. 1-7.

With continued reference to FIG. 8, at step 825, method 800 includes decoding the current block using the first motion vector and the second motion vector. Decoding the current block further comprises smoothing the first predictor and the second predictor across the at least a first partition boundary. First partition boundary includes any of the first partition boundary as described above, in reference to FIGS. 1-7. Decoding the current block further comprises adding residual pixel values to the first predictor and the second predictor. Residual pixel vales includes any of the residual pixel values as described above, in reference to FIGS. 1-7. In an embodiment, and without limitation, decoding current block may include partitioning the current block into a plurality of regions as a function of geometric partition. Decoding may include determining a motion vector associated with at least one region of plurality of regions defined by geometric partition, and decoding current block using the determined motion vector. In an embodiment, bitstream may include a parameter indicating whether the geometric partitioning mode is enabled for the current block; where not enabled, decoder may disregard bitstream parameters regarding numbers of geometric partitioning modes, geometric partition parameters, or the like, and/or such parameters may be excluded from parameter sets such as an SPS, PPS, or the like.

FIG. 9 is a system block diagram illustrating an example decoder 900 capable of decoding a bitstream according to adaptive geometric partitioning as described above. Decoder 900 may include an entropy decoder processor 904, an inverse quantization and inverse transformation processor 908, a deblocking filter 912, a frame buffer 916, a motion compensation processor 920 and/or an intra prediction processor 924.

In operation, and still referring to FIG. 9, bit stream 928 may be received by decoder 900 and input to entropy decoder processor 904, which may entropy decode portions of bit stream into quantized coefficients. Quantized coefficients may be provided to inverse quantization and inverse transformation processor 908, which may perform inverse quantization and inverse transformation to create a residual signal, which may be added to an output of motion compensation processor 920 or intra prediction processor 924 according to a processing mode. An output of the motion compensation processor 920 and intra prediction processor 924 may include a block prediction based on a previously decoded block. A sum of prediction and residual may be processed by deblocking filter 912 and stored in a frame buffer 916.

In an embodiment, and still referring to FIG. 9 decoder 900 may include circuitry configured to implement any operations as described above in any embodiment as described above, in any order and with any degree of repetition. For instance, decoder 900 may be configured to perform a single step or sequence repeatedly until a desired or commanded outcome is achieved; repetition of a step or a sequence of steps may be performed iteratively and/or recursively using outputs of previous repetitions as inputs to subsequent repetitions, aggregating inputs and/or outputs of repetitions to produce an aggregate result, reduction or decrement of one or more variables such as global variables, and/or division of a larger processing task into a set of iteratively addressed smaller processing tasks. Decoder may perform any step or sequence of steps as described in this disclosure in parallel, such as simultaneously and/or substantially simultaneously performing a step two or more times using two or more parallel threads, processor cores, or the like; division of tasks between parallel threads and/or processes may be performed according to any protocol suitable for division of tasks between iterations. Persons skilled in the art, upon reviewing the entirety of this disclosure, will be aware of various ways in which steps, sequences of steps, processing tasks, and/or data may be subdivided, shared, or otherwise dealt with using iteration, recursion, and/or parallel processing.

FIG. 10 is a system block diagram illustrating an example video encoder 1000 capable of encoding for adaptive geometric partitioning as described above. The example video encoder 1000 receives an input video 1005, which can be initially segmented or dividing according to a processing scheme, such as a tree-structured macro block partitioning scheme (e.g., quad-tree plus binary tree). An example of a tree-structured macro block partitioning scheme can include partitioning a picture frame into large block elements called coding tree units (CTU). In some implementations, each CTU can be further partitioned one or more times into a number of sub-blocks called coding units (CU). The final result of this portioning can include a group of sub-blocks that can be called predictive units (PU). Transform units (TU) can also be utilized.

Still referring to FIG. 10, example video encoder 1000 includes an intra prediction processor 1015, a motion estimation/compensation processor 1020 (also referred to as an inter-prediction processor) capable of supporting adaptive cropping, a transform /quantization processor 1025, an inverse quantization/inverse transform processor 1030, an in-loop filter 1035, a decoded picture buffer 1040, and an entropy coding processor 1045. Bit stream parameters can be input to the entropy coding processor 1045 for inclusion in the output bit stream 1050.

In operation, and continuing to refer to FIG. 10, for each block of a frame of the input video 1005, whether to process the block via intra picture prediction or using motion estimation / compensation can be determined. The block can be provided to the intra prediction processor 1010 or the motion estimation / compensation processor 1020. If the block is to be processed via intra prediction, the intra prediction processor 1010 can perform the processing to output the predictor. If the block is to be processed via motion estimation / compensation, the motion estimation / compensation processor 1020 can perform the processing including using adaptive cropping, if applicable.

Still referring to FIG. 10, residual can be formed by subtracting the predictor from the input video. The residual can be received by the transform/quantization processor 1025, which can perform transformation processing (e.g., discrete cosine transform (DCT)) to produce coefficients, which can be quantized. The quantized coefficients and any associated signaling information can be provided to the entropy coding processor 1045 for entropy encoding and inclusion in the output bit stream 1050. The entropy encoding processor 1045 can support encoding of signaling information related to encoding the current block. In addition, the quantized coefficients can be provided to the inverse quantization/inverse transformation processor 1030, which can reproduce pixels, which can be combined with the predictor and processed by the in loop filter 1035, the output of which is stored in the decoded picture buffer 1040 for use by the motion estimation / compensation processor 1020 that is capable of adaptive cropping.

With continued reference to FIG. 10, although a few variations have been described in detail above, other modifications or additions are possible. For example, in some implementations, current blocks can include any symmetric blocks (8x8, 16x16, 32x32, 64x64, 128 x 128, and the like) as well as any asymmetric block (8x4, 16x8, and the like).

Still referring to FIG. 10, in some implementations, a quadtree plus binary decision tree (QTBT) can be implemented. In QTBT, at the Coding Tree Unit level, the partition parameters of QTBT are dynamically derived to adapt to the local characteristics without transmitting any overhead. Subsequently, at the Coding Unit level, a joint-classifier decision tree structure can eliminate unnecessary iterations and control the risk of false prediction. In some implementations, LTR frame block update mode can be available as an additional option available at every leaf node of the QTBT.

In some implementations, and with continued reference to FIG. 10, additional syntax elements can be signaled at different hierarchy levels of the bit stream. For example, a flag can be enabled for an entire sequence by including an enable flag coded in a Sequence Parameter Set (SPS). Further, a CTU flag can be coded at the coding tree unit (CTU) level.

Still referring to FIG. 10, encoder 1000 may include circuitry configured to implement any operations as described above in reference to FIGS. 8 or 10 in any embodiment, in any order and with any degree of repetition. For instance, encoder 1000 may be configured to perform a single step or sequence repeatedly until a desired or commanded outcome is achieved; repetition of a step or a sequence of steps may be performed iteratively and/or recursively using outputs of previous repetitions as inputs to subsequent repetitions, aggregating inputs and/or outputs of repetitions to produce an aggregate result, reduction or decrement of one or more variables such as global variables, and/or division of a larger processing task into a set of iteratively addressed smaller processing tasks. Encoder 1000 may perform any step or sequence of steps as described in this disclosure in parallel, such as simultaneously and/or substantially simultaneously performing a step two or more times using two or more parallel threads, processor cores, or the like; division of tasks between parallel threads and/or processes may be performed according to any protocol suitable for division of tasks between iterations. Persons skilled in the art, upon reviewing the entirety of this disclosure, will be aware of various ways in which steps, sequences of steps, processing tasks, and/or data may be subdivided, shared, or otherwise dealt with using iteration, recursion, and/or parallel processing.

With continued reference to FIG. 10, non-transitory computer program products (i.e., physically embodied computer program products) may store instructions, which when executed by one or more data processors of one or more computing systems, causes at least one data processor to perform operations, and/or steps thereof described in this disclosure, including without limitation any operations described above and/or any operations decoder 700 and/or encoder 1000 may be configured to perform. Similarly, computer systems are also described that may include one or more data processors and memory coupled to the one or more data processors. The memory may temporarily or permanently store instructions that cause at least one processor to perform one or more of the operations described herein. In addition, methods can be implemented by one or more data processors either within a single computing system or distributed among two or more computing systems. Such computing systems can be connected and can exchange data and/or commands or other instructions or the like via one or more connections, including a connection over a network (e.g. the Internet, a wireless wide area network, a local area network, a wide area network, a wired network, or the like), via a direct connection between one or more of the multiple computing systems, or the like.

Embodiments described in this disclosure may include a decoder including circuitry configured to receive a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary, non-parallel to and intersecting the at least a first partition boundary, partition the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions, determine a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function of a line segment slope angle, determine a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector, and decode the current block using the first motion vector and the second motion vector, wherein decoding further includes smoothing the first predictor and the second predictor across the at least a first partition boundary and adding residual pixel values to the first predictor and the second predictor.

In an embodiment, a decoder may be further configured to determine a number of partitioning modes by receiving, in the bitstream, a signal identifying the number of partitioning modes. A decoder may be further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes. In some embodiments, the number of geometric partitioning modes may correspond to a distribution of line segment slope angles. In an embodiment, a number of geometric partitioning modes may be selected from a plurality of possible mode quantities. In an embodiment, a plurality of possible mode quantities may include at least four distinct possible mode quantities. In an embodiment, a plurality of possible mode quantities may include a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes. In some embodiments, a geometric partition of a current block may be signaled in the bitstream. A decoder may be further configured to decode a current block by partitioning the current block into a plurality of regions as a function of geometric partition. Decoder may be further configured to determine a motion vector associated with at least one region of plurality of regions and decode the current block using the determined motion vector. A bitstream may include a parameter indicating whether the geometric partitioning mode is enabled for the current block. Decoder may include an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients, an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform, a deblocking filter, a frame buffer, and an intra prediction processor. A current block may form part of a quadtree plus binary decision tree. A current block may include a non-leaf node of the quadtree plus binary decision tree. A current block may include a coding tree unit or a coding unit. A current block may include a coding unit or a prediction unit.

In an embodiment, a method includes receiving, by a decoder, a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary, non-parallel to and intersecting the at least a first partition boundary, partitioning, by the decoder, the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions, determining, by the decoder, a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function of a line segment slope angle, determining, by the decoder, a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector, and decoding, by the decoder, the current block using the first motion vector and the second motion vector, wherein decoding further includes smoothing the first predictor and the second predictor across the at least a first partition boundary and adding residual pixel values to the first predictor and the second predictor.

In an embodiment, determining a number of partitioning modes may include receiving, in the bitstream, a signal identifying the number of partitioning modes. In some embodiments, determining a number of partitioning modes may include receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes. In some embodiments, a number of geometric partitioning modes corresponds to a distribution of line segment slope angles. In some embodiments, a number of modes may be selected from a plurality of possible mode quantities. In some embodiments, a plurality of possible mode quantities may include at least four distinct possible mode quantities. A plurality of possible mode quantities may include a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes. A geometric partition of the current block may be signaled in the bitstream. Decoding a current block may include partitioning the current block into a plurality of regions as a function of the geometric partition. Some embodiments may include determining a motion vector associated with at least one region of a plurality of regions and decoding a current block using the determined motion vector. In some embodiments, bitstream may include a parameter indicating whether the geometric partitioning mode is enabled for the current block. Decoder may include an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients, an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform, a deblocking filter, a frame buffer, and an intra prediction processor. A current block may form part of a quadtree plus binary decision tree. The current block may be a non-leaf node of the quadtree plus binary decision tree. Current block may include a coding tree unit or a coding unit. Current block may include a coding unit or a prediction unit.

In an embodiment, a decoder may include circuitry configured to receive a bitstream, select a current block, determine, from the bitstream, a number of geometric partitioning modes applicable to the current block, identify a geometric partition of the current block as a function of the number of geometric partitioning modes and decode the current block as a function of the geometric partition. Decoder may be further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying the number of partitioning modes. Decoder may be further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes. A number of geometric partitioning modes may correspond to a distribution of line segment slope angles. A number of modes may be selected from a plurality of possible mode quantities. The plurality of possible mode quantities may include at least four distinct possible mode quantities. The plurality of possible mode quantities may include a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes. The geometric partition of the current block may be signaled in the bitstream. Decoder may be further configured to decode the current block by partitioning the current block into a plurality of regions as a function of the geometric partition. Decoder may be further configured to determine a motion vector associated with at least one region of the plurality of regions and decode the current block using the determined motion vector. Bitstream may include a parameter indicating whether a geometric partitioning mode is enabled for the current block. Decoder may include an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients, an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform, a deblocking filter, a frame buffer, and an intra prediction processor. The current block may form part of a quadtree plus binary decision tree. The current block may be a non-leaf node of the quadtree plus binary decision tree. The current block may include a coding tree unit or a coding unit. The current block may include a coding unit or a prediction unit.

In an embodiment, a method includes receiving, at a decoder, a bitstream, selecting, by the decoder, a current block, determining, by the decoder and from the bitstream, a number of geometric partitioning modes applicable to the current block, identifying, by the decoder, a geometric partition of the current block as a function of the number of geometric partitioning modes, and decoding, by the decoder, the current block as a function of the geometric partition. Determining the number of partitioning modes may include receiving, in the bitstream, a signal identifying the number of partitioning modes. Determining the number of partitioning modes may include receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes. The number of geometric partitioning modes may correspond to a distribution of line segment slope angles. The number of modes may be selected from a plurality of possible mode quantities. The plurality of possible mode quantities may include at least four distinct possible mode quantities. The plurality of possible mode quantities may include a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes. The geometric partition of the current block may be signaled in the bitstream. Decoding the current block may include partitioning the current block into a plurality of regions as a function of the geometric partition.

The method may include determining a motion vector associated with at least one region of the plurality of regions and decoding the current block using the determined motion vector. The bitstream may include a parameter indicating whether the geometric partitioning mode is enabled for the current block. The decoder may include an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients, an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform, a deblocking filter, a frame buffer, and an intra prediction processor. The current block may form part of a quadtree plus binary decision tree. The current block may include a non-leaf node of the quadtree plus binary decision tree. The current block may include a coding tree unit or a coding unit. The current block may include a coding unit or a prediction unit.

It is to be noted that any one or more of the aspects and embodiments described herein may be conveniently implemented using one or more machines (*e.g.*, one or more computing devices that are utilized as a user computing device for an electronic document, one or more server devices, such as a document server, etc.) programmed according to the teachings of the present specification, as will be apparent to those of ordinary skill in the computer art. Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present disclosure, as will be apparent to those of ordinary skill in the software art. Aspects and implementations discussed above employing software and/or software modules may also include appropriate hardware for assisting in the implementation of the machine executable instructions of the software and/or software module.

Such software may be a computer program product that employs a machine-readable storage medium. A machine-readable storage medium may be any medium that is capable of storing and/or encoding a sequence of instructions for execution by a machine (*e.g.*, a computing device) and that causes the machine to perform any one of the methodologies and/or embodiments described herein. Examples of a machine-readable storage medium include, but are not limited to, a magnetic disk, an optical disc (*e.g.*, CD, CD-R, DVD, DVD-R, etc.), a magnetooptical disk, a read-only memory "ROM" device, a random access memory "RAM" device, a magnetic card, an optical card, a solid-state memory device, an EPROM, an EEPROM, and any combinations thereof. A machine-readable medium, as used herein, is intended to include a single medium as well as a collection of physically separate media, such as, for example, a collection of compact discs or one or more hard disk drives in combination with a computer memory. As used herein, a machine-readable storage medium does not include transitory forms of signal transmission.

Such software may also include information (*e.g.*, data) carried as a data signal on a data carrier, such as a carrier wave. For example, machine-executable information may be included as a data-carrying signal embodied in a data carrier in which the signal encodes a sequence of instruction, or portion thereof, for execution by a machine (*e.g.*, a computing device) and any related information (*e.g.*, data structures and data) that causes the machine to perform any one of the methodologies and/or embodiments described herein.

Examples of a computing device include, but are not limited to, an electronic book reading device, a computer workstation, a terminal computer, a server computer, a handheld device (*e.g.*, a tablet computer, a smartphone, etc.), a web appliance, a network router, a network switch, a network bridge, any machine capable of executing a sequence of instructions that specify an action to be taken by that machine, and any combinations thereof. In one example, a computing device may include and/or be included in a kiosk.

FIG. 11 shows a diagrammatic representation of one embodiment of a computing device in the exemplary form of a computer system 1100 within which a set of instructions for causing a control system to perform any one or more of the aspects and/or methodologies of the present disclosure may be executed. It is also contemplated that multiple computing devices may be utilized to implement a specially configured set of instructions for causing one or more of the devices to perform any one or more of the aspects and/or methodologies of the present disclosure. Computer system 1100 includes a processor 1104 and a memory 1108 that communicate with each other, and with other components, via a bus 1112. Bus 1112 may include any of several types of bus structures including, but not limited to, a memory bus, a memory controller, a peripheral bus, a local bus, and any combinations thereof, using any of a variety of bus architectures.

Processor 1104 may include any suitable processor, such as without limitation a processor incorporating logical circuitry for performing arithmetic and logical operations, such as an arithmetic and logic unit (ALU), which may be regulated with a state machine and directed by operational inputs from memory and/or sensors; processor 1104 may be organized according to Von Neumann and/or Harvard architecture as a non-limiting example. Processor 1104 may include, incorporate, and/or be incorporated in, without limitation, a microcontroller, microprocessor, digital signal processor (DSP), Field Programmable Gate Array (FPGA), Complex Programmable Logic Device (CPLD), Graphical Processing Unit (GPU), general purpose GPU, Tensor Processing Unit (TPU), analog or mixed signal processor, Trusted Platform Module (TPM), a floating point unit (FPU), and/or system on a chip (SoC)

Memory 1108 may include various components (*e.g.*, machine-readable media) including, but not limited to, a random-access memory component, a read only component, and any combinations thereof. In one example, a basic input/output system 1116 (BIOS), including basic routines that help to transfer information between elements within computer system 1100, such as during start-up, may be stored in memory 1108. Memory 1108 may also include (*e.g.*, stored on one or more machine-readable media) instructions (*e.g.*, software) 1120 embodying any one or more of the aspects and/or methodologies of the present disclosure. In another example, memory 1108 may further include any number of program modules including, but not limited to, an operating system, one or more application programs, other program modules, program data, and any combinations thereof.

Computer system 1100 may also include a storage device 1124. Examples of a storage device (*e.g.*, storage device 1124) include, but are not limited to, a hard disk drive, a magnetic disk drive, an optical disc drive in combination with an optical medium, a solid-state memory device, and any combinations thereof. Storage device 1124 may be connected to bus 1112 by an appropriate interface (not shown). Example interfaces include, but are not limited to, SCSI, advanced technology attachment (ATA), serial ATA, universal serial bus (USB), IEEE 1394 (FIREWIRE), and any combinations thereof. In one example, storage device 1124 (or one or more components thereof) may be removably interfaced with computer system 1100 (*e.g.*, via an external port connector (not shown)). Particularly, storage device 1124 and an associated machine-readable medium 1128 may provide nonvolatile and/or volatile storage of machine-readable instructions, data structures, program modules, and/or other data for computer system

1100. In one example, software 1120 may reside, completely or partially, within machine-readable medium 1128. In another example, software 1120 may reside, completely or partially, within processor 1104.

Computer system 1100 may also include an input device 1132. In one example, a user of computer system 1100 may enter commands and/or other information into computer system 1100 via input device 1132. Examples of an input device 1132 include, but are not limited to, an alpha-numeric input device (*e.g.*, a keyboard), a pointing device, a joystick, a gamepad, an audio input device (*e.g.*, a microphone, a voice response system, etc.), a cursor control device (*e.g.*, a mouse), a touchpad, an optical scanner, a video capture device (*e.g.*, a still camera, a video camera), a touchscreen, and any combinations thereof. Input device 1132 may be interfaced to bus 1112 via any of a variety of interfaces (not shown) including, but not limited to, a serial interface, a parallel interface, a game port, a USB interface, a FIREWIRE interface, a direct interface to bus 1112, and any combinations thereof. Input device 1132 may include a touch screen interface that may be a part of or separate from display 1136, discussed further below. Input device 1132 may be utilized as a user selection device for selecting one or more graphical representations in a graphical interface as described above.

A user may also input commands and/or other information to computer system 1100 via storage device 1124 (*e.g.*, a removable disk drive, a flash drive, etc.) and/or network interface device 1140. A network interface device, such as network interface device 1140, may be utilized for connecting computer system 1100 to one or more of a variety of networks, such as network 1144, and one or more remote devices 1148 connected thereto. Examples of a network interface device include, but are not limited to, a network interface card (*e.g.*, a mobile network interface card, a LAN card), a modem, and any combination thereof. Examples of a network include, but are not limited to, a wide area network (*e.g.*, the Internet, an enterprise network), a local area network (*e.g.*, a network associated with an office, a building, a campus or other relatively small geographic space), a telephone network, a data network associated with a telephone/voice provider (*e.g.*, a mobile communications provider data and/or voice network), a direct connection between two computing devices, and any combinations thereof. A network, such as network 1144, may employ a wired and/or a wireless mode of communication. In general, any network topology may be used. Information (*e.g.*, data, software 1120, etc.) may be communicated to and/or from computer system 1100 via network interface device 1140.

Computer system 1100 may further include a video display adapter 1152 for communicating a displayable image to a display device, such as display device 1136. Examples of a display device include, but are not limited to, a liquid crystal display (LCD), a cathode ray tube (CRT), a plasma display, a light emitting diode (LED) display, and any combinations thereof. Display adapter 1152 and display device 1136 may be utilized in combination with processor 1104 to provide graphical representations of aspects of the present disclosure. In addition to a display device, computer system 1100 may include one or more other peripheral output devices including, but not limited to, an audio speaker, a printer, and any combinations thereof. Such peripheral output devices may be connected to bus 1112 via a peripheral interface 1156. Examples of a peripheral interface include, but are not limited to, a serial port, a USB connection, a FIREWIRE connection, a parallel connection, and any combinations thereof.

The foregoing has been a detailed description of illustrative embodiments of the invention. Various modifications and additions can be made without departing from the spirit and scope of this invention. Features of each of the various embodiments described above may be combined with features of other described embodiments as appropriate in order to provide a multiplicity of feature combinations in associated new embodiments. Furthermore, while the foregoing describes a number of separate embodiments, what has been described herein is merely illustrative of the application of the principles of the present invention. Additionally, although particular methods herein may be illustrated and/or described as being performed in a specific order, the ordering is highly variable within ordinary skill to achieve methods, systems, and software according to the present disclosure. Accordingly, this description is meant to be taken only by way of example, and not to otherwise limit the scope of this invention.

Exemplary embodiments have been disclosed above and illustrated in the accompanying drawings. It will be understood by those skilled in the art that various changes, omissions and additions may be made to that which is specifically disclosed herein without departing from the spirit and scope of the present invention.

In the descriptions above and in the claims, phrases such as “at least one of” or “one or more of” may occur followed by a conjunctive list of elements or features. The term “and/or” may also occur in a list of two or more elements or features. Unless otherwise implicitly or explicitly contradicted by the context in which it is used, such a phrase is intended to mean any of the listed elements or features individually or any of the recited elements or features in combination with any of the other recited elements or features. For example, the phrases “at least one of A and B;” “one or more of A and B;” and “A and/or B” are each intended to mean “A alone, B alone, or A and B together.” A similar interpretation is also intended for lists including three or more items. For example, the phrases “at least one of A, B, and C;” “one or more of A, B, and C;” and “A, B, and/or C” are each intended to mean “A alone, B alone, C alone, A and B together, A and C together, B and C together, or A and B and C together.” In addition, use of the term “based on,” above and in the claims is intended to mean, “based at least in part on,” such that an unrecited feature or element is also permissible.

The subject matter described herein can be embodied in systems, apparatus, methods, and/or articles depending on the desired configuration. The implementations set forth in the foregoing description do not represent all implementations consistent with the subject matter described herein. Instead, they are merely some examples consistent with aspects related to the described subject matter. Although a few variations have been described in detail above, other modifications or additions are possible. In particular, further features and/or variations can be provided in addition to those set forth herein. For example, the implementations described above can be directed to various combinations and sub-combinations of the disclosed features and/or combinations and sub-combinations of several further features disclosed above. In addition, the logic flows depicted in the accompanying figures and/or described herein do not necessarily require the particular order shown, or sequential order, to achieve desirable results. Other implementations may be within the scope of the following claims.

WHAT IS CLAIMED IS:

1. A decoder, the decoder comprising circuitry configured to:

receive a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary, non-parallel to and intersecting the at least a first partition boundary;

partition the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions;

determine a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function of a line segment slope angle;

determine a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector; and

decode the current block using the first motion vector and the second motion vector, wherein decoding further comprises:

smoothing the first predictor and the second predictor across the at least a first partition boundary; and

adding residual pixel values to the first predictor and the second predictor.

2. The decoder of claim 1, further configured to determine a number of partitioning modes by receiving, in the bitstream, a signal identifying the number of partitioning modes.

3. The decoder of claim 2, further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes.

4. The decoder of claim 2, wherein the number of geometric partitioning modes corresponds to a distribution of line segment slope angles.

5. The decoder of claim 2, wherein the number of geometric partitioning modes is selected from a plurality of possible mode quantities.

6. The decoder of claim 5, wherein the plurality of possible mode quantities includes at least four distinct possible mode quantities.

7. The decoder of claim 5, wherein the plurality of possible mode quantities includes a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes.

8. The decoder of claim 1, wherein the geometric partition of the current block is signaled in the bitstream.

9. The decoder of claim 1, further configured to decode the current block by partitioning the current block into a plurality of regions as a function of the geometric partition.

10. The decoder of claim 9, further configured to:

determine a motion vector associated with at least one region of the plurality of regions; and

decode the current block using the determined motion vector.

11. The decoder of claim 1, wherein the bitstream includes a parameter indicating whether the geometric partitioning mode is enabled for the current block.

12. The decoder of claim 1, further comprising:

an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients;

an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform;

a deblocking filter;

a frame buffer; and

an intra prediction processor.

13. The decoder of claim 1, wherein the current block forms part of a quadtree plus binary decision tree.

14. The decoder of claim 13, wherein the current block is a non-leaf node of the quadtree plus binary decision tree.

15. The decoder of claim 1, wherein the current block is a coding tree unit or a coding unit.

16. The decoder of claim 1, wherein the current block is a coding unit or a prediction unit.

17. A method, the method comprising:

receiving, by a decoder, a bitstream, wherein the bitstream includes a current picture, the current picture including a current block of pixels with multiple geometric partition boundaries, at least a first partition boundary partitioning the block into first and second non-rectangular regions, and a second partition boundary, non-parallel to and intersecting the at least a first partition boundary;

partitioning, by the decoder, the second non-rectangular region of the current block via a geometric partitioning mode to partition the current block into three portions;

determining, by the decoder, a first predictor for use on a first side of the at least a first partition boundary using a first motion vector, wherein the first motion vector extends from the first partition boundary to the second partition boundary as a function of a line segment slope angle;

determining, by the decoder, a second predictor as a function of a second motion vector, wherein the second motion vector originates at a geometric reference of the current block of pixels and extends to the first motion vector; and

decoding, by the decoder, the current block using the first motion vector and the second motion vector, wherein decoding further comprises:

smoothing the first predictor and the second predictor across the at least a first partition boundary; and

adding residual pixel values to the first predictor and the second predictor.

18. The method of claim 17, wherein determining the number of partitioning modes further comprises receiving, in the bitstream, a signal identifying the number of partitioning modes.

19. The method of claim 17, wherein determining the number of partitioning modes further comprises receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes.

20. The method of claim 17, wherein the number of geometric partitioning modes corresponds to a distribution of line segment slope angles.

21. The method of claim 17, wherein the number of modes is selected from a plurality of possible mode quantities.

22. The method of claim 21, wherein the plurality of possible mode quantities includes at least four distinct possible mode quantities.

23. The method of claim 21, wherein the plurality of possible mode quantities includes a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes.

24. The method of claim 17, wherein the geometric partition of the current block is signaled in the bitstream.

25. The method of claim 17, wherein decoding the current block further comprises partitioning the current block into a plurality of regions as a function of the geometric partition.

26. The method of claim 25 further comprising:

determining a motion vector associated with at least one region of the plurality of regions; and

decoding the current block using the determined motion vector.

27. The method of claim 17, wherein the bitstream includes a parameter indicating whether the geometric partitioning mode is enabled for the current block.

28. The method of claim 17, wherein the decoder further comprises:

an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients;

an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform;

a deblocking filter;

a frame buffer; and

an intra prediction processor.

29. The method of claim 17, wherein the current block forms part of a quadtree plus binary decision tree.

30. The method of claim 29, wherein the current block is a non-leaf node of the quadtree plus binary decision tree.

31. The method of claim 17, wherein the current block is a coding tree unit or a coding unit.

32. The method of claim 17, wherein the current block is a coding unit or a prediction unit.

33. A decoder, the decoder comprising circuitry configured to:

receive a bitstream;

select a current block;

determine, from the bitstream, a number of geometric partitioning modes applicable to the current block;

identify a geometric partition of the current block as a function of the number of geometric partitioning modes; and

decode the current block as a function of the geometric partition.

34. The decoder of claim 33, further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying the number of partitioning modes.

35. The decoder of claim 33, further configured to determine the number of partitioning modes by receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes.

36. The decoder of claim 33, wherein the number of geometric partitioning modes corresponds to a distribution of line segment slope angles.

37. The decoder of claim 33, wherein the number of modes is selected from a plurality of possible mode quantities.

38. The decoder of claim 37, wherein the plurality of possible mode quantities includes at least four distinct possible mode quantities.

39. The decoder of claim 37, wherein the plurality of possible mode quantities includes a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes.

40. The decoder of claim 33, wherein the geometric partition of the current block is signaled in the bitstream.

41. The decoder of claim 33, further configured to decode the current block by partitioning the current block into a plurality of regions as a function of the geometric partition.

42. The decoder of claim 41, further configured to:

determine a motion vector associated with at least one region of the plurality of regions; and

decode the current block using the determined motion vector.

43. The decoder of claim 33, wherein the bitstream includes a parameter indicating

whether the geometric partitioning mode is enabled for the current block.

44. The decoder of claim 33, further comprising:

an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients;

an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform;

a deblocking filter;

a frame buffer; and

an intra prediction processor.

45. The decoder of claim 33, wherein the current block forms part of a quadtree plus binary decision tree.

46. The decoder of claim 45, wherein the current block is a non-leaf node of the quadtree plus binary decision tree.

47. The decoder of claim 33, wherein the current block is a coding tree unit or a coding unit.

48. The decoder of claim 33, wherein the current block is a coding unit or a prediction unit.

49. A method, the method comprising:

receiving, at a decoder, a bitstream;

selecting, by the decoder, a current block;

determining, by the decoder and from the bitstream, a number of geometric partitioning modes applicable to the current block;

identifying, by the decoder, a geometric partition of the current block as a function of the number of geometric partitioning modes; and

decoding, by the decoder, the current block as a function of the geometric partition.

50. The method of claim 49, wherein determining the number of partitioning modes further comprises receiving, in the bitstream, a signal identifying the number of partitioning modes.

51. The method of claim 49, wherein determining the number of partitioning modes further comprises receiving, in the bitstream, a signal identifying a label corresponding to a number of partitioning modes.

52. The method of claim 49, wherein the number of geometric partitioning modes corresponds to a distribution of line segment slope angles.

53. The method of claim 49, wherein the number of modes is selected from a plurality of possible mode quantities.

54. The method of claim 53, wherein the plurality of possible mode quantities includes at least four distinct possible mode quantities.

55. The method of claim 53, wherein the plurality of possible mode quantities includes a possible mode quantity of 50 modes, a possible mode quantity of 64 modes, a possible mode quantity of 82 modes, and a possible mode quantity of 140 modes.

56. The method of claim 49, wherein the geometric partition of the current block is signaled in the bitstream.

57. The method of claim 49, wherein decoding the current block further comprises partitioning the current block into a plurality of regions as a function of the geometric partition.

58. The method of claim 57 further comprising:

determining a motion vector associated with at least one region of the plurality of regions; and

decoding the current block using the determined motion vector.

59. The method of claim 49, wherein the bitstream includes a parameter indicating whether the geometric partitioning mode is enabled for the current block.

60. The method of claim 49, wherein the decoder further comprises:

an entropy decoder processor configured to receive the bitstream and decode the bitstream into quantized coefficients;

an inverse quantization and inverse transformation processor configured to process the quantized coefficients including performing an inverse discrete cosine transform;

a deblocking filter;

a frame buffer; and

an intra prediction processor.

61. The method of claim 49, wherein the current block forms part of a quadtree plus binary decision tree.

62. The method of claim 61, wherein the current block is a non-leaf node of the quadtree plus binary decision tree.

63. The method of claim 49, wherein the current block is a coding tree unit or a coding unit.

64. The method of claim 49, wherein the current block is a coding unit or a prediction unit.

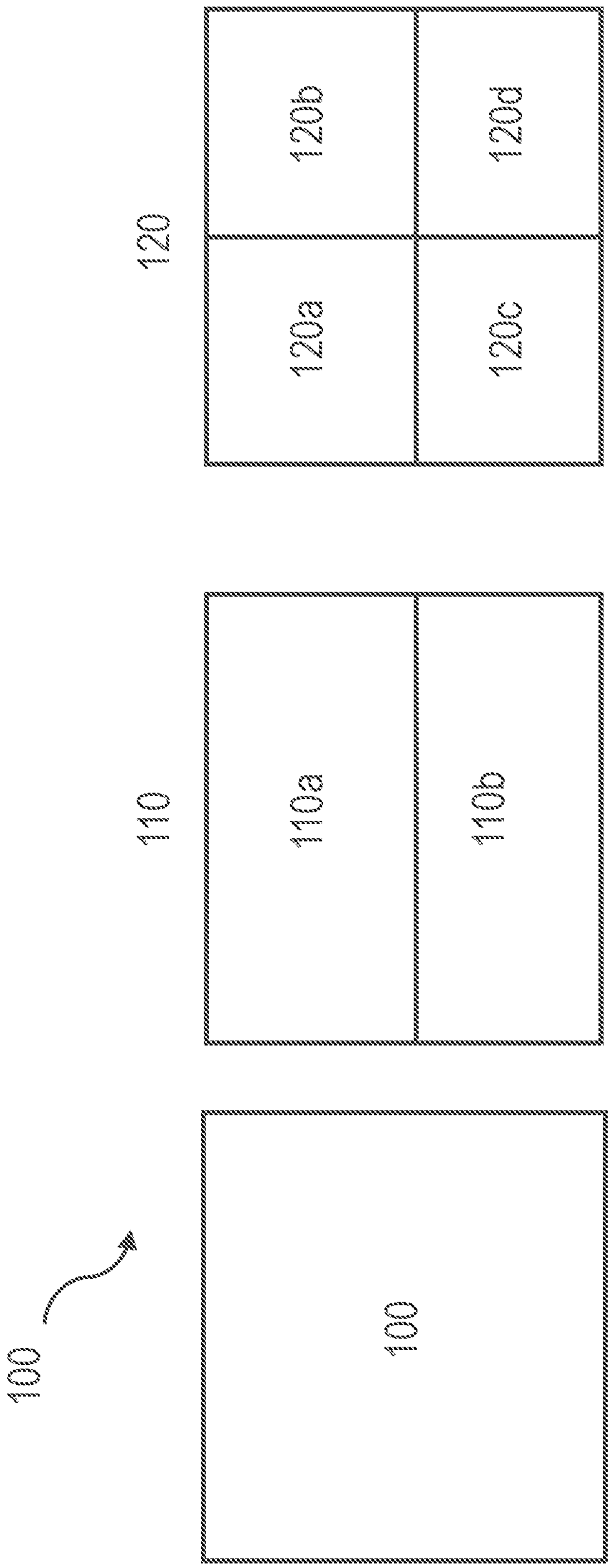


FIG. 1

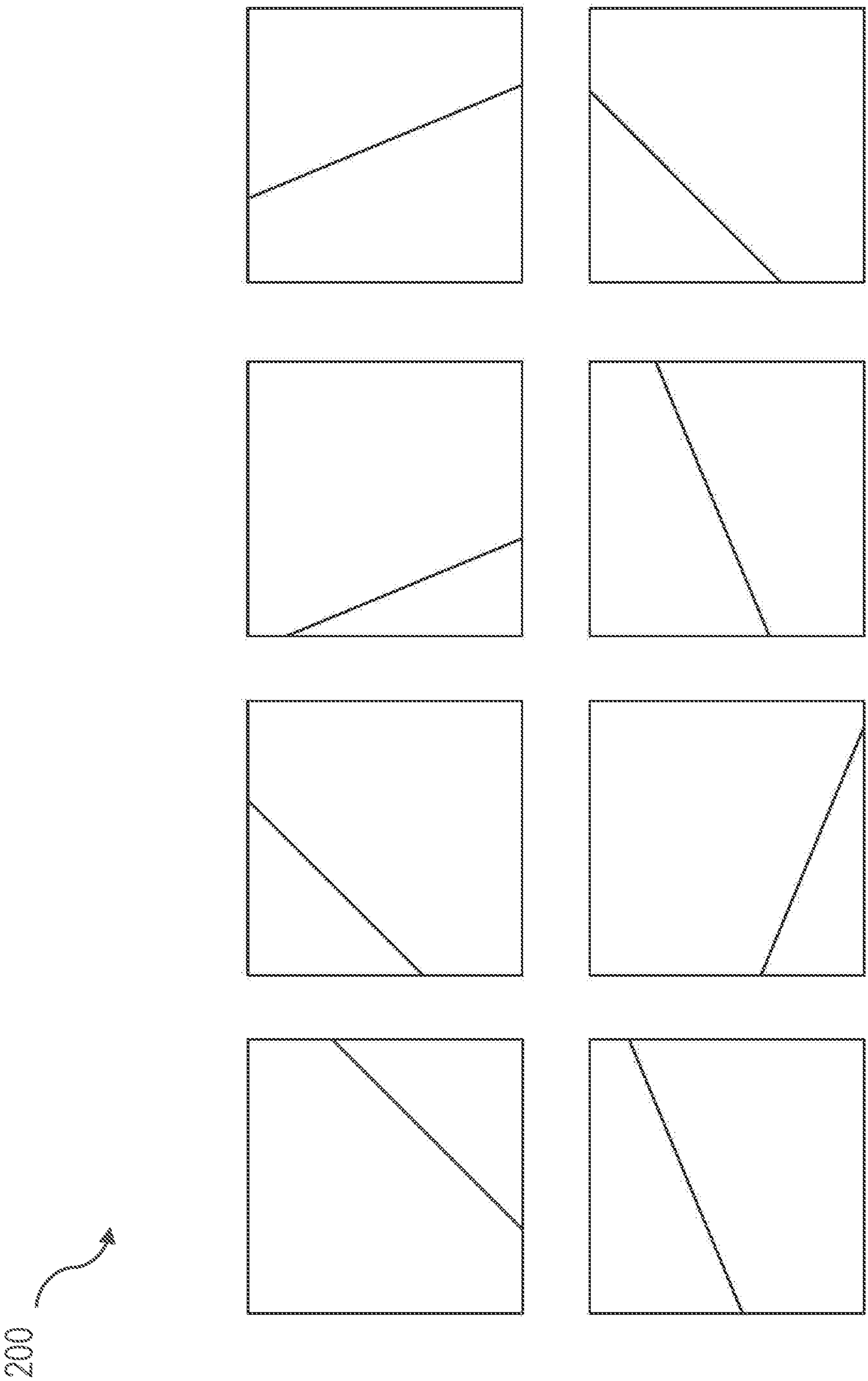


FIG. 2

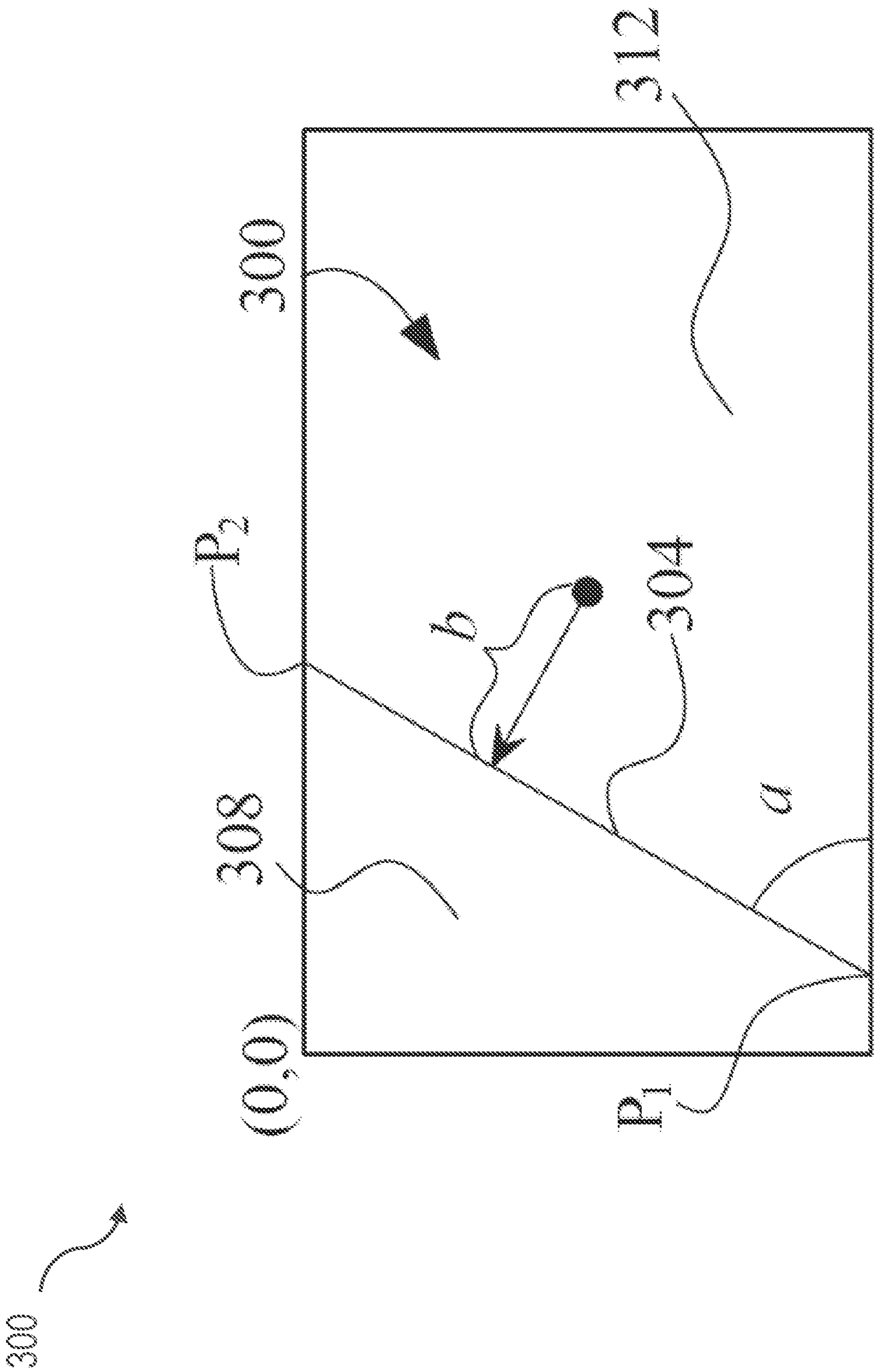
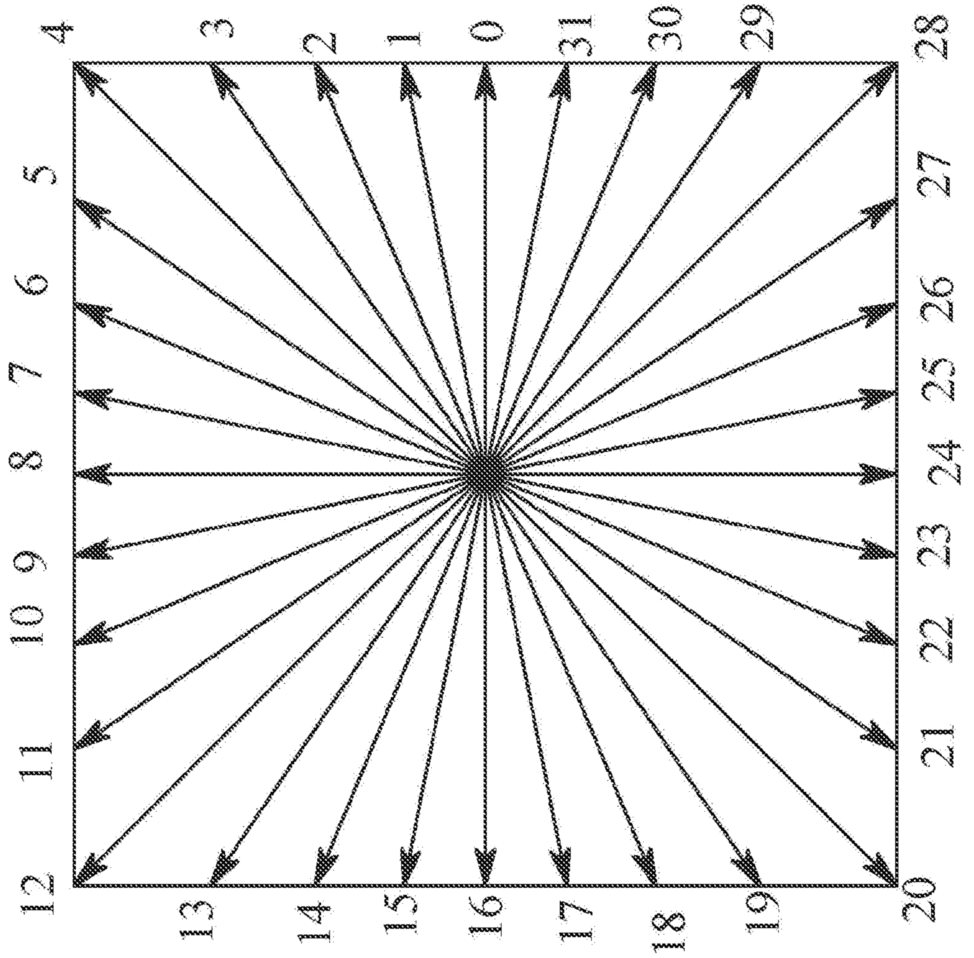


FIG. 3


0
1
2
3
4
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6
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8
9
10
11
12
13
14
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17
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19
20
21
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FIG. 4

400

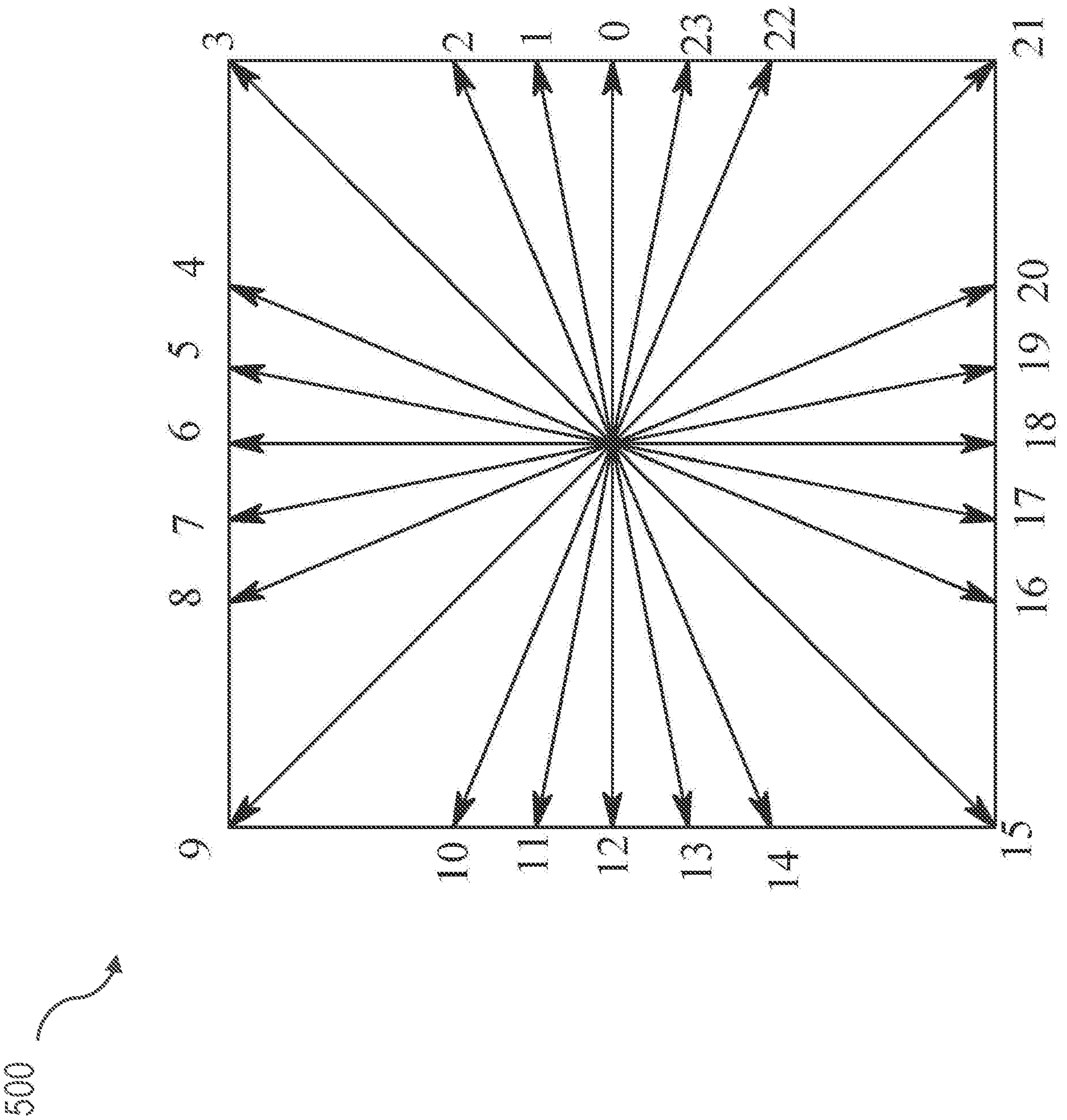

FIG. 5

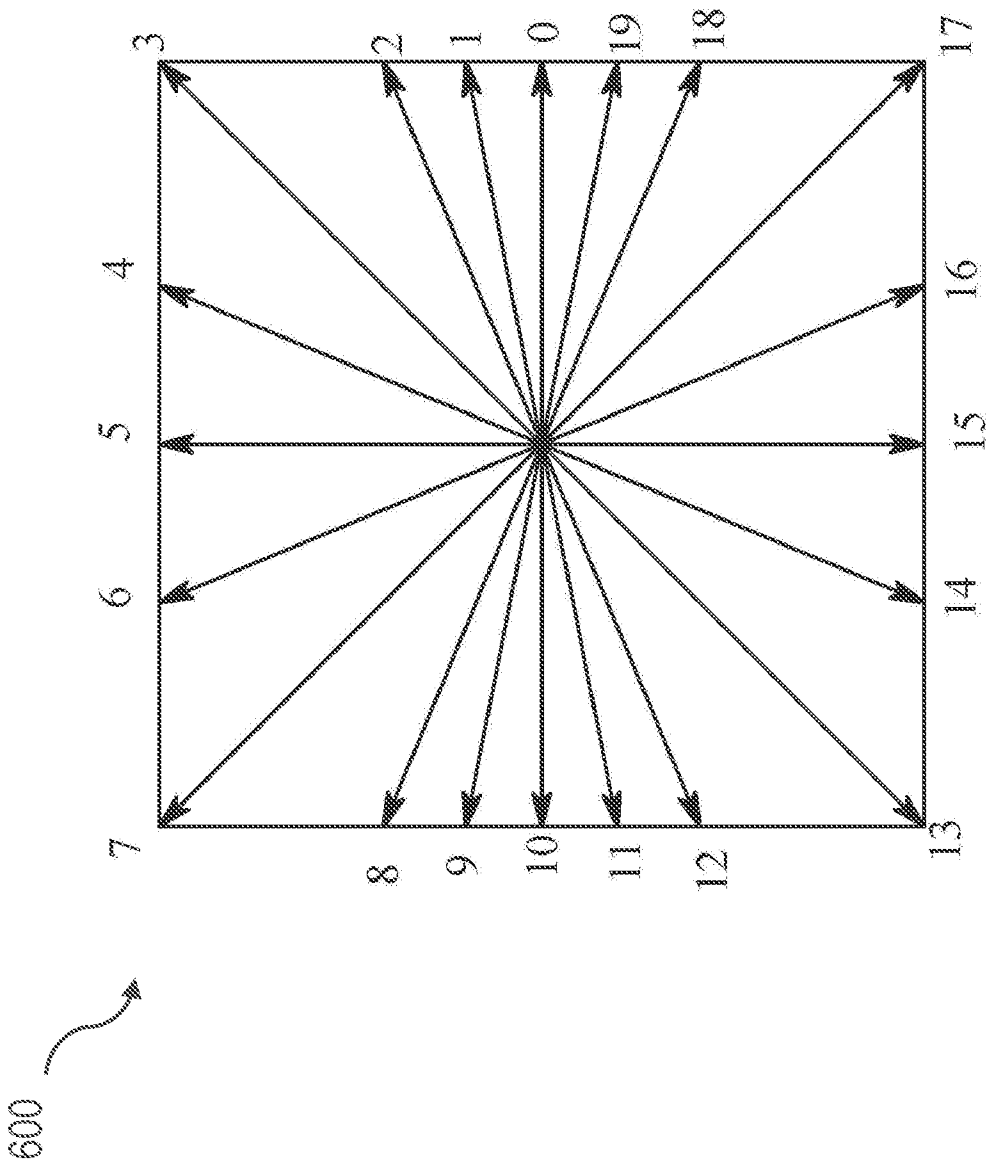

FIG. 6

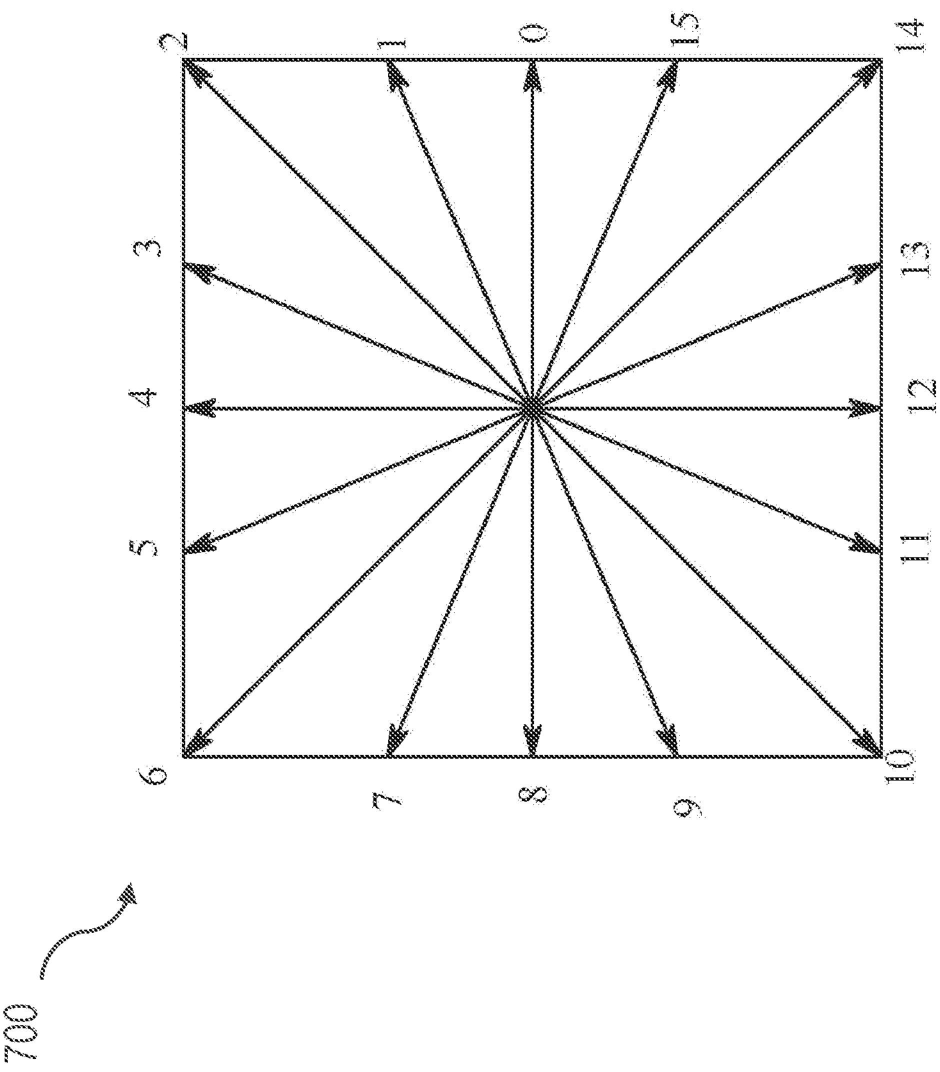

FIG. 7

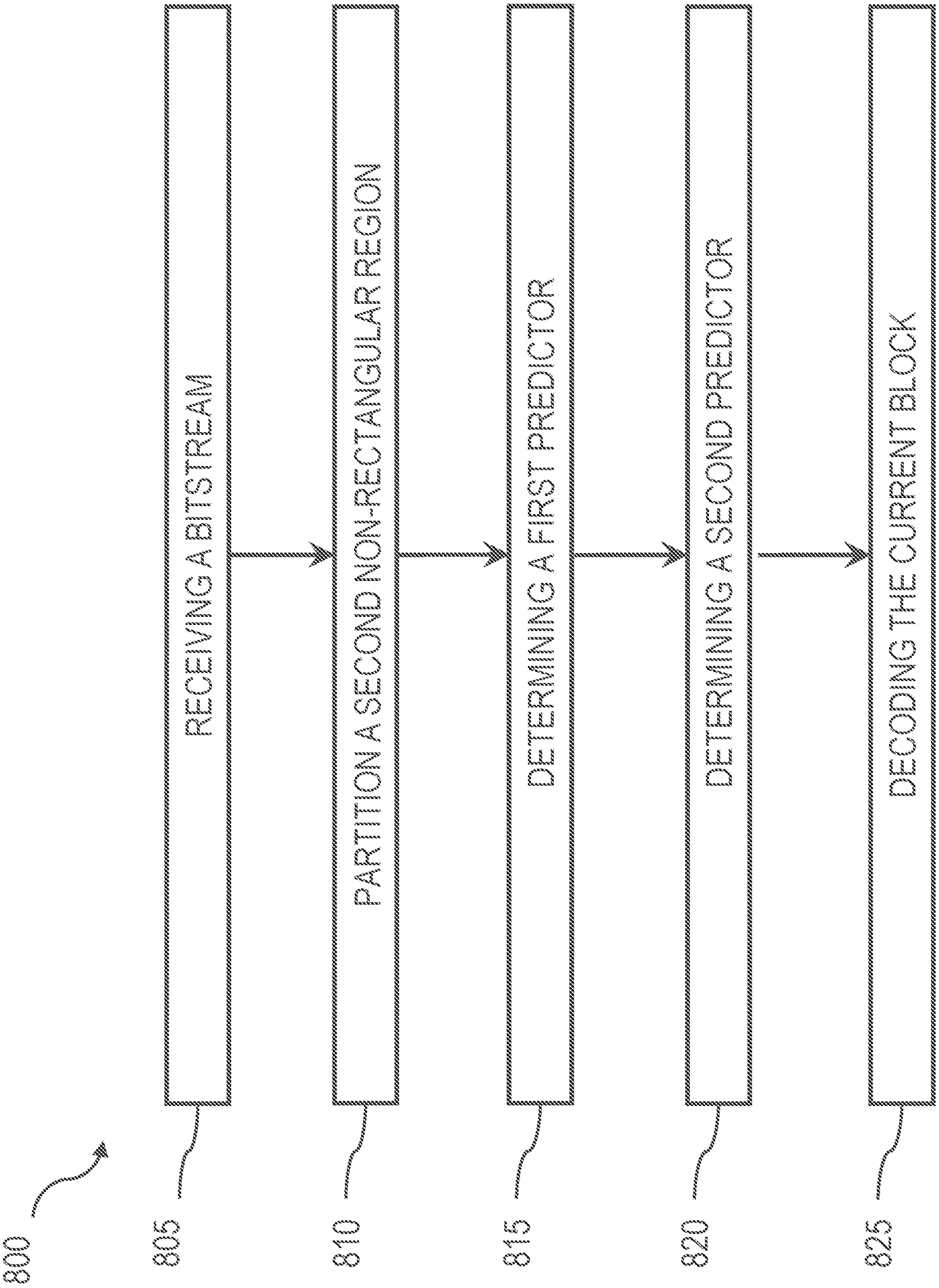
800
805
RECEIVING A BITSTREAM
810
PARTITION A SECOND NON-RECTANGULAR REGION
815
DETERMINING A FIRST PREDICTOR
820
DETERMINING A SECOND PREDICTOR
825
DECODING THE CURRENT BLOCK

FIG. 8

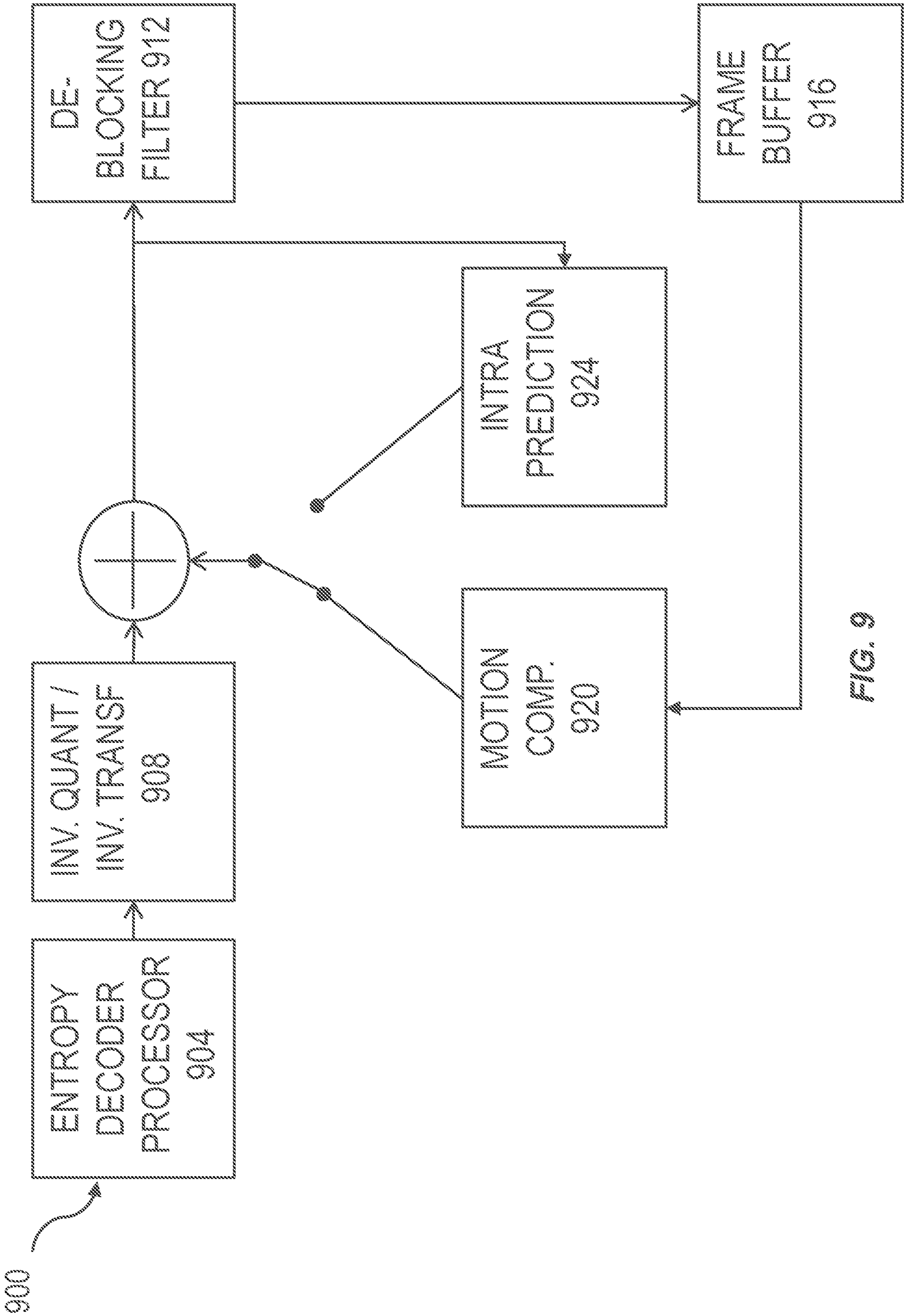
DE-
BLOCKING
FILTER 912
FRAME
BUFFER
916
INTRA
PREDICTION
924
MOTION
COMP.
920
INV. QUANT /
INV. TRANSF
908
ENTROPY
DECODER
PROCESSOR
904
900

FIG. 9

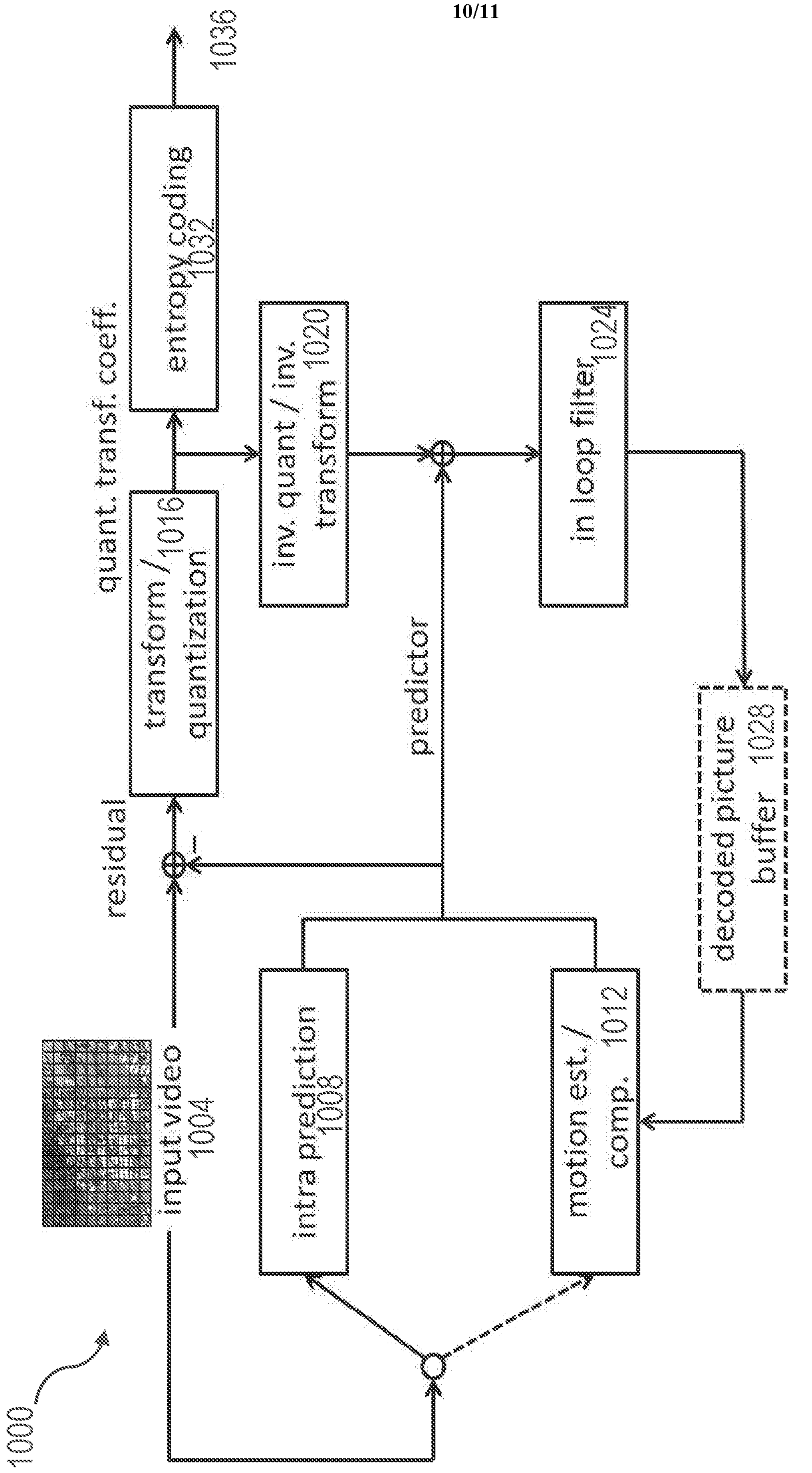
1000
input video 1004
residual
transform / quantization 1016
quant. transf. coeff.
entropy coding 1032
1036
inv. quant / inv. transform 1020
predictor
in loop filter 1024
intra prediction 1008
motion est. / comp. 1012
decoded picture buffer 1028

FIG. 10

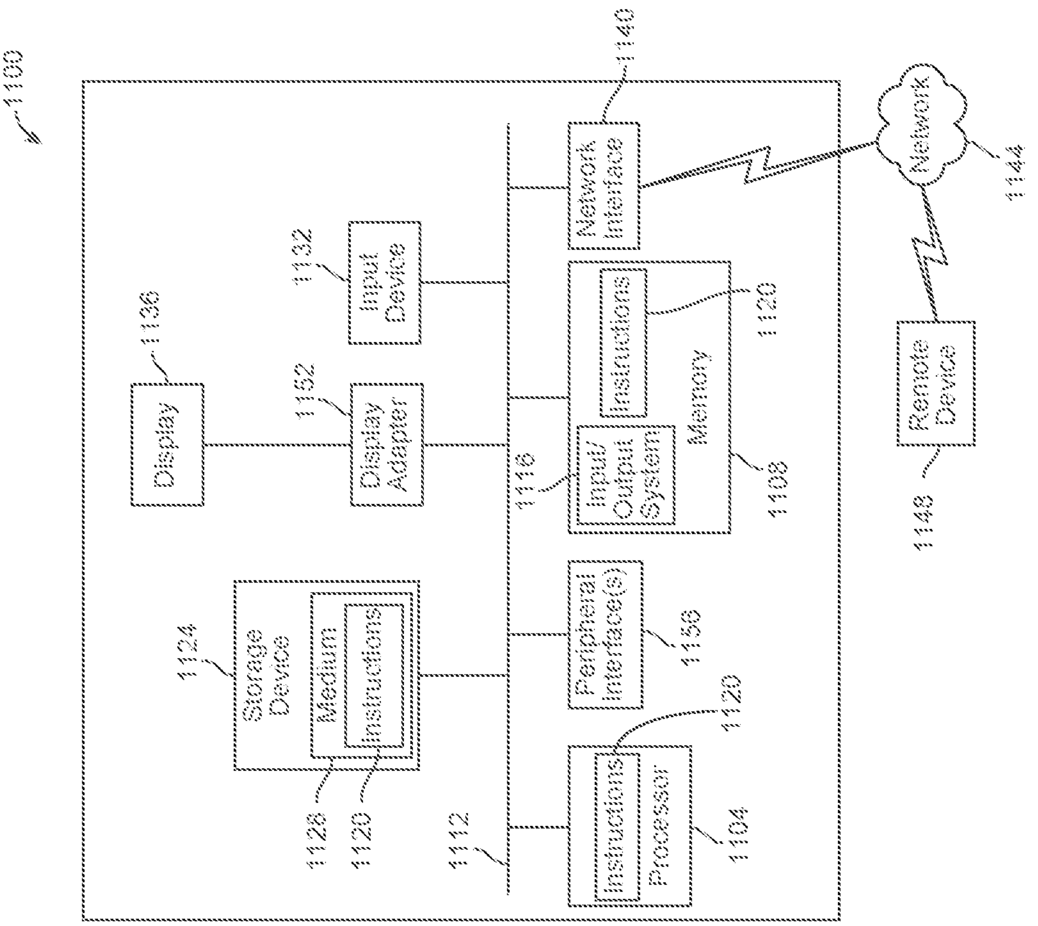
1100
1124
Storage Device
Medium
Instructions
1128
1120
1112
1136
Display
1152
Display Adapter
1132
Input Device
1116
1140
Network Interface
Input/ Output System
Instructions
1120
Memory
1108
Peripheral Interface(s)
1156
Instructions
Processor
1120
1104
Network
1144
Remote Device
1148

FIG. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/47857

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H04N 7/32 (2021.01)

CPC - H04N 19/543, H04N 19/513, H04N 19/17, H04N 19/615, H04N 19/176, H04N 19/122, H04N 19/119, H04N 19/174

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y -- A	WO 2019/246535 A1 (OP SOLUTIONS, LLC), 26 December 2019 (26.12.2019), entire document, especially abstract; para [0037]-[0041], [0053]-[0056]	1-5, 8-21, 24-32 ------------ 6-7 and 22-23
Y -- A	US 2011/0200097 A1 (Chen et al.), 18 August 2011 (18.08.2011), entire document, especially abstract; para [0057]-[0058], [0134]-[0136]	1-5, 8-21, 24-32 ------------ 6-7 and 22-23
Y	US 2012/0106627 A1 (Guo et al.), 03 May 2012 (03.05.2012), entire document, especially abstract; para [0074]-[0076], [0086]-[0087], [0103]-[0106]	3-5, 19-21
A	US 2017/0280156 A1 (THOMSON LICENSING), 28 September 2017 (28.09.2017), entire document	1-32

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 December 2021 (09.12.2021)	JAN 06 2022

Name and mailing address of the ISA/US	Authorized officer
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-8300	Kari Rodriquez Telephone No. PCT Helpdesk: 571-272-4300

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 21/47857

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

--- (See Continuation in Supplemental Box) ---

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:
Claims 1-32

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.

Continuation of:
Box III. Observations where unity of invention is lacking

This application contains the following inventions or groups of inventions which are not so linked as to form a single general inventive concept under PCT Rule 13.1. In order for all inventions to be searched, the appropriate additional search fees must be paid.

Group I - Claims 1-32 are directed to geometric partitioning decoder.

Group II - Claims 33-64 are directed to identify a geometric partition of the current block.

The inventions listed as Groups I-II do not relate to a single general inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons:

Special Technical Features:

The invention of Group I included the features of determine a first predictor for use on a first side of the at least a first partition boundary; determine a second predictor as a function of a second motion vector; and decode the current block using the first motion vector and the second motion vector, smoothing the first predictor and the second predictor across the at least a first partition boundary; and adding residual pixel values to the first predictor and the second predictor, not required by any other group.

The invention of Group II included the features of determine, from the bitstream, a number of geometric partitioning modes applicable to the current block; identify a geometric partition of the current block as a function of the number of geometric partitioning modes; decode the current block as a function of the geometric partition, not required by any other group.

Common Technical Features

Groups I and II share the features of receive a bitstream; select a current block; geometric partitioning modes; geometric partition; decode the current block.

However, the shared technical features do not represent a contribution over prior art as being anticipated by US 2017/0280156 A1 (THOMSON LICENSING), 28 September 2017 (28.09.2017).

THOMSON LICENSING teaches receive a bitstream (para [0122]- receiving an input bitstream); select a current block (para [0141]-[0144]- current block partition); geometric partitioning modes (para [0089]-[0091]- geometric partition mode); geometric partition (para [0089]-[0091]- generation of geometric partitions); decode the current block (para [0175]-[0178]- decoding the information related to parametric model-based coding modes).

As the common features were known in the art at the time of the invention, this cannot be considered a common technical feature that would otherwise unify the groups. Therefore, Groups I-II lack unity under PCT Rule 13.