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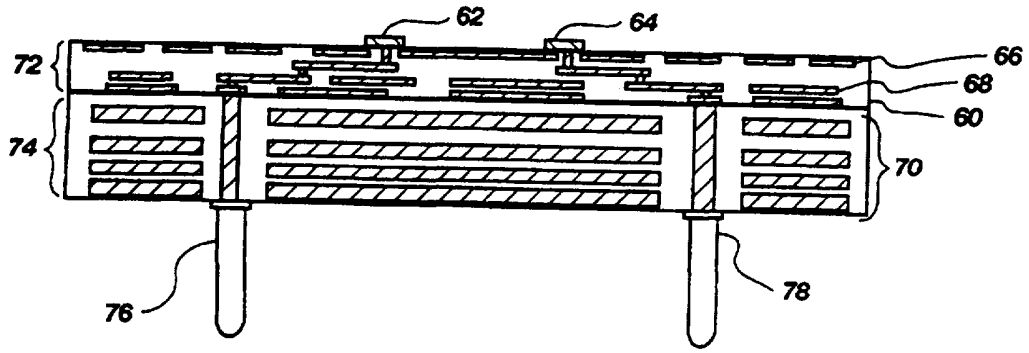

(57) Abstract

A process for making a semiconductor device and the resulting device having standardized die-to-substrate bonding locations are herein disclosed. The semiconductor die (32) provides a standard ball grid or other array of a particular size, pitch and pattern such that as the size, configuration or bond pad arrangement of the die changes, a standard substrate (60) (the term including leadrames) having a similarly standardized array of terminals (62, 64) or trace ends can be employed to form a semiconductor device (30). It is also contemplated that dies having markedly different circuitry but a common array pattern may be employed with the same substrate or other carrier.

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STANDARDIZED BONDING LOCATION PROCESS AND APPARATUS

TECHNICAL FIELD

This invention relates generally to a process for forming semiconductor die-to-substrate conductor interconnections and, more specifically, to a process for forming standardized bonding locations for varying die sizes, configurations, bond pad arrangements and circuitry, and a semiconductor die assembly formed therefrom.

BACKGROUND ART

The first integrated circuits became available in the late 1960s having a minimal number of circuits on each chip of silicon. These first components typically included aluminum or gold-based, thin-film traces to integrate the active and passive devices embedded in the silicon. Since these first simple semiconductor devices, the circuit count per die has grown exponentially. In the early 1970s, bipolar logic chips had about 100 circuits and monolithic memory had 128 bits forming the first commercial, bipolar main memory. Since then, the number of logic circuits has grown to over 10,000 per chip (bipolar) and one gigabit memory chips, with FET transistors replacing bipolar.

The active component or device integration and densification process in integrated circuits has motivated a continuous and ongoing migration of intercircuit wiring and connections from boards, cards, and modules to the chip itself. The surface of the chip, with its multilayer wiring, has become a microcosm of the conductor and insulator configurations that were common on previous multilayer printed-circuit boards and multilayer ceramic packages. A logic chip with 700 circuits and three layers of wiring has approximately 5 m of aluminum wiring on a chip less than 5 mm square. There are over 17,000 via connections from level to level through a micron-thick insulator film of SiO_2. Yet, the conductor capacity in the chip greatly lags behind the densification of the silicon devices. Most of the area of the chip (approximately two-thirds) still serves as a platform for the wiring.

Heretofore, serial wirebonding of one or two rows of bond pad input/outputs (I/Os) around the perimeter or down the center of the chip to leads and sometimes

buses of a leadframe has satisfied the needs of most ceramic or plastic dual in-line packages. Automated wirebonding today is very fast, efficient, and reliable compared to the manual bonding of the 1960s. Wirebonding, however, appears to be yielding for some applications to TAB bonding, in which the density of perimeter connections can be doubled or tripled and all bonds made simultaneously. Solder-bumped connections have evolved into an area array or pattern configuration in which a large portion of the surface of the chip is covered with controlled collapse chip connections (C4s) for the highest possible I/O counts. Unlike wirebonding, C4 usually dictates solder bump formation on the active surface of the chip when the chip is in wafer form. Typically, in such structures, a layer of silicon oxide, silicon nitride, or polyimide passivation must be formed over the final wiring level on the active surface of the chip before formation of the bumps. This has become a commonplace precaution to protect the fine wiring from corrosion and mechanical damage, even in advanced wirebonded chips.

Solder-bump interconnection was initiated in the early 1960s to eliminate the expense, unreliability, and low productivity of manual wirebonding. Whereas the initial, low-complexity, low circuit density chips typically required only peripheral contacts or bond pads, solder-bump technology has allowed considerable extendibility in I/O density as it progressed to full-population area arrays. Typically, C4s utilize solder bumps deposited on wettable metal pads on the chip and a matching footprint of solder wettable terminals at the ends of circuit traces carried by the substrate. The upside-down chip (commonly referred to as a flip chip) is aligned to the substrate, and all joints are made simultaneously by reflowing the solder. It is also known to employ conductive polymer bumps or polymers loaded with conductive particles in lieu of solder bumps in arrays. Fine pitch bump arrays have been generally termed "ball grid arrays," or "BGAs," in the art.

In addition to the densification of C4s or other conductive bumps on a given die (also interchangeably referred to in the art as a "chip"), technological advances in the art have decreased the overall size of semiconductor dies (for a given circuit density). Further, due to ongoing advances in circuit component design and fabrication technology, a given die may be "shrunk" one or more times during its commercial lifespan to enhance per-wafer yield, device speed and performance, and quality. In addition, similar dies from different manufacturers may be of different

size and/or shape, but are adaptable to use on the same printed circuit board or other conductor-carrying substrate. Consequently, the need to allow for varying sized dies for a given substrate has been recognized. For example, U.S. Patent 5,168,345 discloses a substrate having a plurality of conductive leads arranged in a generally radial pattern to which dies of various sizes may be attached. Likewise, in U.S. Patent 5,327,008, a universal leadframe is disclosed which is suitable for use with many different die sizes. In both of the foregoing patents, bond wires are employed to connect die bond pads to lead frame leads.

Such arrangements, however, are not practical for bump-type interconnections (flip-chip bonding) of dies having markedly different bond pad patterns thereon, due to the precise mutual locational requirements of the bump interconnections and the matching terminals or other connector structures on a substrate or other carrier. Thus, it would be advantageous to provide a bumped die to which a standardized array of terminals or trace ends of a substrate or other carrier such as a leadframe could be bonded, regardless of die size or bond pad pattern. Thus, a single substrate or leadframe conductor configuration might be employed to accommodate different generations of the same die or different die altogether.

DISCLOSURE OF INVENTION

Accordingly, the present invention comprises a process of making a semiconductor die having a standardized array of external connections formed thereon and the resulting die and die assembly. That is, a given semiconductor die has a set pattern, pitch and size (also termed an array) of external connections formed on its active surface so that it may physically and electrically mate with a substrate or other carrier having a substantially identical standardized array of trace ends, terminals or other contact structures. As the size of the die is reduced during product development, the newly formed die (commonly referred to as a shrink) has the same configuration and size of array of external connections formed thereon for joining with a substrate. Thus, a single substrate trace end or terminal configuration matching the external connection pattern of the first, oversize generation of a given die will also be usable for subsequent generations of smaller dies.

Similarly, dies from different manufacturers or other dies having differing bond pad patterns may be reconfigured according to the invention with identical I/O bump patterns. For example, a die with two parallel rows of peripheral bond pads, a die with one or two central rows of pads, a die with a hybrid pad pattern of a central pad row with a transverse peripheral row of pads at each end, and a die with pads along all four sides may be reconfigured to a common I/O array pattern.

The die of the invention has a plurality of external contact or connect (bond) pads formed on its surface, to which a plurality of external connections residing on the die are connected by conductive traces extending between the contact pads and the external connections. The contact pads and traces may be at least partially covered by a dielectric material, such as a polyimide or other suitable material known in the art.

In a preferred embodiment, the size of the die employing a standardized external connection (I/O) array can be reduced at least twice for a given integrated circuit device, one such exemplary device being a sixty-four megabit dynamic random access memory (DRAM) die. Moreover, the die size can be reduced in one lateral (x,y) dimension or two without compelling a change in the arrangement of the standardized connection array.

In one preferred embodiment, the I/O array is organized in a series of substantially mutually parallel rows and perpendicular columns. In another embodiment, the array is organized in a pattern of parallel rows with I/O connections of each row offset from an adjacent one. In yet another embodiment, the array forms a substantially rectangular configuration with interconnections positioned only about the perimeter of the rectangle.

In yet another embodiment, the array is organized into at least one row of connectors. If one row is utilized, the row may be formed along a center line of the die, along a side or anywhere in between. If two rows are utilized, the rows may be adjacent one another flanking a center line of the die, proximate opposing sides of the die, or flanking one side of the die with I/O connections of each row offset to minimize pitch.

In still another embodiment, the I/O array is configured with one or two central rows of connections having a transverse row of connections at one or both ends thereof along a side of the die.

In a further embodiment, the I/O array is of circular configuration, employing one or more concentric rings of connections.

A significant aspect of the invention is that any selected single, standardized trace-end array pattern substrate can be utilized for succeeding generations of ever-smaller semiconductor dies including substantially the same integrated circuit, or a circuit that "looks" the same electrically to external devices. That is, regardless of the specific external connection configuration, the layout of external connections remains constant for subsequent reduced-sized, or shrunken, dies.

Another significant aspect of the invention is the ability to interchange dies of different manufacture and having different bond pad arrangements by standardizing their external connections.

Still another significant aspect of the invention is the ability to mount dies with markedly differing bond pad arrangements to a single lead frame having inner lead ends configured to contact the bond pads of each die. Such interchangeability may be effected by reconfiguring the diverse I/O pattern on the different dies to a common one for connection to the leadframe leads.

Yet another significant aspect of the invention is the ability to connect dies having different circuitry to a substrate or other carrier employing a standardized terminal or trace end array.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1 is a top view of a three-generation progression of a first embodiment of a semiconductor die in accordance with the present invention;

FIG. 2 is a partial cross-sectional view of a die-and-substrate semiconductor device in accordance with the present invention;

FIG. 2A is a partial cross-sectional view of a variation of the die I/O connection structure depicted in FIG. 2;

FIG. 3 is a top view of a three-generation progression of a second embodiment of a semiconductor device in accordance with the present invention;

FIG. 4 is a top view of a three-generation progression of a third embodiment of a semiconductor device in accordance with the present invention;

FIG. 5 is a top view of a three-generation progression of a fourth embodiment of a semiconductor device in accordance with the present invention;

FIG. 6 is a top view of a three-generation progression of a fifth embodiment of a semiconductor device in accordance with the present invention;

FIG. 7 is a top view of a three-generation progression of a sixth embodiment of a semiconductor device in accordance with the present invention;

FIG. 8 is a top view of a three-generation progression of a seventh embodiment of a semiconductor device in accordance with the present invention;

FIG. 9 is a top schematic view of a die with bond pads rerouted to I/O connections on a single edge of the die;

FIG. 10 is a top schematic view of two dice with different bond pads rerouted to a common circular array of I/O connections in accordance with the present invention; and

FIG. 11 is a top schematic view of two dice with different bond pads rerouted to accommodate a lead frame configured for yet another, different I/O pattern and providing a common external lead configuration.

BEST MODES FOR CARRYING OUT THE INVENTION

Referring to FIG. 1, an exemplary semiconductor die 10 in accordance with the present invention is shown. The die 10 is the first generation of a series of increasingly-smaller dice 12 and 14 including the same integrated circuit, such as a DRAM. The dies 10, 12, and 14 each have an array of external connections 16 and spacing formed on their active surfaces. As can be seen, the connections 16 maintain a constant configuration and spacing for each generation of shrinking dies 10, 12, and 14. That is, the size and locations of the connections 16 remain constant from one generation of die 10 to the next 12, and so on to the smallest die shrink, in this case die 14. An exemplary configuration of the external connections 16, as shown in FIG. 1, is a generally rectangular array 15 comprised of a series of substantially mutually perpendicular rows and columns of connections 16.

Proximate the first and second ends 18 and 20, respectively of the dies 10, 12, and 14, is a plurality of die contact or connect (bond) pads 22. The pads 22 are connected to remote external connections 16 through circuit runs or traces 24 extending from selected pads 22 to the external connections 16. As shown, traces 24 may electrically connect all or a portion of the connections 16 to the pads 22. Moreover, some of the traces 24 may merge with others as shown at 26 along their

paths as design requirements and preferences dictate. Because the connections 16 are in a predetermined, fixed location for each generation of dies 10, 12, and 14, the traces 24 between the pads 22 and the connections 16 generally decrease in length from one generation to the next. It should be noted that traces 24 are shown extending from bond pads 22 of the first generation 10 of the die through those of the two succeeding shrinks 12 and 14 for purposes of clarity and identification of corresponding bond pads of each die generation. However, in practice, traces 24 of each generation may be routed more directly from a bond pad 22 to its corresponding connection 16 as shown by exemplary broken line traces 24a on FIG. 1.

As shown in FIG. 2, a bare die device 30, representative of a device in accordance with the present invention, includes a semiconductor die 32 having rows of pads 34 and 36 (perpendicular to the plane of the drawing figure) proximate its ends 38 and 40, respectively. Circuit runs or traces 42 and 44 extending over a passivation layer (typically silicon dioxide or silicon nitride) on the die active surface are used to connect the pads 34 and 36 to external connections 46 and 48, respectively (such as solder or conductive epoxy balls or polymer balls containing conductive particles for forming a ball grid array (BGA), or other connectors as known in the art). Runs or traces 42, 44 may be formed by methods known in the art, such as sputtering (low melt metals), stencilling (conductive inks or polymers), or may be preformed before application to die 32 as by metallization of a polymer film (such as a polyimide) and formation of circuit traces thereon, such structures being commonly referred to as TAB (tape automated bonding) tape, or more generically as flex circuits. The trace material and dielectric are not critical to the invention as long as performance parameters are met.

As shown in FIG. 2, traces 42 and 44 may reside on a polymer film layer 50 and may be sandwiched between layer 50 and a cover layer 52, although neither layer is a requirement of the invention. Layers 50 and 52 may be formed of a polyimide or other suitable dielectric material, preformed or formed in situ, each such layer if employed being (by way of example) approximately 6 μm thick. As shown in FIG. 2A, traces 42 and 44 may reside on a dielectric layer 50, no cover layer 52 being employed. The FIG. 2A structure is particularly suitable for a flex circuit-type bond pad rerouting structure. The layers 50 (and 52, if used) also

incidentally provide additional protection to delicate circuitry on the surface 54 of the die 32. Layers 50 and 52 may also comprise a siloxane polyimide or a spin-on glass layer, as desired.

Any substrate 60 having terminals 62 and 64 oriented to match the location of the interconnections 46 and 48, respectively, may be utilized to form a bare die device 30 in accordance with the present invention. As shown, the substrate 60 may be a combination thin- and thick-film package or any other substrate known in the art, such as a printed circuit board or other chip carrier element. The substrate trace ends or other terminals, such as terminals 62 and 64, are configured to mate with the bump connections 46 and 48, respectively, or vice versa. Such a substrate 60 may include ground and signal circuitry 66 and 68 and power and ground circuitry 70. Thin- or thick-film layer 72 may be comprised of polyimide, or any other suitable material known in the art, and thick-film layer 74 may comprise a ceramic material, or some other appropriate material. The substrate 60 may also include I/O pins 76 and 78 for connection to higher-level packaging. As will be understood by those in the art, most of the details of the substrate 60 are not essential to the functionality of a device 30 in accordance with the present invention and are merely provided for illustrative purposes.

The die 32 and cooperating substrate 60 may be mutually aligned by any suitable means known in the art, such as mechanical or optical alignment systems. If the latter is used, it is desirable to provide a so-called "null point" at the center of the die in the bump pattern to serve as a reference for translational and rotational alignment. Use of an optical system, such as a pattern recognition system, in combination with tight manufacturing tolerances, will permit use of extremely fine-pitch small ball or bump arrays in the smallest possible patterns.

FIGS. 3-8 illustrate various embodiments of the dies 10, 12, and 14 in accordance with the present invention and having varying configurations of the connections 16. (For simplification purposes, the circuit runs or traces 24 extending from the bond pads 22 to the external connections 16 are not illustrated in FIGS. 3-8.)

The array 80 shown in FIG. 3 forms a staggered row pattern on the surface 54 of the die 10.

In FIG. 4, the array 90 of external connections 16 forms the outline of a rectangle. Of course, a second, inner rectangle of connections 16 might be added.

In FIG. 5, the external connections 16 form an array 100 comprised of two rows of external connections 16 adjacent and flanking the center line 102 of the die 10. Each of the connections 16 are slightly offset from corresponding connections 16 in the other row in relation to a line 104 perpendicular to center line 102.

Similarly, in FIG. 6, the array 110 is comprised of two rows of connections 16 where the connections 16 of one row are a mirror image of the other row about the center line 112 of the die 10 and are separated by a distance 114 so as to be close to the periphery of third-generation die 14.

In FIG. 7, the array 120 is formed by a single row of connections 16 along the center line 122. As illustrated, the array 120 is comprised of six connections 16. The number of connections 16, however, may vary, depending on design parameters and required minimum number of I/Os.

FIG. 8 illustrates that the various dies 130, 132, and 134 representing three generations of die shrinks may not necessarily shrink in two or more dimensions. That is, the die 130 may simply be reduced with regard to its longitudinal length for the next generation of die 132. Similarly, the subsequent (third) generation of die 134 may only be reduced in one dimension, as illustrated.

FIG. 9 illustrates a die 200 having a central row of bond pads 22 thereon reconfigured through the use of traces 24, as previously described, to an edge-connect configuration wherein I/O connections 16 are disposed along one side of the die. It will also be recognized that connections 16 may, in this instance, be other than conductive bumps and may (as shown) comprise plate-type contacts engagable with clip-type connectors of a carrier for a direct die connect or DDC arrangement wherein the die is inserted in a slot in the carrier, or with the leads of a single in-line package (SIP), one such structure being illustrated in U.S. Patent 5,138,434, assigned to the assignee of the present invention.

FIG. 10 illustrates, for illustrative purposes, two superimposed dice 300 and 302, the first, smaller die (300) with two parallel rows of peripheral bond pads 322 and the second, larger die (302) with a central row of bond pads 322', each bond pad pattern being reconfigured into a common circular configuration or array of I/O interconnections 16 such as conductive bumps. As is shown in broken lines, traces

24 may easily be configured to extend from each set of bond pads 322, 322' of the respective different dies to a common array of I/O connections 16. An I/O array comprising multiple concentric connections 16 might also be employed.

FIG. 11 illustrates two exemplary superimposed dies 400 and 402 of the same size, each die with a respective different arrangement of bumped bond pads 422 and 422', mountable to a leadframe 410, the inner lead ends 412 of the leadframe 410 being configured to accommodate a common, rerouted I/O pattern (cross-hatched) employed with both dice and to provide a common I/O arrangement of external lead ends 430 for connection to a substrate or other carrier. Bond pads 422 have been rerouted by traces 24 shown in solid lines, while bond pads 422' have been rerouted by traces 24 shown in broken lines. It will be understood that only one die I/O pattern need be rerouted if the lead frame is configured to match the I/O pattern of the other die. It will be appreciated, however, that in some instances the I/O patterns of both dice are desirably rerouted. FIG. 11 is also illustrative of the use of two face-to-face dice mounted, if desired, on opposing sides of a leadframe in a lead-between-chip (LBC) arrangement, and the manner in which LBC is facilitated by the invention.

It is contemplated that the use of a standardized die-to-substrate connection array is adaptable to conform different-sized dies and dies with different circuitry to standardized packaging employed by the industry for connection of a variety of dies to carriers such as printed circuit boards. For example, a substrate configured as an insert having external leads or other terminal or pin elements extending therefrom and a standardized array of terminals may receive and carry any die having a matching bump configuration, regardless of its size, origin, or even the type of integrated circuits carried thereon. For example, using the invention, a die with a peripheral bond pad arrangement may be substituted for one employing a central row of bond pads. Thus, a substrate configured with external leads for a small-outline J-lead package may carry any matching-connection die. The substrate may, in fact, be a leads-under-chip (LUC) or leads-over-chip (LOC) design lead frame, with inner lead ends configured as pads and suitably plated, if necessary, to bond with the connection bumps of the die. Of course, the aforementioned LBC arrangement with two facing dice and an interposed lead frame is also a viable arrangement. The resulting assembly may then be packaged, as by transfer molding

of a plastic package. Alternatively, an insulative substrate defining a die carrier area with a terminal array and including leads, such as a ceramic substrate with leads extending therefrom, may receive a bumped die and a cover or other protection, such as a glob-top, preformed cover, or a dammed silicone gel, may be placed thereover. An insulative underfill may be employed between the die and substrate.

Those skilled in the art will appreciate that the layout of external connections for a semiconductor die according to the invention may be independent of the substrate and/or die materials used or the internal circuit configurations thereof. It will also be appreciated by one of ordinary skill in the art that one or more features of one of the illustrated embodiments may be combined with one or more features from another to form yet another combination within the scope of the invention as described and claimed herein. Thus, while certain representative embodiments and details have been shown for purposes of illustrating the invention, it will be apparent to those skilled in the art that various changes in the invention disclosed herein may be made without departing from the scope of the invention, which is defined in the appended claims. For example, various additional array configurations may be utilized; the number of generations of die shrinks employing a single standardized array may be increased or decreased; the number of external connections may vary; and the form of the die-size reduction may be altered to include one-dimensional shrinking in the plane of the die. The invention may be employed with functionally different dies mateable with the same substrate. For example, a SIMM (single in-line memory module) and a plug-in processor may be employed on a common design of daughter board, which in turn is connectable to a mother board. Only some of the bond pads of a die may be rerouted as desired, for example power and ground, to simplify external connections.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a die having an active surface including integrated circuitry;

a plurality of bond pads arranged on the die and over the active surface in electrical communication with said integrated circuitry of the die;

a plurality of external connections on the die, offset from the bond pads, and in an array over the active surface;

a plurality of circuit traces on the die connecting at least some of the plurality of external connections to at least some of the plurality of bond pads; and

a substrate to which the die is electrically connected by at least some of the external connections, the substrate including conductors on a surface thereof facing the active surface of the die, at least some of the conductors being in mating contact with external connections of the die.

2. The semiconductor device of claim 1, wherein at least a portion of at least one of said plurality of circuit traces is disposed on a discrete layer of dielectric material residing on said major surface.

3. The semiconductor device of claim 2, wherein said dielectric material is selected from the group comprising a polyimide, a siloxane polyimide and a spin-on glass.

4. The semiconductor device of claim 1, wherein at least a portion of at least one of said plurality of circuit traces is covered by a dielectric material.

5. The semiconductor device of claim 4, wherein said dielectric material is selected from the group comprising a polyimide, a siloxane polyimide and a spin-on glass.

6. The semiconductor device of claim 1, wherein said external connection array comprises an array of conductive bumps.

7. The semiconductor device of claim 6, wherein said bumps are of a material selected from the group comprising a reflowable metal material, a conductive polymer and a polymer carrying conductive material.

8. The semiconductor device of claim 6, wherein said external connection array comprises a BGA.

9. The semiconductor device of claim 1, wherein said die is a second die substituted for a first die having an active surface with an external connection array thereover and differing from said first die in at least one of the following respects: size, shape, bond pad arrangement, and circuitry, the external connection array of said second die being of the same size, pitch and pattern as the external connection array of said first die.

10. The semiconductor device of claim 9, wherein said second die is reduced in size in at least one dimension in comparison to said first die.

11. The semiconductor device of claim 10, wherein said second die is a shrink of said first die.

12. The semiconductor device of claim 1, wherein said external connection array is arranged in a single row on a center line of said die.

13. The semiconductor device of claim 1, wherein said external connection array is arranged in at least two rows.

14. The semiconductor device of claim 1, wherein said external connection array is arranged in a rectangular configuration comprising at least one rectangle of connections.

15. The semiconductor device of claim 1, wherein said external connection array is arranged in rows and columns.

16. The semiconductor device of claim 1, wherein said external connection array comprises a circular array including at least one circle of connections.

17. A process of manufacturing a semiconductor device, comprising:
fabricating a die having an active surface with a plurality of bond pads arranged on said die and over said active surface;
extending a plurality of circuit traces on said die and over said active surface from at least some of said bond pads to remote locations over said active surface and offset from said bond pads; and
forming external connections projecting from said active surface at said remote locations to define an array.

18. The process of claim 17, further including covering at least a portion of at least one of said plurality of circuit traces with a layer of dielectric material.

19. The process of claim 17, further including forming at least a portion of at least one of said circuit traces over a layer of dielectric material applied to said major surface.

20. The process of claim 17, further including forming said external connections as conductive bumps.

21. The process of claim 20, wherein said external connections are formed of a material selected from the group comprising a metal, a conductive polymer, and a polymer carrying conductive material.

22. The process of claim 17, wherein fabricating said die includes shrinking another die which is larger in at least one dimension and carries an external connection array thereon, and forming said external connection array of said die includes forming an external connection array of the same size, pattern and pitch as the connection array of said another die.

23. The process of claim 17, further including providing a substrate bearing conductors thereon having contact areas in a pattern matching said external connection array and connecting said die by said external connections of said array to at least some of said substrate conductor contact areas.

24. The process of claim 23, wherein said contact areas of said substrate conductors are arrayed to connect to another die which differs from said die in at least one of the following respects: size, shape, bond pad arrangement and circuitry, said another die carrying an identical external connection array to that of said die.

25. A method of designing a die-adaptable semiconductor device assembly, comprising:

identifying at least one integrated circuit function to be fabricated on an active surface of a semiconductor die;

identifying a number of external connections for electrically communicating said at least one integrated circuit function to external circuitry;

selecting an external connection array of a given size, configuration and pitch of connections for effecting said electrical communication between said active surface of a die and said external circuitry; and

positioning said external connection array on the active surfaces of at least two semiconductor dies differing in at least one of the following respects: size, shape, and bond pad arrangement thereon, and including said at least one identified integrated circuit function.

26. The method of claim 25, wherein said at least two dies comprise a first die, and a second die which comprises a shrink of said first die.

27. The method of claim 25, wherein said at least two dies comprise first and second dies of different manufacturing origin.

28. The method of claim 25, further including configuring circuit traces on at least one of said at least two semiconductor dies extending between locations

of said external connections of said external connection array on said at least one semiconductor die and at least some bond pad locations on the active surface of the same semiconductor die.

29. The method of claim 28, wherein said at least some of said bond pads are located peripherally on said active surface of said at least one of said at least two semiconductor dies, and said external connection array is located relatively centrally on said active surfaces of said at least two semiconductor dies.

30. The method of claim 25, wherein said at least two dies comprise a first die and at least one shrink of said first die, and further including selecting a pattern of circuit traces, at least some of said circuit traces extending from selected bond pad locations on said first die to said external connections and through selected bond pad locations of said at least one shrink.

31. The method of claim 25, further comprising designing an external connection array adapter usable with at least one of said at least two semiconductor dies and carrying said selected external connection array thereon, said at least one of said at least two semiconductor dies including bond pads offset from locations of said selected external connection array, said adapter being locatable on the active surface of said at least one of said plurality of dies and including circuit traces communicating between bond pad locations of that die and external connections of said selected external connection array on said adapter, said positioning of said external connection array on said at least one of said at least two semiconductor dies comprising applying said adapter to the active surface thereof with bond pads of said at least one semiconductor die in communication with at least some of said circuit traces.

32. A semiconductor device, comprising;

a die having an active surface including integrated circuitry;

a plurality of bond pads arrayed on said die and over the active surface of the die in electrical communication with said integrated circuitry of the die;

a plurality of external connections on said die, at least some of which external connections are laterally remote from said bond pads and arranged in an array over said active surface; and

a plurality of circuit traces extending over said active surface and connecting at least some of said plurality of external connections to at least some of said plurality of bond pads.

33. The semiconductor device of claim 32, wherein said plurality of circuit traces are formed on said die.

34. The semiconductor device of claim 32, wherein said circuit traces are preformed on a dielectric carrier applied to said active surface of said die.

35. The semiconductor device of claim 32, wherein said plurality of traces are at least partially covered by a dielectric material.

36. The semiconductor device of claim 32, wherein said external connections comprise conductive bumps.

37. A method of reconfiguring die I/O patterns, comprising:

selecting a first die having an active surface bearing a first I/O pattern;

selecting a second die having an active surface bearing a second I/O pattern different from said first I/O pattern; and

reconfiguring at least one of said first and said second active surface I/O patterns on an active surface of at least one of said respective dies so that said first die and said second die present a common I/O pattern from their respective active surfaces.

38. The method of claim 37, wherein said common I/O pattern differs from both said first I/O pattern and said second I/O pattern.

39. An adapter for rerouting a bond pad pattern on an active surface of a semiconductor die, comprising:

a two-sided sheet of dielectric material;

a plurality of conductive traces on said sheet, each of said traces extending from a first location on a first side of said sheet corresponding to a bond pad of said pattern of said die to a second, laterally remote location on said sheet; and

a plurality of external connections disposed at said laterally remote locations in communication with said conductive traces and projecting from a second side of said sheet for electrically communicating said die with external circuitry.

40. The semiconductor device of claim 13, wherein an arrangement of said at least two rows is selected from an arrangement wherein said at least two rows are mutually parallel and an arrangement wherein said at least two rows include a first row and a second row which are mutually perpendicular.

41. The semiconductor device of claim 15, wherein said external connections of a row are offset from connections of at least one adjacent row.

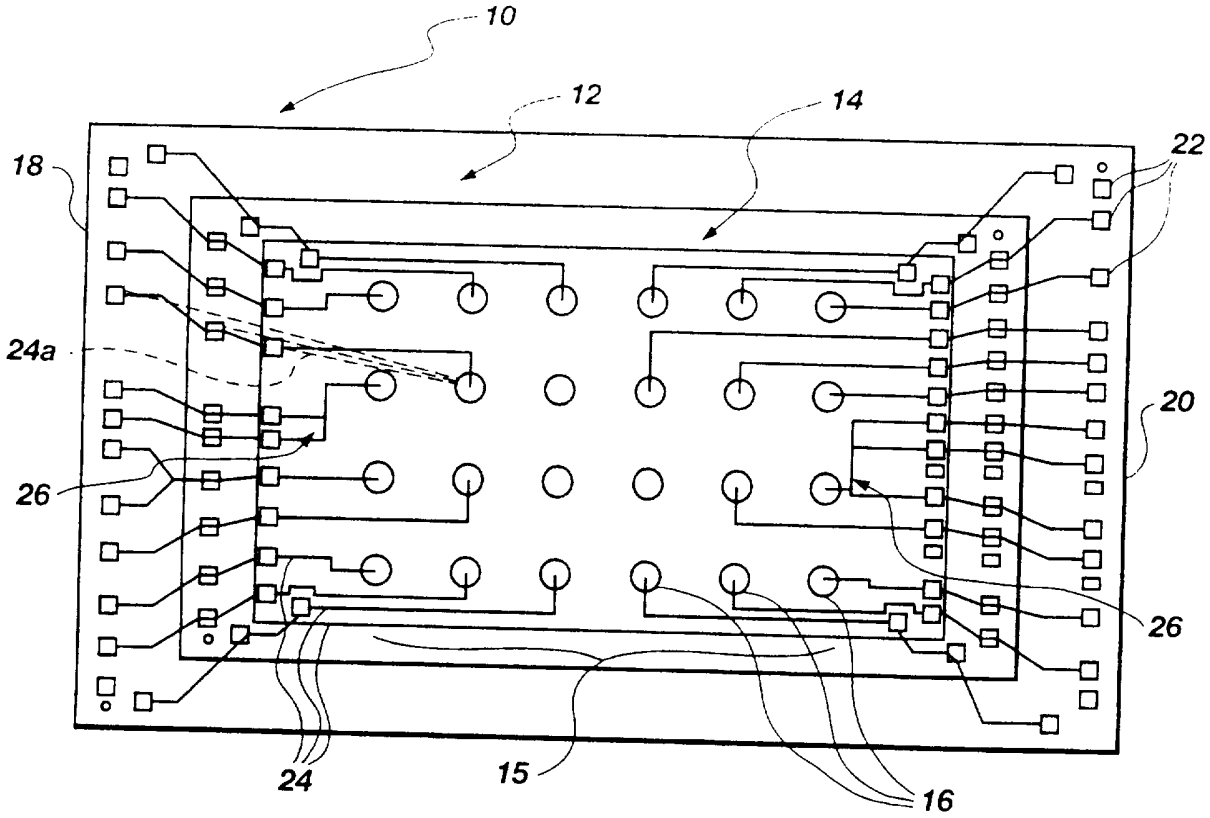

Fig. 1

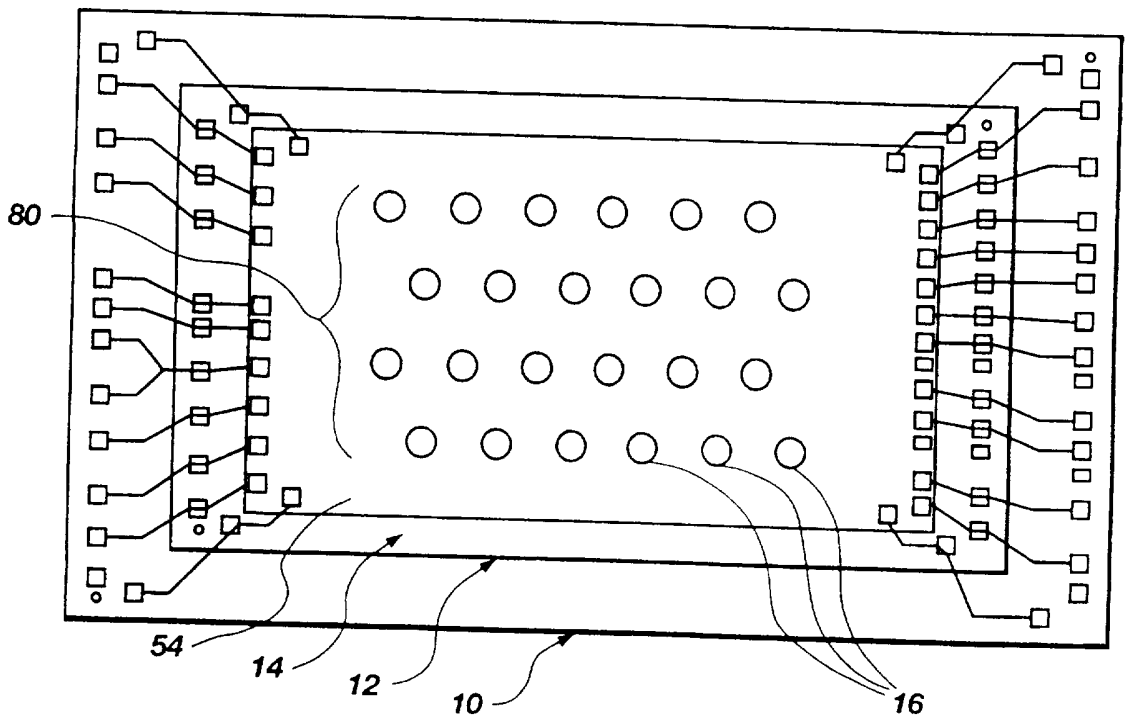

Fig. 3

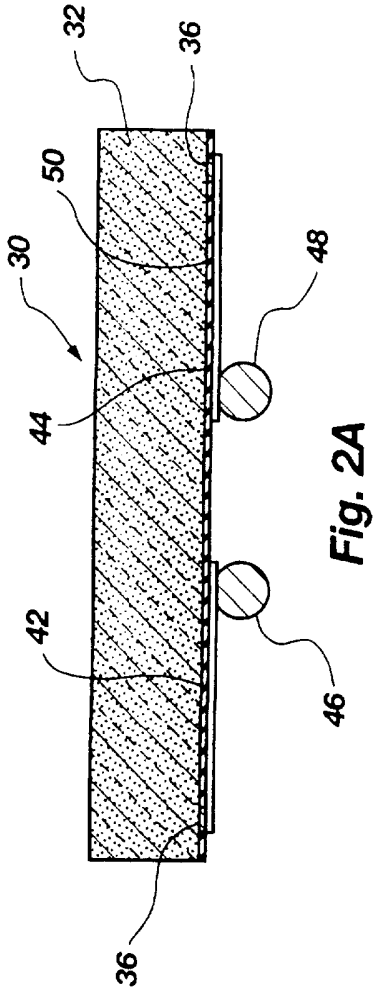
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Fig. 2A

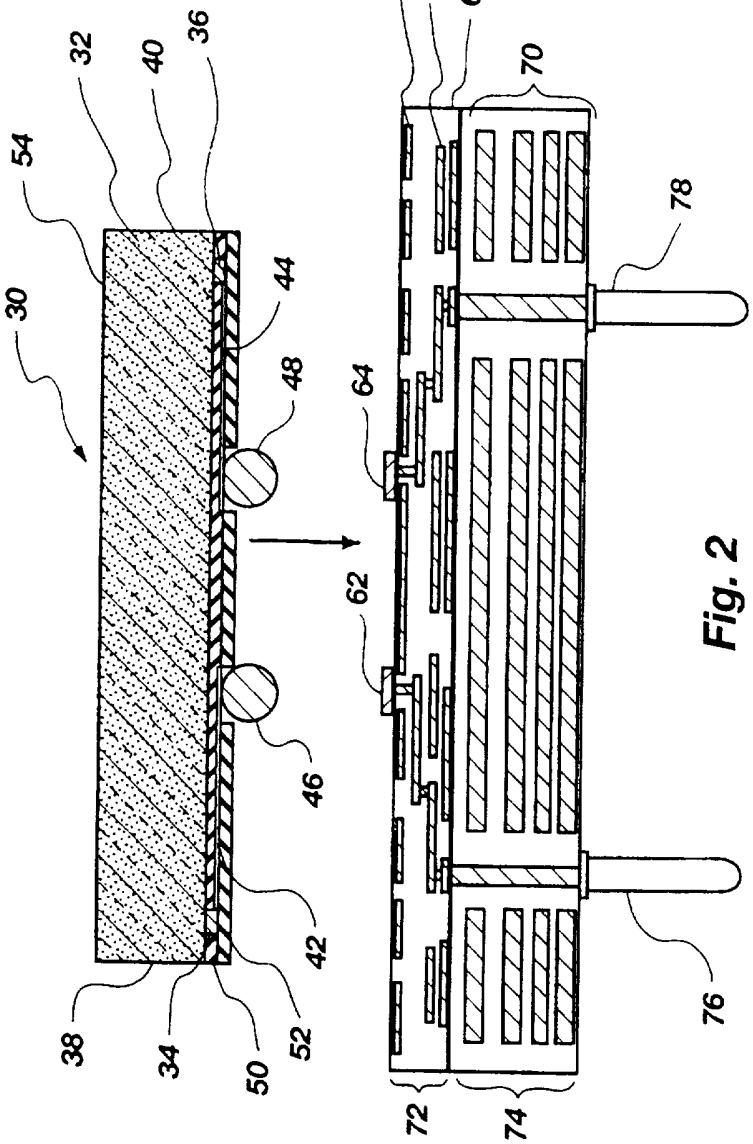
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Fig. 2

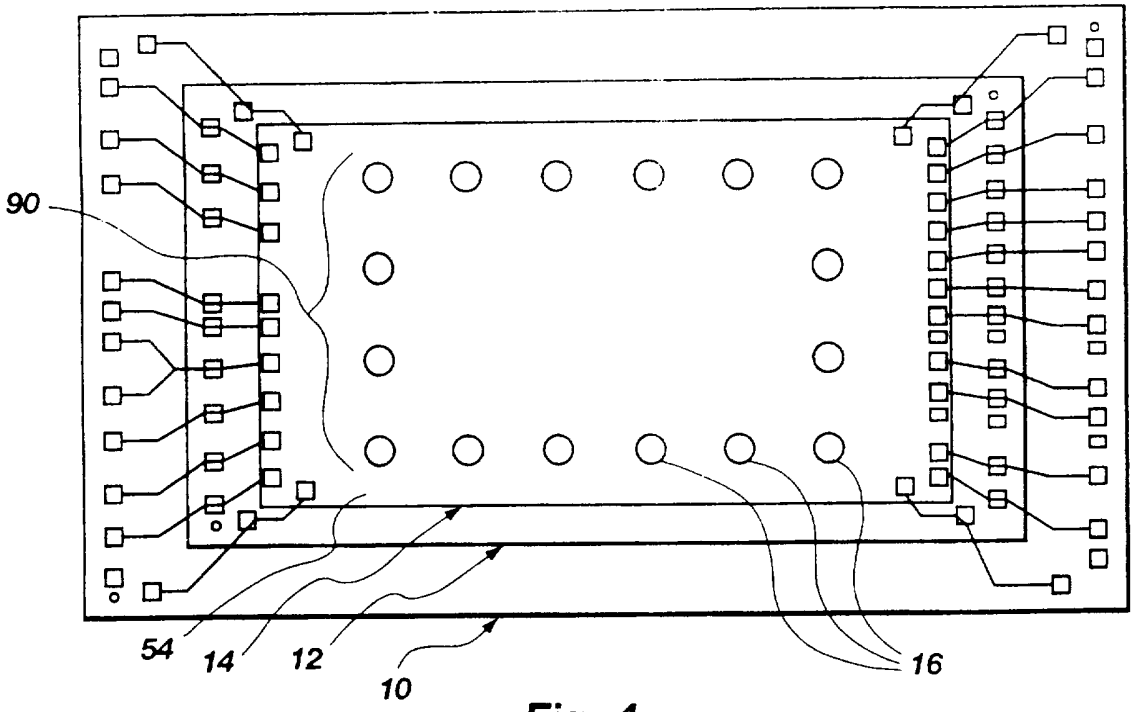

Fig. 4

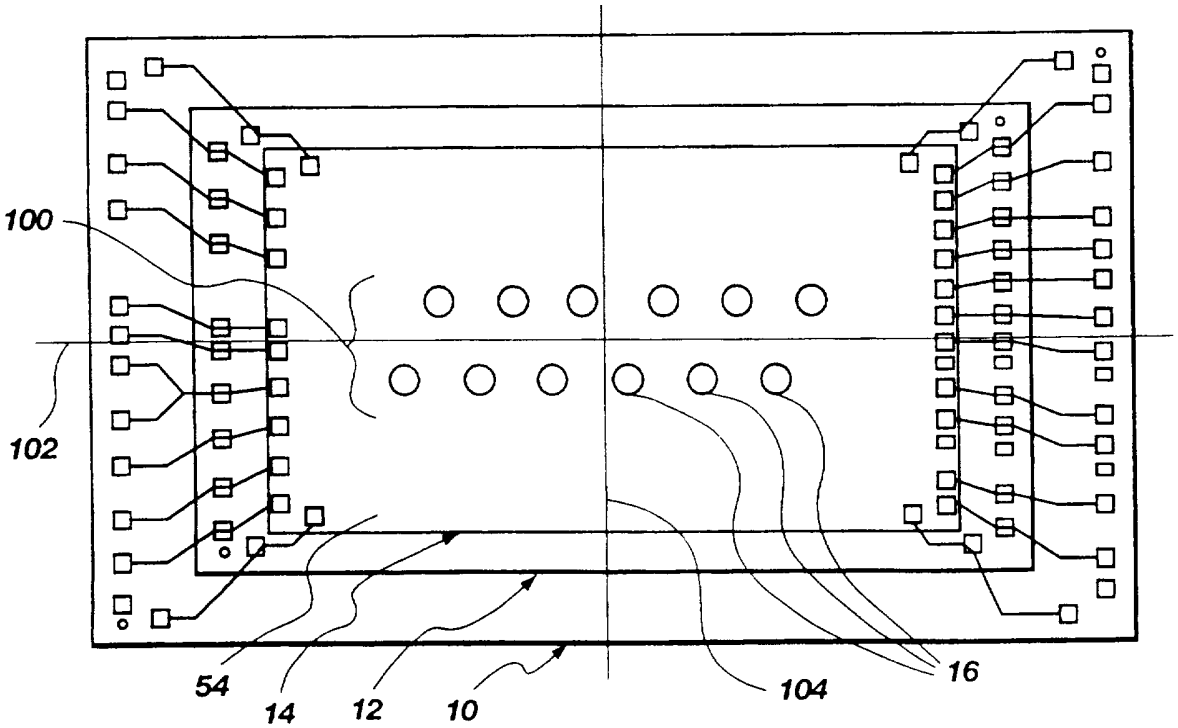

Fig. 5

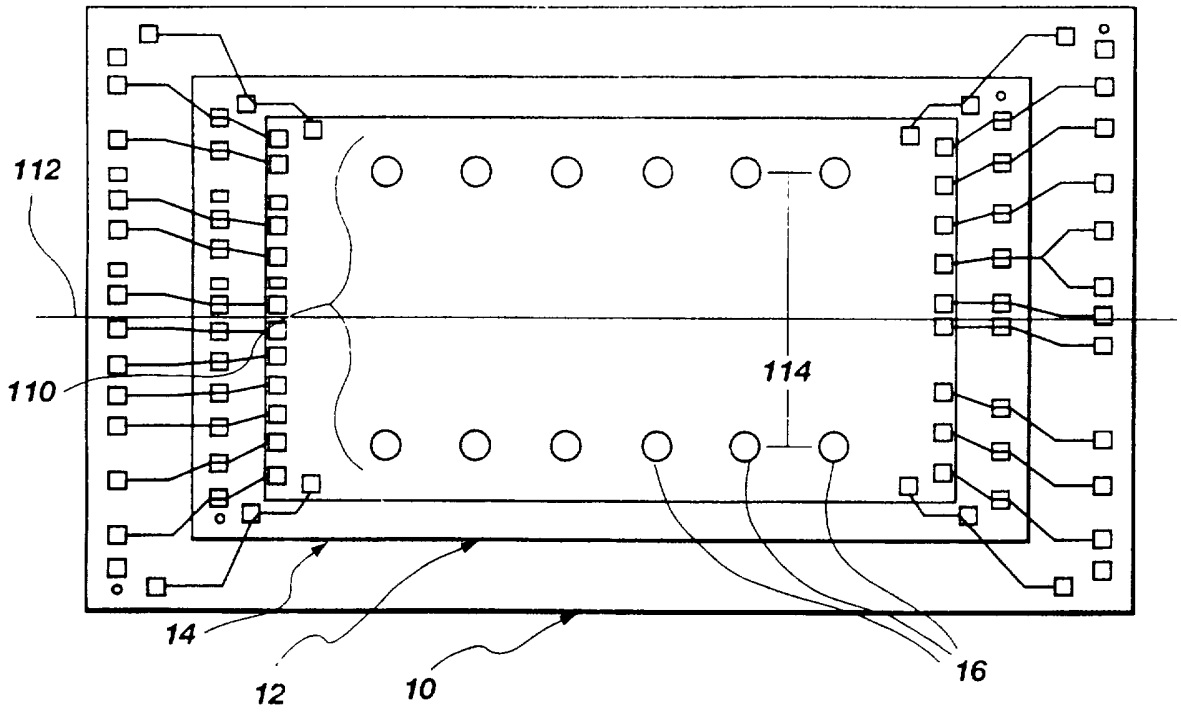

Fig. 6

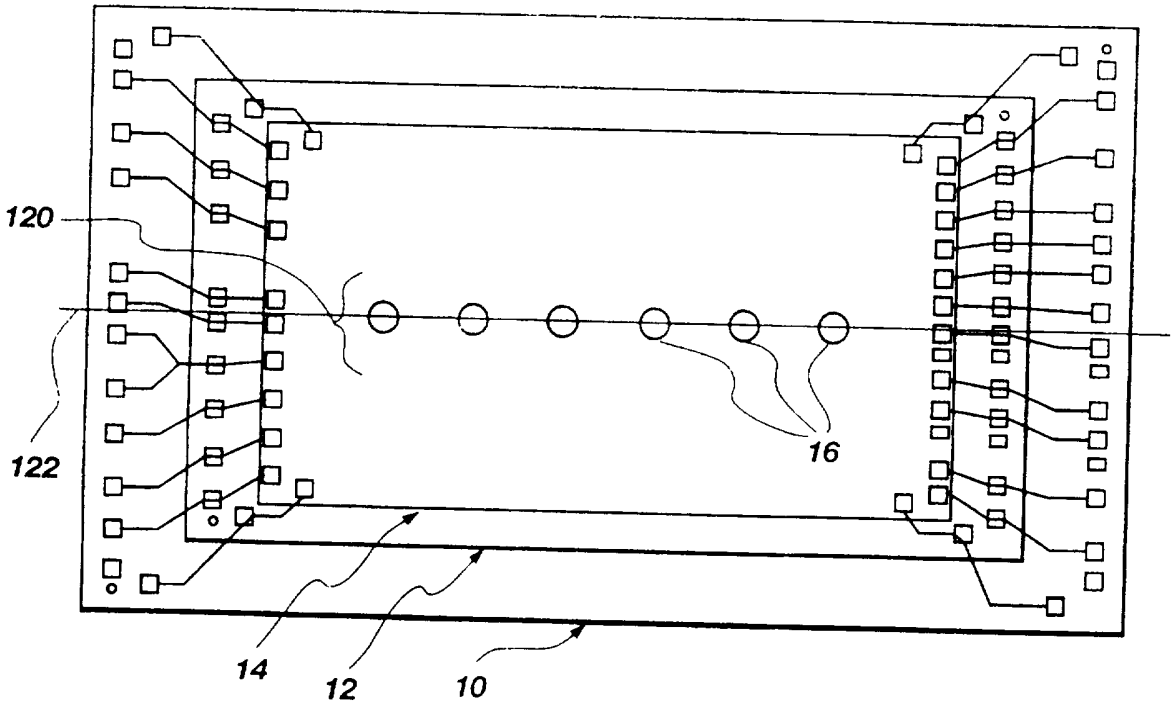

Fig. 7

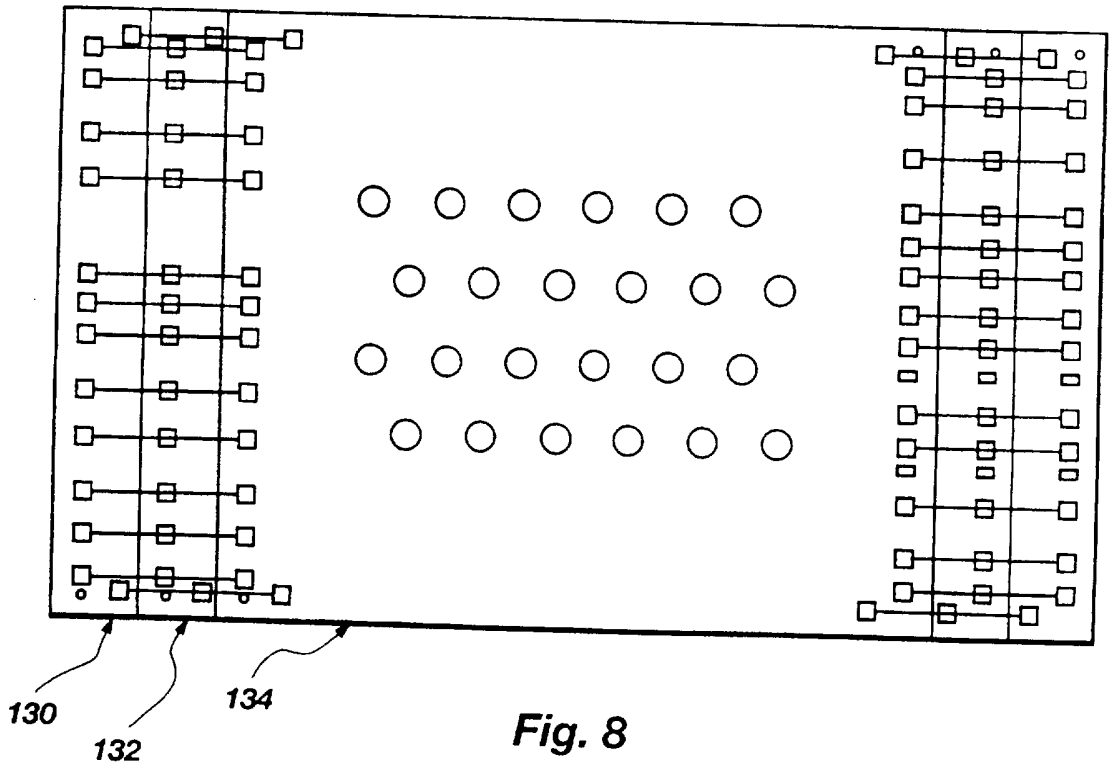

Fig. 8

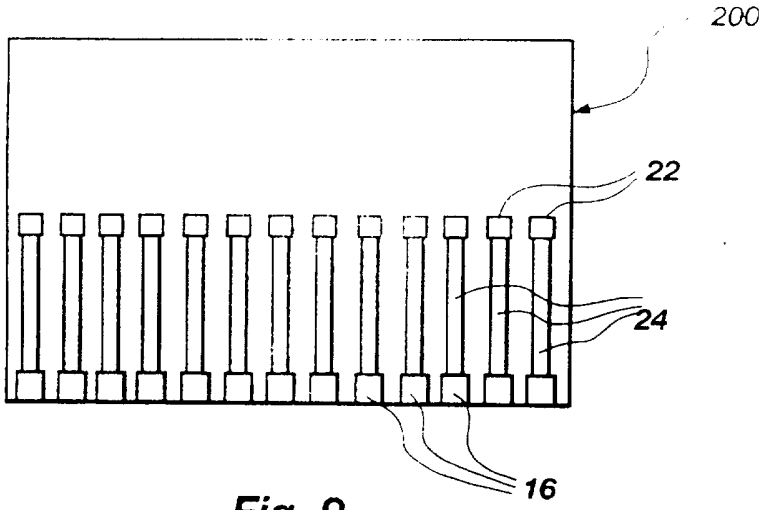

Fig. 9

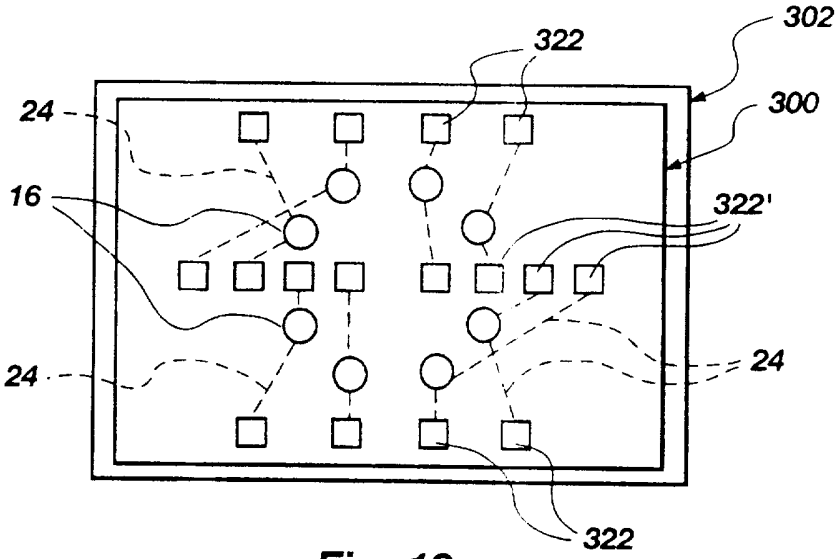

Fig. 10

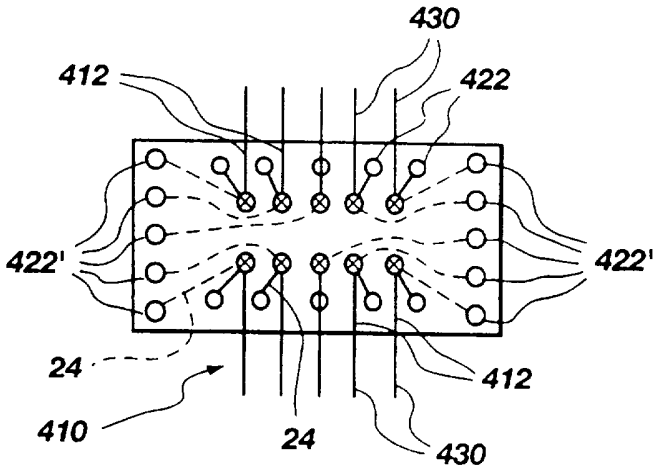

Fig. 11

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/05433

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 23/28; H05K 7/02, 3/36
US CL : 257/780,738,778,735,777,693
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/780,738,778,735,777,693,723,730,673,697,725

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

U.S. Patent and Japan Abstract

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5,490,324 A (NEWMAN) 13 FEBRUARY 1996, FIGURE 4	17-22 & 32-41
X	US 5,355,283 A (MARRS ET AL.) 11 OCTOBER 1994, FIGURE 3	1-41
X, P	US 5,506,756 A (HALEY) 09 APRIL 1996, FIGURES 1-3	17-22 & 32-41
A	US 5,281,151 A (ARIMA ET AL.) 25 JANUARY 1994	1-41
A,P	US 5,521,435 A (MIZUKOSHI) 28 MAY 1996	1-41

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 06 MAY 1997	Date of mailing of the international search report 02 JUN 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer ALEXANDER WILLIAMS Telephone No. (703) 308 4863

Form PCT/ISA/210 (second sheet)(July 1992)*