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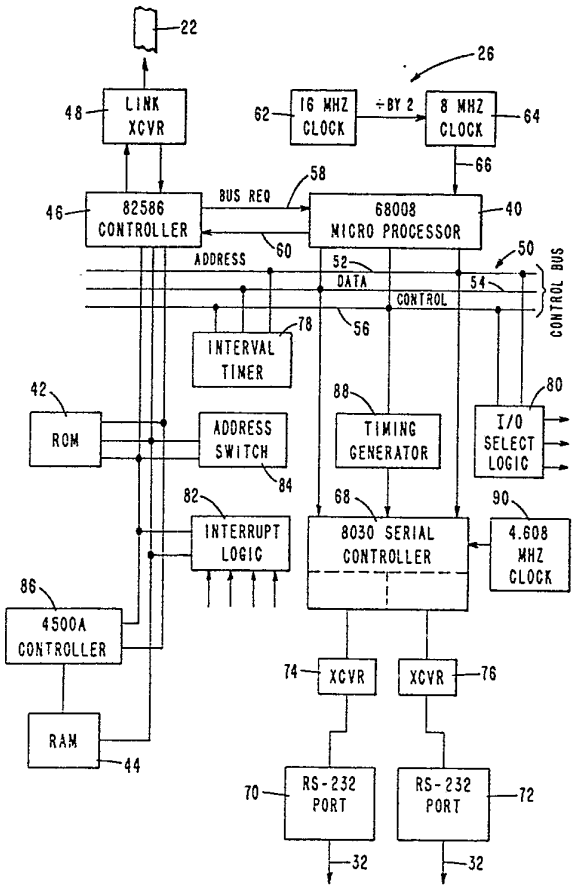
(54) Title: COMMUNICATION PROTOCOL SELECTION FOR DATA PROCESSING SYSTEM

(57) Abstract

A data processing system includes a host processor and a plurality of controllers (26) which are coupled to a common communication channel (22) and which are arranged to control the transfert of data between the host processor and a plurality of remote processing devices. The system also includes means for storing a look-up table containing sets of instructions corresponding to a number of different communication protocols for use with the remote processing devices. Switching means (84) located in each controller (26) provides an address for the controller. During a power-up operation, the address of a controller (26) associated with a selected remote processing device is transmitted to the host processor for use in addressing the look-up table to obtain a communication protocol for the selected processing device, and this information is then loaded into the controller (26) for controlling the transfer of data between the host processor and the selected processing device.



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COMMUNICATION PROTOCOL SELECTION FOR DATA PROCESSING SYSTEM

Technical Field

The present invention relates to a data processing system, and to a method for establishing communication protocols for a data processing system. The invention has application, for example, to a local area network communication system which includes a plurality of processing devices connected to a common communication channel for enabling data to be transferred between the processing devices and a host processing device.

Background Art

With the advent of low cost data processing devices such as personal computers, point-of-sale data terminal devices, etc., local communication networks have been developed to handle a large number of processing devices that may be used within a local business environment. In prior data processing systems, because of the complexity of the communication protocol associated with each processing device, a single communication protocol has been utilized for each data processing system. Thus, if a processing device were added to a processing system after the system had been installed and in operation, such processing device would have been required to operate with the same communication protocol as that of the other processing devices in the system. This restriction has limited the sales appeal of such prior data processing systems.

Disclosure of the Invention

It is therefore an object of the invention to provide a data processing system for transferring data between a host processor and a plurality of remote processing devices, in which the remote processing

devices can operate under different communication protocols.

According to one aspect of the invention there is provided a data processing system for transmitting data between a host processing device and a plurality of remote processing devices, including a communication channel coupled to said host processing device, characterized by storage means coupled to said host processing device for storing a plurality of sets of program instructions corresponding to a number of different communication protocols, and a plurality of controllers coupled to said communication channel for controlling the transfer of data between said host processing device and said remote processing devices, each controller including: data generating means for generating data identifying the controller; and processing means arranged to transmit over said communication channel the identifying data to said host processing device enabling said host processing device, using the identifying data as an address, to retrieve from said storage means a set of program instructions for controlling the transfer of data between said host processing device and a remote processing device controlled by said controller and to transfer this set of program instructions to said controller.

According to another aspect of the invention there is provided a method for establishing communication protocols for a data processing system which includes a host processor and remote processing devices, characterized by the steps of: storing a plurality of sets of program instructions in storage means in which each set of instructions controls the transfer of data between said host processor and a remote processing device; generating a plurality of binary signals identifying a selected remote processing device in the data processing system;

addressing said storage means using the binary signals as an address to retrieve a predetermined set of program instructions from said storage means for the selected remote processing device; and transferring the predetermined set of program instructions to control means associated with the selected remote processing means for controlling the transfer of data between said host processor and the selected remote processing means.

Brief Description of the Drawings

An embodiment of the invention will now be described by way of example with reference to the accompanying drawings, in which:

Fig. 1 is a block diagram of a data processing system in which the present invention is incorporated;

Fig. 2 is a block diagram of a communication controller used in the data processing system of Fig. 1;

Fig. 3 is a schematic representation of a rotary switch included in the controller of Fig. 2 for generating binary signals representing the address of the controller;

Fig. 4 is a flow chart of some of the events which occur during a power-up operation of the controller of Fig. 2; and

Fig. 5 is a flow chart of some of the events which occur during a power-up operation of a host processor included in the system of Fig. 1.

Best Mode for Carrying Out the Invention

Referring to Fig. 1, there is shown a block diagram of a data processing system in which a host processor 20 is coupled over a communication channel or link 22 to a plurality of remote processing devices which include a plurality of data terminal devices 24

(only one of which is shown in Fig. 1) and communication controllers 26 which control the transfer of data between the terminal devices 24 and the host processor 20. Each controller 26 and each terminal device 24 is connected to the channel 22 through a tap box 28 and a bus 30, and also the host processor 20 is connected to the channel 22 through a tap box 28. Each of the controllers 26 is capable of being coupled over communication lines 32 through modems 33 to remote controllers 34 which in turn control the transferring of data between the host processor 20 and processing devices such as data terminal devices 35 which are more remote from the host processor 20 than are the devices 24, the devices 35 being connected to the remote controllers 34. A disk file memory 37 connected to the host processor 20 has stored therein a look-up table which contains a plurality of sets of program instructions with different types of communication protocols such as A sync, bi-sync and bit sync that are used by the processing devices in transferring data over the channel 22.

Referring now to Fig. 2, the controller 26 shown therein includes a Motorola 68008 microprocessor 40 which is commercially available from the Motorola Corporation of Phoenix, Arizona, U.S.A. The microprocessor 40 is supported by a 32K ROM memory 42 and a 32K dynamic RAM memory 44. An Intel 82586 controller device 46 which is commercially available from the Intel Corporation of Santa Clara, California, U.S.A., interfaces the controller 26 through a link transceiver 48 to the communication channel 22. The controller 46 also interfaces with a local control bus generally indicated by the numeral 50 which includes an address line 52, a data line 54 and a control line 56. The interface device 46 is also connected to the microprocessor 40 over a bus request line 58 and a bus

granted line 60. Clock generators 62 and 64 supply 8 Mhz clock signals over line 66 to the microprocessor 40.

Further included in the controller 26 is a Zilog Z8030 serial controller 68 which controls the transfer of data through transceivers 74 and 76, and over a pair of RS-232 ports, and over lines 32 to the remote controllers 34 (Fig. 1). The serial controller 68 is commercially available from the Zilog Corporation of Santa Clara, California, U.S.A. The lines 32 are normally connected to the controllers 34 for use in transferring data between the controller 68 and the processing devices 35 associated with the controllers 34 in a manner that is well known in the art. The controller 68 is capable of supporting a large variety of communication protocols such as SDLC/HDLC, asynchronous data formats, and all RS232 type synchronous formats including character, byte and bit oriented protocols. Further included in the controller 26 are an interval timer 78, an I/O select logic circuit 80, an interrupt logic circuit 82 and an address switch 84, the details of which will be described more fully hereinafter. Associated with the RAM memory 44 is a Texas Instruments TWS4500A controller 86, while a timing generator 88 and a 4.608 MHZ clock source 90 are associated with the serial controller 68. The controller 86 is commercially available from the Texas Instruments Corporation of Dallas, Texas, U.S.A.

Referring now to Fig. 3, there is shown a schematic diagram of the address switch 84 (Fig. 2). The switch 84 comprises a 16 position hexadecimal rotary switch which is manually set to provide the address of the respective controller 26. The switch 84 is commercially available from ALPS USA of Rockville Center, N.Y., U.S.A. as Part No. SRQH010. The setting of the switch 84 results in a four bit

binary word, representing the address of the controller 26, appearing on the output lines 86-92 inclusive of the switch which is transmitted to a 74LS244 buffer member 94. The binary signals for each of the output lines are derived from a 5-volt power source 95 applied through a respective pull-up resistor 97. The buffer member 94 is enabled by a signal CR/W appearing on a control line 96 of the control bus 50 (Fig. 2) and a signal SELASW/ appearing on a control line 98. These signals are outputted by the microprocessor 40 and the I/O select logic circuit 80 respectively. When the signal SELASW/ is low, the buffer member 94 will be enabled to output on lines 106 the binary signals applied to the buffer 94 on input lines 86-92 inclusive, upon the signal CR/W going high. The signal CR/W is transmitted through an inverter gate 100 and into one input of an AND gate 102 which also receives the signal SELASW/ on line 98. The AND gate 102 will output a control signal over line 104 to the buffer 94, enabling the buffer to output the binary signals appearing on input lines 86-92 inclusive over the output lines 106 to the microprocessor 40.

It should be understood that the address switches 84 of the various controllers 26 are manually set so that each controller 26 has a different address.

Referring now to Fig. 4, there is shown a flow diagram of the events which occur during a power-up operation of a selected controller 26. Upon the application of power (block 108) to the selected controller 26, the respective microprocessor 40 will initialize the memory 44 (block 109) and read (block 110) the binary signals appearing on the output lines 106 (Fig. 3) of the buffer 94. The microprocessor 40 will then multiply the address value read by two (block 112) and add 190 to the product (block 114) to

obtain an address identifying the selected controller 26. The microprocessor 40 will then store the address in the RAM memory 44 (block 116), and the controller 46 will transmit the address (block 118) as part of an identification message to the host processor 20. The microprocessor 40 will then initialize buffers (not shown) in the RAM memory 44 (block 120) preparatory to receiving the data from the host processor 20, which data includes the communication protocol for the selected controller 26. After the buffers in the RAM memory 44 have been initialized, the microprocessor 40 will send a message to the host processor 20 requesting (block 122) data for use in its operation.

The host processor 20, during a power-up operation (block 124) (Fig. 5), will wait until it receives a power up message (block 126) from the selected controller 26 identifying the controller, which message includes the controller address. The host processor 20 will then store the power up message including the address (block 128) in a RAM memory located in the processor (not shown) and wait (block 130) until it receives a message from the controller 26 requesting a load message. By sending this request, the controller 26 indicates that the RAM memory 44 (Fig. 2) is ready to receive the load data. The host processor 20 then retrieves the controller address from its storage in memory, and using this address to address the table 37 (Fig. 1), located in the processor 20, will obtain the communication protocol instructions (block 132) stored in the look-up table 37 assigned to the controller 26. The processor then sends a message (block 134) to the controller 26 indicating that it is ready to download the data. After receiving an acknowledge message (block 136) from the controller indicating that it is ready to receive the data, the host processor 20 proceeds to transmit the data message including the

instructions for the particular communication protocol (block 138) assigned to the controller 26 to the controller where it is stored in the RAM memory 44 (Fig. 2). This procedure will be repeated with respect to any communication controller that is coupled to the host processor 20.

CLAIMS

1. A data processing system for transmitting data between a host processing device (20) and a plurality of remote processing devices (24, 35), including a communication channel (22) coupled to said host processing device, characterized by storage means (27) coupled to said host processing device (20) for storing a plurality of sets of program instructions corresponding to a number of different communication protocols, and a plurality of controllers (26) coupled to said communication channel (22) for controlling the transfer of data between said host processing device (20) and said remote processing devices (24, 25), each controller (26) including: data generating means (84) for generating data identifying the controller (26); and processing means (40) arranged to transmit over said communication channel (22) the identifying data to said host processing device (20) enabling said host processing device, using the identifying data as an address, to retrieve from said storage means (37) a set of program instructions for controlling the transfer of data between said host processing device and a remote processing device controlled by said controller (26) and to transfer this set of program instructions to said controller.

2. A data processing system according to claim 1, characterized in that said data generating means includes settable means (84) settable to a selected position for generating data identifying said controller (26).

3. A data processing system according to claim 2, characterized in that said settable means (84) comprises a switching member settable to a

plurality of positions in which said switching member will output data representing its set position.

4. A data processing system according to either claim 2 or claim 3, characterized in that said settable member (84) comprises a rotary switch member.

5. A data processing system according to any one of the preceding claims, characterized in that said generating means (84) is arranged to generate identifying data in the form of a plurality of binary signals.

6. A data processing system according to claim 5, characterized in that the identifying data comprises a four-bit binary word.

7. A data processing system according to any of the preceding claims, characterized in that said storing means (37) has a look-up table stored therein.

8. A method for establishing communication procotols for a data processing system which includes a host processor (20) and remote processing devices (24, 35), characterized by the steps of: storing a plurality of sets of program instructions in storage means (37) in which each set of instructions controls the transfer of data between said host processor and a remote processing device; generating a plurality of binary signals identifying a selected remote processing device in the data processing system; addressing said storage means (37) using the binary signals as an address to retrieve a predetermined set of program instructions from said storage means (37) for the selected remote processing device; and transferring the predetermined set of program

instructions to control means (26) for controlling the transfer of data between said host processor and the selected remote processing means.

9. A method according to claim 8, characterized in that the step of generating a plurality of binary signals includes the step of setting a switching member (84) associated with the selected remote processing device to a position enabling the switching member to generate the binary signals identifying the selected remote processing device.

FIG. 1

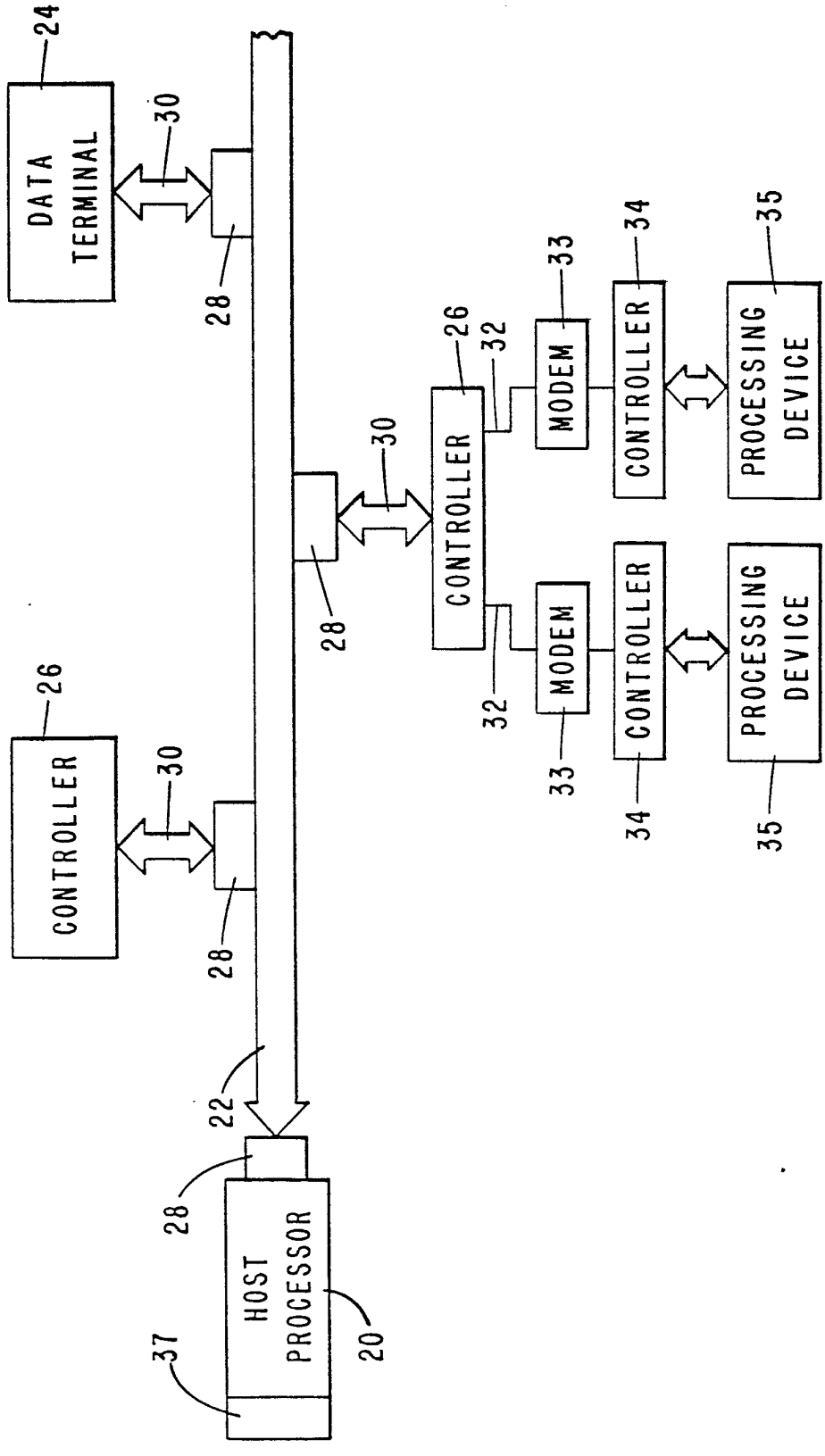

DATA TERMINAL
24
30
28
CONTROLLER
26
30
28
22
28
HOST PROCESSOR
20
37
CONTROLLER
26
30
28
32
MODEM
33
CONTROLLER
34
PROCESSING DEVICE
35
32
MODEM
33
CONTROLLER
34
PROCESSING DEVICE
35

FIG. 2

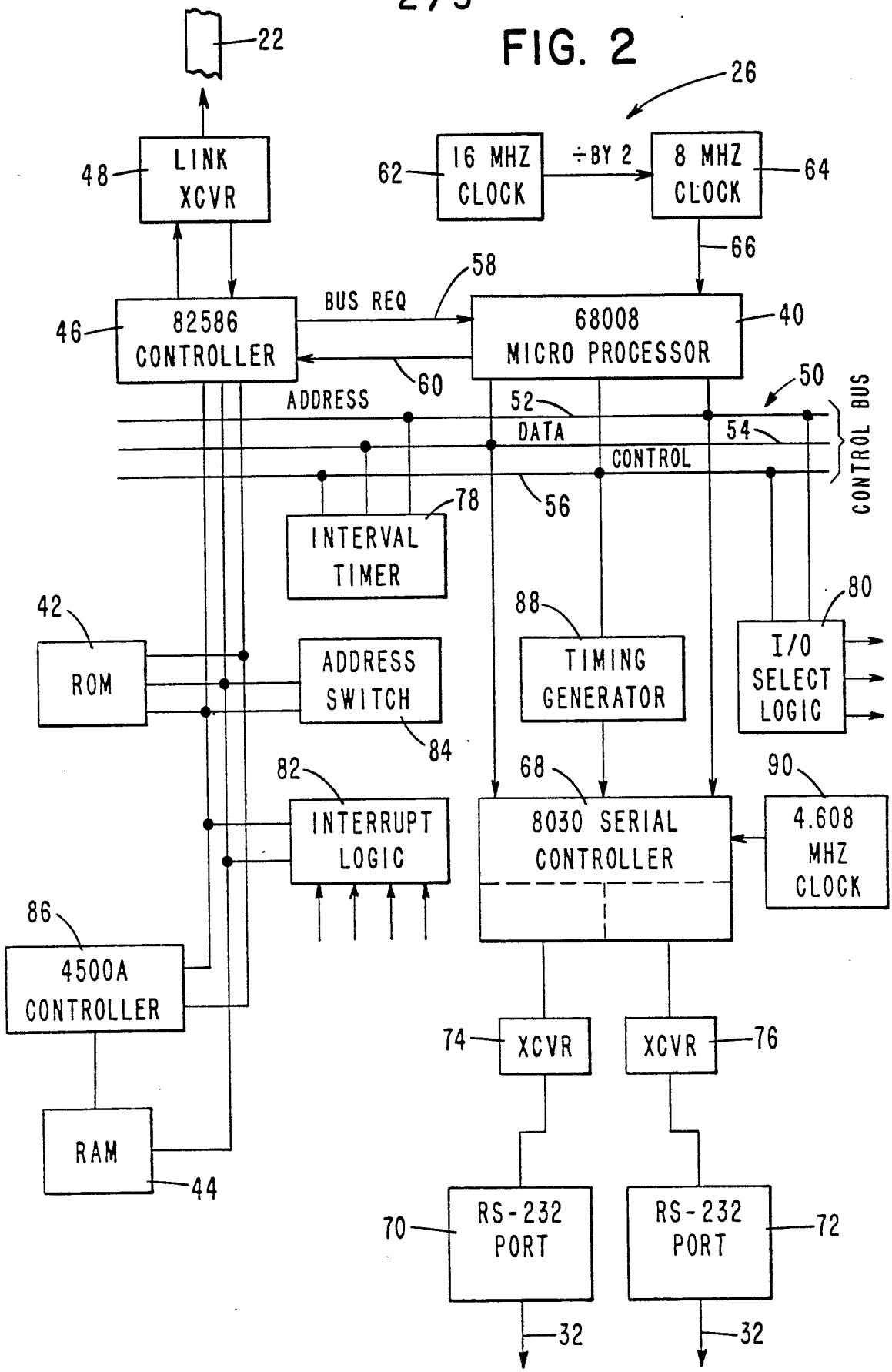

22
26
48
LINK XCVR
62
16 MHZ CLOCK
÷BY 2
8 MHZ CLOCK
64
66
58
BUS REQ
46
82586 CONTROLLER
68008 MICRO PROCESSOR
40
60
50
ADDRESS
52
DATA
54
CONTROL
CONTROL BUS
78
INTERVAL TIMER
56
42
ROM
ADDRESS SWITCH
84
88
TIMING GENERATOR
80
I/O SELECT LOGIC
82
INTERRUPT LOGIC
68
8030 SERIAL CONTROLLER
90
4.608 MHZ CLOCK
86
4500A CONTROLLER
74
XCVR
XCVR
76
RAM
44
70
RS-232 PORT
RS-232 PORT
72
32
32

FIG. 3

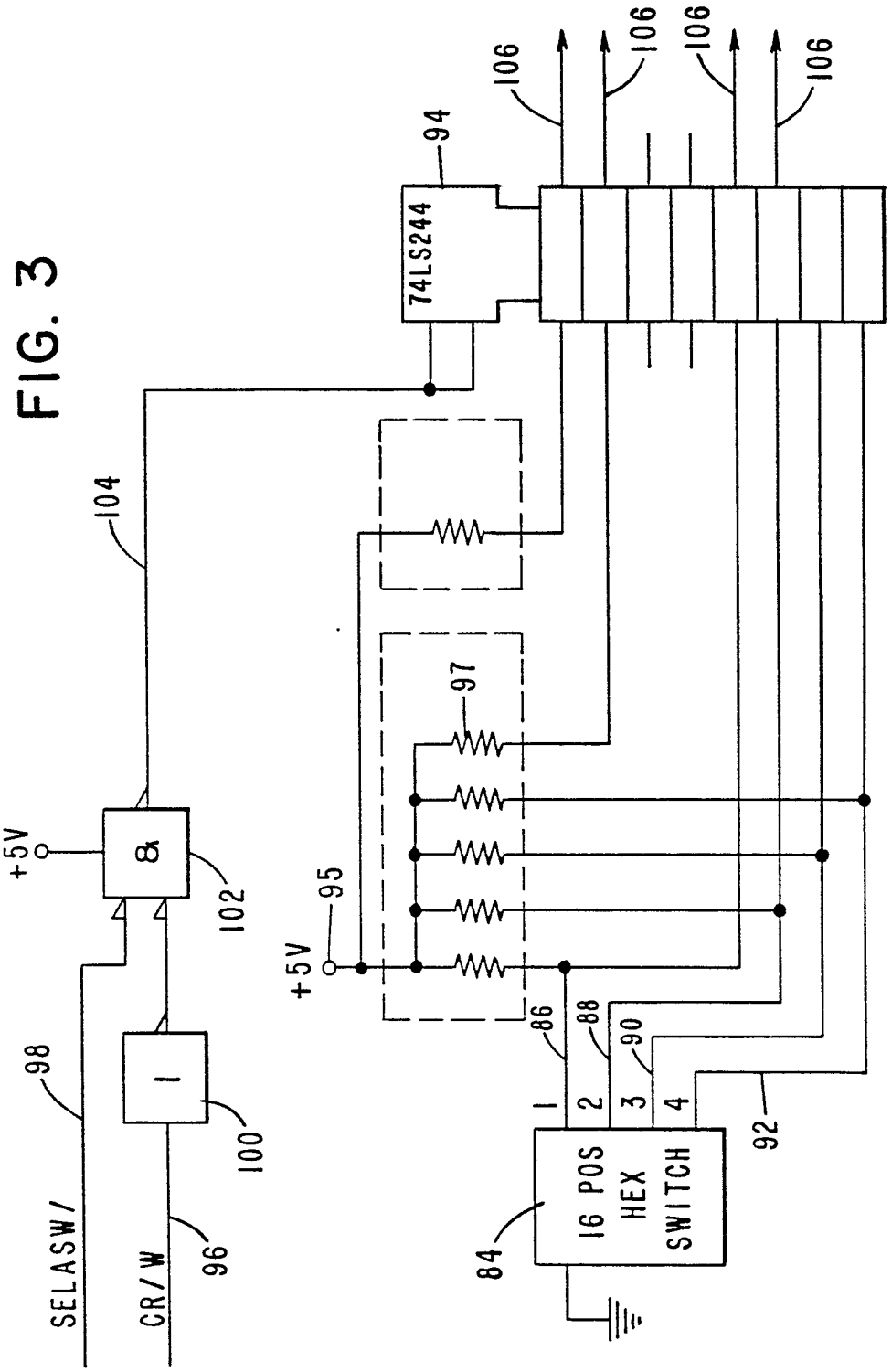

106
106
106
106
94
74LS244
104
97
+5V
8
102
95
+5V
98
1
100
SELASW/
CR/W
96
86
88
90
1
2
3
4
92
16 POS
HEX
SWITCH
84

FIG. 4

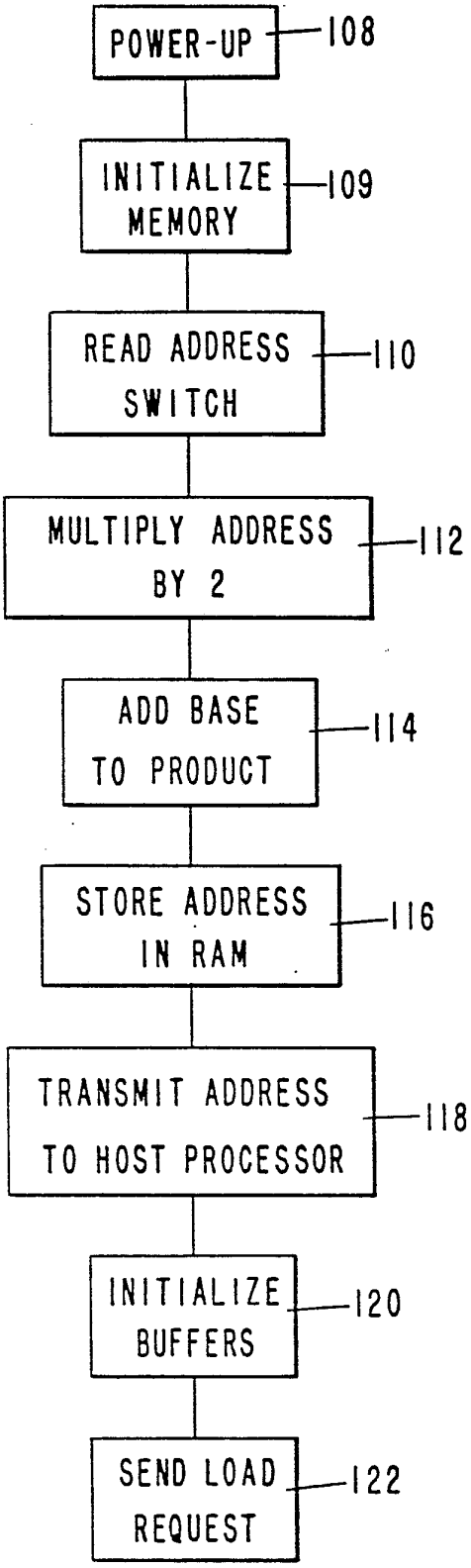
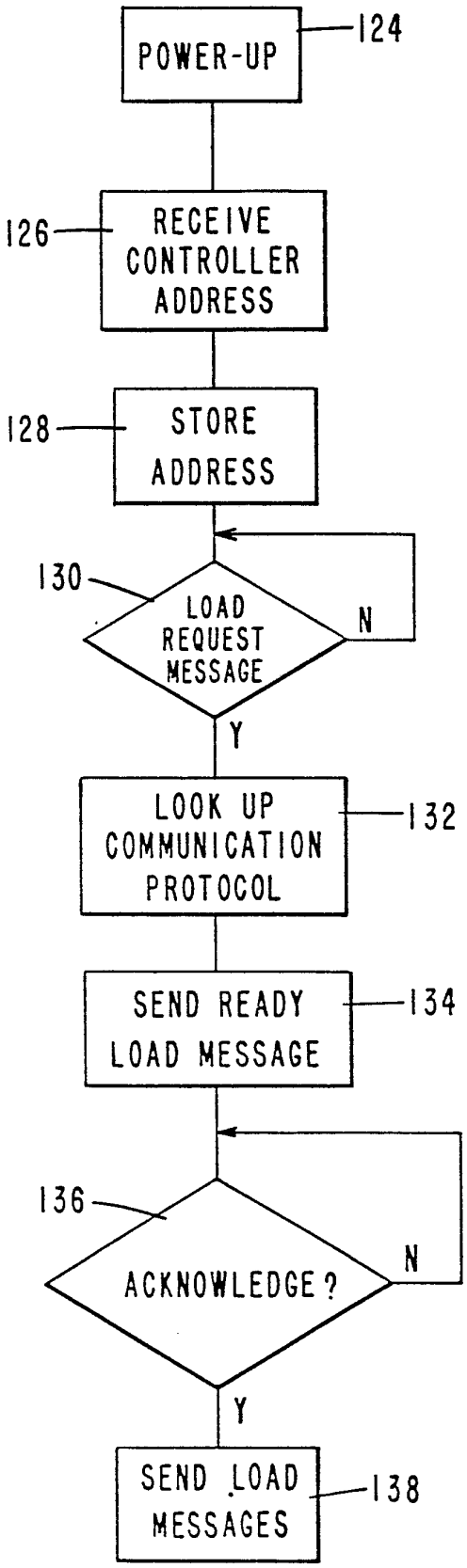

POWER-UP
108
INITIALIZE MEMORY
109
READ ADDRESS SWITCH
110
MULTIPLY ADDRESS BY 2
112
ADD BASE TO PRODUCT
114
STORE ADDRESS IN RAM
116
TRANSMIT ADDRESS TO HOST PROCESSOR
118
INITIALIZE BUFFERS
120
SEND LOAD REQUEST
122

FIG. 5


POWER-UP
124
126
RECEIVE CONTROLLER ADDRESS
128
STORE ADDRESS
130
LOAD REQUEST MESSAGE
N
Y
LOOK UP COMMUNICATION PROTOCOL
132
SEND READY LOAD MESSAGE
134
136
ACKNOWLEDGE?
N
Y
SEND LOAD MESSAGES
138

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/01660

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 13/42

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F 13/42

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	Patents Abstracts of Japan, volume 6, no. 104 (P-122)(982), 15 June 1982, & JP, A, 5736340 (Fujitsu) (27 February 1982) see the whole abstract	1,7,8
A	WO, A, 82/03285 (MACKEY) 30 September 1982 see page 5, lines 23-24; page 12, lines 12-19; page 14; page 15, lines 1-5; page 19, lines 1-21; figures 1,2	2,3,5,6
A	EP, A3, 0068831 (HONEYWELL) 5 January 1983 see page 2, lines 5-16; page 5, lines 11-26; figure 5	2,3,5
A	EDN Electrical Design News, volume 25, no. 3, February 1980, (Denver, US), Bonney: "For µP-system data entry, thumbwheel switches excel", pages 161-165 see page 163, figure 4; page 164, figure 5	4

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
13th November 1986	16 DEC 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	L. ROSSI

Form PCT/ISA/210 (second sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/01660 (SA 14279)

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
WO-A- 8203285	30/09/82	EP-A-	0074396	23/03/83
EP-A- 0068831	05/01/83	JP-A-	58006646	14/01/83
		AU-A-	8414482	06/01/83
		CA-A-	1180126	25/12/84