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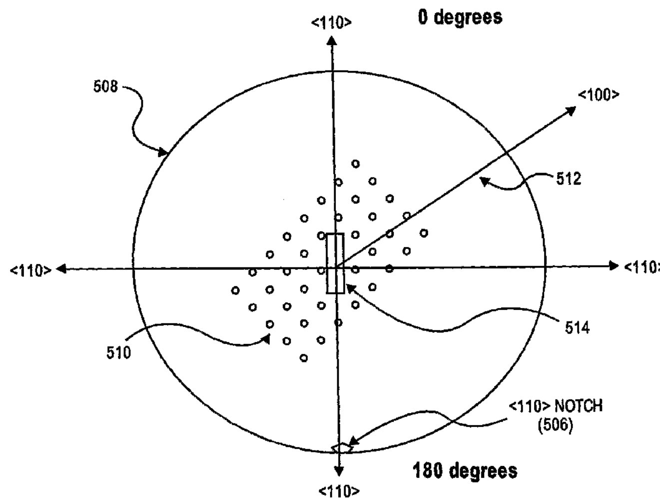

(57) Abstract: A high mobility semiconductor assembly. In one exemplary aspect, the high mobility semiconductor assembly includes a first substrate having a first reference orientation located at a <110> crystal plane location on the first substrate and a second substrate formed on top of the first substrate. The second substrate has a second reference orientation located at a <100> crystal plane location on the second substrate, wherein the first reference orientation is aligned with the second reference orientation. In another exemplary aspect, the second substrate has a second reference orientation located at a <110> crystal plane location on the second substrate, wherein the second substrate is formed over the first substrate with the second reference orientation being offset to the first reference orientation by about 45 degrees.

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HIGH MOBILITY TRI-GATE DEVICES AND METHODS OF FABRICATION

FIELD

[0001] The present invention relates to the field of semiconductor integrated circuit manufacturing, and more particularly to a high mobility tri-gate device such as a high mobility tri-gate transistor and their methods of fabrication.

DISCUSSION OF RELATED ART

[0002] In order to increase device performance, silicon on insulator (SOI) transistors have been proposed for the fabrication of modern integrated circuits. Figure 1 illustrates a standard fully depleted silicon on insulator (SOI) transistor 100. The SOI transistor 100 includes a single crystalline silicon substrate 102 having an insulating layer 104, such as a buried oxide formed thereon. A single crystalline silicon body 106 is formed on the insulating layer 104. A gate dielectric layer 108 is formed on the single crystalline silicon body 106 and a gate electrode 110 is formed on the gate dielectric 108. Source 112 and drain 114 regions are formed in the silicon body 106 along laterally opposite sides of the gate electrode 110.

[0003] Fully depleted SOI have been proposed as a transistor structure to take advantage of ideal sub-threshold gradients for optimized on current/off current ratios. In order to achieve ideal subthreshold gradients with the transistor 100, the thickness (Tsi) of the silicon body 106 must be about 1/3 the size of the gate length (Lg) of the transistor or Tsi = Lg/3. However, as gate lengths scale, especially as they approach 30nm, the need for ever decreasing silicon film thickness makes this approach increasingly impractical. At 30 nanometer gate length, the thickness required of the silicon body is thought to need to be less than 10 nanometers, and around 6 nanometer for a 20 nanometer gate length. The fabrication of thin silicon films with thicknesses of less than 10 nanometers, is considered to be extremely difficult. On one hand, obtaining wafer uniformity on the order of one nanometer is a difficult challenge. On the other

hand, to be able to contact these thin films to form raised source/drain regions to decrease junction resistance, becomes almost impossible since the thin silicon layer in the source/drain regions becomes consumed during the gate etch and various cleans following the gate etch and spacer etch leaving insufficient silicon 106 for silicon to grow on.

[0004] A double gate (DG) device, such as shown in Figures 2A and 2B, have been proposed to alleviate the silicon thickness issue. The double gate (DG) device 200 includes a silicon body 202 formed on an insulating substrate 204. A gate dielectric 206 is formed on two sides of the silicon body 202 and a gate electrode 208 is formed adjacent to the gate dielectric 206 formed on the two sides of the silicon body 202. A sufficiently thick insulating layer 209, such as silicon nitride, electrically isolates the gate electrode 208 from the top of silicon body 202.

[0005] Double gate (DG) device 200 essentially has two gates, one on either side of the channel of the device. Because the double gate device 200 has a gate on each side of the channel, thickness (Tsi) of the silicon body can be double that of a single gate device and still obtain a fully depleted transistor operation. That is, with a double gate device 200 a fully depleted transistor can be formed where Tsi = (2xLg)/3. The most manufacturable form of the double gate (DG) device 200, however, requires that the body 202 patterning be done with photolithography that is 0.7 x smaller than that used to pattern the gate length (Lg) of the planar device (e.g., the transistor 100). In order to obtain high density integrated circuits, it is generally desirable to have the most aggressive lithography occur with respect to the gate length (Lg) of the gate electrode 208. Although, double gate structures double the thickness of the silicon film (since there now is a gate on either side of the channel) these structures, however, are hideously difficult to fabricate. For example, the silicon body 202 requires a silicon body etch which can produce a silicon body 202 with an aspect ratio (height to width) of about 5:1. Additionally, with demand for high device performance continue to increase, devices with high mobility to increase device performance are desirable.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] Figure 1 is an illustration of a cross-sectional view of a depleted substrate transistor.

[0007] Figures 2A and Figure 2B illustrate a double gate depleted substrate transistor.

[0008] Figure 3 is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

[0009] Figure 4 is an illustrative comparison of <100> and <110> mobility characteristics.

[0010] Figure 5 is an illustration of a silicon ingot grown in a <100> crystal plane direction and having a reference orientation at a <110> crystal plane location.

[0011] Figure 6 is an illustration of a wafer sliced from the silicon ingot shown in Figure 5.

[0012] Figures 7A-7B illustrate a wafer sliced from the silicon ingot shown in Figure 5 with a device formed thereon.

[0013] Figures 8A-8B illustrate a wafer with a reference notch formed at a <100> crystal plane location.

[0014] Figure 9 is an illustration of a tri-gate transistor in accordance with an embodiment of the present invention.

[0015] Figure 10 is an illustration of a method of forming a high mobility silicon substrate for a tri-gate device in accordance to an embodiment of the present invention.

[0016] Figures 11-13 illustrate exemplary methods of forming a high mobility silicon substrate for a tri-gate device in accordance to an embodiment of the present invention.

[0017] Figure 14A illustrates an exemplary silicon ingot with a <100> reference notch.

[0018] Figure 14B illustrates the bonding of a wafer having a <100> reference notch to a wafer having a <110> reference notch.

[0019] Figures 15A-15J illustrate an exemplary method of making a tri-gate transistor in accordance to an embodiment of the present invention.

DETAILED DESCRIPTION

[0020] Embodiments of the present invention pertain to a novel high mobility non-planar device or a tri-gate device such as a tri-gate transistor structure and methods of fabricating the same. In the following description numerous specific details are set forth in order to provide a thorough understanding in the embodiments of the present invention. In other instances, well-known semiconductor process and manufacturing techniques have not been described in particular detail in order to not unnecessarily obscure the embodiments of the present invention.

[0021] Embodiments of the present invention pertain to a high mobility non-planar device (e.g., a tri-gate transistor). The high mobility characteristic of the non-planar device is achieved by rotation or relocation of a reference orientation of a substrate wafer that is used to form the high mobility non-planar device. Figure 3 illustrates an exemplary non-planar device 300 (e.g., a tri-gate transistor).

[0022] In an embodiment of the present invention, the tri-gate transistor 300 is a semiconductor on insulator (SOI) transistor. The tri-gate transistor 300 includes a thin semiconductor body 308 formed on a substrate 302; the substrate 302 can be an insulating substrate (e.g., the substrate 302 including an oxide film) or a semiconductor substrate. The semiconductor body 308 includes a gate dielectric 305 which is formed on the top surface and the sidewalls of the semiconductor body 308, and a gate electrode 307 which is formed on the gate dielectric 305 on the top surface of the semiconductor body 308 and is formed adjacent to the gate dielectric 307 formed on the sidewalls of the semiconductor body 308. Source and drain regions 330 and 332, respectively, are formed in the semiconductor body 308 on opposite sides of the gate electrode 307. Because the gate electrode 307 and the gate dielectric 305 surround the semiconductor

body 308 on three sides, the transistor 300 essentially has three separate channels and gates. The gate "width" of a transistor is equal to the sum of each of the three sides of the semiconductor body.

[0023] Because there are three separate channels formed in the semiconductor body, the semiconductor body can be fully depleted when the transistor is turned "ON", thereby enabling the formation of a fully depleted transistor with gate lengths of less than 30 nanometers without requiring the use of ultra-thin semiconductor bodies or requiring photolithographic patterning of the semiconductor bodies to dimensions less than the gate length (Lg) of the device. Because the tri-gate transistor of the present invention can be operated in a fully depleted manner, the device is characterized by ideal (e.g., very sharp) subthreshold slope and a reduced drain induced barrier lowering (DIBL) short channel effect of less than 100mV/V and ideally about 60 mV/V which results in a lower leakage current when the device is turned "OFF" resulting in lower power consumption.

[0024] It is desirable to have non-planar devices such as the tri-gate transistor 300 being high mobility devices for improved device performance. In the embodiments of the present invention, in order to improve the mobility of the non-planar device 300, the crystal plane structure of the semiconductor body 308 is altered. As shown in Figure 3, the non-planar device 300 has a vertical field on the top surface of the semiconductor body 308 that has a <100> crystal plane. The vertical field for the sides of semiconductor body 308 has a <110> crystal plane. It has been shown that there is a significant difference between the <100> and the <110> crystal planes in term of mobility. The <110> crystal plane has a mobility value that is about half of the <100> crystal plane as shown in Figure 4. As shown in Figure 4, the Takagi line for the <100> crystal plane is significantly higher than the Takagi line for the <110> crystal plane. One way to improve the mobility of the non-planar device is to have the vertical fields for all sides of the semiconductor body 308 have the <100> crystal plane.

[0025] Most often, the substrate 302 is made of a semiconductor wafer, which is then processed where films and structures are formed therein to form semiconductor devices such as the tri-gate device 300. In one instance, the substrate 302 is a bulk silicon wafer. An insulation layer (e.g., a silicon dioxide film) is formed over the substrate 302, and a device quality semiconductor film (e.g., a monocrystalline silicon) is formed over the insulation layer. The device 300 is then formed in the device quality semiconductor film. It is a practice in the semiconductor fabrication field to create a reference orientation on a wafer or wafers that are used to form devices. The reference orientation is typically a small notch created in the wafer. The reference orientation is useful for equipments (e.g., etching tool or lithography tool) alignment purpose and especially for fabrication repeatability (e.g., device processes such as lithography and etching). The processing tools thus have an alignment point where each notch on a particular wafer is aligned for processing. As is known, silicon or other semiconductor material has different crystal cubic orientation at different planes of the wafer. Thus, for repeatability of the crystal orientation, the reference orientation is created to mark a uniform direction for the wafer. The reference orientation also provides repeatability of processes from wafer to wafer.

[0026] One way to create the reference orientation in a wafer is to make a notch at a particular position on the wafer. Currently, an ingot, e.g., a silicon ingot, is grown with seed in the direction of the <100> crystal plane. As illustrated in Figure 5, the ingot 502 is grown in the <100> crystal plane direction. The ingot 502 is the placed in an X-Ray-Diffraction tool to allow one to find the <110> plane direction. During the X-Ray-Diffraction process, the ingot 502 is rotated radially so that the X-Ray-Diffraction beam can visualize and locate the <110> location. Once the <110> location is found, the ingot 502 is marked along the line 504 so that the notch 506 can be formed in each wafer as shown in Figure 6. Grinding may be used to create the line 504. Slicing is then used to slice the ingot 502 to create a plurality of wafer 508. As illustrated in Figure 6, the wafer 508 has a <100> crystal plane in the direction point out

of the page. The notch 506 has a <110> crystal plane and is located at the 180-degree or 6 o'clock position of the wafer 508.

[0027] Figure 7A illustrates further the crystal structure properties of the wafer 508. Circles 510 represent the crystal plane of the crystal structure of the wafer 508 with respect to the plane of the page. As illustrated, the <100> crystal plane is the surface of the wafer 508 and as such in the direction of the arrow 512 pointing out of the page. When a non-planar device 514 is formed in the wafer 508, the sides 514-S of the non-planar device 514 will have the <110> crystal planes as illustrated in Figure 7A. The top side 514-T of the device 514 has the <100> crystal plane. One way to alter the crystal plane structures of the sides of the device 514 formed in the wafer 508 is to rotate or relocate the notch 506. In one embodiment of the present invention, instead of having the notch 506 located at the <110> crystal plane location as conventionally done, the notch 506 is located at a <100> crystal plane location on the wafer 508. In another embodiment, the notch 506 can be marked at the <110> location as conventionally done and the wafer 508 is rotated about 45 degrees (or -45 degrees) in the fabrication tool so that the crystal planes as illustrated by the circles 510 are rotated by about 45 degrees (or -45 degrees).

[0028] Figure 8A illustrates a wafer 802 having a notch 804 at a <100> crystal plane location. The circles 810 shown in the wafer 802 indicate the crystal plane of the crystal structure of the wafer 802 with respect to the plane of the page. Pointing out of the page, the crystal plane of the wafer 802 is <100>. When a non-planar device 806 is formed in the wafer 802, all sides of the devices 806 have a <100> crystal plane. Thus, the top surface 806-T of the device 806 has a <100> crystal plane and all sides 806-S of the devices 806 also have a <100> crystal plane.

[0029] Alternatively, when the wafer has the notch at the <110> location, during processing, the wafer can be rotated by 45 degrees (or -45 degrees). In doing so, when a non-planar device is formed on the wafer, all sides of the devices also have a <100> crystal plane.

[0030] With all sides of the non-planar device having the <100> crystal planes, the non-planar device will have the high mobility characteristic that is desirable for high performance devices.

[0031] Figure 9 illustrates an exemplary non-planar device such as a tri-gate device (e.g., a tri-gate transistor 900) that can benefit from the high mobility characteristic of the device by having the notch of the wafer relocated or rotated. The non-planar device is thus a high mobility non-planar device, which can be a high mobility tri-gate transistor.

[0032] The tri-gate transistor 900 is formed on a substrate 902. In an embodiment of the present invention, the substrate 902 is an insulating substrate which includes a lower monocrystalline silicon substrate 904 upon which is formed an insulating layer 906, such as a silicon dioxide film. The tri-gate transistor 900, however, can be formed on any well-known insulating substrate such as substrates formed from silicon dioxide, nitrides, oxides, and sapphires. In an embodiment of the present invention, the substrate 902 can be a semiconductor substrate, such as but not limited to monocrystalline silicon substrate and gallium arsenide substrate.

[0033] The tri-gate transistor 900 includes a semiconductor body 908 formed on the insulating layer 906 of the insulating substrate 902. The semiconductor body 908 can be formed from a semiconductor film. With the semiconductor film on the insulating substrate 902, the tri-gate transistor 900 can be thought of as an SOI transistor. The semiconductor body 908 can be formed of any well-known semiconductor material, such as but not limited to silicon (Si), germanium (Ge), silicon germanium (Si_xGe_y), gallium arsenide (GaAs), InSb, GaP, GaSb and carbon nanotubes. The semiconductor body 908 is ideally a single crystalline film when the best electrical performance of the transistor 900 is desired such as in microprocessors. The semiconductor body 908, however, can be a polycrystalline film when the transistor 900 is used in applications requiring less stringent performance, such as in liquid crystal displays. The wafer used to form the semiconductor body 908 is processed so that all

sides of the semiconductor body 908 will have a <100> crystal planes as previously described.

[0034] In one embodiment, the semiconductor material used to form the semiconductor body 908 is a wafer (e.g., a silicon wafer) processed or formed with a reference notch located at a <100> crystal plane location on the wafer. In another embodiment, the semiconductor material used to form the semiconductor body 808 is a wafer (e.g., a silicon wafer) processed or formed with a reference notch located at a <110> crystal plane location on the wafer. In this another embodiment, the wafer used to form the semiconductor body 908 is rotated so that the reference notch is offset by about 45 degrees or by -45 degrees.

[0035] The semiconductor body 908 has a pair of laterally opposite sidewalls 910 and 912 separated by a distance, which defines a semiconductor body width 914. Additionally, the semiconductor body 908 has a top surface 916 opposite a bottom surface 918 formed on the substrate 902. The distance between the top surface 916 and the bottom surface 918 defines a body height 920 or the thickness Tsi of the semiconductor body 908. In an embodiment of the present invention the body height 920 is substantially equal to the body width 914. In an embodiment of the present invention, the body 908 has a width 914 and height 920 less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, the body height 920 is between ½ the body width 914 to 2 times the body width 914. The side walls 910 and 912, the top surface 916, and the bottom surface 918 all have a vertical field having the <100> crystal plane structure.

[0036] The tri-gate transistor 900 has a gate dielectric layer 922. The gate dielectric layer 922 is formed on and around three sides of the semiconductor body 908 as shown in Figure 9. The gate dielectric layer 922 is formed on or adjacent to the sidewall 912, on the top surface 916, and on or adjacent to the sidewall 910 of the body 908 as shown in Figure 9. The gate dielectric layer 922 can be any well-known gate dielectric layer. In an embodiment of the present invention, the gate dielectric layer is a

silicon dioxide (SiO_2), silicon oxynitride (SiO_xN_y) or a silicon nitride (Si_3N_4) dielectric layer. In an embodiment of the present invention, the gate dielectric layer 922 is a silicon oxynitride film formed to a thickness of between 5-20Å. In an embodiment of the present invention, the gate dielectric layer 922 is a high K gate dielectric layer, such as a metal oxide dielectric, such as but not limited to tantalum pentaoxide (Ta_2O_5), and titantium oxide (TiO_2). The gate dielectric layer 922 can be other types of high K dielectric, such as but not limited to PZT (lead zirconate titanate).

[0037] The tri-gate device 900 has a gate electrode 924. The gate electrode 924 is formed on and around the gate dielectric layer 922 as shown in Figure 9. The gate electrode 924 is formed on or adjacent to the gate dielectric 922 formed on the sidewall 912 of the semiconductor body 908, is formed on the gate dielectric 922 formed on the top the surface 916 of the semiconductor body 908, and is formed adjacent to or on the gate dielectric layer 922 formed on the sidewall 910 of the semiconductor body 908. The gate electrode 924 has a pair of laterally opposite sidewalls 926 and 928 separated by a distance which defines the gate length (Lg) 930 of the transistor 900. In an embodiment of the present invention the laterally opposite sidewalls 926 and 928 of the gate electrode 924 run in a direction perpendicular to the laterally opposite sidewalls 910 and 912 of the semiconductor body 908.

[0038] The gate electrode 924 can be formed of any suitable gate electrode material. In an embodiment of the present invention the gate electrode 924 comprises of polycrystalline silicon doped to a concentration density between $1x10^{19}$ atoms/cm^3 – $1x10^{20}$ atoms/cm^3. In an embodiment of the present invention the gate electrode can be a metal gate electrode, such as but not limited to, tungsten, tantalum, titanium, and their nitrides. In an embodiment of the present invention the gate electrode is formed from a material having a mid-gap work function between 4.6-4.8 eV. It is to be appreciated, the gate electrode 924 need not necessarily be a single material and can be a composite stack of thin films, such as but not limited to a polycrystalline silicon/metal electrode or a metal/polycrystalline silicon electrode.

[0039] The tri-gate transistor 900 has a source region 930 and a drain region 932. The source region 930 and drain region 932 are formed in semiconductor body 908 on opposite sides of gate electrode 924 as shown in Figure 9. The source region 930 and the drain region 932 are formed of the same conductivity type such as N-type or P-type conductivity. In an embodiment of the present invention the source region 930 and the drain region 932 have a doping concentration of between $1x10^{19}$, and $1x10^{21}$ atoms/cm^3. The source region 930 and the drain region 932 can be formed of uniform concentration or can include sub-regions of different concentrations or doping profiles such as tip regions (e.g., source/drain extensions). In an embodiment of the present invention when the transistor 900 is a symmetrical transistor, the source region 930 and the drain region 932 will have the same doping concentration and profile. In an embodiment of the present invention when the tri-gate transistor 900 is formed as an asymmetric transistor then the doping concentration and profile of the source region 930 and the drain region 932 may vary in order to obtain a particular electrical characteristic.

[0040] The portion of semiconductor body 908 located between the source region 930 and the drain region 932, defines the channel region 950 of the transistor 900. The channel region 950 can also be defined as the area of the semiconductor body 908 surrounded by the gate electrode 924. At times however, the source/drain region may extend slightly beneath the gate electrode through, for example, diffusion to define a channel region slightly smaller than the gate electrode length (Lg). In an embodiment of the present invention, the channel region 950 is intrinsic or undoped monocrystalline silicon. In an embodiment of the present invention, the channel region 950 is doped monocrystalline silicon. When channel region 950 is doped, it is typically doped to a conductivity level of between $1x10^{16}$ to $1x10^{19}$ atoms/cm^3. In an embodiment of the present invention, when the channel region 950 is doped it is typically doped to the opposite conductivity type of the source region 930 and the drain region 932. For example, when the source and drain regions are N-type conductivity the channel region 950 would be doped to p type conductivity. Similarly, when the source and drain

regions are P type conductivity the channel region 950 would be N-type conductivity. In this manner the tri-gate transistor 900 can be formed into either a NMOS transistor or a PMOS transistor respectively. The channel region 950 can be uniformly doped or can be doped non-uniformly or with differing concentrations to provide particular electrical and performance characteristics. For example, the channel regions 950 can include well-known "halo" regions, if desired.

[0041] By providing a gate dielectric and a gate electrode which surrounds the semiconductor body 908 on three sides, the tri-gate transistor 900 is characterized in having three channels and three gates, one (g1) which extends between the source and drain regions on side 912 of silicon body 908, a second (g2) which extends between the source and drain regions on the top surface 916 of silicon body 908, and the third (g3) which extends between the source and drain regions on the sidewall 910 of silicon body 908. Each of the gate g1, g2, and g3 has a <100> crystal plane structure due to the construction of the semiconductor body 908 as previously discussed. The mobility is thus improved with three <100> crystal plane gates making the transistor 900 a high mobility non-planar device. The gate "width" (Gw) of transistor 900 is the sum of the widths of the three channel regions. Thus, the gate width of the transistor 900 is equal to the height 920 of the silicon body 908 at the sidewall 910, plus the width of the silicon body of 908 at the top surface 916, plus the height 920 of the silicon body 908 at the sidewall 912. Larger "width" transistors can be obtained by using multiple devices coupled together (e.g., multiple silicon bodies 908 surrounded by a single gate electrode 924).

[0042] Because the channel region 950 is surrounded on three sides by the gate electrode 924 and the gate dielectric 922, the transistor 900 can be operated in a fully depleted manner. When the transistor 900 is turned "on," the channel region 950 fully depletes thereby providing the advantageous electrical characteristics and performance of a fully depleted transistor. Additionally, when the transistor 900 is turned "ON" a depletion region is formed and a channel region 950 along with an

inversion layer at the surfaces of the channel region 950 (e.g., an inversion layer is formed on the side surfaces and the top surface of the semiconductor body 908). The inversion layer has the same conductivity type as the source and drain regions and forms a conductive channels between the source and drain regions to allow current to flow there between. The tri-gate transistor 900 is a nonplanar transistor because the channel regions are formed in both the horizontal and vertical directions in the semiconductor body 908. The depletion region depletes free carriers from beneath the inversion layers. The depletion region extends to the bottom of the channel region 950, thus the transistor can be said to be a "fully depleted" transistor. Fully depleted transistors have improved electrical performance characteristics over non-fully depleted or partially depleted transistors. For example, by operating the transistor 900 in the fully depleted manner, the transistor 900 has an ideal or very steep subthreshold slope. The tri-gate transistor can be fabricated with very steep sub-threshold slope of less than 80 mV/decade, and ideally about 60 mV/decade even when fabricated with semiconductor body thicknesses of less than 30 nm. Additionally, with the transistor 900 being fully depleted, the transistor 900 has an improved drain induced barrier (DIBL) low in effect which provides for better "OFF" state leakage which results in lower leakage and thereby lower power consumption. In an embodiment of the present invention the tri-gate transistor 900 has a DIBL effect of less than 100mV/V and ideally less than 40 mV/V.

[0043] Because the transistor 900 has gates with high mobility characteristic due to the <100> crystal plane, the electrical characteristic of the transistor 900 is even better than devices with only the top surface having the <100> crystal planes.

[0044] Figure 10 illustrates an exemplary method of fabricating a substrate for a non-planar device such as the tri-gate transistor 900 in accordance with embodiments of the present invention. In one embodiment, a substrate 1002 is the first provided. The substrate 1002 can be a semiconductor substrate such as but not limited to a bulk silicon substrate, a monocrystalline silicon substrate, a lower monocrystalline

silicon substrate, a polysilicon substrate, or a gallium arsernide substrate or other suitable semiconductor material. In one embodiment, the substrate 1002 includes an insulating layer 1004 such as a silicon dioxide film, a silicon nitride film, or other suitable dielectric films. The insulating layer 1004 may have a thickness between about 200-2000 angstroms.

[0045] A semiconductor device substrate 1006 is bonded to the substrate 1002. In the embodiment where the substrate 1002 includes the insulating layer 1004, the device substrate 1006 is bonded to the substrate 1002 at the insulating layer 1004. The semiconductor device substrate 1006 is the substrate with which a semiconductor body or bodies of the tri-gate transistor are fabricated. In one embodiment, the semiconductor device substrate 1006 is of a high quality silicon. In other embodiments, the semiconductor device substrate 1006 can be other types of semiconductor films such as but not limited to germanium (Ge), silicon germanium alloy (SiGe), gallium arsenide (GaAs), indium antimony (InSb), gallium phosphide (GaP), gallium antimony (GaSb), as well as carbon nanotubes.

[0046] In an embodiment of the present invention, the semiconductor device substrate 1006 is an intrinsic (undoped) silicon film. In other embodiments, the semiconductor device substrate 1006 is doped to a p type or n type conductivity with a concentration level between $1x10^{16}$-$1x10^{19}$ atoms/cm^3. The semiconductor device substrate 1006 can be insitu doped (e.g., doped while it is deposited) or doped after it is formed on the substrate 1002 by for example ion-implantation. Doping after formation enables both PMOS and NMOS tri-gate devices to be fabricated can be easily done on the same insulating substrate. The doping level of the semiconductor body at this point determines the doping level of the channel region of the non-planar device. In one embodiment, the semiconductor device substrate 1006 includes an insulating layer 1008 which can be a silicon dioxide film or a silicon nitride film, or other suitable dielectric film. The insulating layer 1008 may have a thickness between about 200 angstrom to about 2000 angstroms.

[0047] The semiconductor device substrate 1006 has a thickness which is approximately equal to the height desired for the subsequently formed semiconductor body or bodies of the fabricated tri-gate transistor. In an embodiment of the present invention, the semiconductor device substrate 1006 has a thickness or height 1016 of less than 30 nanometers and ideally less than 20 nanometers. In an embodiment of the present invention, the semiconductor device substrate 1006 has a thickness 1016 approximately equal to the gate "length" desired of the fabricated tri-gate transistor. In an embodiment of the present invention, the semiconductor device substrate 1006 has a thickness 1016 that is thicker than the desired gate length of the tri-gate transistor to be formed. In an embodiment of the present invention, the semiconductor device substrate 1006 has a thickness 1016 that will enable the fabricated tri-gate transistor to be operated in a fully depleted manner for its designed gate length (Lg). After the device substrate 1006 is bonded to or formed on the substrate 1002, an SOI substrate is formed. The semiconductor body for a tri-gate device is formed in the device substrate 1006. The device substrate 1006 is bonded to the substrate 1002 such that the tri-gate device formed in the device substrate 1006 will have <100> crystal plane in all sides.

[0048] The semiconductor device substrate 1006 can be formed on (or bonded to) the insulating substrate 1002 using any well-known method. In one exemplary method, the substrate 1002 includes a notch 1010 located at a <110> crystal plane location. The substrate 1002 can be a wafer sliced from an ingot that has a reference notch created at the <110> location as previously described. In one embodiment, the device substrate 1006 includes a notch 1012, also located at a <110> crystal plane location. Similar to the substrate 1002, the device substrate 1006 can be a wafer sliced from an ingot that has a reference notch created at the <110> crystal plane location. The device substrate 1006 may be of a higher quality than the substrate 1006. In one embodiment, the substrate 1002 includes an insulating layer 1004 and the device substrate 1006 includes an insulating layer 1008. The device substrate 1006 and the substrate 1002 are bonded together at the insulating layers using methods such as

SMARTCUT or Bonded and Etch Back SOI (BESOI), or other bonding method. Before being bonded together, the device substrate 1006 is rotated so that the notch 1012 is offset by 45 degrees or -45 degrees with respect to the notch 1010. The crystal plane structure of the device substrate 1006 is thus altered.

[0049] In the SMARTCUT method, (Figure 11), the device substrate 1006 may be oxidized to create the insulating layer 1008. The substrate 1002 may also be oxidized to create the insulating layer 1004. Ion implantation is then used implant ions to a predetermined depth in the device substrate 106 to induce formation of an in-depth weakened layer in the device substrate 1006. The substrates 1002 and 1006 are then cleaned and bonded to each other at the insulating layers 1004 and 1008. Prior to bonding, the substrate 1002 and the device substrate 1006 are offset with each other by about 45-degrees (or -45 degrees). In one embodiment, the substrates 1002 and 1006 are aligned over each other so that the notch 1012 of the substrate 1006 and the notch 1010 of the substrate 1002 are offset by 45 degrees to each other. In more particular, the substrate 1006, when bonded to the substrate 1002 has the notch 1012 rotated 45 degrees or -45 degrees with respect to the notch 1010 of the substrate 1002 (see Figure 10). The offset of the notches 1012 to the notch 1010 will provide the tri-gate with a <100> crystal planes in all sides of the gate as previously discussed. Cleavage is then used to cleave a portion of the device substrate 1006 at the depth of the ion implantation. The remaining portion of the device substrate 1006 including the insulating layer 1008 is transferred (via bonding) to the substrate 1002. Annealing and polishing (e.g., chemical mechanical polishing (CMP)) may be used to complete the formation of an SOI substrate. The substrate 1002 and the device substrate 1006 having the oxides layers 1004 and 1008 sandwiched there between is referred to as the SOI substrate. The tri-gate device having <100> crystal plane structure on all sides will be formed on the device substrate 1006 surface.

[0050] In the BESOI method, (Figure 12), the device substrate 1006 may be oxidized to create the insulating layer 1008. The substrate 1002 may also be oxidized to

create the insulating layer 1004. The substrates 1002 and 1006 are cleaned and bonded to each other at the insulating layers 1004 and 1008. Prior to bonding, the substrate 1002 and the device substrate 1006 are offset with each other by about 45 degrees (or -45 degrees). In one embodiment, the substrates 1002 and 1006 are aligned over each other so that the notch 1012 of the substrate 1006 and the notch 1010 of the substrate 1002 are offset by 45 degrees to each other. In more particular, the substrate 1006, when bonded to the substrate 1002 has the notch 1012 rotated 45 degrees or –45 degrees with respect to the notch 1010 of the substrate 1002 (see Figure 10). The offset of the notches 1012 to the notch 1010 will provide the tri-gate with a <100> crystal planes in all sides of the gate as previously discussed. After the bonding, the substrate 1006 is etched and polished (Figure 11) to obtain the desired thickness. Annealing and polishing (e.g., CMP) may be used to complete the formation of the SOI substrate. The tri-gate device having <100> crystal plane structure on all sides will be formed on the device substrate 1006 surface.

[0051] In one embodiment, a Separation by Implantation of Oxygen (SIMOX) method is used to form the SOI substrate. In this embodiment, (Figure 13) a substrate 1300 is provided and deep implantation of oxygen ions (typically high dose) is performed into the substrate 1300 to form the SOI substrate. The substrate 1300 is annealed to complete the formation of the SOI substrate. A buried oxide layer 1302 will be formed within the substrate 1300. In one embodiment, the substrate 1300 is a single crystalline silicon substrate. The tri-gate device will be formed above the silicon portion that is above the buried oxide layer 1302. Thus, the silicon portion that is above the oxide layer 1302 is essentially the device substrate 1006. In one embodiment, the substrate 1300 is formed from an ingot having a reference line created at the <110> crystal plane location such that when spliced from the ingot, the substrate 1300 has a reference notch created at a <110> crystal plane location. When placed on a processing tool, the notch is offset by 45 degrees or –45 degrees with respect to an alignment point on the processing tool. Thus, instead of processing the substrate 1300 where the notch

is aligned as conventionally would (e.g., aligned to a designated location on the processing tool designated for the notch), the substrate 1300 is rotated so that the notch is offset during processing. Offsetting the notch will provide the tri-gate with a <100> crystal planes in all sides of the gate as previously discussed. In alternative embodiments, the substrate 1300 can be-created from an ingot 1400 (Figure 14A) wherein a reference line is located at a <100> crystal plane location. When the ingot 1400 is spliced into wafers to create the substrate 1300, a notch 1404 will be created at a <100> crystal plane location. The substrate 1300 with the <100> notch can be processed using the SIMOX method previously discussed. A tri-gate device can be formed in the substrate 1300 without the need to rotate the substrate 1300 by 45 degrees or -45 degrees to create the tri-gate with all sides having the <100> crystal plane structure.

[0052] In other embodiments, instead of rotating the device substrate 1006 relative to the substrate 1002 as illustrated in Figures 11-12 or realigning the device substrate 1300 as discussed in Figure 13, the device substrate for the non-planar device can be made so that the notch is relocated. The notch for the wafer used to form the device substrate thus is relocated to a <100> crystal plane location. When the device substrate has to be rotated, the mechanical rotation will dictate the reliability, accuracy, and/or repeatability of the rotation of the device substrate. For example, when the substrate 1006 and the substrate 1002 are offset to each other by 45 degrees or –45 degrees with respect to offsetting the notch on each wafer, the accuracy of the offset may be affected by the accuracy of the wafer bonding process or equipment. Thus, the mechanical rotation of the substrate 1006 with respect to the substrate 1002 may dictate the degrees of the offset (for example, by a few degrees). To minimize the potential for misalignment, the device substrate 1006 or the substrate 1300 can be created with the notch at the <100> crystal plane location (as opposed to the <100> location). As illustrated in Figure 14A, an ingot 1400 that is used to later form the device substrate 1006 or the substrate 1300 can be formed with a reference line 1402 created at a <100>

crystal plane location using X-Ray Diffraction, which has a much more accurate mechanical rotation than that of the wafer bonding process. When the ingot 1400 is spliced to generate a plurality of wafers 1406, which can be used to form substrates 1006 or 1300, each wafer 1406 will have a notch 1404 located at a <100> crystal plane location.

[0053] In Figure 14B, the wafer 1406 is bonded to another wafer, the substrate 1002, in one embodiment, to create the SOI substrate. The wafer 1404 may include insulating layer 1408 and the substrate 1002 may include the insulating layer 1004 as previously discussed. As before, the substrate 1002 includes a notch 1010 created at the <110> crystal plane location as previously discussed. The wafer 1406, however, has the notch 1404 located at the <100> crystal plane location. The notches 1404 and 1010 are aligned over each other during processing as shown in Figure 14B. There is no need to rotate the wafer 1406 to realign the crystal structure of the wafer 1406 during processing. The wafer 1406 will have the 45 degrees or –45 degrees offset due to the relocation of the notch 1404 to the <100> crystal plane location to realign the crystal plane structure in the wafer 1404. The relocation of the notch 1404 to the <100> crystal plane allow the non-planar device formed in the wafer 1406 to have all sides having the <100> crystal plane desirable for high mobility.

[0054] Figures 15A-15J illustrate an exemplary method of making a non-planar device or devices 1500 (e.g., tri-gate transistors) in accordance with embodiments of the present invention. In Figure 15A, a substrate 1502 is provided. The substrate 1502 includes a semiconductor substrate 1504 (e.g., bulk silicon) and an insulating film 1506 (e.g., silicon dioxide). Upon the insulating film 1506, a device semiconductor substrate 1508 (e.g., monocrystalline silicon) is formed. Together, the substrate 1502 and the device substrate 1508 are referred to as the SOI substrate previously described. The device substrate 1508, in one embodiment, has a notch (not shown) created at a <100> crystal plane location and the substrate 1502 has a notch (not shown) created at a <110> crystal plane location. The notches are aligned over each other as previously

discussed. In an alternative embodiment, the device substrate 1508 and the substrate 1502 both have a notch created at the <110> crystal plane location. When bonded together to form the SOI substrate, the device substrate 1508 is rotated by 45 degree (or -45 degrees) so that the notches are offset to each other as previously discussed. Isolation regions (not shown) can be formed into the device substrate 1508 in order to isolate the various transistors to be formed therein from one another. Isolation regions can be formed by etching away portions of the device substrate 1508 surrounding a tri-gate transistor, by for example well-known photolithographic and etching techniques, and then back filling the etched regions with an insulating film, such as SiO_2.

[0055] Next, a photoresist mask 1510 is formed on the device substrate 1508 as shown in Figure 5B. The photoresist mask 1510 contains a pattern or plurality of patterns 1512 defining locations where semiconductor bodies or fins 1520 for the devices 1500 will be subsequently formed. The photoresist pattern 1512 defines the width 1518 desired of the subsequently formed semiconductor bodies 1520. In an embodiment of the present invention, the pattern 1512 define bodies 1520 having a width 1518 which is equal to or greater than the width desired of the gate length (Lg) of the fabricated transistor. In this way, the most stringent photolithography constraints used to fabricate the transistor are associated with the gate electrode patterning and not the semiconductor body or fin definition. In an embodiment of the present invention, the bodies 1520 will have a width 1518 less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers. In an embodiment of the present invention, the patterns 1512 for the bodies 1520 have a width 1518 approximately equal to the silicon body height 1509. In an embodiment of the present invention, the photoresist patterns 1512 have a width 1518 which is between ½ the semiconductor body height 1509 and two times the semiconductor body height 1509.

[0056] The photoresist mask 1510 can also include patterns 1514 and 1516 for defining locations where source landing pads 1522 and drain landing pads 1524 are to be formed. The landing pads can be used to connect together the various source

regions and to connect together the various drain regions of the fabricated transistor. The photoresist mask 1510 can be formed by well-known photolithographic techniques including masking, exposing, and developing a blanket deposited photoresist film.

[0057] Next, the device substrate 1508 is etched in alignment with photoresist mask 1510 to form one or more silicon bodies or fins and source and drain landing pads (if desired) as shown in Figure 5C. The substrate 1508 is etched until the underlying buried oxide layer 1506 is exposed. Well-known semiconductor etching techniques, such as anisotropic plasma etching or reactive ion etching can be used to etch the substrate 1508.

[0058] Next, the photoresist mask 1510 is removed by well-known techniques, such as by chemical stripping and O_2 ashing, to produce the substrate shown in Figure 5D.

[0059] Next, a gate dielectric layer 1526 is formed on and around each semiconductor body 1520. A gate dielectric layer 1526 is formed on the top surface 1527 as well as on the laterally opposite sidewalls 1528 and 1529 of each of the semiconductor bodies 1520. The gate dielectric can be a deposited dielectric or a grown dielectric. In an embodiment of the present invention, the gate dielectric layer 1526 is a silicon dioxide dielectric film grown with a dry/wet oxidation process. In an embodiment of the present invention, the silicon oxide film is grown to a thickness of between 5-15Å. In an embodiment of the present invention, the gate dielectric film 1526 is a deposited dielectric, such as but not limited to a high dielectric constant film, such as metal oxide dielectric, such as tantalum pentaoxide (Ta_2O_5) and titanium oxide (TiO_2) or other high-K dielectrics, such as PZT. A high dielectric constant film can be formed by any well-known technique, such as by chemical vapor deposition (CVD).

[0060] Next, as shown in Figure 5E, a gate electrode 1530 is formed. The gate electrode 1530 is formed on the gate dielectric layer 1526 formed on the top surface 1527 and on or adjacent to the sidewalls 1528 and 1529 of each of the semiconductor bodies 1520. The gate electrode 1530 has a top surface 1532 opposite of bottom surface

formed on the insulating substrate 1502 and has a pair of laterally opposite sidewalls 1534 and 1536. The distance between the laterally opposite sidewalls 1534 and 1536 define the gate length (Lg) 1538 of the tri-gate transistor. The gate electrode 1530 can be formed by blanket depositing a suitable gate electrode material over the substrate shown in Figure 5D. The gate electrode can be formed to a thickness 1533 (Figure 5F) between 200-9000Å. In an embodiment, the gate electrode has a thickness or height 1533 of at least three times the height 1509 of semiconductor bodies 1520. The gate electrode material is then patterned with well-known photolithography and etching techniques to form the gate electrode 1530 from the gate electrode material. The gate electrode material may comprise polycrystalline silicon, polycrystalline silicon germanium alloy, and metal, such as tungsten, tantalum, and their nitrides. In an embodiment of the present invention, the gate electrode 1530 has the gate length 1538 of less than or equal to 30 nanometers and ideally less than or equal to 20 nanometers.

[0061] Next, source 1540 and drain 1542 regions for the transistor are formed in semiconductor body 1520 on opposite sides of the gate electrode 1530. In an embodiment of the present invention, the source 1540 and drain 1542 regions include tip or source/drain extension regions. The source and drain regions and extensions can be formed by placing dopants 1544 into semiconductor bodies 1520 on both sides 1534 and 1536 of gate electrode 1530. If source and drain landing pads are utilized, they may be doped at this time also. For a PMOS tri-gate transistor, the semiconductor fins or bodies 1520 are doped to a p type conductivity and to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. For a NMOS tri-gate transistor, the semiconductor fins or bodies 1520 is doped with n type conductivity ions to a concentration between $1x10^{20}$-$1x10^{21}$ atoms/cm^3. In an embodiment of the present invention, the silicon films are doped by ion-implantation. In an embodiment of the present invention, the ion-implantation occurs in a vertical direction as shown in Figure 5F. When the gate electrode 1530 is a polysilicon gate electrode, it can be doped during the ion-implantation process. The gate electrode 1530 acts as a mask to prevent the ion-implantation step from doping the

channel region(s) 1548 of the tri-gate transistor. The channel region 1548 is the portion of the silicon body 1520 located beneath or surrounded by the gate electrode 1530. If the gate electrode 1530 is a metal electrode, a dielectric hard mask maybe used to block the doping during the ion-implantation process. In other embodiments, other methods, such as solid source diffusion, may be used to dope the semiconductor body to form source and drain extensions.

[0062] Next, if desired, the substrate shown in Figure 5F can be further processed to form additional features, such as heavily doped source/drain contact regions, deposited silicon on the source and drain regions as well as the gate electrode, and the formation of silicide on the source/drain contact regions as well as on the gate electrode. For examples, dielectric sidewall spacers 1550 (Figure 5G) can be formed on the sidewalls of the gate electrode 1530; semiconductor films 1560 and 1562 (Figure 5H) can be formed on the exposed surfaces of the body 1520 for certain applications (e.g., for forming raised source and drain regions); additional doping can be performed (e.g., to form the raised source and drain regions) (Figure 5I); and a refractory metal silicide 1580 can be formed on the source and drain regions and/or on the gate electrode 1530 (Figure 5J). Techniques for forming these components are known in the art.

[0063] While the invention has been described in terms of several embodiments, those of ordinary skill in the art will recognize that the invention is not limited to the embodiments described. The method and apparatus of the invention, but can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of limiting.

[0064] Having disclosed exemplary embodiments, modifications and variations may be made to the disclosed embodiments while remaining within the spirit and scope of the invention as defined by the appended claims.

IN THE CLAIMS

We claim:

1. A high mobility semiconductor assembly comprising:
   a first substrate having a first reference orientation located at a <110> crystal plane location on the first substrate; and
   a second substrate formed on top of the first substrate, the second substrate having a second reference orientation located at a <100> crystal plane location on the second substrate,
   wherein the first reference orientation is aligned with the second reference orientation.

2. The high mobility semiconductor assembly of claim 1 further comprising: an insulating layer disposed between the first substrate and the second substrate.

3. The high mobility semiconductor assembly of claim 1 wherein each of the first reference orientation and the second reference orientation includes a notch formed into each of the first substrate and the second substrate, respectively.

4. The high mobility semiconductor assembly of claim 1 wherein the second substrate providing a surface for a non-planar device to be formed therein and wherein the non-planar device having a top surface and side surfaces all having a <100> crystal plane.

5. The high mobility semiconductor assembly of claim 1 wherein the first substrate further comprises a first insulating layer and the second substrate comprises a

second insulating layer, and wherein the first substrate and the second substrate are bonded to each other at the first and second insulating layer.

6. The high mobility semiconductor assembly of claim 1 wherein the second substrate has a top field having a <100> crystal plane and a plurality of sides fields each having a <100> crystal plane.

7. The high mobility semiconductor assembly of claim 1 wherein the first substrate is made of a material selected from a group consisting of bulk silicon, polycrystalline silicon, lower monocrystalline silicon, and gallium arsenide.

8. The high mobility semiconductor assembly of claim 1 wherein the second substrate is made of a material selected from a group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

9. The high mobility semiconductor assembly of claim 1 further comprising a non-planar device formed in the second substrate, wherein the non-planar device comprises,

a semiconductor body having a top surface and laterally opposite sidewalls formed on the first substrate and in the second substrate, wherein each of the top surface and the laterally opposite sidewalls of the semiconductor body has a <100> crystal plane;

a gate dielectric formed on the top surface and on the laterally opposite sidewalls of the semiconductor body; and

a gate electrode formed adjacent the gate dielectric formed on the top of surface and on the laterally opposite sidewalls of the semiconductor body,

10. The high mobility semiconductor device of claim 9 further comprising:

a pair of source/drain regions formed in the silicon body on opposite sides of the gate electrode.

11. A high mobility semiconductor substrate comprising:

a first substrate having a first reference orientation located at a <110> crystal plane location on the first substrate; and

a second substrate formed on top of the first substrate, the second substrate having a second reference orientation located at a <110> crystal plane location on the second substrate,

wherein the second substrate is formed over the first substrate with the second reference orientation being offset to the first reference orientation by about 45 degrees.

12. The high mobility semiconductor substrate of claim 11 further comprising: an insulating layer disposed between the first substrate and the second substrate.

13. The high mobility semiconductor substrate of claim 11 wherein each of the first reference orientation and the second reference orientation includes a notch formed into each of the first substrate and the second substrate, respectively.

14. The high mobility semiconductor substrate of claim 11 wherein the first substrate further comprises a first insulating layer and the second substrate comprises a second insulating layer, and wherein the first substrate and the second substrate are bonded to each other at the first and second insulating layer.

15. The high mobility semiconductor substrate of claim 11 wherein the second substrate has a top field having a <100> crystal plane and a plurality of sides fields each having a <100> crystal plane.

16. The high mobility semiconductor substrate of claim 11 wherein the first substrate is made of a material selected from a group consisting of bulk silicon, polycrystalline silicon, lower monocrystalline silicon, and gallium arsenide.

17. The high mobility semiconductor substrate of claim 11 wherein the second substrate is made of a material selected from a group consisting of silicon, germanium, silicon germanium, gallium arsenide, InSb, GaP, GaSb and carbon nanotubes.

18. The high mobility semiconductor assembly of claim 11 further comprising a non-planar device formed in the second substrate, wherein the non-planar device comprises,

a semiconductor body having a top surface and laterally opposite sidewalls formed on the first substrate and in the second substrate, wherein each of the top surface and the laterally opposite sidewalls of the semiconductor body has a <100> crystal plane;

a gate dielectric formed on the top surface and on the laterally opposite sidewalls of the semiconductor body; and

a gate electrode formed adjacent the gate dielectric formed on the top of surface and on the laterally opposite sidewalls of the semiconductor body.

19. The high mobility semiconductor device of claim 18 further comprising:

a pair of source/drain regions formed in the silicon body on opposite sides of the gate electrode.

20. A method of fabricating a high mobility semiconductor assembly comprising:

providing a first substrate having a first reference orientation located at a <110> crystal plane location on the first substrate; and

forming a second substrate on top of the first substrate, the second substrate having a second reference orientation located at a <100> crystal plane location on the second substrate,

wherein the forming includes aligning the first reference orientation with the second reference orientation.

21. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein each of the second substrate and the first substrate includes an insulating layer and wherein the second substrate and the first substrate are bonded to each other at the insulating layer.

22. The method of fabricating a high mobility semiconductor assembly of claim 20 further comprising:

forming a non-planar device in the second substrate, wherein the non-planar device having a top surface and side surfaces all having a <100> crystal plane.

23. The method of fabricating a high mobility semiconductor assembly of claim 20 further comprising:

forming a tri-gate transistor in the second substrate, wherein the tri-gate transistor comprises,

a semiconductor body having a top surface and laterally opposite sidewalls, wherein each of the top surface and the laterally opposite sidewalls of the semiconductor body has a <100> crystal plane;

a gate dielectric formed on the top surface and on the laterally opposite sidewalls of the semiconductor body; and

a gate electrode formed adjacent the gate dielectric formed on the top of surface and on the laterally opposite sidewalls of the semiconductor body.

24. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein the forming the second substrate on top of the first substrate further includes transferring the second substrate to the first substrate using any one of a SMARTCUT method and a Bonded and Etch Back method.

25. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate that is used to form the second substrate, the third substrate having a third reference orientation located at a <100> crystal plane location on the third substrate;

implanting ions into a predetermined depth in the third substrate;

bonding the third substrate to the first substrate with the third reference orientation substantially aligned with the first reference orientation; and

cleaving the third substrate to transfer a portion of the third substrate to the first substrate, wherein the transferred portion of the third substrate forms the second substrate.

26. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate having an insulation layer, the third substrate being used to form the second substrate, the third substrate having a third

reference orientation located at a <100> crystal plane location on the third substrate;

implanting ions into a predetermined depth in the third substrate;

bonding the third substrate to the first substrate with the third reference orientation substantially aligned with the first reference orientation, wherein the first substrate further includes an insulation layer and wherein the third substrate is bonded to the first substrate at the insulation layers; and

cleaving the third substrate to transfer a portion of the third substrate to the first substrate, wherein the transferred portion of the third substrate forms the second substrate.

27. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate that is used to form the second substrate, the third substrate having a third reference orientation located at a <100> crystal plane location on the third substrate;

bonding the third substrate to the first substrate with the third reference orientation substantially aligned with the first reference orientation; and

etching the third substrate to a predetermined depth leaving a portion of the third substrate on the first substrate, wherein the portion of the third substrate forms the second substrate.

28. The method of fabricating a high mobility semiconductor assembly of claim 20 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate having an insulation layer, the third substrate being used to form the second substrate, the third substrate having a third

reference orientation located at a <100> crystal plane location on the third substrate;

bonding the third substrate to the first substrate with the third reference orientation substantially aligned with the first reference orientation, wherein the first substrate further includes an insulation layer and wherein the third substrate is bonded to the first substrate at the insulation layers; and

etching the third substrate to a predetermined depth leaving a portion of the third substrate on the first substrate, wherein the portion of the third substrate forms the second substrate.

29. A method of fabricating a high mobility semiconductor assembly comprising:

providing a first substrate having a first reference orientation located at a <110> crystal plane location on the first substrate; and

forming a second substrate on top of the first substrate, the second substrate having a second reference orientation located at a <110> crystal plane location on the second substrate,

wherein the forming includes forming the second substrate over the first substrate with the second reference orientation being offset to the first reference orientation by about 45 degrees.

30. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein each of the second substrate and the first substrate includes an insulating layer and wherein the second substrate and the first substrate are bonded to each other at the insulating layer.

31. The method of fabricating a high mobility semiconductor assembly of claim 29 further comprising:

forming a non-planar device in the second substrate, wherein the non-planar device having a top surface and side surfaces all having a <100> crystal plane.

32. The method of fabricating a high mobility semiconductor assembly of claim 29 further comprising:

forming a tri-gate transistor in the second substrate, wherein the tri-gate transistor comprising

a semiconductor body having a top surface and laterally opposite sidewalls, wherein each of the top surface and the laterally opposite sidewalls of the semiconductor body has a <100> crystal plane;

a gate dielectric formed on the top surface and on the laterally opposite sidewalls of the semiconductor body; and

a gate electrode formed adjacent the gate dielectric formed on the top of surface and on the laterally opposite sidewalls of the semiconductor body.

33. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein the forming the second substrate on top of the first substrate further includes transferring the second substrate to the first substrate using any one of a SMARTCUT method and a Bonded and Etch Back method.

34. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate that is used to form the second substrate, the third substrate having a third reference orientation located at a <110> crystal plane location on the third substrate;

implanting ions into a predetermined depth in the third substrate;

bonding the third substrate to the first substrate with the third reference orientation substantially offset with respect to the first reference orientation by about 45 degrees; and

cleaving the third substrate to transfer a portion of the third substrate to the first substrate, wherein the transferred portion of the third substrate forms the second substrate.

35. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate having an insulation layer, the third substrate being used to form the second substrate, the third substrate having a third reference orientation located at a <110> crystal plane location on the third substrate;

implanting ions into a predetermined depth in the third substrate;

bonding the third substrate to the first substrate with the third reference orientation being substantially offset with respect to the first reference orientation by about 45 degrees, wherein the first substrate further includes an insulation layer and wherein the third substrate is bonded to the first substrate at the insulation layers; and

cleaving the third substrate to transfer a portion of the third substrate to the first substrate, wherein the transferred portion of the third substrate forms the second substrate.

36. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate that is used to form the second substrate, the third substrate having a third reference orientation located at a <110> crystal plane location on the third substrate;

bonding the third substrate to the first substrate with the third reference orientation being substantially offset with respect to the first reference orientation by about 45 degrees; and

etching the third substrate to a predetermined depth leaving a portion of the third substrate on the first substrate, wherein the portion of the third substrate forms the second substrate.

37. The method of fabricating a high mobility semiconductor assembly of claim 29 wherein the forming the second substrate on top of the first substrate further includes:

providing a third substrate having an insulation layer, the third substrate being used to form the second substrate, the third substrate having a third reference orientation located at a <110> crystal plane location on the third substrate;

bonding the third substrate to the first substrate with the third reference orientation being substantially offset with respect to the first reference orientation by about 45 degrees, wherein the first substrate further includes an insulation layer and wherein the third substrate is bonded to the first substrate at the insulation layers; and

etching the third substrate to a predetermined depth leaving a portion of the third substrate on the first substrate, wherein the portion of the third substrate forms the second substrate.

38. A method of fabricating a high mobility semiconductor assembly comprising:

providing a substrate having a reference orientation located at a <100> crystal plane location on the substrate;

forming a buried oxide region in the substrate; and

forming a non-planar device in a portion of the substrate that is above the buried oxide, wherein the non-planar device having a top surface and side surfaces all having a <100> crystal plane.

39. The method of fabricating a high mobility semiconductor assembly of claim 38 wherein forming the non-planar device further comprising:

forming a tri-gate transistor in the portion of the substrate that is above the buried oxide, wherein the tri-gate transistor comprises a semiconductor body having a top surface and laterally opposite sidewalls, wherein each of the top surface and the laterally opposite sidewalls of the semiconductor body has a <100> crystal plane, a gate dielectric formed on the top surface and on the laterally opposite sidewalls of the semiconductor body, and a gate electrode formed adjacent the gate dielectric formed on the top of surface and on the laterally opposite sidewalls of the semiconductor body.

40. The method of fabricating a high mobility semiconductor assembly of claim 39 further comprising:

forming source and drain regions on opposite sides of the gate electrode.

41. The method of fabricating a high mobility semiconductor assembly of claim 38 wherein forming the buried oxide region in the substrate is done using a SIMOX method.

42. The method of fabricating a high mobility semiconductor assembly of claim 38 wherein forming the buried oxide region in the substrate further includes implanting oxygen into the substrate and annealing the substrate.

43. The method of fabricating a high mobility semiconductor assembly of claim 38 wherein forming the buried oxide region in the substrate further includes implanting oxygen into the substrate and annealing the substrate and wherein the substrate has a reference orientation located at a <100> crystal plane location.

44. The method of fabricating a high mobility semiconductor assembly of claim 38 wherein forming the buried oxide region in the substrate further includes implanting oxygen into the substrate and annealing the substrate and wherein the substrate has a reference orientation located at a <110> crystal plane location and wherein the substrate is rotated by about 45 degrees.

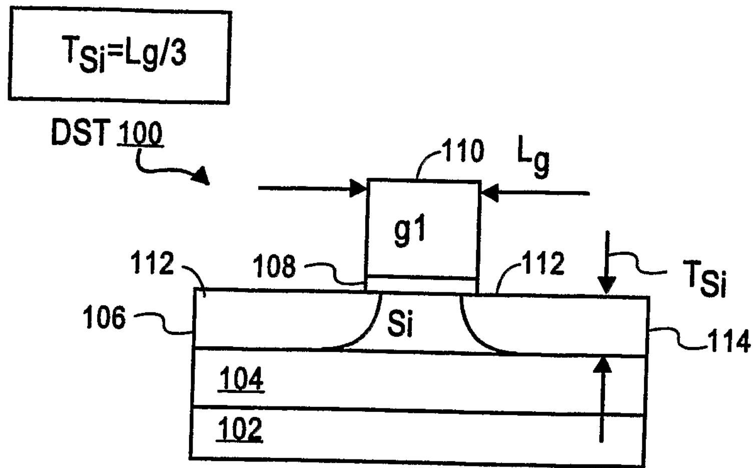


FIG. 1
(PRIOR ART)

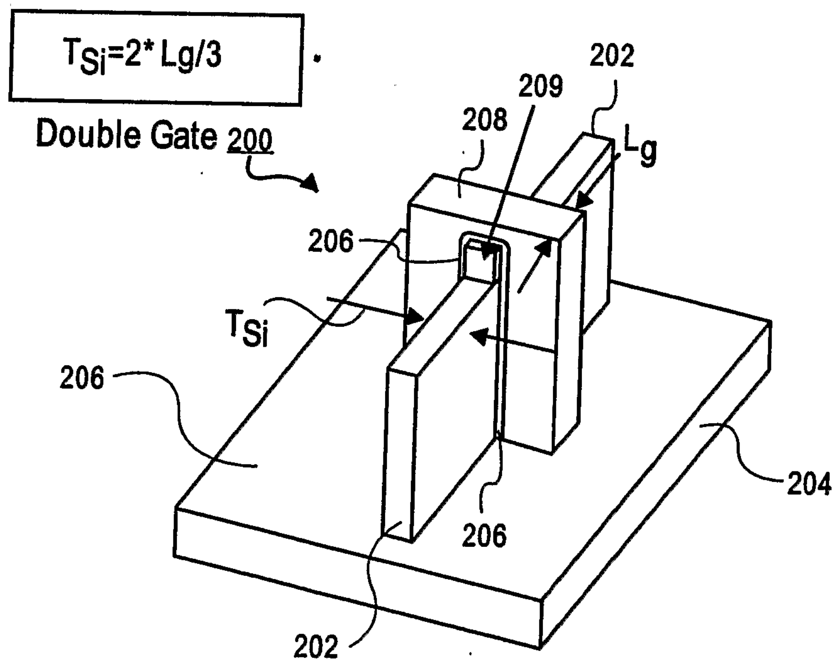


FIG. 2A
(PRIOR ART)

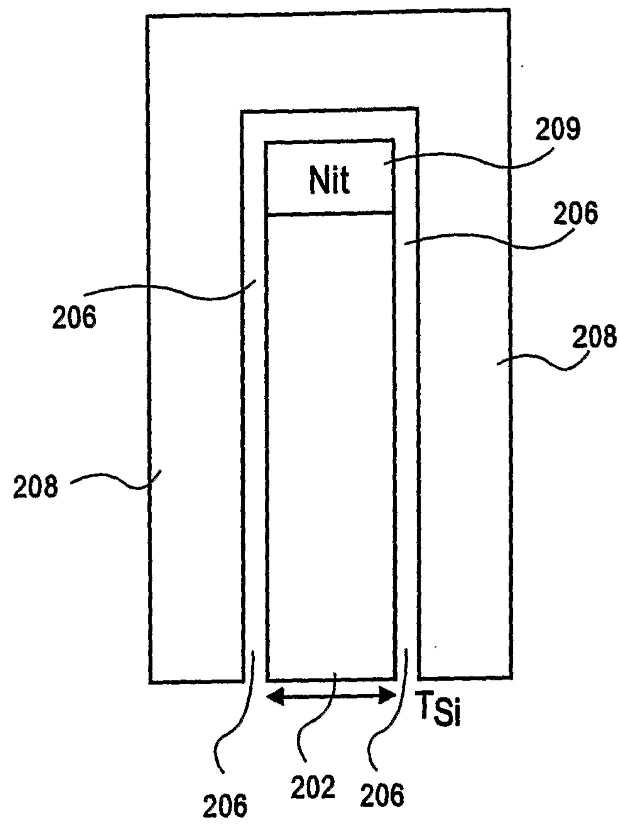


FIG. 2B

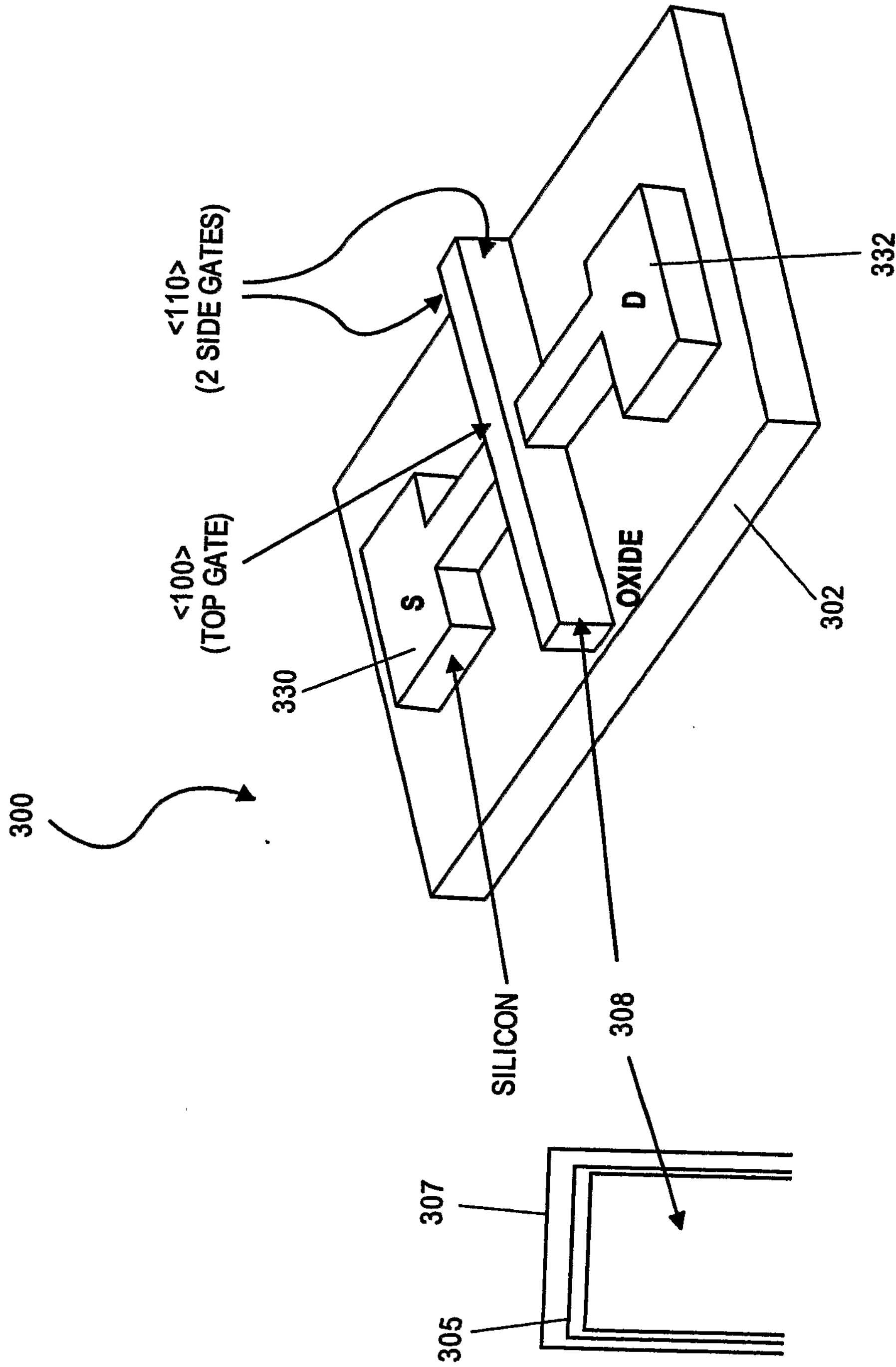
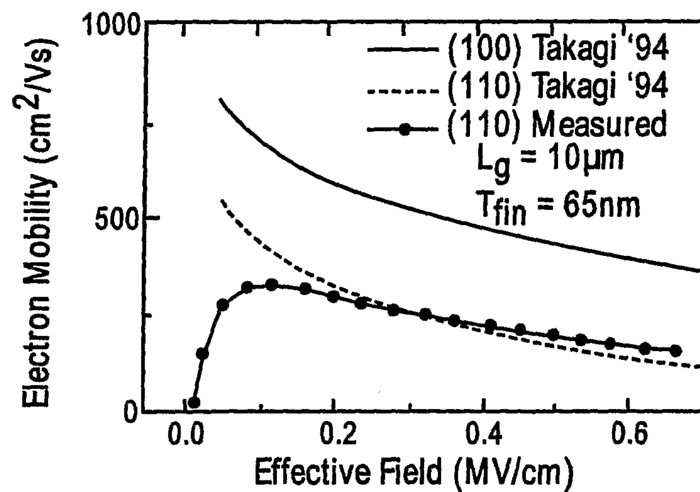


FIG. 3

FIG. 4

<110> : <100> COMPARISON



Mobility along <100> and <110>
directions. <110> is significantly lower than <100>

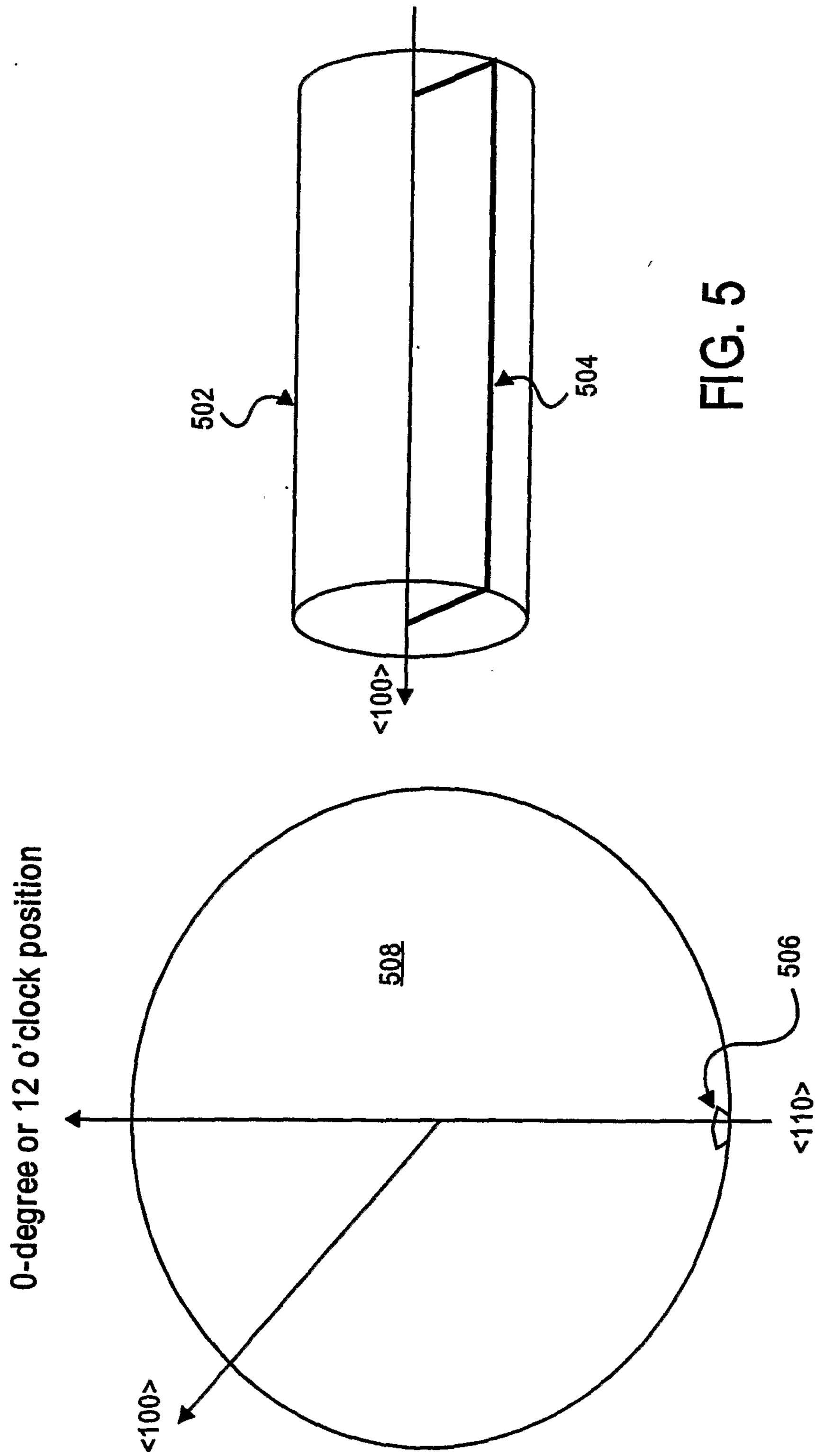


FIG. 5

FIG. 6

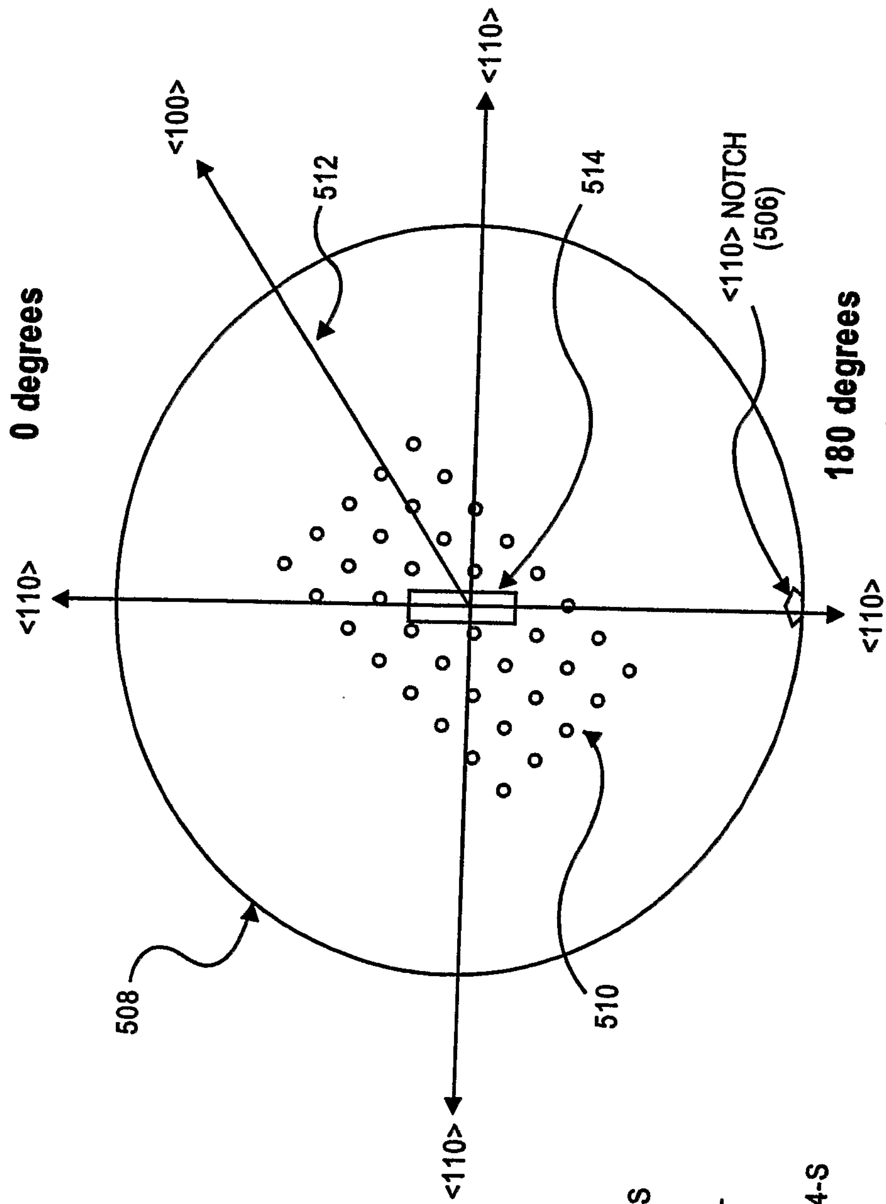


FIG. 7A

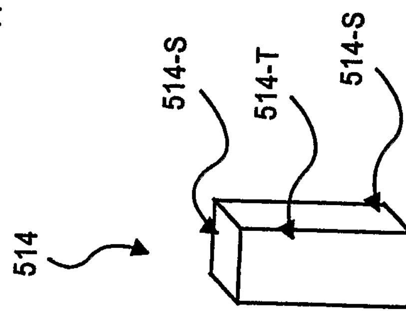


FIG. 7B

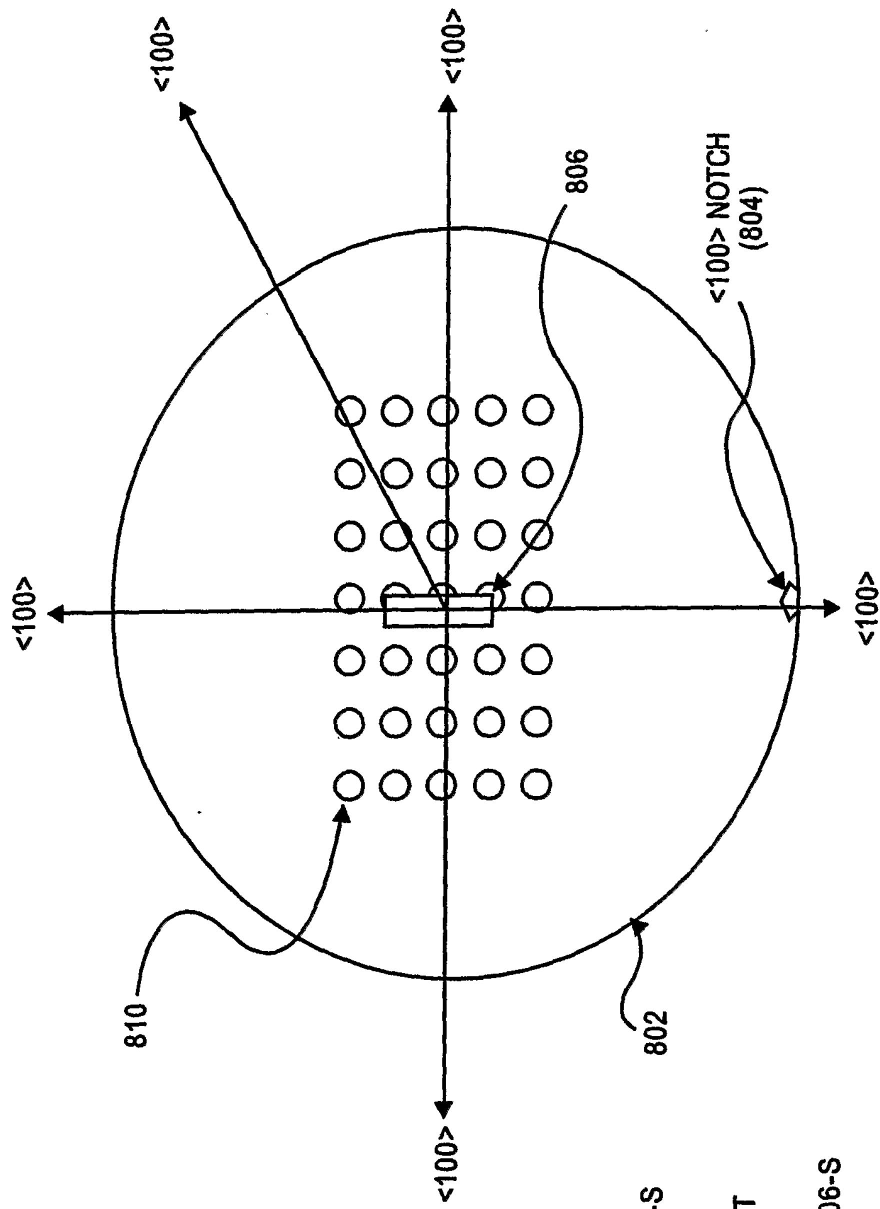


FIG. 8A

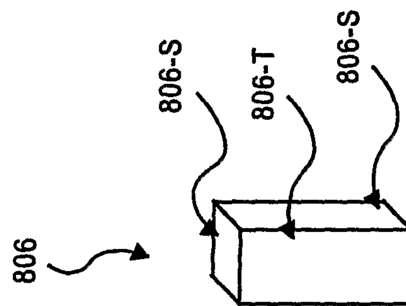


FIG. 8B

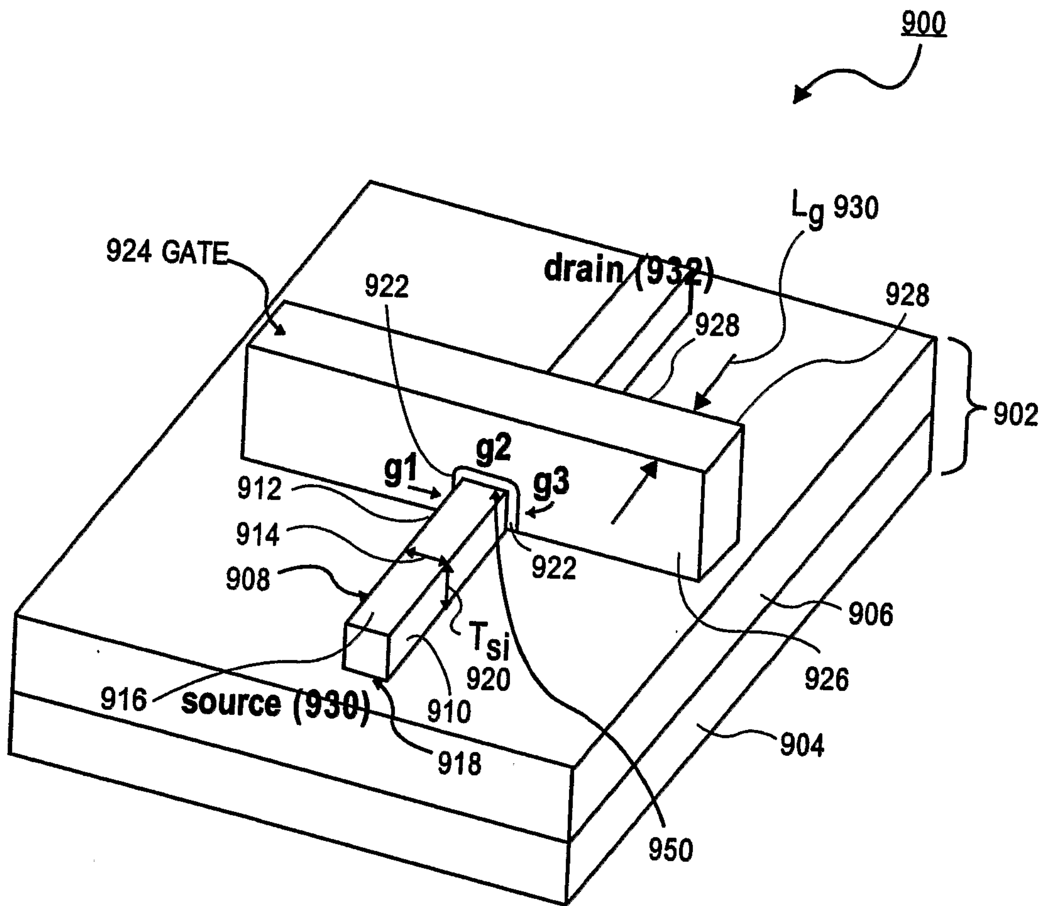


FIG. 9

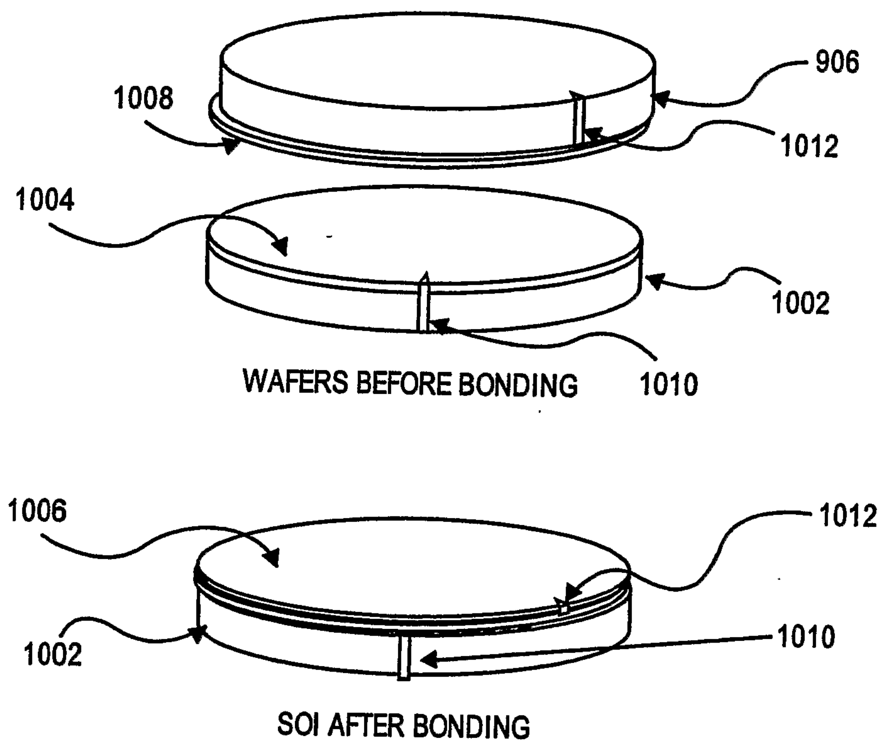


FIG. 10

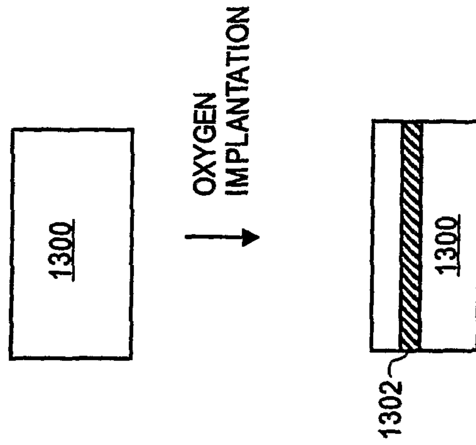


FIG. 13

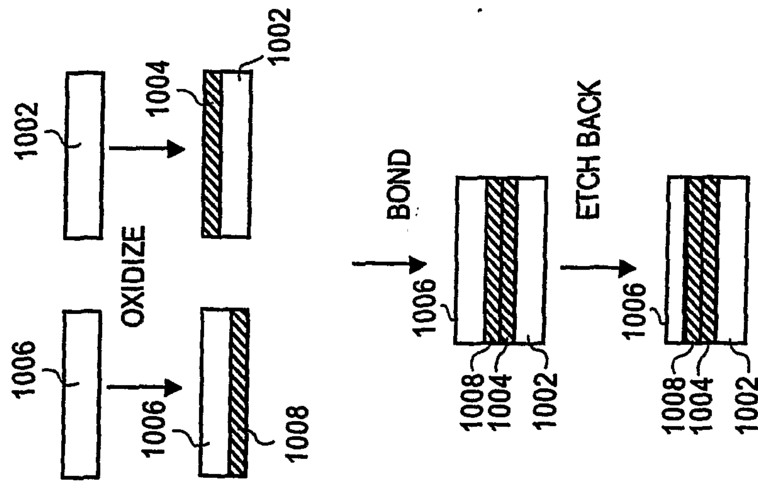


FIG. 12

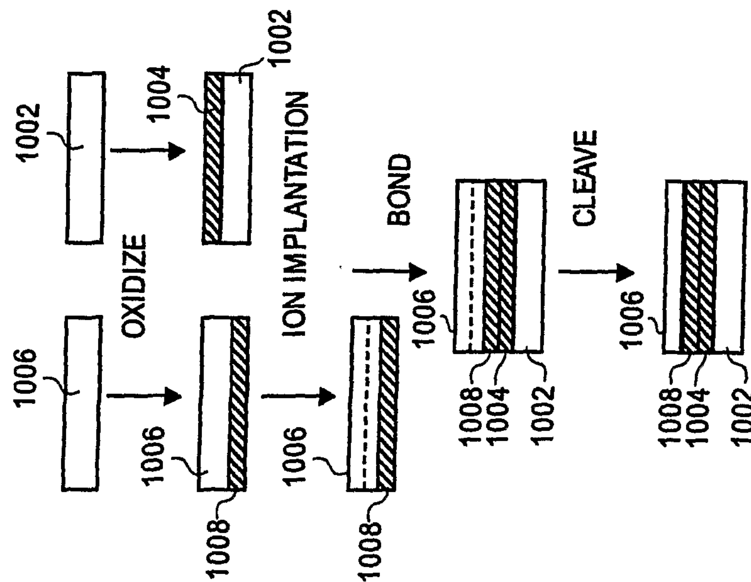


FIG. 11

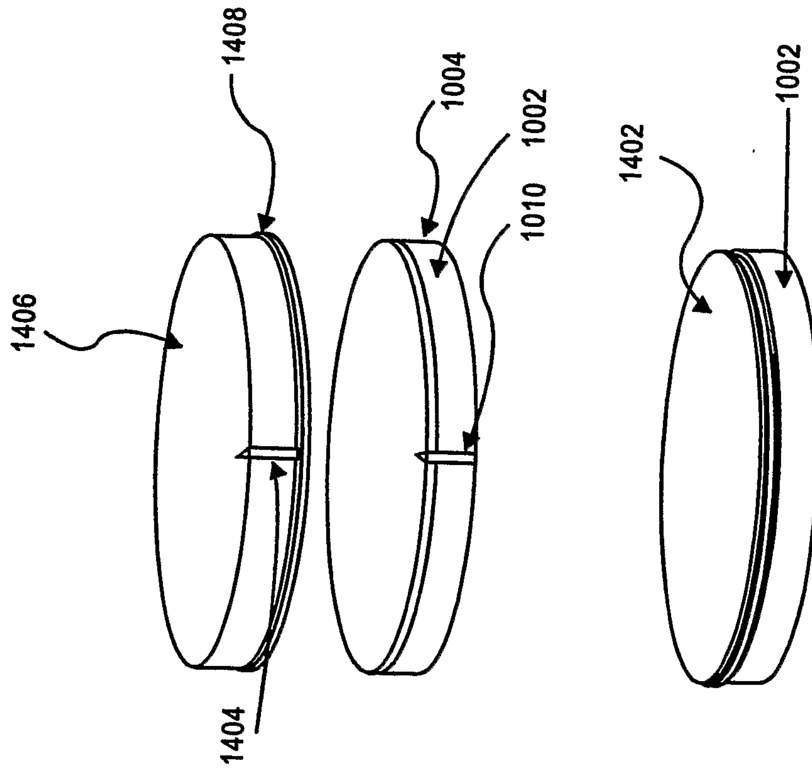


FIG. 14B

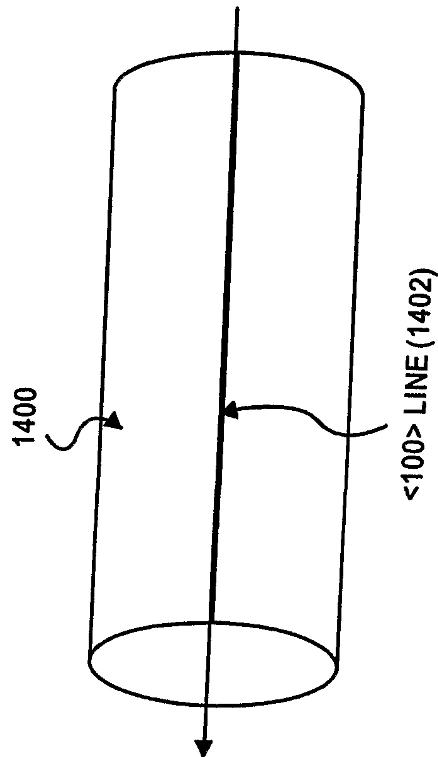


FIG. 14A

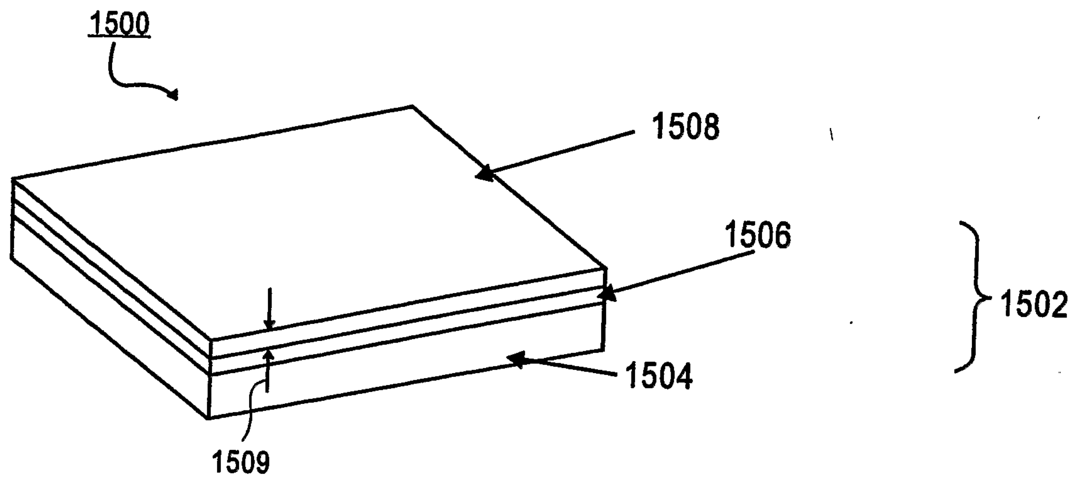


FIG. 15A

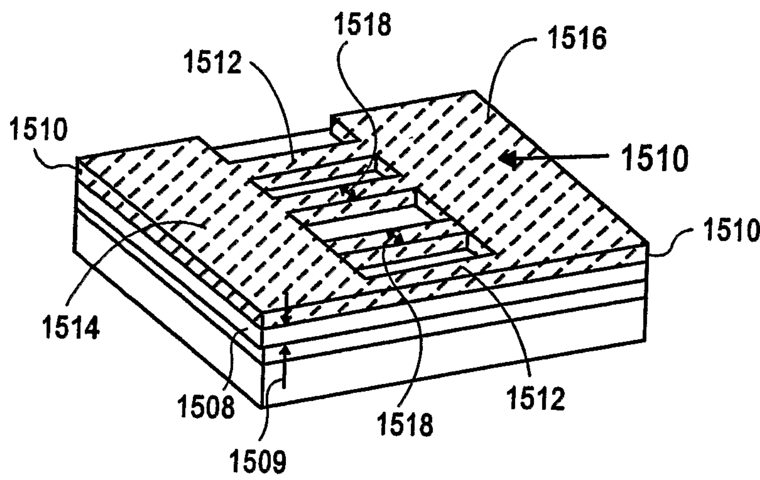


FIG. 15B

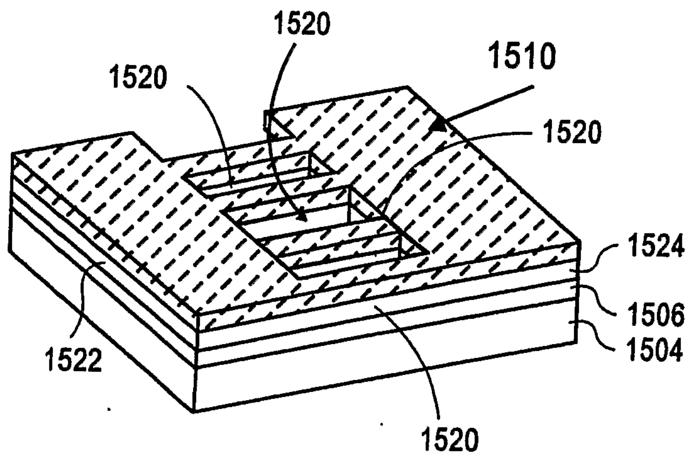


FIG. 15C

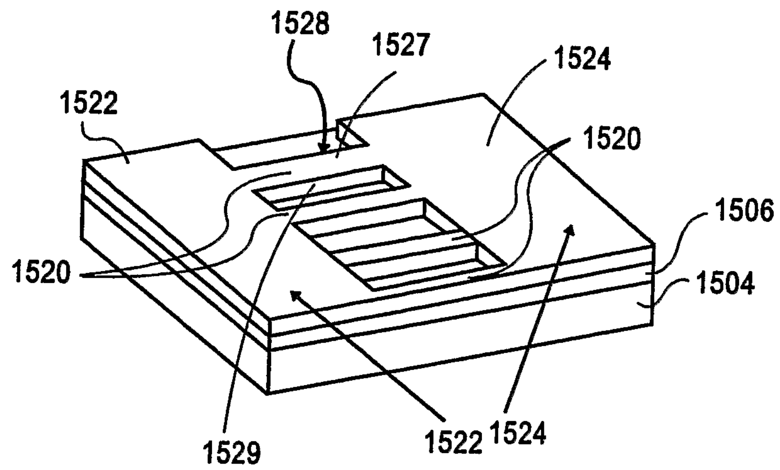


FIG. 15D

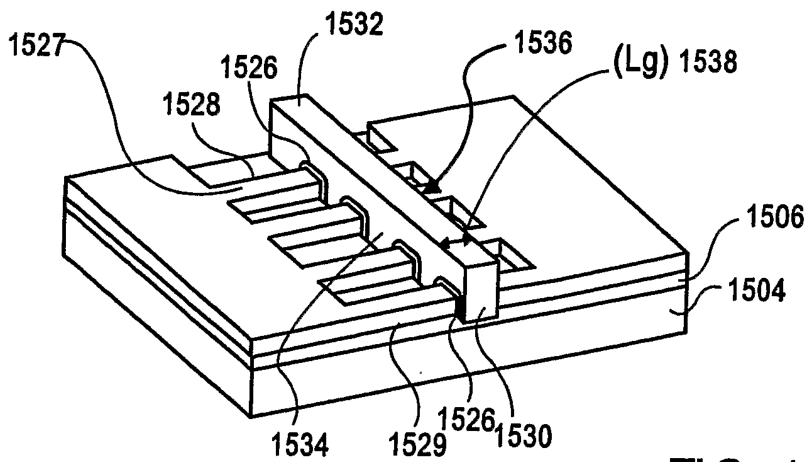


FIG. 15E

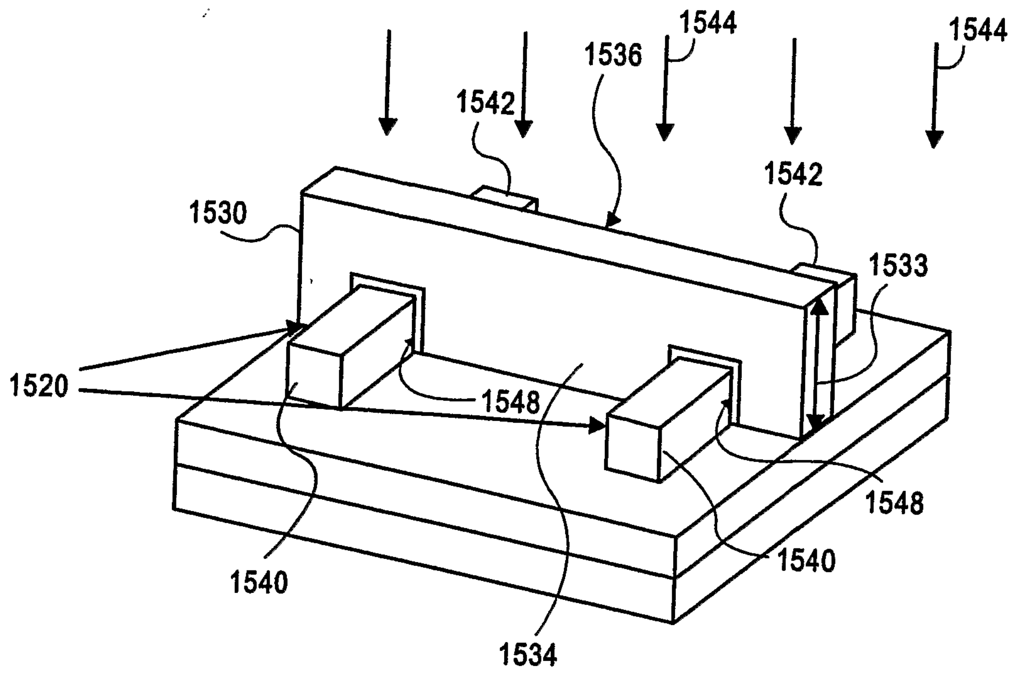


FIG. 15F

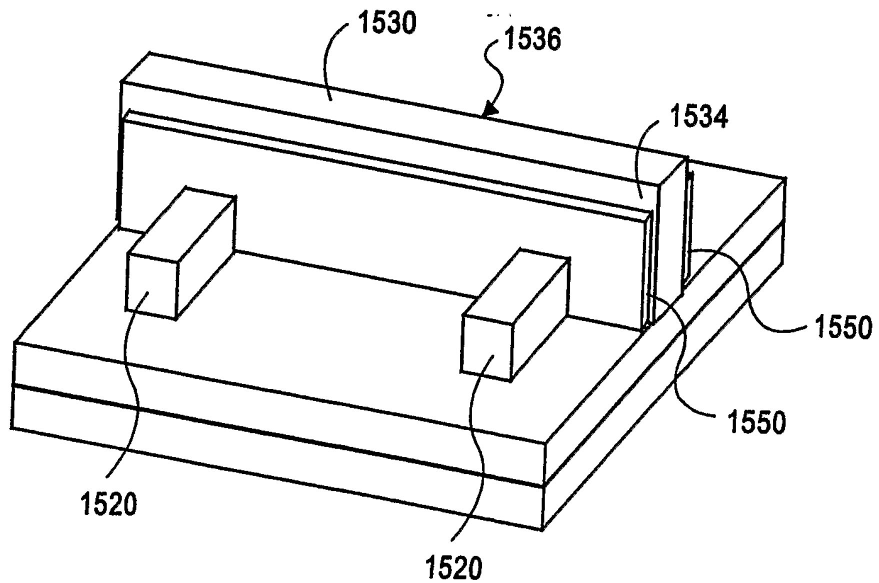


FIG. 15G

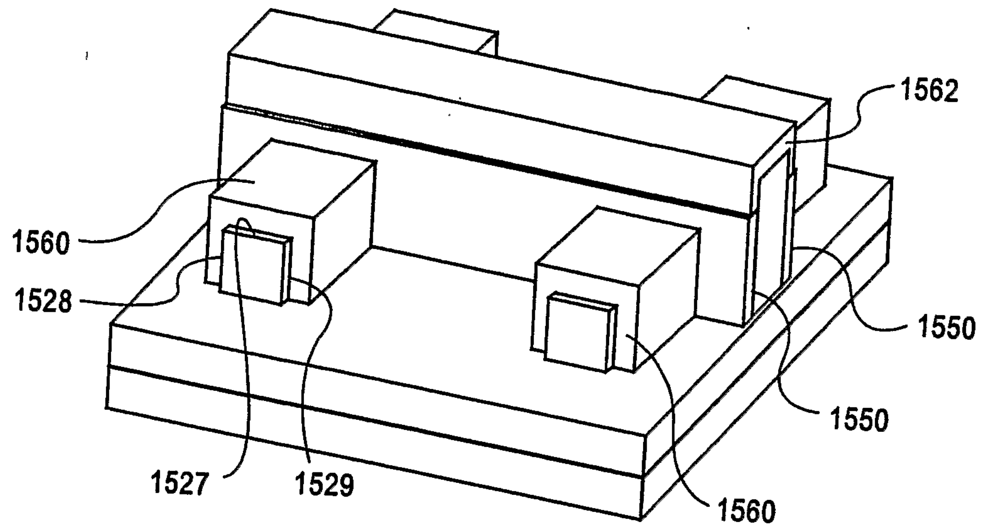
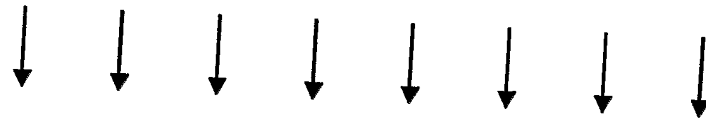


FIG. 15H



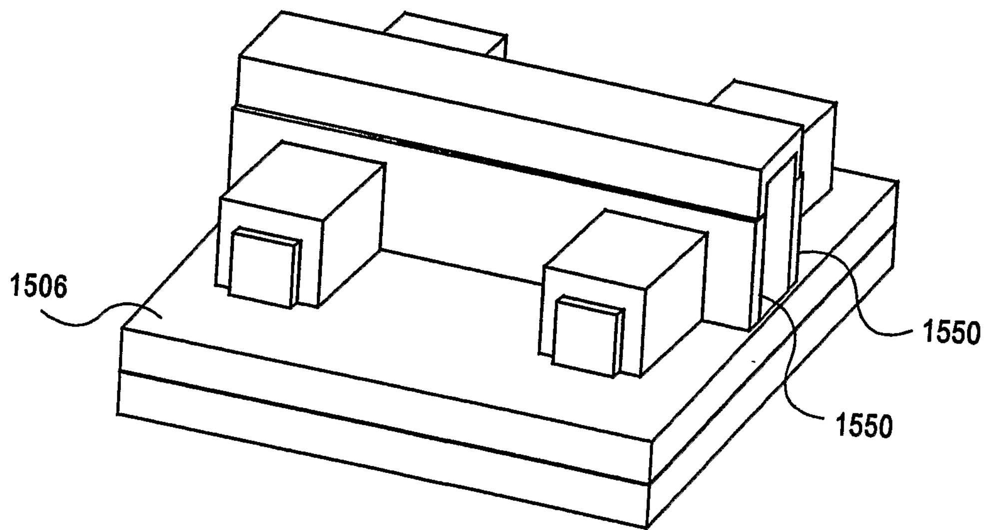


FIG. 15I

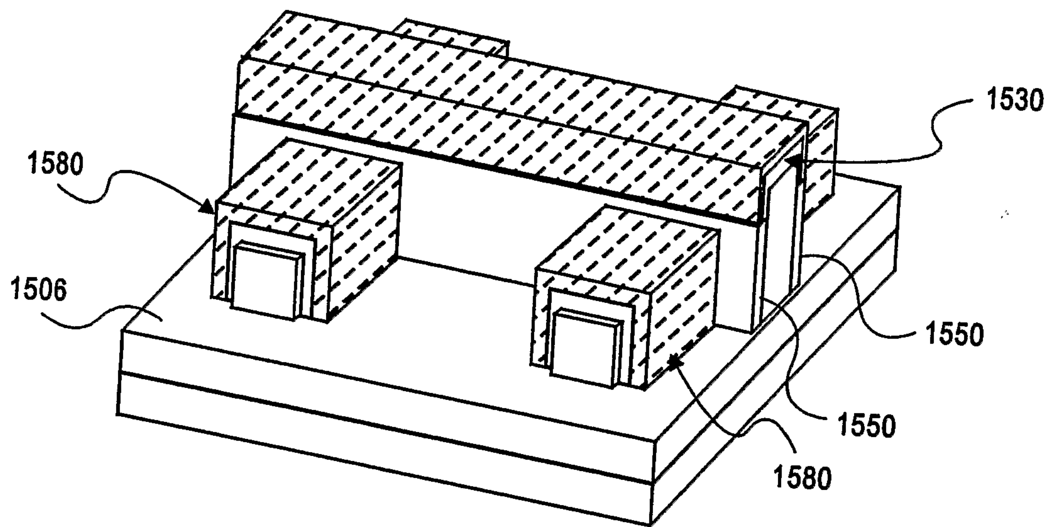


FIG. 15J

INTERNATIONAL SEARCH REPORT

Int nal Application No
PL ., _S2005/020339

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L29/786 H01L29/04 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/119100 A1 (NOWAK EDWARD J ET AL) 24 June 2004 (2004-06-24) paragraphs '0007!, '0028!; figure 2	1-44
X	US 2003/102497 A1 (FRIED DAVID M ET AL) 5 June 2003 (2003-06-05) paragraph '0009!	1-44
E	EP 1 566 844 A (SAMSUNG ELECTRONICS CO., LTD) 24 August 2005 (2005-08-24) figures 3-5	11-19, 29-44

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"P" document published prior to the international filing date but later than the priority date claimed

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 September 2005	04/10/2005

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Juhl, A

INTERNATIONAL SEARCH REPORT

International Application No
PC [illegible]2005/020339

Patent document cited in search report		Publication date	Patent family member(s)			Publication date
US 2004119100	A1	24-06-2004	AU	2003293380	A1	29-07-2004
			EP	1573823	A1	14-09-2005
			WO	2004061972	A1	22-07-2004
US 2003102497	A1	05-06-2003	US	2004038464	A1	26-02-2004
EP 1566844	A	24-08-2005	NONE			