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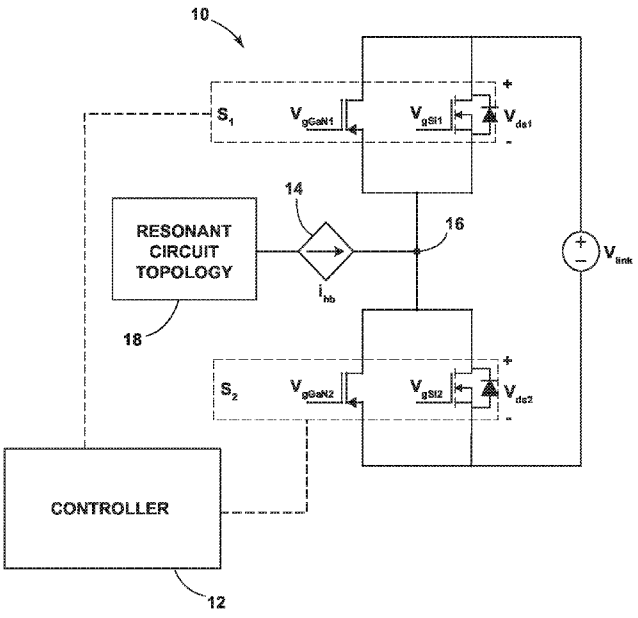

FIG. 2

(57) Abstract: A power converter is provided. The power converter includes two or more hybrid switching circuits electrically connected to a source or storage element. Each switching circuit includes a wide bandgap device that is parallel-connected to a silicon-based device. The converter further includes a controller that is operatively coupled to each device of the first and second switching circuits. The controller is configured to operate each hybrid switching circuit by (i) activating the silicon-based device for an activation period, (ii) activating the wide bandgap device for a predetermined duty cycle less than the activation period, (iii) deactivating the silicon-based device while the wide bandgap device is activated, and (iv) deactivating the wide bandgap device. The hybrid switching circuits are sequentially operated to convert an alternating current of a power supply into a link voltage for a power converter, for example.

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PERFORMANCE ENHANCEMENT OF SILICON-BASED DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application 62/716,011, filed August 8, 2018, the disclosure of which is incorporated by reference in its entirety.

FIELD OF THE INVENTION

[0002] The present invention relates to switch-mode power converters (SMPCs) including multiple semiconductor switches in a parallel arrangement and, in particular, power converters employing soft-switching techniques to provide zero voltage switching (ZVS) and minimal switching losses.

BACKGROUND OF THE INVENTION

[0003] In power electronics, a high-current power capability can be provided by electrically connecting multiple semiconductor switches in parallel to permit the undertaking of a load current together. For example, multiple dissimilar switching devices have been used in parallel arrangements because they provide a hybrid switching circuit having a much lower conduction resistance as compared to a single switch. Further by example, Si MOSFETs and GaN high electron mobility transistor (HEMTs) have been used in parallel arrangements to augment the Si MOSFET switching speed with a faster GaN HEMT switching speed.

[0004] For example, in ZVS applications both devices turn on with zero voltage stress and the GaN device carries the turn-off stress, allowing the hybrid switching circuit to benefit from the GaN device's faster fall time and lower E_{off} loss. Also by example, in hard switching applications

the GaN device is turned on first and turned off last. This requires more complex control but also allows the combination to benefit from the GaN's faster rise and fall times and lower E_{on} and E_{off} losses. However, during the conduction region of both ZVS and hard switching, the GaN device has to share current with the Si device, which limits the current capabilities of the hybrid switching circuit due to the GaN's poor thermal characteristics, which are in turn due to its small die size combined with the poor thermal conduction of silicon. Accordingly, there remains a continued need for an improved switching circuit, for example a power converter, which optimizes operation of Si devices using GaN devices and/or other wide bandgap (WBG) devices.

[0005] Figure 1 illustrates a prior art SMPC and is included as background for the present invention. Figure 1 generally shows the role of hybrid switching in an SMPC. The SMPC is generally designated 100 and is modeled by resonant circuit topology 180, controlled current source 140, switches S_1 and S_2, and arbitrary source or storage element V_{DClink}. The controlled current source 140 represents the behavior of an arbitrary soft-switched topology employing ZVS. S_1 is turned on when the voltage across it is 0V which allows the SMPC to reduce losses.

SUMMARY OF THE INVENTION

[0006] An SMPC and a related switching sequence are provided. In one embodiment, the SMPC includes a first hybrid switching circuit and a second hybrid switching circuit electrically connected to a power supply at a common node as a half-bridge. Each hybrid switching circuit includes a wide bandgap (WBG) device, for example a GaN HEMT, that is parallel-connected to a silicon-based device, for example a Si MOSFET. The converter further includes a controller that is operatively coupled to each device of the first and second switching circuits. The controller is configured to operate the first hybrid switching circuit and second hybrid switching circuit

sequentially and respectively by (i) activating the silicon-based device of one hybrid switching circuit for an activation period, (ii) activating the WBG device of the same hybrid switching circuit for a predetermined duty cycle less than the activation period, (iii) deactivating the silicon-based device while the WBG device is activated, and (iv) deactivating the WBG device.

[0007] In one method of operation as a half-bridge within a soft-switching SMPC, the controller activates the first silicon-based device for an activation period, activates the first WBG device for a predetermined duty cycle less than the activation period, and deactivates the first silicon-based device while the first WBG device is activated. After the first WBG is deactivated, the controller then activates the second silicon-based device for the activation period, activates the second WBG device for a predetermined duty cycle less than the activation period, and deactivates the second silicon-based device while the second WBG device is activated.

[0008] In another method of operation as a dual-active bridge (DAB) SMPC, eight hybrid switching circuits contain a WBG device and a silicon-based device connected in parallel. Four hybrid switching circuits are connected in a full-bridge topology on both sides of a transformer. When the voltage across a given hybrid switching circuit is zero, a controller activates the corresponding silicon-based device for an activation period and then activates the corresponding WBG device for a predetermined duty cycle less than the activation period. While the WBG device is still active, the silicon-based device is deactivated. After the silicon-based device is deactivated, the WBG is deactivated before the next hybrid switching circuit is activated.

[0009] The present invention provides a number of advantages over existing topologies. By using the WBG device for only a short period while the silicon-based device turns off, the RMS current is kept low in the WBG device. The present invention can therefore be used to absorb larger currents than its continuous rating during the silicon-based device's commutation without

violating its safe operating area. This allows a lower number of WBG devices in parallel with the silicon-based device and/or less expensive WBG devices with lower current ratings. In addition, by keeping the WBG device off during the conduction of the parallel silicon-based device, the i^2R losses are primarily confined to the silicon-based device, which can take advantage of its larger die to absorb and dissipate thermal stresses. These and other features and advantages of the present invention will become apparent from the following description of the invention, when viewed in accordance with the accompanying drawings and the appended claim.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] Figure 1 is an embodiment of a prior art SMPC utilizing ZVS.

[0011] Figure 2 is a circuit diagram in accordance with one embodiment.

[0012] Figure 3 is a timing diagram for operation of the circuit of Figure 2.

[0013] Figure 4 is a circuit diagram in accordance with another embodiment.

DETAILED DESCRIPTION OF THE CURRENT EMBODIMENT

[0014] Referring to Figure 2, a power converter including a half-bridge is illustrated and generally designated 10. The power converter 10 is an SMPC that provides ZVS in the present embodiment, and includes resonant circuit topology 18 connected to the half-bridge converter. The power converter 10 also includes a controller 12 operatively coupled to each switch of first and second hybrid switching circuits, S_1 and S_2. The hybrid switching circuits S_1 and S_2 are electrically connected to a controlled current source 14 at a common node 16. Each hybrid switching circuit S_1 and S_2 includes first and second dissimilar switches that are parallel connected along respective first and second branches. Each parallel switching circuit S_1 and S_2 includes a silicon-based device

parallel connected to a WBG device. In the illustrated embodiment, the silicon-based device is an Si MOSFET and the WBG device is a GaN HEMT. Other silicon-based devices can include, for example, an Si insulated-gate bipolar transistor (IGBT). Other WBG devices can include, for example, silicon nitride devices, silicon carbide devices, boron nitride devices, aluminum nitride devices, and semiconductor devices with diamond material.

[0015] As noted above, the controller 12 is operatively connected to each of the switching devices such that each switching device can independently be turned on and off. The input node 16 is connected to the controlled current source 14 and accepts AC current i_{hb}, and a voltage source V_{link} is connected in series across the two parallel circuits. The controlled current source 14 is depicted as modelling the behavior of the resonant converter topology 18. The AC current is not necessarily sinusoidal or of fixed frequency, and can be a high frequency waveform. For example, in embodiments where the SMPC is embodied as a dual active bridge (DAB) converter, the leakage inductance of the DAB transformer acts as a current source during the period in which both hybrid switching circuits S_1 and S_2 are off, forcing current into or out of the midpoint, thereby moving the midpoint voltage from one rail to the other. The current in the leakage inductance is simultaneously being driven by the voltage across it, which includes the midpoint voltage. Thus, the current is changing as it is driving the half-bridge voltage. Further, the voltage source V_{link} in Figure 2 represents an arbitrary source or storage element, created by the SMPC topology or by connection to the load, across the half-bridge connection of hybrid switching circuits S_1 and S_2. The resonant circuit topology 18 represents the greater circuit topology which in combination with S_1 and S_2 comprises the entirety of the SMPC, positioned between a power supply and a load.

[0016] In ZVS applications, shown at bottom in Figure 3, the controller 12 is configured to operate each of the WBG devices and silicon-based devices in the following manner. First, the

silicon-based device of either S_1 or S_2 is turned on for an activation period. Toward the end of the activation period, the corresponding WBG device is turned on for a small duty ratio. The silicon-based device is turned off during the duty ratio of the WBG device, after which time the WBG device is turned off. The controller 12 waits a predetermined delay period and then turns on the other silicon-based device for an equivalent activation period. Toward the end of the activation period, the corresponding WBG device is turned on for a small duty ratio. The silicon-based device is turned off during the duty ratio of the WBG device, after which time the WBG device is turned off. The controller 12 waits a predetermined delay period and then starts the process over again. The predetermined delay period is equivalent to the time it takes for the drain-to-source voltage corresponding to the hybrid switching circuit that is about to be activated (V_{ds1}, V_{ds2}) to reach zero. The silicon-based device for each switching circuit is only turned on when the corresponding voltage V_{ds1}, V_{ds2} passes zero volts and is clamped by the anti-parallel diode of the silicon-based device, being approximately between 0V and 7V in the present embodiment. Persons of skill in the art will note that the waveform at the top of Figure 3 is highly idealized for conceptualization. The idealized waveform is used for demonstration only and in no way limits the operation of the present invention.

[0017] Referring to Figure 4, a dual-active bridge (DAB) SMPC is shown and generally designated 20. Eight hybrid switching circuits labeled S_1 through S_8 are connected in two full-bridge configurations, one on each side of transformer. Each hybrid circuit contains a WBG device and a silicon-based device connected in parallel. A controller 22 is operatively coupled to each device in each hybrid switching circuit. The controller 22 operates the SMPC using a ZVS technique. The controller 22 operates each switching circuit by first activating the silicon-based device for an activation period and then activating the WBG device for a small duty ratio that is

smaller than the activation period. The silicon-based device is deactivated while the WBG device is activated and the controller does not activate the next switching circuit until the WBG device is deactivated.

[0018] In the method described above, the silicon-based devices and the WBG devices turn on with zero voltage stress because of the delay period described above. Only the silicon-based device is used during conduction to take advantage of its larger die for enhanced thermal performance. This also allows the parallel switching circuit to accept larger currents than if both switches were turned on because the circuit is not limited by the WBG device's poorer thermal characteristics, which is in turn due to its small die size. There is no significant benefit in turning on the WBG device during turn-on of the silicon-based device because the silicon-based device is soft-switching during turn-on and has a sufficiently fast rise time.

[0019] The WBG device is used during commutation to undertake the voltage stress and to take advantage of its faster fall time and lower E_{off} loss relative to the silicon-based device. Using the WBG device for only a short period while the silicon-based device turns off has additional advantages. For example, it keeps the RMS current low in the WBG device and therefore the device can absorb larger currents than its continuous rating during the silicon-based device's commutation. This means a lower number of WBG devices can be used in parallel with the silicon-based device and/or less expensive WBG devices with lower current ratings can be used in parallel with the silicon-based device.

[0020] When the WBG device is activated the voltage is held low across the silicon-based device while it turns off. This eliminates the silicon-based device's turn-off loss and its miller plateau, which increases its turn-off speed. Since the WBG device has significantly faster fall-time and smaller turn-off loss, both the switch losses and total turn-off time can be reduced. Not

activating the WBG device during the silicon-based device's conduction period allows i^2R losses to primarily be confined to the silicon-based device. This is optimal because the silicon-based device can use its larger die to absorb and dissipate the thermal stresses more effectively than the WBG device. Additionally, the silicon-based device can also absorb and dissipate a larger amount of thermal stresses than the WBG device.

[0021] The above description is that of a current embodiment of the invention. Various alterations and changes can be made without departing from the spirit and broader aspects of the invention. This disclosure is presented for illustrative purposes and should not be interpreted as an exhaustive description of all embodiments of the invention or to limit the scope of the claims to the specific elements illustrated or described in connection with these embodiments. Any reference to elements in the singular, for example, using the articles "a," "an," "the," or "said," is not to be construed as limiting the element to the singular.

CLAIMS

1. A method for achieving zero voltage switching in a switch mode power converter:

providing first and second hybrid switching circuits electrically connected in series, the first hybrid switching circuit including a first wide bandgap device that is parallel connected to a first silicon-based device, the second hybrid switching circuit including a second wide bandgap device that is parallel connected to a second silicon-based device;

activating the first silicon-based device for a first activation period;

activating the first wide bandgap device to cover-up deactivation of the first silicon-based device at the conclusion of the first activation period;

activating the second silicon-based device for a second activation period; and

activating the second wide bandgap device to cover-up deactivation of the second silicon-based device at the conclusion of the second activation period.

2. The method of claim 1 further including activating the first silicon-based device to cover-up activation of the first silicon-based device for a duty cycle less than the first activation period.

3. The method of claim 1 further including activating the second silicon-based device to cover-up activation of the second silicon-based device for a duty cycle less than the second activation period.

4. The method of claim 1 further including waiting a delay period after the deactivation of the first silicon-based device before the activation of the second silicon-based device.

5. The method of claim 4 wherein the delay period is equal to or greater than the time it takes for a voltage in the first hybrid switching circuit to reach zero.

6. The method of claim 1 wherein the first silicon-based device and the second silicon-based device each include a silicon MOSFET or a silicon IGBT.

7. The method of claim 1 wherein the first wide bandgap device and the second wide bandgap device are selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

8. The method of claim 1 wherein a duty cycle of the first wide bandgap device is equal to a duty cycle of the second wide bandgap device.

9. The method of claim 1 wherein the first activation period of the first silicon-based device is equal to the second activation period of the second silicon-based device.

10. A hybrid device comprising:

a first hybrid switching circuit and a second hybrid switching circuit each including a wide bandgap device that is parallel-connected to a silicon-based device; and

a controller electrically connected to the first hybrid switching circuit and the second hybrid switching circuit;

wherein the first hybrid switching circuit and the second hybrid switching circuit are electrically connected to a power supply at a common node;

wherein the controller is configured to operate the first hybrid switching circuit and second hybrid switching circuit respectively according the following switching sequence:

(i) activate the silicon-based device for an activation period,

(ii) activate the wide bandgap device for a predetermined duty cycle less than the activation period, and

(iii) deactivate the silicon-based device while the wide bandgap device is activated,

wherein the first and second hybrid switching circuits are sequentially operated to convert an alternating current of the power supply into a link voltage for a power converter.

11. The hybrid device of claim 10 wherein the first hybrid switching circuit and the second

hybrid switching circuit comprise a branch of an H-bridge.

12. The hybrid device of claim 10 wherein the H-bridge is a primary side H-bridge for a dual active bridge converter.

13. The hybrid device of claim 10 wherein the H-bridge is a secondary side H-bridge for a dual active bridge converter.

14. The hybrid device of claim 10 wherein the silicon-based device of the first and second hybrid switching circuits includes a silicon MOSFET or a silicon IGBT.

15. The hybrid device of claim 10 wherein the wide bandgap device of the first and second hybrid switching circuits is selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

16. A method comprising:

providing first and second hybrid switching circuits electrically connected in series, the first hybrid switching circuit including a first wide bandgap device parallel connected to a first silicon-based device, the second hybrid switching circuit including a second wide bandgap device parallel connected to a second silicon-based device, wherein the first and second hybrid switching circuits are connected to a power supply at a common node;

activating the first silicon-based device for an activation period;

activating the first wide bandgap device for a first predetermined duty cycle less than the activation period;

deactivating the first silicon-based device while the first wide bandgap device is activated;

activating the second silicon-based device for the activation period;

activating the second wide bandgap device for a second predetermined duty cycle less than the activation period; and

deactivating the second silicon-based device while the second wide bandgap device is activated, such that the first and second hybrid switching circuits convert an alternating current from the power supply into a link voltage for a power converter.

17. The method of claim 16 wherein the first silicon-based device and the second silicon-based device each include a silicon MOSFET or a silicon IGBT.

18. The method of claim 16 wherein the first wide bandgap device and the second wide bandgap device are selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

19. The method of claim 16 wherein the first predetermined duty cycle of the first wide bandgap device is equal to the second predetermined duty cycle of the second wide bandgap device.

20. The method of claim 16 further including waiting a predetermined delay period after the deactivation of the first silicon-based device before the activation of the second silicon-based device.

AMENDED CLAIMS
received by the International Bureau on 16.01.2020

1. A method for achieving zero voltage switching in a switch mode power converter:

providing first and second hybrid switching circuits electrically connected in series, the first hybrid switching circuit including a first wide bandgap device that is parallel connected to a first silicon-based device, the second hybrid switching circuit including a second wide bandgap device that is parallel connected to a second silicon-based device;

activating the first silicon-based device for a first activation period;

activating the first wide bandgap device for a first duty cycle less than the first activation period to cover-up deactivation of the first silicon-based device at the conclusion of the first activation period;

activating the second silicon-based device for a second activation period; and

activating the second wide bandgap device for a second duty cycle less than the second activation period to cover-up deactivation of the second silicon-based device at the conclusion of the second activation period.

2. The method of claim 1 further including waiting a delay period after the deactivation of the first silicon-based device before the activation of the second silicon-based device.

3. The method of claim 2 wherein the delay period is equal to or greater than the time it takes for a voltage in the first hybrid switching circuit to reach zero.

4. The method of claim 1 wherein the first silicon-based device and the second silicon-based device each include a silicon MOSFET or a silicon IGBT.

5. The method of claim 1 wherein the first wide bandgap device and the second wide bandgap device are selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

6. The method of claim 1 wherein the first duty cycle of the first wide bandgap device is equal to the second duty cycle of the second wide bandgap device.

7. The method of claim 1 wherein the first activation period of the first silicon-based

device is equal to the second activation period of the second silicon-based device.

8. A hybrid device comprising:

a first hybrid switching circuit and a second hybrid switching circuit each including a wide bandgap device that is parallel-connected to a silicon-based device; and

a controller electrically connected to the first hybrid switching circuit and the second hybrid switching circuit;

wherein the first hybrid switching circuit and the second hybrid switching circuit are electrically connected to a power supply at a common node;

wherein the controller is configured to operate the first hybrid switching circuit and second hybrid switching circuit respectively according the following switching sequence:

(i) activate the silicon-based device for an activation period,

(ii) activate the wide bandgap device for a predetermined duty cycle less than the activation period, and

(iii) deactivate the silicon-based device while the wide bandgap device is activated,

wherein the first and second hybrid switching circuits are sequentially operated to convert an alternating current of the power supply into a link voltage for a power converter.

9. The hybrid device of claim 8 wherein the first hybrid switching circuit and the second hybrid switching circuit comprise a branch of an H-bridge.

10. The hybrid device of claim 8 wherein the H-bridge is a primary side H-bridge for a dual active bridge converter.

11. The hybrid device of claim 8 wherein the H-bridge is a secondary side H-bridge for a dual active bridge converter.

12. The hybrid device of claim 8 wherein the silicon-based device of the first and second hybrid switching circuits includes a silicon MOSFET or a silicon IGBT.

13. The hybrid device of claim 8 wherein the wide bandgap device of the first and second

hybrid switching circuits is selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

14. A method comprising:

providing first and second hybrid switching circuits electrically connected in series, the first hybrid switching circuit including a first wide bandgap device parallel connected to a first silicon-based device, the second hybrid switching circuit including a second wide bandgap device parallel connected to a second silicon-based device, wherein the first and second hybrid switching circuits are connected to a power supply at a common node;

activating the first silicon-based device for an activation period;

activating the first wide bandgap device for a first predetermined duty cycle less than the activation period;

deactivating the first silicon-based device while the first wide bandgap device is activated;

activating the second silicon-based device for the activation period;

activating the second wide bandgap device for a second predetermined duty cycle less than the activation period; and

deactivating the second silicon-based device while the second wide bandgap device is activated, such that the first and second hybrid switching circuits convert an alternating current from the power supply into a link voltage for a power converter.

15. The method of claim 14 wherein the first silicon-based device and the second silicon-based device each include a silicon MOSFET or a silicon IGBT.

16. The method of claim 14 wherein the first wide bandgap device and the second wide bandgap device are selected from a group consisting of gallium nitride (GaN), silicon carbide (SiC), boron nitride (BN), aluminum (AlN), and diamond.

17. The method of claim 14 wherein the first predetermined duty cycle of the first wide

bandgap device is equal to the second predetermined duty cycle of the second wide bandgap device.

18. The method of claim 14 further including waiting a predetermined delay period after the deactivation of the first silicon-based device before the activation of the second silicon-based device.

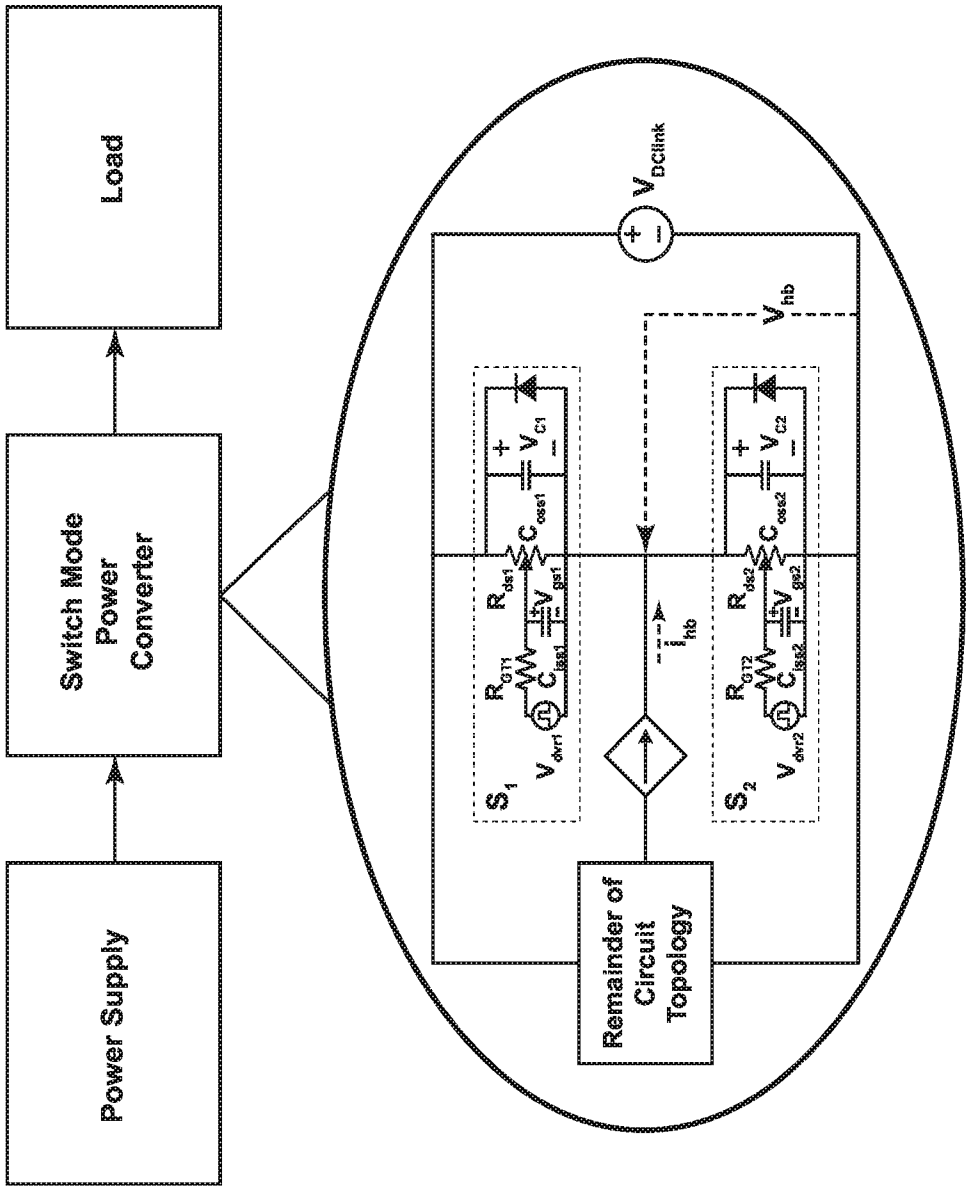

FIG. 1 (PRIOR ART)

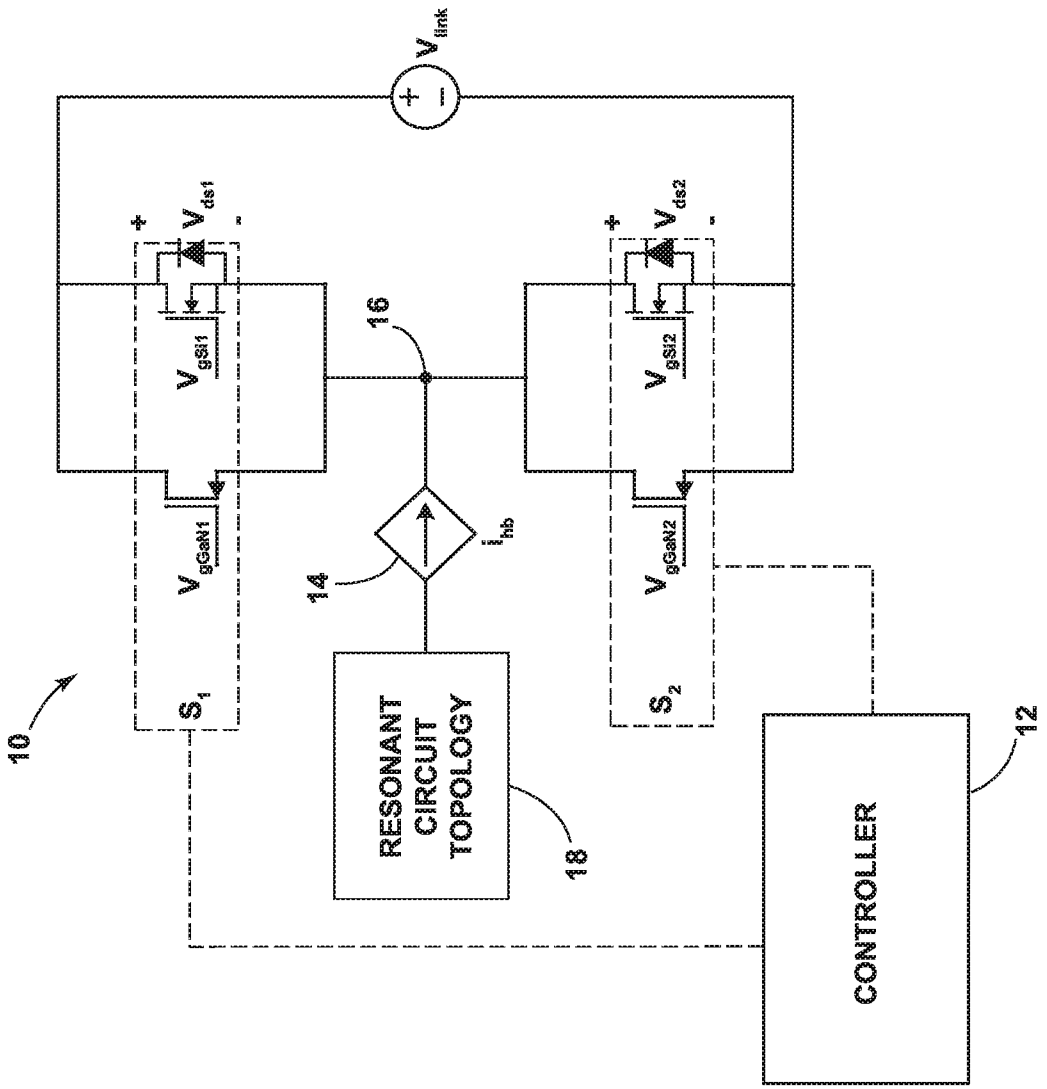
V_{link}
+
−
V_{ds1}
+
-
V_{gSi1}
V_{gGaN1}
S_1
16
14
i_{hb}
RESONANT CIRCUIT TOPOLOGY
18
V_{ds2}
+
-
V_{gSi2}
V_{gGaN2}
S_2
CONTROLLER
12
10

FIG. 2

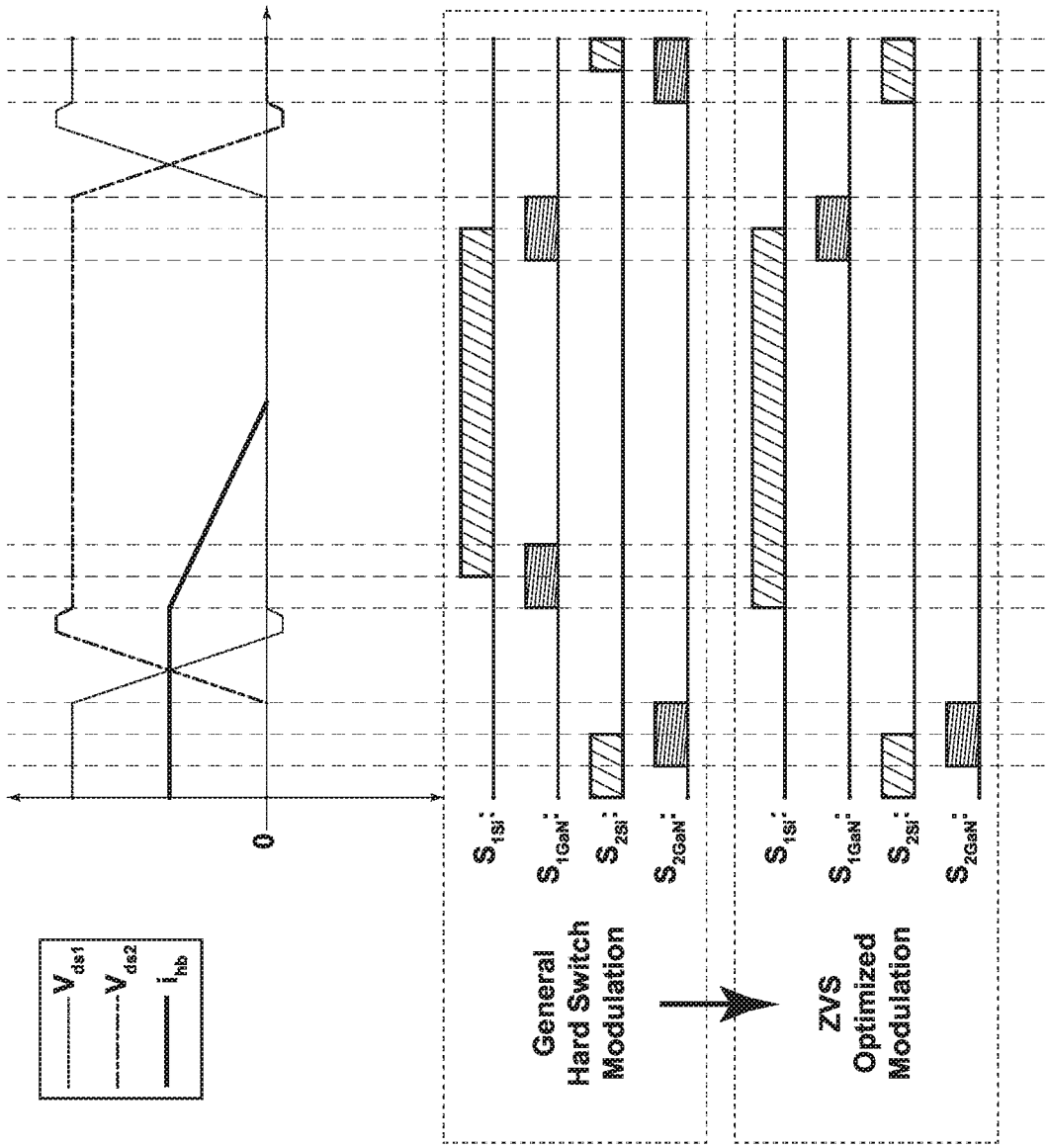
V_{ds1}
V_{ds2}
i_{hb}
0
S_{1Si}
S_{1GaN}
S_{2Si}
S_{2GaN}
General Hard Switch Modulation
ZVS Optimized Modulation

FIG. 3

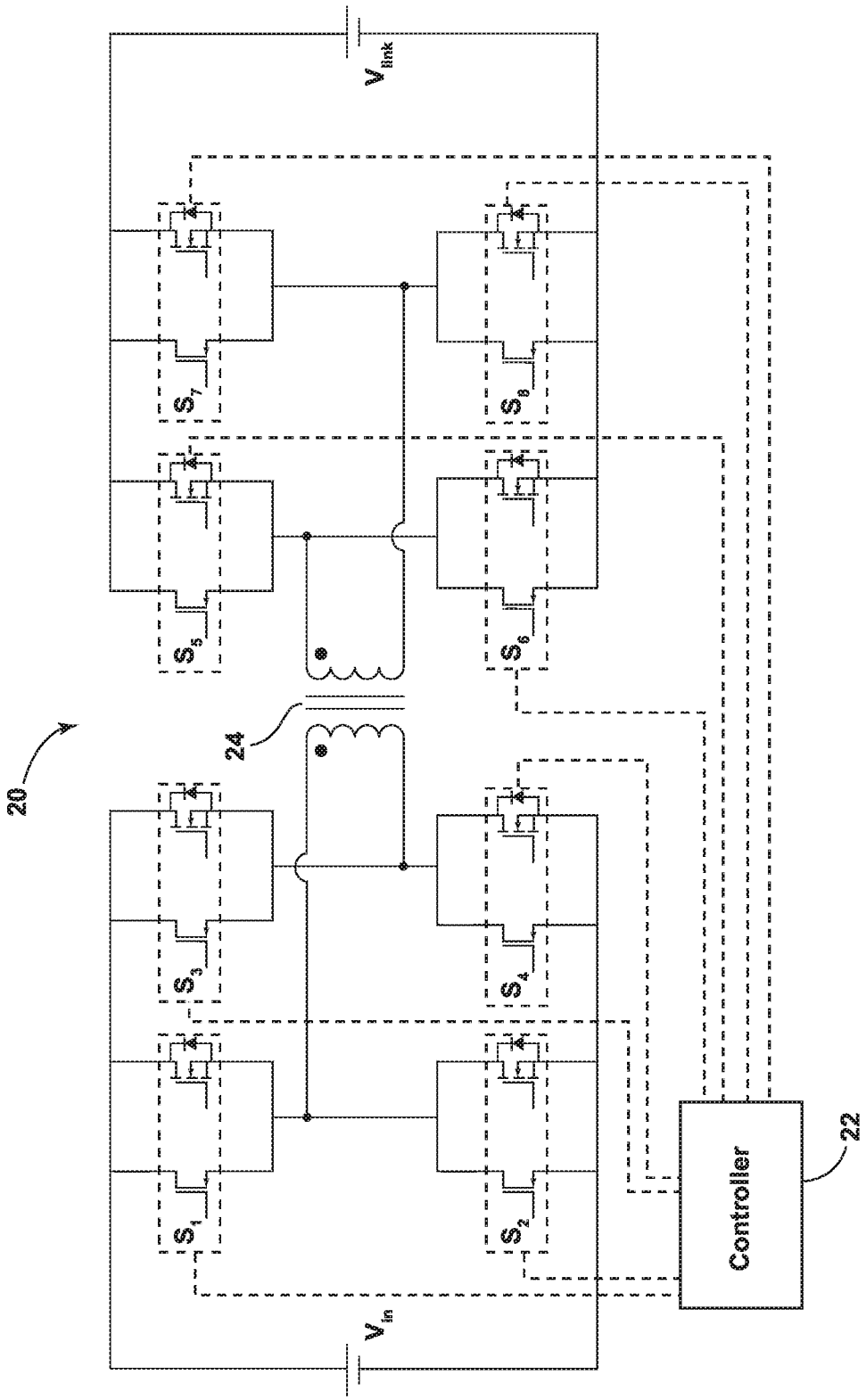

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2019/056726

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M1/08 H02M3/335 H03K17/567
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 9 735 771 B1 (LU JUNCHENG [US] ET AL) 15 August 2017 (2017-08-15) columns 1-6; figures 2-4	1-20
X	LI ZONGJIAN ET AL: "Gate Control Optimization of Si/SiC Hybrid Switch Within Wide Power Rating Range", 2018 1ST WORKSHOP ON WIDE BANDGAP POWER DEVICES AND APPLICATIONS IN ASIA (WIPDA ASIA), IEEE, 16 May 2018 (2018-05-16), pages 265-269, XP033560361, DOI: 10.1109/WIPDAASIA.2018.8734640 [retrieved on 2019-06-10] paragraph [SectionIII]; figure 1	1-20

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

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Date of the actual completion of the international search	Date of mailing of the international search report
22 November 2019	29/11/2019

Name and mailing address of the ISA/	Authorized officer
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INTERNATIONAL SEARCH REPORT

International application No
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