(54) Title: GATE DRIVE VOLTAGE BOOST SCHEMES FOR MEMORY ARRAY II

(57) Abstract: This invention describes a circuit and method to write information into individual memory cells while minimizing the gate voltage stress in the cell transistors of the memory cells in which no information is being written. The circuit of this invention has a separately controllable word line voltage supply for each row of the memory array and a separately controllable voltage supply for each bit line of the memory array. During the write operation the voltage is raised for the word line of only one row of the array. The bit line voltages are then adjusted so that a 1 is written into the desired cells in that row and a 0 is written into the desired cells in that row.

FIG. 1
BACKGROUND OF THE INVENTION

(1) FIELD OF THE INVENTION

This invention relates to gate drive voltage for magnetic memory technologies, such as Phase Change RAM and Spin Moment Transfer MRAM, sometimes referred to as Spin Torque Transfer MRAM, cells which require programming currents higher than the minimum cell transistor can provide without degrading the life of the cell transistor. More particularly the invention relates to circuits and methods for programming these cell transistors by applying high voltages between the gate and source or drain of the cell transistor only to those cell transistors into which a one or zero is being written.

(2) DESCRIPTION OF RELATED ART

U.S. Patent No. 7,046,547 B2 and U.S. Pat. No. 6,961,265 B2 to Witcraft et al. describe methods and apparatus that allow data to be stored in a magnetic memory cell, such as a giant magneto-resistance cell. The inventions describe advantageously winding a word line around a magnetic memory cell to increase the magnetic field induced by the word line.
U. S. Patent No. 6,985,382 B2 to Fulkerson et al. describe a technique to read a stored state in a magneto-resistive random access memory device, MRAM, such as a giant magneto-resistance MRAM device or a tunneling magneto-resistance device, TMR. The technique uses a bit line that is segmented into a first portion and a second portion. An interface circuit compares the resistance of a first portion and a second portion of a first bit line to the resistance of a first portion and a second portion of a second bit line to determine the logical state of a cell in the first bit line.

U. S. Patent No. 6,754,055 B2 to Ono et al. describes a giant magneto-resistive effect element which includes a laminated layer film having a ferromagnetic film, a non-magnetic film, and an anti-ferromagnetic film.

U.S. Patent No. 6,714,390 B2 describes a giant magneto-resistive effect element capable of producing a high output and a high resistance and which can cope with a high recording density and a magneto-resistive effect type head, a thin film magnetic memory, and a thin film magnetic sensor each of which includes this giant magneto-resistive effect element.
SUMMARY OF THE INVENTION

Magnetic memory elements using the Giant magneto-resistive effect, such as Phase Change RAM and Spin Moment Transfer MRAM, sometimes referred to as Spin Torque Transfer MRAM, require high programming currents. Since these currents are controlled by a cell transistor, which is a field effect transistor, a high voltage between the source and/or drain is required to produce sufficient memory cell current to program the memory cells. This high gate to source/drain voltage and high memory cell current can significantly reduce the life of the cell transistor.

It is a principal objective of this invention to provide a circuit which can write information into individual memory cells, a one or a zero, while minimizing the gate voltage stress in the cell transistors of the memory cells in which no information is being written.

It is another principal objective of this invention to provide a method of writing information into individual memory cells, a one or a zero, while minimizing the gate voltage stress in the cell transistors of the memory cells in which no information is being written.
These objectives are achieved by methods and circuits which apply the high gate to drain voltage, or gate to source voltage only to those cells in which a 1 or a 0 is to be written so that only these cells see the high gate to source/drain voltage stress.

Since these cell transistors see the high stress only when that cell is written the reliability of the cell transistors is not significantly degraded.

The circuit of this invention has a separately controllable word line voltage supply for each row of the memory array and a separately controllable voltage supply for each bit line of the memory array. During the write operation the voltage is raised for the word line of only one row of the array. The bit line voltages are then adjusted so that a 1 is written into the desired cells in that row and a 0 is written into the desired cells in that row.
BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a schematic diagram of the circuit of this invention.

Fig. 2 shows a schematic diagram of a 2 X 2 section of the memory array.

Figs. 3A and 3B show a schematic diagram of circuits used to produce data line voltages for the circuit of this invention.

Fig. 4 shows a timing diagram of the voltages used to write a 0 into cell 000 and a 1 into cell 001.
DESCRIPTION OF THE PREFERRED EMBODIMENTS

Refer now to the Drawings for a description of the preferred embodiments of this invention. Fig. 1 shows one section, section 0, of a magnetic memory comprising an n column by m row array of magnetic memory cells 000, 001, ..., 00n, 010, 011, ..., 01n,OmO, 0ml, ...Omn. Fig. 1 also shows the beginning of another section, section 1, of the magnetic memory showing magnetic memory cells 110, 111, ..., ImO. This description will describe the example of section 0, as those skilled in the art will readily understand how the invention is applied to other sections as they are selected. Fig. 2 shows a schematic diagram of memory cells 000, 001, 010, and 011 showing each memory cell having a cell transistor 30 and a magnetic memory element 32 with one terminal of the magnetic memory element 32 connected to one of the source/drain terminals of the cell transistor 30. In Fig. 2 this node between the cell transistor 30 and magnetic memory element 32 is designated by the reference number DR0 in cell 000 and the reference number Si in cell 001 because the following example will describe writing a 0 in cell 000, where this node is a drain, and a 1 in cell 001, where this node is a source. Whether the source/drain terminals of the cell transistor are considered a source or a drain depends on the direction of the current through the cell transistor. All transistors in this description are field effect transistors.

Refer again to Fig. 1 which shows that each memory cell has a BLC line; \( BLC_0, BLC_1, \ldots BLC_N \); and a BLT line; \( BLT_0, BLT_1, \ldots BLT_N \). Each of the BLC and BLT lines are connected through a bit line transistor 12 to a data line, the BLC0 line to the DLCT line, the BLCi line to the DLCi line, the BLT0 line to the DLT0 line, the BLT1 line to the DLT1 line and so forth with the BLCN line connected to the DLCN line and the BLTN line.
line connected to the DLT \(_N\) line. The gates of the bit line transistors \(12\) in the first section are all connected together to bit line signal source \(y_0\) so that all of the bit line transistors \(12\) in this section are turned on or off at the same time. This allows a particular voltage to be supplied to each of the BLC and BLT lines independently by the data lines DLC\(_0\), DLTo, DLCi, DLTi, ..., DLC\(_N\), and DLT\(_N\). The data lines provide a supply of selected voltages to the BLT and BLC lines. The signal source \(y_0\) also allows the enhanced voltage level, \(V_{WL}\), to be applied to selected rows of section 0 of the memory when desired. The gates of the bit line transistors \(13\) in the second section are also all connected together to bit line signal source \(y_i\) so that all of the bit line transistors \(13\) in this section are turned on or off at the same time. The signal source \(y_i\) prevents voltage from being applied to the BLT and BLC lines in section 1 of the memory and prevents the enhanced voltage level, \(V_{WL}\), to be applied to any rows of section 1 of the memory while section 0, or other sections of the memory, are being written. The memory may have other sections which are connected and operated in similar fashion. This invention will be described with reference to section one only, however those skilled in the art will recognize that the invention can be applied to other sections in similar fashion.

The voltages on the DLC lines are supplied by first data line drivers 18 and the voltages on the DLT lines are supplied by second data line drivers 20. The voltages to the first data line drivers 18 are supplied by VIL and VOH voltage supplies and the inverse data line signals DOi, Dli, ..., DNi. The voltages to the second data line drivers 20 are supplied by VIH and VOL voltage supplies and the data line signals DO, DI, ..., DN. The first data line drivers 18 are shown in Fig. 3A where an inverse data line signal for memory cell N, DNi, switches the output DLC\(_N\) signal for memory line N between VOH and VIL. The second data line drivers 20 are shown in Fig. 3B where a data line
signal for memory cell N, DN, switches the output DLT \(_N\) signal for memory line N between V\(_{IH}\) and VOL.

The word lines WLOO, WLIO, ..., WLmO and the global word lines GWLO, GWL1, ..., GWLm are driven by row decoders 14. The word lines WL00, WL10, ..., WLm0 are also driven by high voltage word line segment drivers 16 which can supply a higher voltage V\(_{WL}\) to a selected word line during the writing operation which will be described next.

Refer now to Figs. 2 and 4 for description of the circuit and method of this invention for writing a 1 and/or a 0 into magnetic memory elements. This example will show simultaneously writing a 0 in cell 000 and a 1 into cell 001. Fig. 2 shows a smaller section of the memory array showing memory cells 000, 001, 010, and 011. Writing a 0 in a cell requires causing a current to flow from the magnetic memory element 32 into the cell transistor 30. Writing a 1 in a cell requires causing a current to flow from the cell transistor 30 into the magnetic memory element 32. The magnetic memory element 32 can be approximated as a resistor and this approximation will be used in this example. In this example, the current required to write a 0 in a magnetic memory element 32 causes a voltage drop of about 0.4 volts across the magnetic memory element 32. In this example, the current required to write a 1 in a magnetic memory element 32 also causes a voltage drop of about 0.4 volts across the magnetic memory element 32.

Fig. 4 shows a timing diagram for the example of simultaneously writing a 0 in cell 000 and a 1 in cell 001. As shown in Fig. 4 in the interval between T1 and T2, data line DLT\(_0\) goes from 0 volts to 0.4 volts, data line DLC\(_0\) goes from 0 volts to 1.0.
volts, data line DLTi goes from 0 volts to 0.6 volts, and data line DLCi remains at 0 volts. Also in the interval between T1 and T2 the signal y₀ to the bit line transistors 12 remains low so that the bit line transistors 12 are turned off, bit line BLT₀, bit line BLCo, bit line BLTi, and bit line BLCi remain at 0 volts. Also between T1 and T2 the node between the cell transistor 30 and the magnetic memory element 32 in cell 000, designated here as node DRo since it is connected to the cell transistor terminal acting as a drain in this case, the node between the cell transistor 30 and the magnetic memory element 32 in cell 001, designated here as node Si since it is connected to the cell transistor terminal acting as a source in this case; and the word line WL₀₀ connected to the cell transistors 30 in the row in which cells 000 and 001 are located remain at 0 volts.

In the interval between T2 and T3 data line DL₀ remains at 0.4 volts, data line DLCo remains at 1.0 volts, data line DLTi remains at 0.6 volts, and data line DLCi remains at 0 volts. Also in the interval between T2 and T3 the signal y₀ to the bit line transistors 12 becomes high so that the bit line transistors 12 are turned on, bit line BLTo goes to 0.4 volts, bit line BLCo goes to 1.0 volts, bit line BLTi goes to 0.6 volts, bit line BLCi and word line WL₀₀ remain at 0 volts. Since the word line WL₀₀ voltage remains at 0 volts the cell transistors 30 in cells 000 and 001 remain turned off so that the voltage of the Do node goes to 1.0 volts, because of the voltage of the BLCo line, and the voltage of the Si node remains at 0 volts, because of the voltage of the BLCi line.

In the interval between T3 and T4 data line DLTo remains at 0.4 volts, data line DLCo remains at 1.0 volts, data line DLTi remains at 0.6 volts, data line DLCi remains at 0 volts, the signal y₀ to the bit line transistors 12 remains high so that the bit line transistors 12 remain turned on, bit line BLT₀ remains at 0.4 volts, bit line BLCo
remains at 1.0 volts, bit line BLTi remains at 0.6 volts, and bit line BLCi remains at 0 volts. In the interval between T3 and T4 the word line WLoo voltage goes to 2.2 volts which allows the cell transistors 30 in cells 000 and 001 to pass sufficient current to write a 0 in cell 000 and a 1 in cell 001. With the cell transistor 30 in cell 000 passing sufficient current to write a 0 in cell 000 and a 1 in cell 001 the voltage drop across the magnetic memory element in these cells is 0.4 volts reducing the voltage at the DR0 node in cell 000 to 0.6 volts and raising the voltage at the Si node in cell 001 to 0.4 volts.

During the writing of a 0 in cell 000 and a 1 in cell 001 the worst case voltage stress between the gate, at 2.2 volts, and the source/drain terminals of the cell transistor in cells 000 and 001 is 1.8 volts, since the BLTo node is at 0.4 volts in cell 000 and the Si node is at 0.4 volts in cell 001. The high voltage of 2.2 volts is only applied to one row of the cells in the section being written and the same worst case voltage applies whether a 1 or a 0 is being written in a cell in that row. After T4 the voltages revert to the beginning levels and a new cycle can begin.

During this write cycle the signal yi to the bit line transistors 13 in section 1 of the memory as well as the signals to the other bit line transistors in other sections of the memory, not shown, remains low so that these bit line transistors remain turned off. The high voltage is restricted to that section by signals to the corresponding bit line transistors, such as the signal yi to the bit line transistors 13 in that part of the next section of the memory shown in Fig. 1 and to the global word lines GLWO, GLWL, ..., GLWm. Similar signals are applied to those bit line transistors and global word lines not shown in Fig. 1. Memory cells 100, 110, ..., ImO are also shown in Fig. 1.
The voltages described here are for a particular example and different voltages could be used to achieve the same effect.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:
1. A method of writing magnetic random access memory elements requiring high programming currents, comprising:

    providing a plurality of memory cells arranged in an array of m rows and n columns, wherein each memory cell has a magnetic memory element, each said magnetic memory element having a first terminal and a second terminal, and a cell transistor, each said cell transistor having a first source/drain terminal connected to said second terminal of said magnetic memory element, a gate, and a second source/drain terminal, and

wherein said memory cell stores a 1 by causing a first current to flow from said cell transistor into said magnetic memory element and stores a 0 by causing a second current to flow from said magnetic memory element into said cell transistor;

    providing a BLT line and a BLC line for each column of said array;

    providing a word line for each row of said array;

    connecting said first terminal of said magnetic memory elements in those said
magnetic memory cells in each of said n columns to one of said BLC lines;

    connecting said second source/drain terminal, of each of said cell transistors in those said magnetic memory cells in each of said n columns to one of said BLT lines;

    connecting said gate of each of said cell transistors in those said magnetic memory cells in each of said m rows to one of said word lines;

    selecting one of said rows of said array; and

    writing a 1 or a 0 in selected magnetic memory cells in said selected row of said array by applying a first voltage to said word line for that said row, a second voltage to those BLC lines and a third voltage to those BLT lines connected to those magnetic memory cells in which a 1 is to be written, a fourth voltage to those BLC lines and a fifth voltage to those BLT lines connected to those magnetic memory cells in which a 0 is to
be written, and a sixth voltage to the remaining word lines in said array wherein said sixth
voltage is less than said first voltage.

2. The method of claim 1 wherein said first voltage is about 2.2 volts.

3. The method of claim 1 wherein said second voltage is about 0 volts and said third
voltage is about 0.6 volts.

4. The method of claim 1 wherein said fourth voltage is about 1.0 volts and said fifth
voltage is about 0.4 volts.

5. The method of claim 1 wherein said cell transistors are field effect transistors.

6. The method of claim 1 wherein the maximum voltage between said gate of said cell
transistor and either said first or second said source/drain terminal of said cell transistor is
1.8 volts when writing a 1 or a 0 into said magnetic memory element.

7. The method of claim 1 wherein said sixth voltage is about zero volts.

8. The method of claim 1 wherein said magnetic memory elements can be approximated
as a resistor.

9. The method of claim 1 wherein said writing a 1 or a 0 in said magnetic memory
element causes a voltage drop across said magnetic memory element of about 0.4 volts.
10. The method of claim 1 wherein said writing a 1 or a 0 in said magnetic memory element requires a voltage drop between said first source/drain terminal of said cell transistor and said second source/drain terminal of said cell transistor of about 0.4 volts.

11. A circuit for writing magnetic random access memory elements requiring high programming currents, comprising:

   a plurality of memory cells arranged in an array of m rows and n columns, wherein each memory cell has a magnetic memory element, each said magnetic memory element having a first terminal and a second terminal, and a cell transistor, each said cell transistor having a first source/drain terminal connected to said second terminal of said magnetic memory element, a gate, and a second source/drain terminal, and wherein said memory cell stores a one by causing a first current to flow from said cell transistor into said magnetic memory element and stores a zero by causing a second current to flow from said magnetic memory element into said cell transistor;

   a BLC line connected to said first terminal of said magnetic memory elements in those said magnetic memory cells in each of said n columns of said array;

   a BLT line connected to said second source/drain connection of each of said cell transistors in those said magnetic memory cells in each of said n columns of said array;

   a word line connected to said gate of each of said cell transistors in those said magnetic memory cells in each of said m rows of said array;

   a first variable voltage source connected to said gates of said cell transistors in each of said rows of said array;

   a second variable voltage source connected to each of said BLC lines in said array; and

   a third variable voltage source connected to each of said BLT lines of said array.
12. The circuit of claim 11 wherein said first voltage source can supply a voltage of about
2.2 volts or about 0 volts.

13. The circuit of claim 11 wherein said second voltage source can supply voltages of
about 0.4 volts or about 0.6 volts.

14. The circuit of claim 11 wherein said third voltage source can supply voltages of about
0 volts or about 1.0 volts.

15. The circuit of claim 11 wherein said first voltage source can supply different voltages
for different rows of said array.

16. The circuit of claim 11 wherein said second voltage source and said third voltage
source can supply different voltages for different columns of said array.
17. The circuit of claim 11 wherein said cell transistors are field effect transistors and the
maximum voltage between said gate of said cell transistor and either said first or second
said source/drain terminal of said cell transistor is 1.8 volts when writing a 1 or a 0 into
said magnetic memory element.

18. The circuit of claim 11 wherein said magnetic memory elements can be approximated
as a resistor.

19. The circuit of claim 11 wherein said writing a 1 or a 0 in said magnetic memory
element causes a voltage drop across said magnetic memory element of about 0.4 volts.

20. The circuit of claim 11 wherein said writing a 1 or a 0 in said magnetic memory
element requires a voltage drop between said first source/drain terminal of said cell
transistor and said second source/drain terminal of said cell transistor of about 0.4 volts.
FIG. 2

FIG. 3A

FIG. 3B
FIG. 4
INTERNATIONAL SEARCH REPORT

International application No
PCT/US 10/01896

A  CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G 11 C 11/06 (201 001 )
USPC - 365/225.5

According to International Patent Classification (IPC) or to both national classification and IPC

B  FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC  365/225 5

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC  365/225 5,55,66,230 0 1,230 07 (keyword limited, terms below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWEST (USPT, PGPB, EPAB, JPAB), Google, Google Patents
Keywords MRAM, cell, magnetic element, transistor, word line, BLT, BLC, voltage, current

C  DOCUMENTS CONSIDERED TO BE RELEVANT

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Date of the actual completion of the international search
13 August 2010 (13 08 2010)

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<td>This invention describes a circuit and method to write information into individual memory cells while minimizing the gate voltage stress in the cell transistors of the memory cells in which no information is being written. The circuit of this invention has a separately controllable word line voltage supply for each row of the memory array and a separately controllable voltage supply for each bit line of the memory array. During the write operation, the voltage is raised for the word line of only one row of the array. The bit line voltages are then adjusted so that a 1 is written into the desired cells in that row and a 0 is written into the desired cells in that row.</td>
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