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OH et al.(10) **Pub. No.: US 2016/0149125 A1**(43) **Pub. Date: May 26, 2016**(54) **RESISTIVE MEMORY DEVICE AND
FABRICATION METHOD THEREOF**(71) Applicant: **SK hynix Inc.**, Gyeonggi-do (KR)(72) Inventors: **Dong Yean OH**, Gyeonggi-do (KR);
Chang Soo WOO, Gyeonggi-do (KR)(21) Appl. No.: **14/668,296**(22) Filed: **Mar. 25, 2015**(30) **Foreign Application Priority Data**

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(57)

ABSTRACT

A semiconductor integrated circuit device and a fabrication method thereof are disclosed. The resistive memory device includes a lower electrode, a resistive layer formed in a resistance change region on the lower electrode, an upper electrode formed on the resistive layer, and an insertion layer configured to allow a reset current path of the resistive layer, which is formed from the upper electrode to the lower electrode, to be bypassed in a direction perpendicular to or parallel to a surface of the lower electrode.

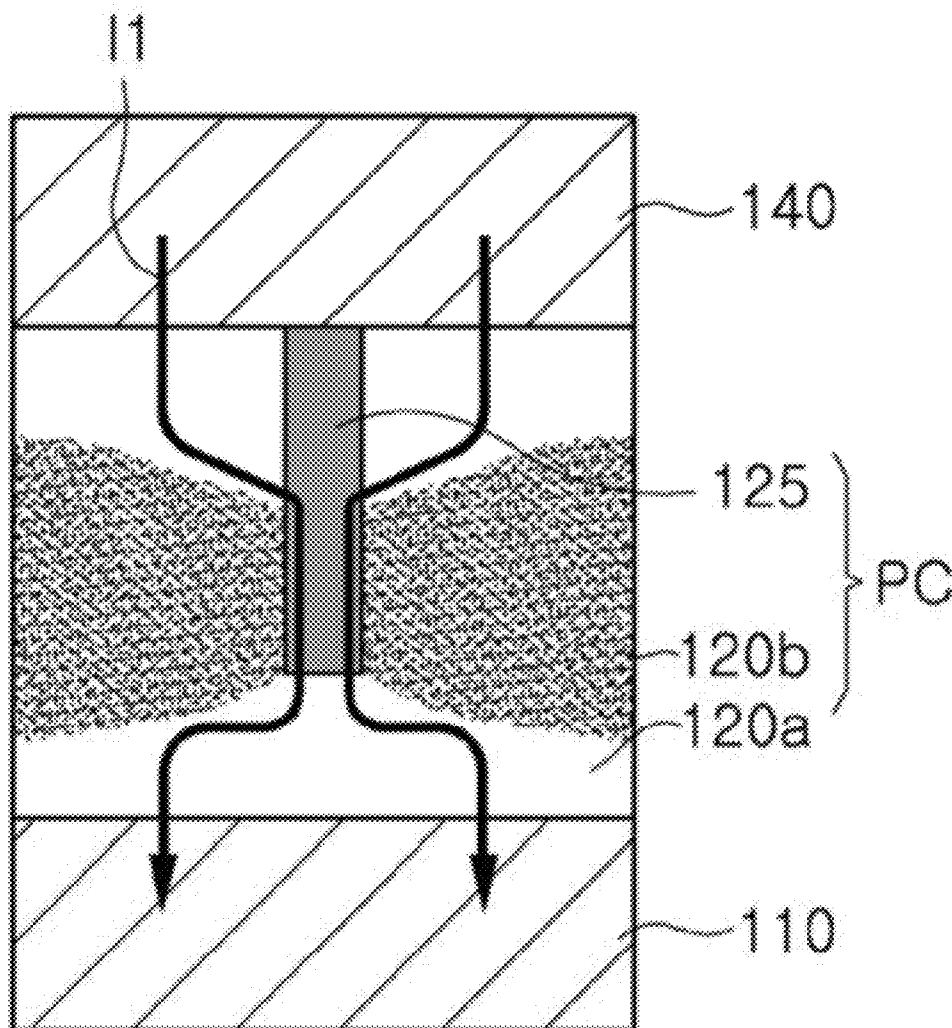


FIG.1

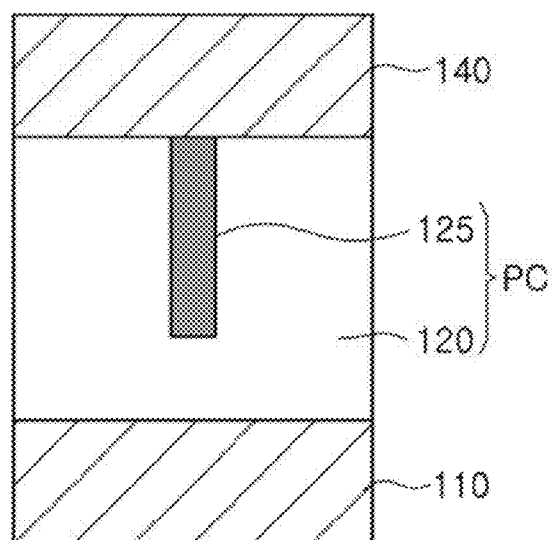


FIG.2

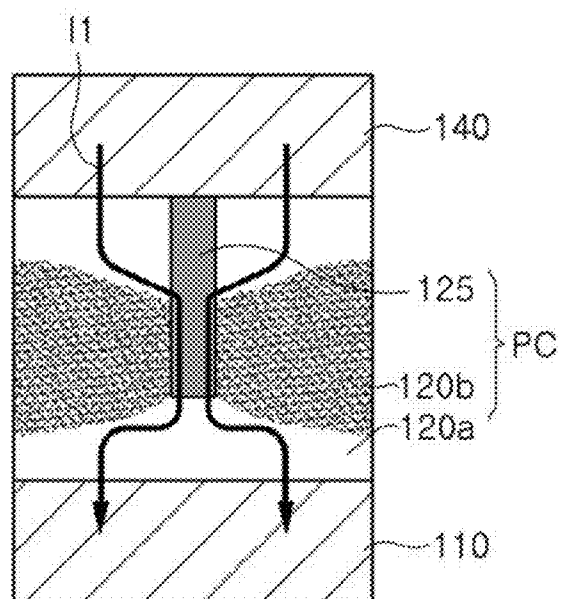


FIG.3

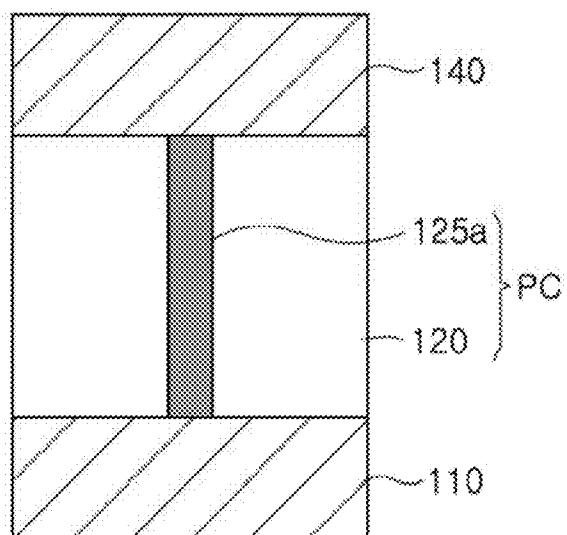


FIG.4

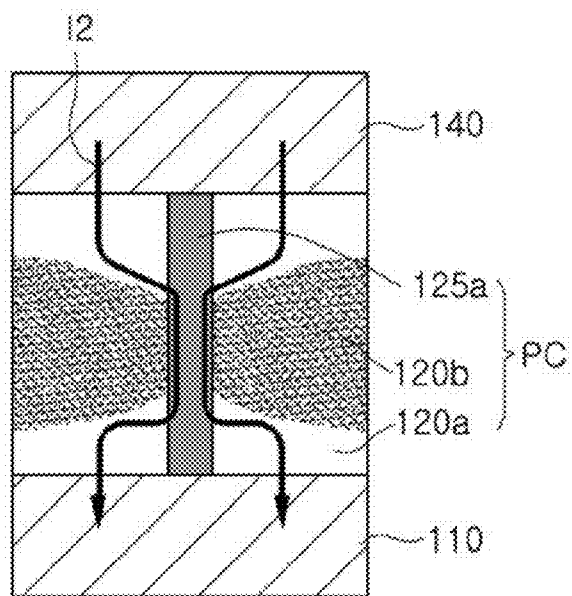


FIG.5

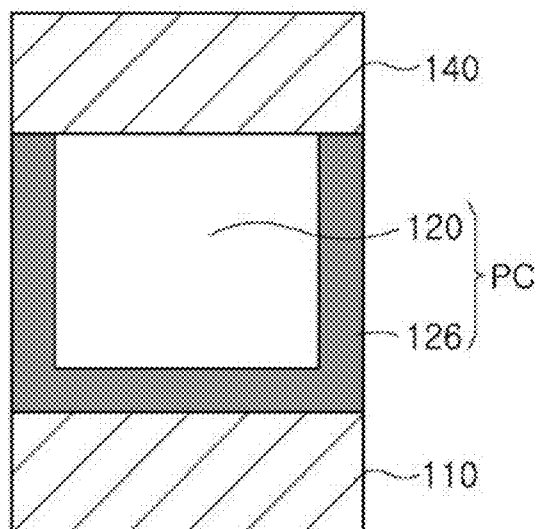


FIG.6

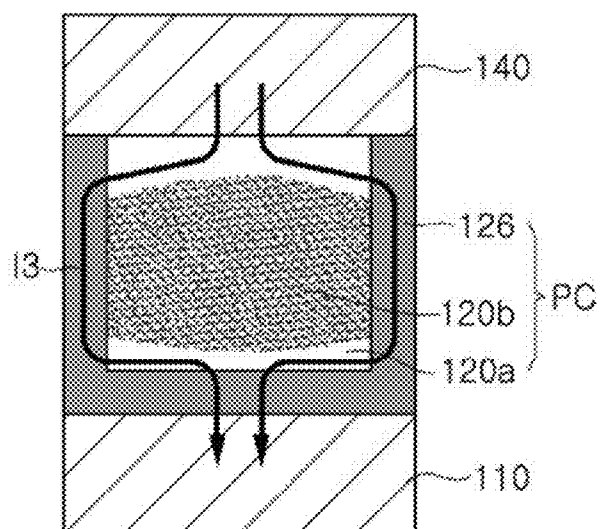


FIG.7

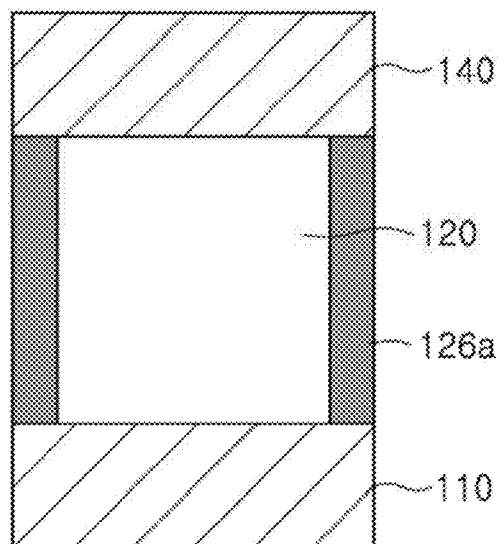


FIG.8

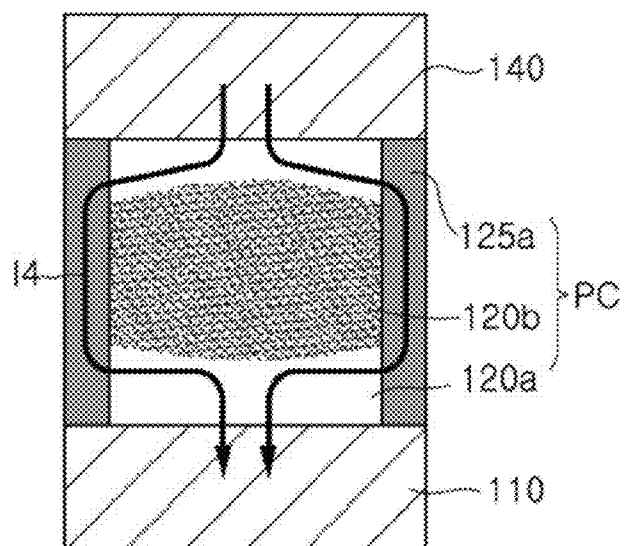


FIG.9

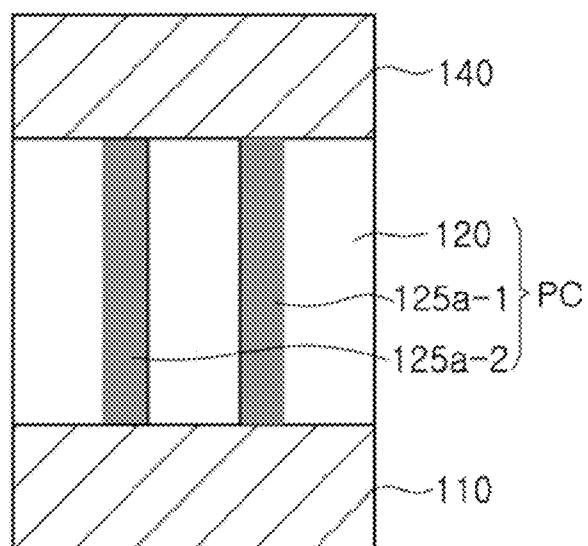


FIG.10

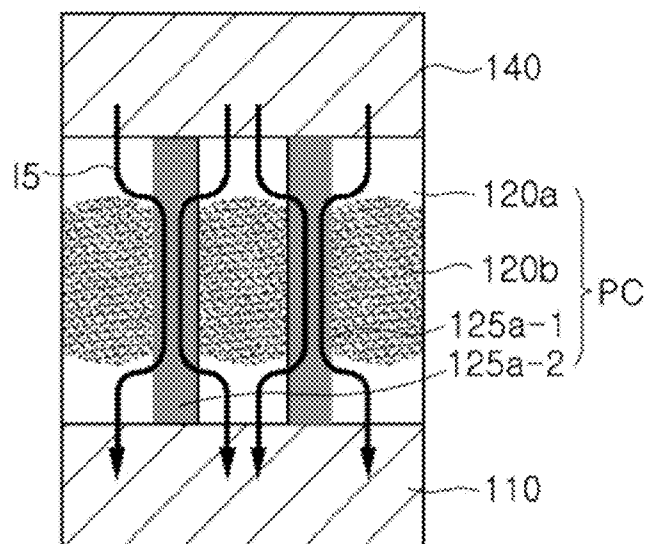


FIG.11

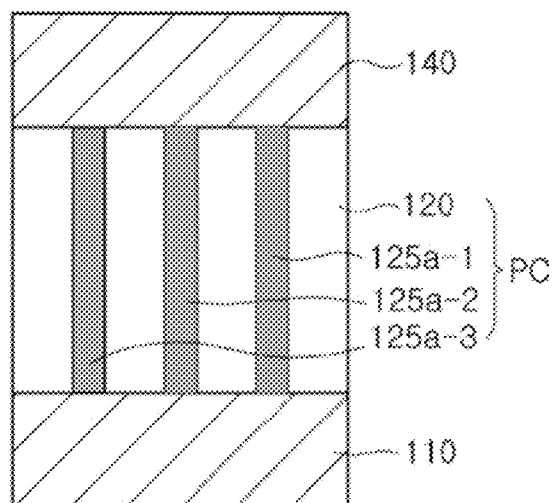


FIG.12

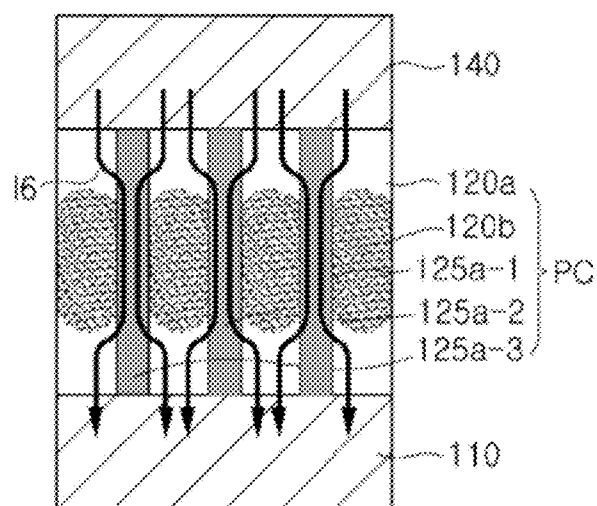


FIG.13

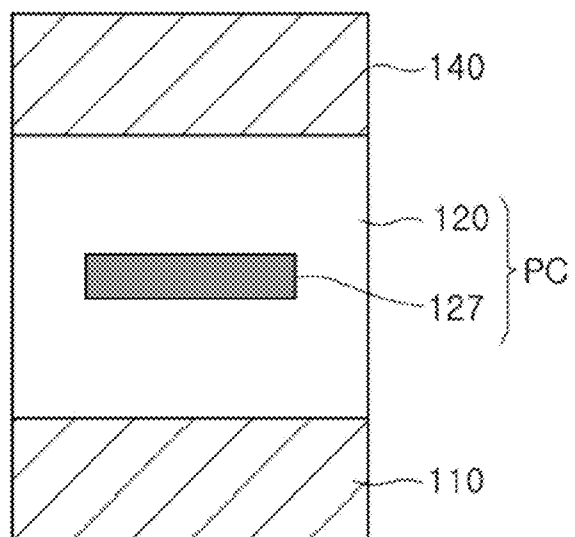


FIG.14

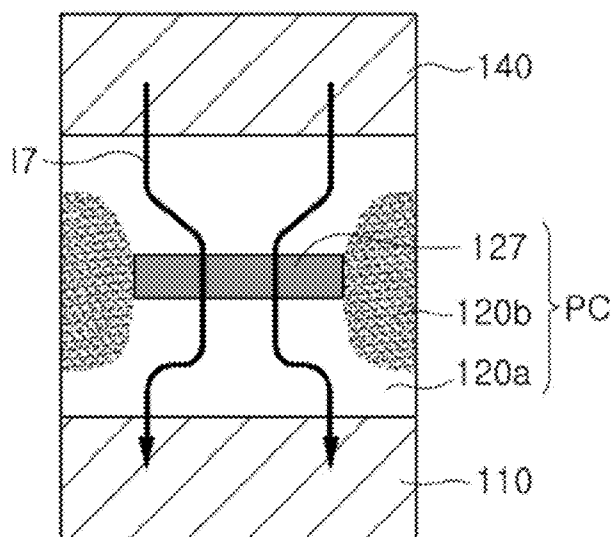


FIG.15

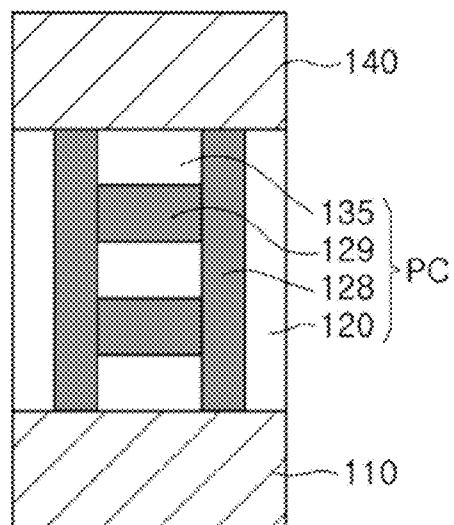
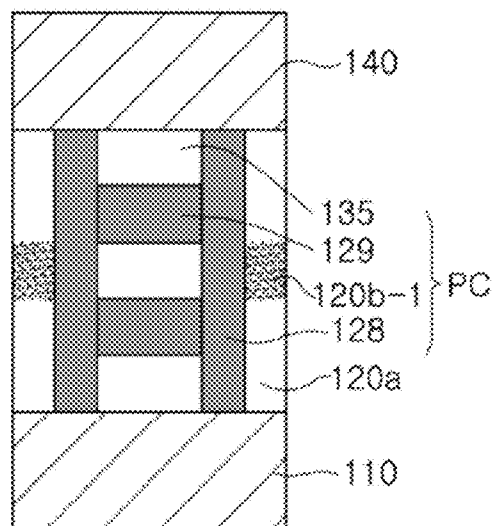


FIG.16



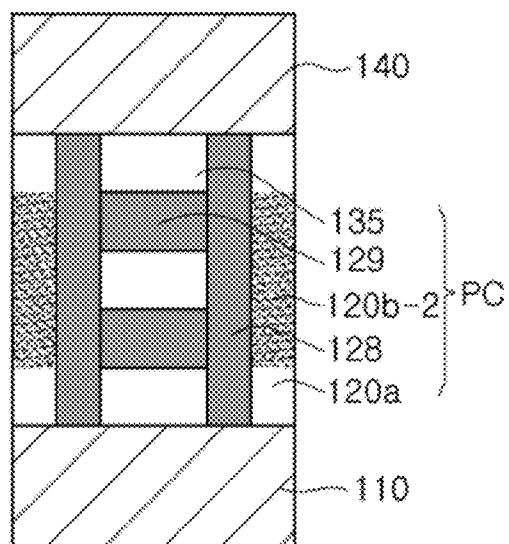


FIG.19A

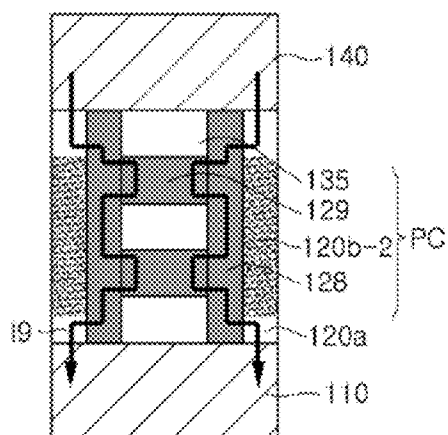


FIG.19B

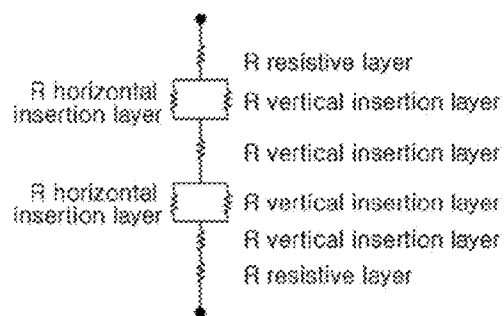


FIG.20

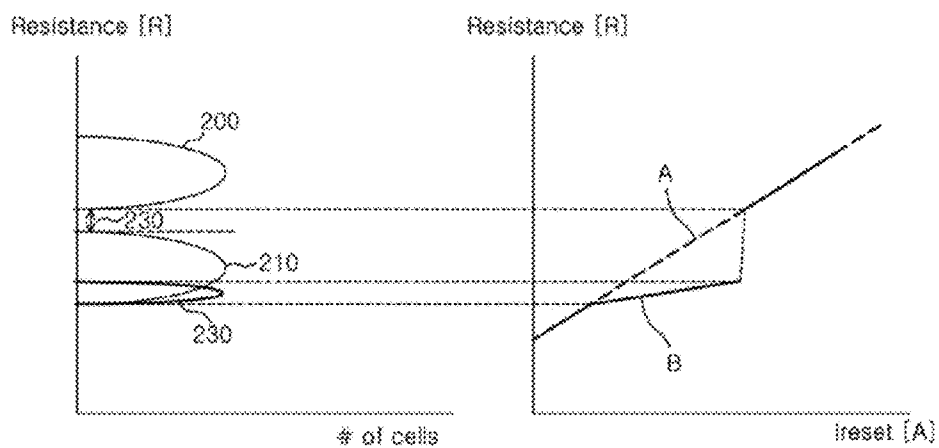


FIG.21

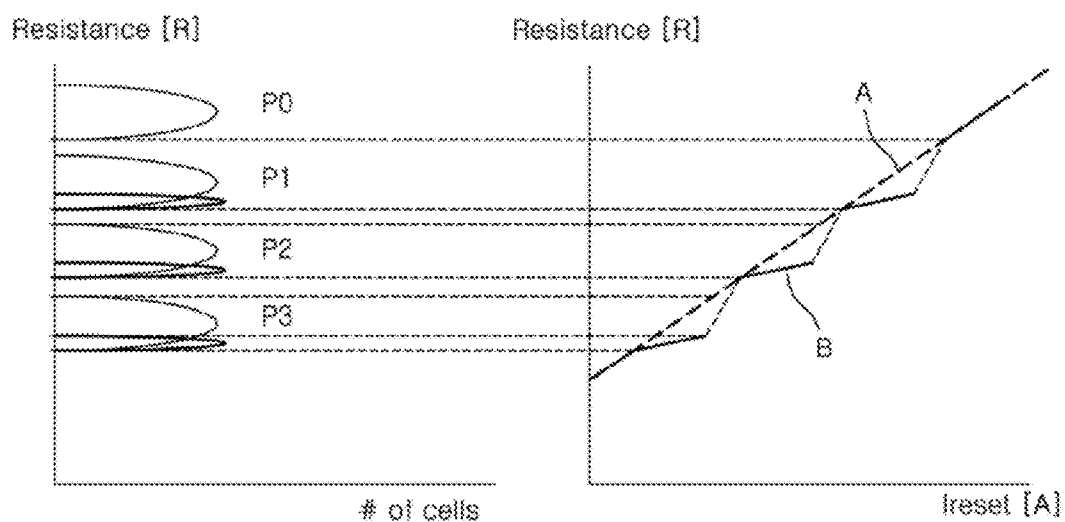


FIG.22

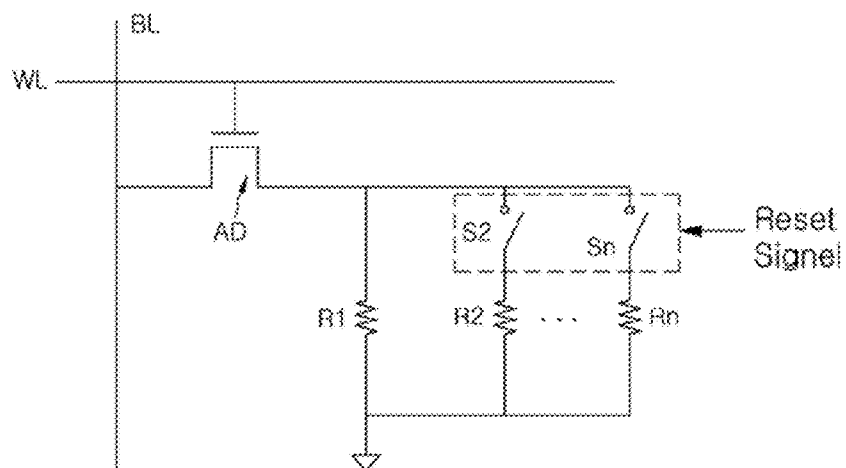


FIG.23

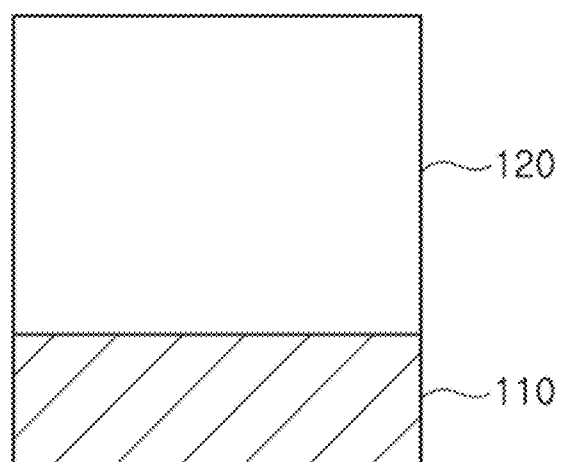


FIG.24

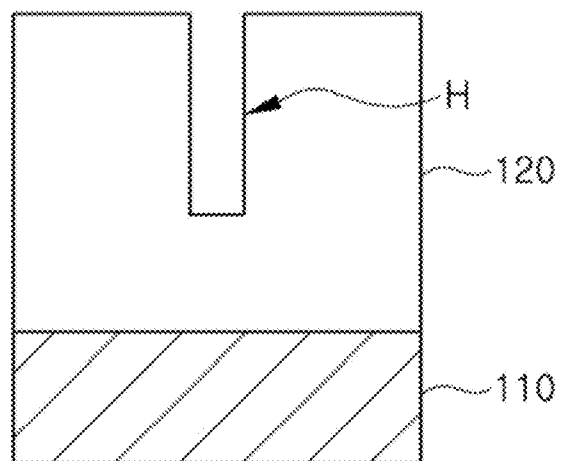


FIG.25

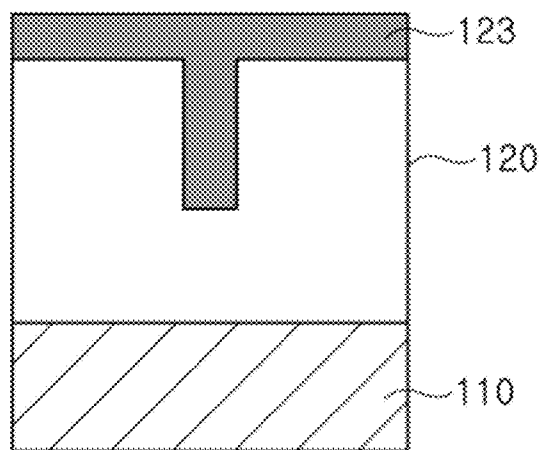


FIG.26

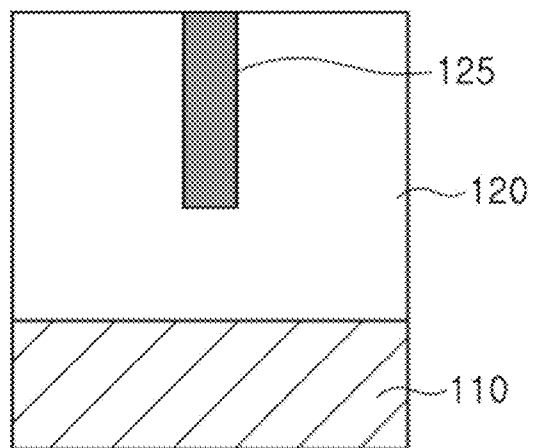


FIG.27

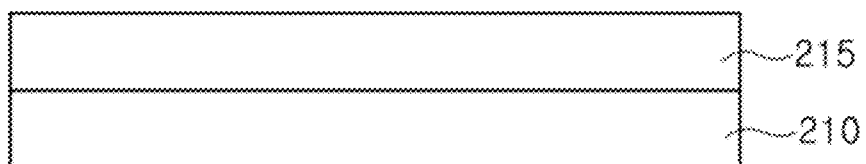


FIG.28

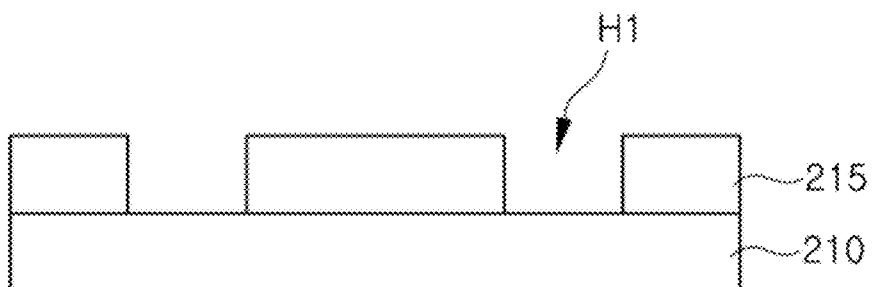


FIG.29

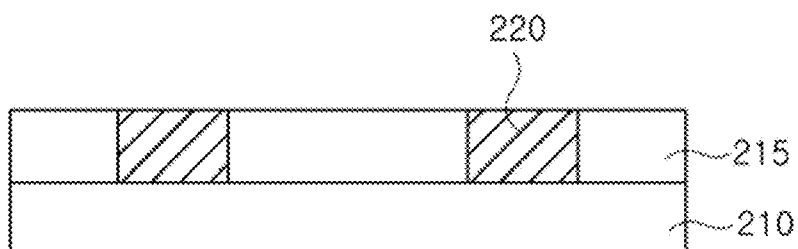


FIG.30

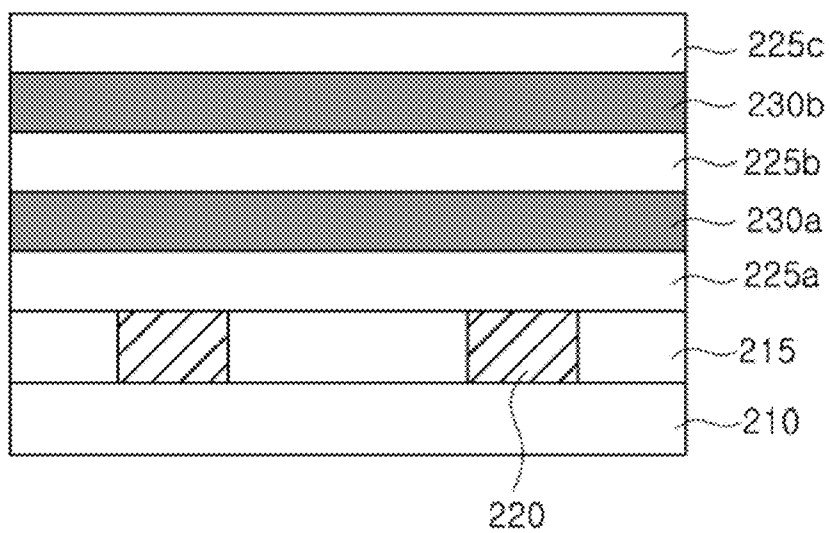


FIG.31

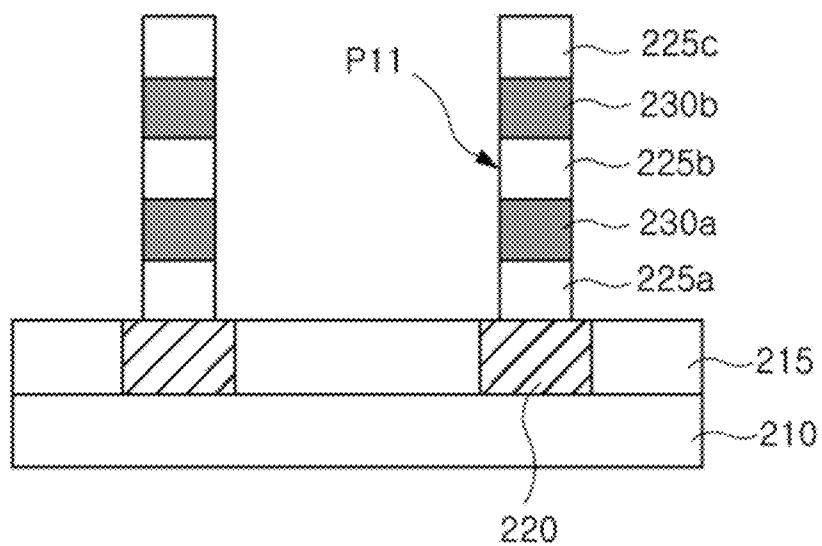


FIG.32

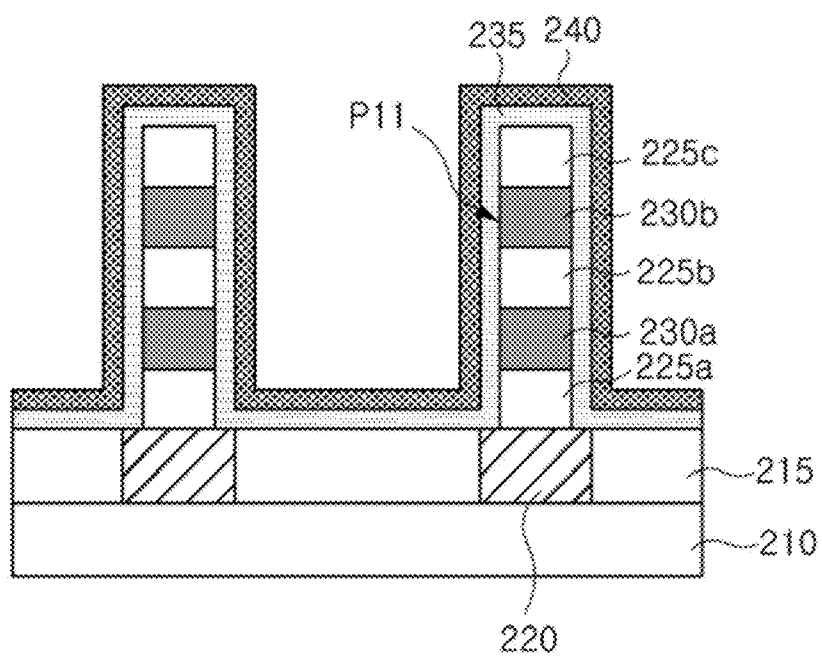


FIG.33

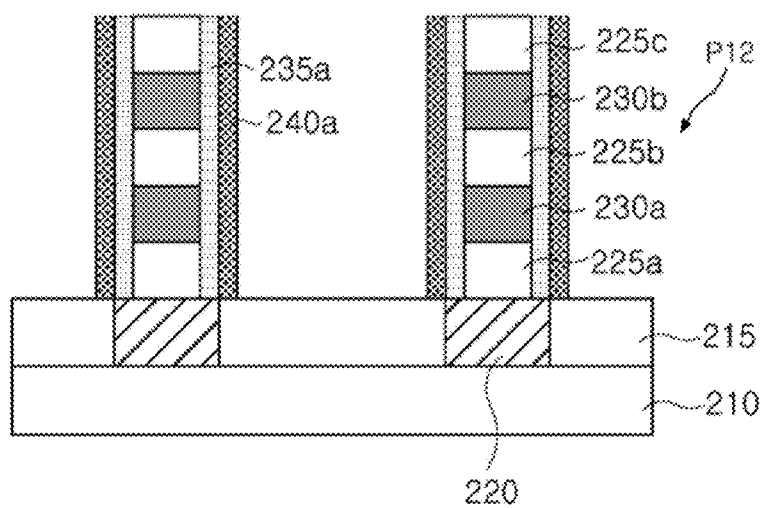


FIG.34

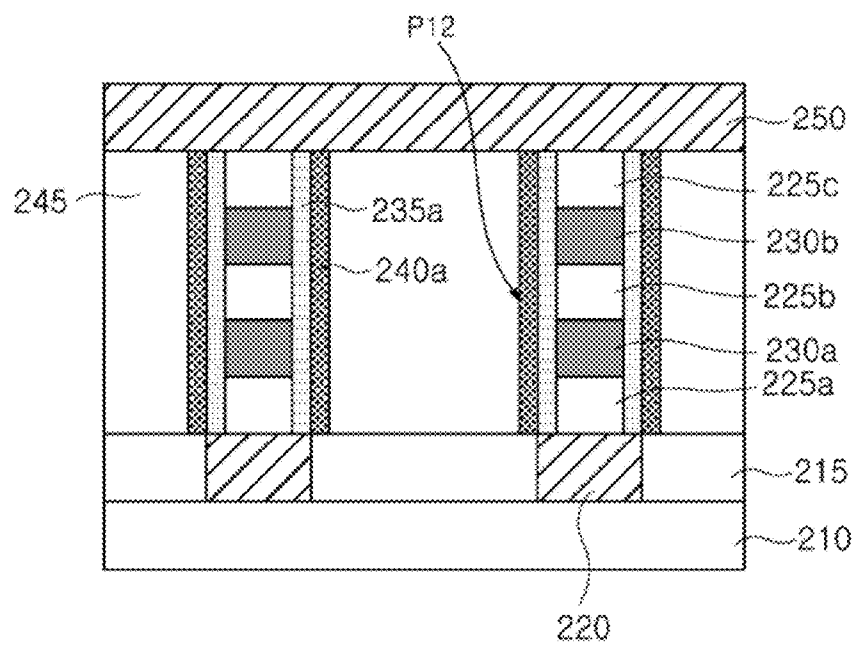


FIG.35

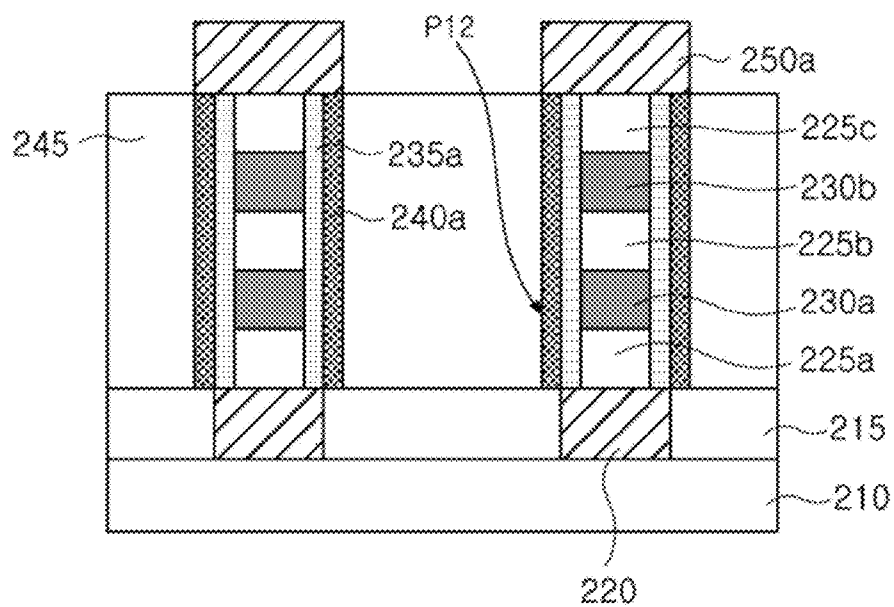
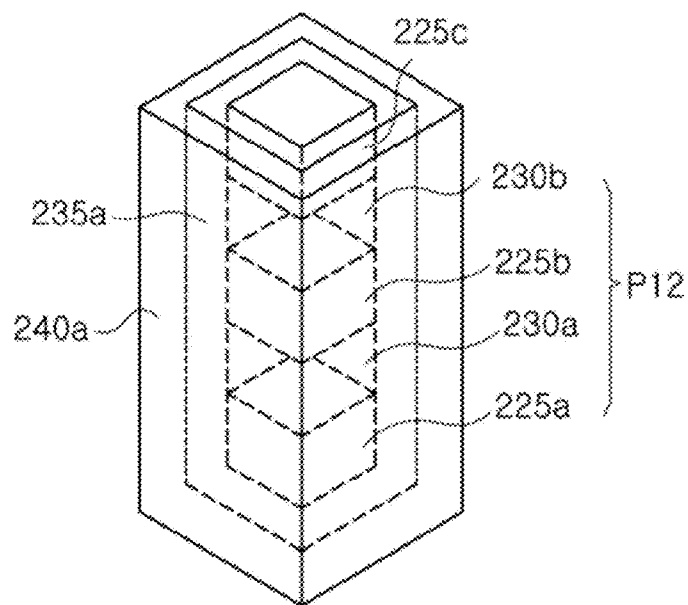


FIG.36



RESISTIVE MEMORY DEVICE AND FABRICATION METHOD THEREOF

CROSS-REFERENCES TO RELATED APPLICATION

[0001] This application claims priority under 35 U.S.C. 119(a) to Korean application No. 10-2014-0166605, filed on Nov. 26, 2014, which is incorporated by reference in its entirety as set forth in full.

BACKGROUND

[0002] 1. Technical Field

[0003] The inventive concept relates to a semiconductor integrated circuit device, and more particularly, to a resistive memory device and a fabrication method thereof.

[0004] 2. Related Art

[0005] With the rapid development of IT technology, next-generation memory devices with ultra-high speed, large capacity, or the like, which are suitable for mobile information communication systems and apparatuses for wirelessly processing large capacity of information, are needed. The next-generation memory devices require nonvolatile characteristics of general flash memory devices, high-speed operation characteristics of static random access memories (SRAMs), and high integration of dynamic RAMs (DRAMs). Additionally, the next generation memory devices need to have lower power consumption. Research has been done comparing devices with good power consumption, good data retention and write/read characteristics with general memory devices, such as ferroelectric RAMs (FRAMs), magnetic RAMs (MRAMs), phase-change RAMs (PCRAMs), or nano floating gate memories. Among the next-generation memory devices, the PCRAMs have a simple structure, can be fabricated in low costs, and operate in high speed. Thus, the PCRAMs are being actively used as the next-generation semiconductor memory devices.

[0006] The PCRAMs include a phase-change layer having a crystalline state that is changed according to heat generated by an applied current. A chalcogenide compound Ge—Sb—Te (GST) consisting of germanium (Ge), antimony (Sb), and tellurium (Te) have been mainly used as the phase-change layer applied to the current PCRAMs. The crystalline state of the phase-change layer such as GST is changed by the heat generated according to the intensity and application time of the applied current. The phase-change layer has high resistivity in an amorphous state and low resistivity in a crystalline state. Thus the phase-change layer may be used as a data storage media of memory devices.

[0007] The phase-change of the phase-change layer from the amorphous state to the crystalline state is relatively easy due to the crystallization characteristic thereof, but a large amount of current is necessary to phase-change the phase-change layer from the crystalline state to the amorphous state. Efforts to reduce the reset current in the current PCRAMs are continuing.

SUMMARY

[0008] According to an embodiment, there is provided a resistive memory device. The resistive memory device may include a resistive layer serving as a primary current path and an insertion layer as a bypass current path in a reset mode. The insertion layer may have a resistance value smaller than that

of the resistive layer of an amorphous state and greater than that of the resistive layer of a crystalline state.

[0009] According to an embodiment, there is provided a resistive memory device. The resistive memory device may include a lower electrode, a resistive layer formed over the lower electrode and serving as a primary current path; an upper electrode formed over the resistive layer, and an insertion layer serving as a bypass current path between the upper electrode and the lower electrode. The insertion layer includes a vertical insertion layer extending in a direction perpendicular to an upper surface of the lower electrode, a horizontal insertion layer extending in a direction parallel to the upper surface of the lower electrode, or both.

[0010] According to an embodiment, there is provided a method of fabricating a resistive memory device. The method may include forming a lower electrode, forming a variable resistor structure including an insertion layer over the lower electrode, and forming an upper electrode over the variable resistor structure. The insertion layer forms a bypass current path in a reset mode and the bypass current path extends in a direction perpendicular to an upper surface of the lower electrode, in a direction parallel to the upper surface of the lower electrode, or both.

[0011] These and other features, aspects, and embodiments are described below in the section entitled “DETAILED DESCRIPTION”.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The above and other aspects, features and other advantages of the subject matter of the present disclosure will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0013] FIG. 1 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0014] FIG. 2 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 1 to an amorphous state;

[0015] FIG. 3 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0016] FIG. 4 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 3 to an amorphous state;

[0017] FIG. 5 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0018] FIG. 6 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 5 to an amorphous state;

[0019] FIG. 7 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0020] FIG. 8 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 7 to an amorphous state;

[0021] FIG. 9 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0022] FIG. 10 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 9 to an amorphous state;

[0023] FIG. 11 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0024] FIG. 12 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 11 to an amorphous state;

[0025] FIG. 13 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0026] FIG. 14 is a cross-sectional view illustrating current flow in phase-change of the resistive memory device of FIG. 13 to an amorphous state;

[0027] FIG. 15 is a schematic cross-sectional view illustrating a resistive memory device according to an embodiment;

[0028] FIG. 16 is a cross-sectional view illustrating a structure of the resistive memory device of FIG. 15 at a state in which the resistive layer is partially transformed into an amorphous state;

[0029] FIG. 17A is a cross-sectional view illustrating current flow of the resistive memory device of FIG. 16;

[0030] FIG. 17B is an equivalent circuit diagram of the resistive memory device shown in FIG. 17A;

[0031] FIG. 18 is a cross-sectional view illustrating a structure of the resistive memory device of FIG. 15 at a state in which the resistive layer is completely transformed into an amorphous state;

[0032] FIG. 19A is a cross-sectional view illustrating current flow of the resistive memory device of FIG. 18;

[0033] FIG. 19B is an equivalent circuit diagram of the resistive memory device shown in FIG. 19A;

[0034] FIG. 20 is a graph illustrating resistance distribution in a resistive memory cell and a resistance change in a reset mode according to an embodiment;

[0035] FIG. 21 is a graph illustrating resistance distribution in a resistive memory cell and a resistance change in a reset mode according to another embodiment;

[0036] FIG. 22 is an equivalent circuit diagram illustrating a resistive memory cell according to an embodiment;

[0037] FIGS. 23 to 26 are cross-sectional views illustrating a method of fabricating a resistive memory device according to an embodiment;

[0038] FIGS. 27 to 35 are cross-sectional views illustrating a method of fabricating a resistive memory device according to an embodiment; and

[0039] FIG. 36 is a perspective view illustrating a resistive memory device according to an embodiment.

DETAILED DESCRIPTION

[0040] Hereinafter, exemplary embodiments will be described in greater detail with reference to the accompanying drawings. Exemplary embodiments are described herein with reference to cross-sectional illustrations that are schematic illustrations of exemplary embodiments (and intermediate structures). As such, variations from the shapes of the illustrations as a result of, for example, manufacturing techniques and/or tolerances, are to be expected. Thus, exemplary embodiments should not be construed as limited to the particular shapes of regions illustrated herein but may include deviations in shapes that result, for example, from manufacturing. In the drawings, lengths and sizes of layers and regions may be exaggerated for clarity. Like reference numerals in the drawings denote like elements. It is also understood that when a layer is referred to as being “on” another layer or substrate, it can be directly on the other layer or substrate, or intervening layers may also be present.

[0041] The inventive concept is described herein with reference to cross-section and/or plan illustrations that are schematic illustrations of exemplary embodiments of the inventive concept. However, the embodiments of the inventive concept described should not be construed as limiting the inventive concept. Although several embodiments of the

inventive concept will be shown and described, it will be appreciated by those of ordinary skill in the art that changes may be made in these exemplary embodiments without departing from the principles and spirit of the inventive concept.

[0042] Referring to FIGS. 1 and 2, a resistive memory cell may include a lower electrode 110 formed on a base layer (not shown). The base layer may be a layer including a switching device (not shown) or a semiconductor substrate including a switching device (not shown).

[0043] A resistive layer 120 having at least one current path may be formed on the lower electrode 110. For example, a resistance change region, that is, a phase change region (“PC”), may be configured to generate at least one current path I1 parallel to or perpendicular to an upper surface of the lower electrode 110 or an upper surface of the resistive layer 120. The resistance change region PC may include the resistive layer 120 and an insertion layer 125 formed in the resistive layer 120. The insertion layer 125 may have a certain width and may be formed in the resistive layer 120 to have a plug shape. In the embodiment, when measured from the upper surface of the resistive layer 120, a thickness, which is a vertical length of the insertion layer 125, may be smaller than that of the resistive layer 120.

[0044] The resistive layer 120 may include, for example, a PCMO ($\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$) layer wherein x is a stoichiometric number of from about 0.05 to about 0.95 (Examples of the stoichiometric number for PCMO include, but are not limited to, $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$, $\text{Pr}_{0.5}\text{Ca}_{0.5}\text{MnO}_3$, and $\text{Pr}_{0.67}\text{Ca}_{0.33}\text{MnO}_3$) for a resistive RAM (ReRAM), a chalcogenide layer for a PCRAM, a magnetic layer for a MRAM, a magnetization reversal device layer for a spin-transfer torque magnetoresistive RAM (STTMRAM), or a polymer layer for a polymer RAM (PoRAM). The insertion layer 125 may include a material having a resistance value smaller than that of the resistive layer 120 when the resistive layer 120 is in an amorphous state and greater than that of the resistive layer 120 when the resistive layer 120 is in a crystalline state. The insertion layer 125 may include one of a conductive layer, a nitride material layer having conductivity, and an oxide material layer having conductivity. For example, the insertion layer 125 may include aluminum nitride (AlN), boron nitride (BN), alumina (Al_2O_3), tantalum nitride (TaN), tungsten (W), tungsten nitride (WN), cobalt tungsten (CoW), nickel tungsten (NiW), yttrium oxide (YiOx), or a combination thereof.

[0045] An upper electrode 140 is formed on the resistance change region (PC).

[0046] When a reset voltage for changing the resistive layer 120 into a reset state is applied, a portion of the resistive layer 120 transforms into an amorphous state due to heat applied from the lower electrode 110. Referring to FIG. 2, the resistive layer 120 may have two or more resistive states, for example, a crystalline resistive layer 120a and an amorphous resistive layer 120b. The transformation of the resistive layer 120 into an amorphous state starts from the center of the resistive layer 120 then proceeds outward. As shown in FIG. 2, the amorphization of the resistive layer 120 starts from a central portion of the resistance change region PC, that is, the resistive layer 120 then proceeds gradually outward.

[0047] When the current path I1 generated in the resistance change region PC moves along the crystalline resistive layer 120a from the upper electrode 140 in a vertical direction, the current path I1 reaches the amorphous resistive layer 120b. Then the current path I1 takes a bypass formed along the

insertion layer **125** having a smaller resistance value than that of the amorphous resistive layer **120b** in a horizontal direction. When the current path **11** moving along the insertion layer **125** reaches the crystalline resistive layer **120a** again, the current path **11** flows back onto the original current path which is along the crystalline resistive layer **120a** that has a smaller resistance value than that of the insertion layer **125**.

[0048] The current path **11** is changed by the insertion layer **125**, and the current amount and a reset resistance may change accordingly. Thus, a ratio (slope) of the resistance of the resistance change region **PC** to a reset current is changed. That is, an additional resistance level is created which is defined between the set resistance and the reset resistance of the resistive layer **120**. Therefore, the resistive memory cell can have multi-level resistance.

[0049] Referring to FIGS. **3** and **4**, when measured from the upper surface of the resistive layer **120** an insertion layer **125a** may have the same depth or vertical length, as the thickness of a resistive layer **120**.

[0050] Under this structure, when a current path **12** reaches an amorphous resistive layer **120b**, the current path **12** may change from the resistive layer **120b** to the insertion layer **125a**. As a result, a bypass passing through the insertion layer **125a** is formed. The insertion layer **125a** may be formed to pass through the resistive layer **120**.

[0051] As illustrated in FIG. **5**, an insertion layer **126** may be formed in a resistance change region **PC**, and surround the resistive layer **120**.

[0052] When a reset voltage for changing the resistance change region **PC** into a reset state is applied, the amorphization slowly starts from the resistive layer **120** located in the center of the resistance change region **PC**.

[0053] As illustrated in FIG. **6**, a current path **13** is formed from an upper electrode **140** to the lower electrode **110** through the resistive layer **120** shown in FIG. **5**, and the insertion layer **126**. Specifically, the current path **13** flows through the crystalline resistive layer **120a**. When the current path **13** reaches an amorphous resistive layer **120b**, the current path **13** takes a bypass which is formed through the insertion layer **126**, rather than staying on the amorphous resistive layer **120b**. When the current path **13** moving along the insertion layer **126** reaches a crystalline resistive layer **120a** again, the current path **13** returns back to the crystalline resistive layer **120a**.

[0054] Referring to FIG. **7**, an insertion layer **126a** may surround a resistance change region **PC**. As illustrated in FIG. **8**, when a current path **14** extending from an upper electrode **140** reaches an amorphous resistive layer **120b**, the current **14** takes a bypass which is formed along the insertion layer **126a**. The insertion layer **126a** has a smaller resistance value than that of the amorphous resistive layer **120b**. Then, the current **14** flows through the insertion layer **126a**. When the current path **14** reaches a crystalline resistive layer **120a** again, the current path **14** gets out of the bypass and returns back to the crystalline resistive layer **120a** again.

[0055] Referring to FIGS. **9** and **11**, a plurality of insertion layers **125a-1**, **125a-2**, and **125a-3** each having a plug shape and each penetrating a resistive layer **120** may be formed in the resistive layer **120**.

[0056] Through the formation of the plurality of insertion layers **125a-1**, **125a-2**, and **125a-3**, as illustrated in FIGS. **10** and **12**, a plurality of amorphous resistive layers **120b** may be formed in one resistance change region **PC**. Thus, a plurality of current paths **15** and **16** are generated in a horizontal

direction and a vertical direction in the resistance change region **PC**. Due to the various types of current paths **15** and **16**, a resistance slope may vary, and a plurality of resistance levels may be obtained.

[0057] Referring to FIG. **13**, an insertion layer **127** may be formed in parallel to an upper surface of a lower electrode **110**. As illustrated in FIG. **14**, through the formation of the insertion layer **127**, a current path **17** bypasses an amorphous resistive layer **120b**. That is, the current path **17** is formed along the insertion layer **127**, rather than along the amorphous resistive layer **120b**. Then, the current path **17** is formed through the insertion layer **127** and the crystalline resistive layer **120a**.

[0058] As illustrated in FIG. **15**, a resistance change region **PC** may include a resistive layer **120**, a vertical insertion layer **128**, and a horizontal insertion layer **129**.

[0059] The resistive layers **120** may be formed in the resistance change region in a cylinder shape. The vertical insertion layers **128** may be formed between the resistive layers **120** in a cylinder shape. The vertical insertion layers **128** may be formed perpendicular to an upper surface of a lower electrode **110**. The horizontal insertion layer **129** may extend between the vertical insertion layers **128**. There may be at least one or more horizontal insertion layer **129** which may extend substantially in parallel to the upper surface of the lower electrode **110**.

[0060] Insulating layers **135** may be interposed between the horizontal insertion layers **129**, between the horizontal insertion layer **129** and the lower electrode **110**, and between the horizontal insertion layer **129** and an upper electrode layer **140**.

[0061] In an embodiment, the vertical insertion layer **128** may have substantially the same resistance value as the horizontal insertion layer **129**. In another embodiment, the horizontal insertion layer **129** may have a smaller resistance value than the vertical insertion layer **128**. For example, when a thickness of the horizontal insertion layer **129** is larger than a width of the vertical insertion layer **128**, the vertical insertion layer **128** and the horizontal insertion layer **129** may be formed of the same material. When the thickness of the horizontal insertion layer **129** is equal to the width of the vertical insertion layer **128**, the horizontal insertion layer **129** may be formed of a material having a smaller resistance value than the vertical insertion layer **128**.

[0062] Further, the vertical and horizontal insertion layers **128** and **129** may have resistance values smaller than that of an amorphous resistive layer (see **120b-1** and **120b-2** of FIGS. **16** to **19**) and greater than that of a crystalline resistive layer **120a**. The vertical and horizontal insertion layers **128** and **129** may be designed in such a manner that in a reset mode current chooses the path through the vertical and horizontal insertion layers **128** and **129** rather than choosing the path through the amorphous resistive layer **120b-1** and **120b-2**. As described above, the vertical and horizontal insertion layers **128** and **129** may include one of a conductive layer, a nitride material layer having conductivity, and an oxide material layer having conductivity. For example, the vertical and horizontal insertion layers **128** and **129** may include AlN , BN , Al_2O_3 , TaN , W , WN , CoW , NiW , YiOx , where x is an integer, or a combination thereof.

[0063] As illustrated in FIG. **16**, when an initial reset voltage is supplied to the resistive memory cell having the above-described configuration, phase-change starts from a central portion of the resistive layer **120**. The amorphous resistive

layer **120b-1** is formed according to a supply of the initial reset voltage. The amorphous resistive layer **120b-1** according to the initial reset voltage may occupy a small part of the entire resistive layer **120**.

[0064] An amorphous layer has a greater resistance value than a crystalline layer. Therefore, as illustrated in FIG. 17A, a current path **18** traveling from the upper electrode **140** toward the lower electrode **110** may move along the crystalline resistive layer **120a** and then bypass the initial amorphous resistive layer **120b-1** toward the vertical insertion layer **128** having a relatively small resistance value. Thus, the current path **18** is formed in a vertical insertion layer **128** corresponding to the initial amorphous resistive layer **120b-1**. Since the initial amorphous resistive layer **120b-1** occupies a relatively small area in the resistive layer **120** as compared with a length of the entire resistive layer **120**, the current path **18** may not be bypassed toward the horizontal insertion layer **129**. Rather the current path **18** may return toward the crystalline resistive layer **120a**. As the current path **18** is bypassed to the vertical insertion layer **128** having a smaller resistance value than the initial amorphous resistive layer **120b-1**, the slope of the resistance according to the current may be varied. An equivalent resistor for the current path **18** is illustrated in FIG. 17B.

[0065] As illustrated in FIG. 18, when the reset voltage is sufficiently supplied, the resistive memory cell is completely reset. Thus, most of the resistive layer **120** becomes the amorphous resistive layer **120b-2**, and an edge portion of the resistive layer **120** is maintained in the crystalline resistive layer **120a**.

[0066] As illustrated in FIG. 19A, a current path **19** extending from the upper electrode **140** bypasses the amorphous resistive layer **120b-2** and chooses an alternative path passing through the vertical insertion layer **128** and/or the horizontal insertion layer **129** which have a smaller resistance value than the amorphous resistive layer **120b-2**. As described above, the current path **19** takes the path passing through the horizontal insertion layer **129** when the resistance value of the horizontal insertion layer **129** is smaller than that of the amorphous resistive layer **120b-2**, or when the thickness of the horizontal insertion layer **129** is greater than the width of the vertical insertion layer **128**.

[0067] Since a length of the current path **19** passing through the insertion layers **128** and **129** is greater than that of the current path **18** of FIG. 17A, the resistance value according to the current and the slope of the resistance value may be varied. An equivalent resistor for the current path **19** is illustrated in the right portion of FIG. 19B. In the complete amorphous state of the resistive layer **120**, the length of the current path extending through resistors is longer than in the initial amorphous state. Comparing the current path **18** of FIG. 17A and the current path **19** shown in FIG. 19A, an equivalent resistor path varies as the amorphous state proceeds, and the resistance value varies accordingly.

[0068] Through the formation of various types of insertion layers, as shown in FIG. 20, resistance distribution of the resistive memory cell and the resistance according to the current may vary. That is, through the formation of the insertion layers capable of forming a current bypass, additional resistance distribution **230** is generated in addition to general resistance distributions **200** (Reset) and **210** (Set). Since the additional resistance distribution **230** has a different peak and amplitude from the general resistance distributions **200** and **210**, data for the additional resistance distribution **230** can be

read separately and distinctively from resistance distributions **200** and **210**. In the right 2) drawing of FIG. 20, "A" indicates the slope of the resistance when the insertion layer is not included, and "B" indicates the slope of the resistance when the insertion layer is included. Therefore, since the current path varies according to the intervention of the insertion layer, the effective resistance value and the slope of the resistance varies.

[0069] When a plurality of insertion layers are intervened as illustrated in FIGS. 17A to 19B, a plurality of current paths are formed. Therefore, as illustrated in FIG. 21, a plurality of resistance distributions may be formed in addition to resistance distribution **P3** (SET) and resistance distribution **P0** (RESET). Thus, a multi-level cell may be implemented.

[0070] Furthermore, as shown in FIG. 22 when the various types of insertion layers are intervened as described above, the resistive memory cell may be implemented into an equivalent circuit.

[0071] Referring to FIG. 22, the resistive memory cell may include an access device **AD** coupled to a word line **WL** and a bit line **BL**, and a first resistor **R1** and a second resistor **R2** each coupled to the access device **AD**. The first resistor **R1** may be formed by a resistor of a resistive layer and may substantially store data. The second resistor **R2** may be formed by a resistor of at least one insertion layer. Since a resistance value of the resistor **R2** may vary according to a type and structure of the insertion layer, the resistor **R2** may be configured in various forms. The resistance value in a set state may be determined by a resistance value of a variable resistance material in a crystalline state. The resistance value in a reset state may be determined by a sum of a resistance value of the variable resistance material in an amorphous state and resistance values of the insertion layers. Thus, a resistive memory cell having various resistance distributions and resistance values may be formed.

[0072] A method of fabricating a resistive memory device including a plug-shaped vertical insertion layer according to an embodiment will be described with reference to FIGS. 23 to 26.

[0073] Referring to FIG. 23, a lower electrode **110** is formed. A resistive layer **120** is formed on the lower electrode **110**.

[0074] Referring to FIG. 24, a predetermined portion of the resistive layer **120** is etched to form a hole **H**. The hole **H** may have a depth smaller than a thickness of the resistive layer **120** when measured from the upper surface of the resistive layer **120**, as illustrated in FIG. 1. In another embodiment, the hole **H** may have a depth equal to the thickness of the resistive layer **120** when measured from the upper surface of the resistive layer **120**, as illustrated in FIG. 3. One hole **H** may be formed per memory cell as illustrated in FIGS. 1 and 3, or a plurality of holes **H** may be formed per memory cell as illustrated in FIGS. 7, 9, and 11.

[0075] Referring to FIG. 25, an insertion layer material **123** is formed on the resistive layer **120** to fill in the hole **H**. Referring to FIG. 26, the insertion layer material **123** is planarized to expose the upper surface of the resistive layer **120**, forming an insertion layer **125**. Then, although not shown in FIG. 26, an upper electrode may be formed on the insertion layer **125** and the resistive layer **120**.

[0076] A method of fabricating a resistive memory device according to another embodiment will be described with reference to FIGS. 27 to 30.

[0077] Referring to FIG. 27, a first interlayer insulating layer 215 is formed on a semiconductor substrate 210. The first interlayer insulating layer 215 insulates lower electrodes, which will be formed in a subsequent process, from each other. The first interlayer insulating layer 215 may include a silicon nitride layer having good heat-endurance.

[0078] Referring to FIG. 28, a predetermined portion of the first interlayer insulating layer 215 is patterned to form a hole H1. For example, a lower electrode may be formed in the hole H1, to constitute one resistive memory cell.

[0079] Referring to FIG. 29, a conductive layer fills in the inside of the hole H1 shown in FIG. 28. The conductive layer is planarized to expose the first interlayer insulating layer 215 to form a lower electrode 220 in the hole H1.

[0080] Referring to FIG. 30, an insulating layer and an insertion layer material are alternately stacked on the first interlayer insulating layer 215 in which the lower electrode 220 is formed. The reference numerals 225a to 225c denote a first insulating layer, a second insulating layer, and a third insulating layer, respectively. The reference numerals 230a and 230b denote a first insertion layer material and a second insertion layer material, respectively. The first insertion layer material 230a and the second insertion layer material 230b may have substantially the same resistance value. The first to third insulating layers 225a, 225b, and 225c each may include a silicon oxide layer, a silicon nitride layer, or a silicon oxynitride layer. The first and second insertion layer materials 230a and 230b each may include a conductive layer, a nitride material layer having conductivity, an oxide material layer having conductivity, or a combination thereof. For example, the first and second insertion layer materials 230a and 230b may include AlN, BN, Al₂O₃, TaN, W, WN, CoW, NiW, or Y₂O₃, where x is an integer.

[0081] Referring to FIG. 31, a stack including the third insulating layer 225c, the second insertion layer material 230b, the second insulating layer 225b, the first insertion layer material 230a, and the first insulating layer 225a are patterned to form a preliminary resistor structure P11. The preliminary resistor structure P11 may be located on the lower electrode 220. The width of the preliminary resistor structure P11 may be smaller than the width of the lower electrode 220.

[0082] Referring to FIG. 32, a third insertion layer material 235 and a resistive layer material 240 are sequentially formed on the first interlayer insulating layer 215 and the preliminary resistor structure P11. The third insertion layer material 235 and the resistive layer material 240 may be formed with a uniform thickness. For example, the third insertion layer material 235 may be formed to have the same thickness as either the first or second insertion layer materials 230a and 230b. In this case, the third insertion layer material 235 may have a resistance value greater than either the first or second insertion layer materials 230a, 230b. The third insertion layer material 235 may be formed to have a thickness smaller than either the first or second insertion layer materials 230a, 230b. In this case, the first to third insertion layer materials 230a, 230b, and 235 may have substantially the same resistance value. Furthermore, the first to third insertion layer materials 230a, 230b, and 235 may have resistance values substantially smaller than that of the resistive layer material 240 in an amorphous state.

[0083] The resistive layer material 240 may include, for example, a PCMO (Pr_{1-x}Ca_xMnO₃) layer wherein x is a stoichiometric number of from about 0.05 to about 0.95 (Ex-

amples of the stoichiometric number for PCMO include, but are not limited to, Pr_{0.7}Ca_{0.3}MnO₃, Pr_{0.5}Ca_{0.5}MnO₃, and Pr_{0.67}Ca_{0.33}MnO₃) for a ReRAM, a chalcogenide layer for a PCRAM, a magnetic layer for a MRAM, a magnetization reversal device layer for a STTMRAM, or a polymer layer for a PoRAM.

[0084] Referring to FIG. 33, the resistive layer material 240 and the third insertion layer material 235 are anisotropically etched to expose the first interlayer insulating layer 215, forming a resistive layer 240a and a third insertion layer 235a each in a spacer shape. As a result, a variable resistor structure P12 is formed on the lower electrode 220.

[0085] Referring to FIG. 34, a second interlayer insulating layer 245 fills between variable resistor structures P12. The variable resistor structures P12 may be electrically insulated by the second interlayer insulating layer 245. An upper electrode material layer 250 is formed on the second interlayer insulating layer 245 and the variable resistor structure P12. The second interlayer insulating layer 245 may include a silicon nitride layer and it is desirable that the silicon nitride layer has good heat-endurance.

[0086] Referring to FIG. 35, the upper electrode material layer 250 is patterned to form an upper electrode 250a.

[0087] As illustrated in FIG. 36, in the resistive memory device which is substantially in a ring shape, at least one insertion layer 230a, 230b, and 235a is formed inside the resistive layer 240a. A bypass current is formed through the insertion layers 230a, 230b, and 235a in a vertical direction and a horizontal direction. In an embodiment, the insertion layers 230a, 230b, and 235a may include a vertical insertion layer 235a formed in the resistive layer 240a in a cylinder shape, and at least one horizontal insertion layer 230a, 230b extending from a first inner sidewall of the vertical insertion layer 235a to a second inner sidewall of the vertical insertion layer 235a.

[0088] Accordingly, when the resistive layer 240a undergoes a phase-change into an amorphous state, current may flow via the bypass path formed through the vertical and/or horizontal insertion layers 235a and/or 230a and 230b which have a relatively small resistance value. Thus, a total effective resistance value of the entire variable resistor structure P12 may be varied. The variable resistor structure P12 may have various resistance values according to the resistor path, and a multi-level memory cell may be realized.

[0089] The above embodiments are illustrative and not limitative, that is, the embodiments are not limited to any specific type of semiconductor device.

What is claimed is:

1. A semiconductor integrated circuit device comprising: a resistive layer serving as a primary current path; and an insertion layer serving as a bypass current path in a reset mode, wherein the insertion layer has a resistance value smaller than that of the resistive layer in an amorphous state and greater than that of the resistive layer in a crystalline state.
2. The semiconductor integrated circuit device of claim 1, wherein the insertion layer is formed in the resistive layer and extends in a direction perpendicular to an upper surface of the resistive layer.
3. The semiconductor integrated circuit device of claim 2, wherein a depth of the insertion layer is smaller than a thickness of the resistive layer when measured from the upper surface of the resistive layer.

4. The semiconductor integrated circuit device of claim 2, wherein the insertion layer passes through the resistive layer.

5. The semiconductor integrated circuit device of claim 1, wherein the insertion layer surrounds the resistive layer.

6. The semiconductor integrated circuit device of claim 1, wherein the insertion layer is formed in the resistive layer and extends in a direction substantially parallel to an upper surface of the resistive layer.

7. The semiconductor integrated circuit device of claim 1, wherein the bypass current path includes a vertical path extending in a direction perpendicular to an upper surface of the resistive layer, a horizontal path extending in a direction parallel to the upper surface of the resistive layer, or both.

8. The semiconductor integrated circuit device of claim 7, wherein the insertion layer includes:

- a vertical insertion layer formed in a ring shape and surrounded by the resistive layer; and
- a horizontal insertion layer extending from a first inner sidewall of the vertical resistive layer to a second inner sidewall of the vertical resistive layer.

9. The semiconductor integrated circuit device of claim 8, wherein a thickness of the horizontal insertion layer is greater than a width of the vertical insertion layer.

10. The semiconductor integrated circuit device of claim 8, wherein a resistance value of the horizontal insertion layer is smaller than that of the vertical insertion layer.

11. The semiconductor integrated circuit device of claim 1, further comprising:

- a lower electrode provided under the resistive layer and the insertion layer.

12. The semiconductor integrated circuit device of claim 11, further comprising:

- an upper electrode provided over the resistive layer and the insertion layer.

13. A semiconductor integrated circuit device comprising:
a lower electrode;
a resistive layer formed over the lower electrode and serving as a primary current path;
an upper electrode formed over the resistive layer; and
an insertion layer serving as a bypass current path between the upper electrode and the lower electrode,
wherein the insertion layer includes a vertical insertion layer extending in a direction perpendicular to an upper surface of the lower electrode, a horizontal insertion layer extending in a direction parallel to the upper surface of the lower electrode, or both.

14. The semiconductor integrated circuit device of claim 13, wherein the insertion layer is formed in the resistive layer and extends in the direction perpendicular to the upper surface of the resistive layer.

15. The semiconductor integrated circuit device of claim 14, wherein a depth of the insertion layer is smaller than a thickness of the resistive layer when measured from the upper surface of the resistive layer.

16. The semiconductor integrated circuit device of claim 14, wherein the insertion layer passes through the resistive layer.

17. The semiconductor integrated circuit device of claim 13, wherein the insertion layer surrounds the resistive layer.

18. The semiconductor integrated circuit device of claim 13, wherein the insertion layer is formed in the resistive layer and extends in the direction substantially parallel to the upper surface of the resistive layer.

19. The semiconductor integrated circuit device of claim 13, wherein the insertion layer includes:

- a vertical insertion layer formed in a ring shape and surrounded by the resistive layer; and
- a horizontal insertion layer extending from a first inner sidewall of the vertical resistive layer to a second inner sidewall of the vertical resistive layer.

20. The semiconductor integrated circuit device of claim 19, wherein a thickness of the horizontal insertion layer is greater than a width of the vertical insertion layer.

21. The semiconductor integrated circuit device of claim 19, wherein a resistance value of the horizontal insertion layer is smaller than that of the vertical insertion layer.

22. A method of fabricating a semiconductor integrated circuit device, the method comprising:

- forming a lower electrode;
 - forming a variable resistor structure including an insertion layer over the lower electrode; and
 - forming an upper electrode over the variable resistor structure,
- wherein the insertion layer forms a bypass current path in a reset mode, and
wherein the bypass current path extends in a direction perpendicular to an upper surface of the lower electrode, in a direction parallel to the upper surface of the lower electrode, or both.

23. The method of claim 22, wherein the forming of the variable resistor structure includes:

- forming a resistive layer over the lower electrode;
- forming a hole in the resistive layer; and
- forming the insertion layer in the hole.

24. The method of claim 22, wherein the forming of the variable resistor structure includes:

- alternately stacking an insulating layer and a horizontal insertion layer over the lower electrode to form a stack;
- forming a preliminary resistor structure by etching the stack;
- forming a vertical insertion layer surrounding the preliminary resistor structure; and
- forming a resistive layer surrounding the vertical insertion layer.

25. The method of claim 22, further comprising:

- forming an interlayer insulating layer between the variable resistor structure and an adjacent variable resistor structure,
- wherein the forming of the interlayer insulating layer is performed between the forming of the variable resistor structure and the forming of the upper electrode.

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