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Circuit arrangement for deriving a field synchronizing signal from an incoming signal

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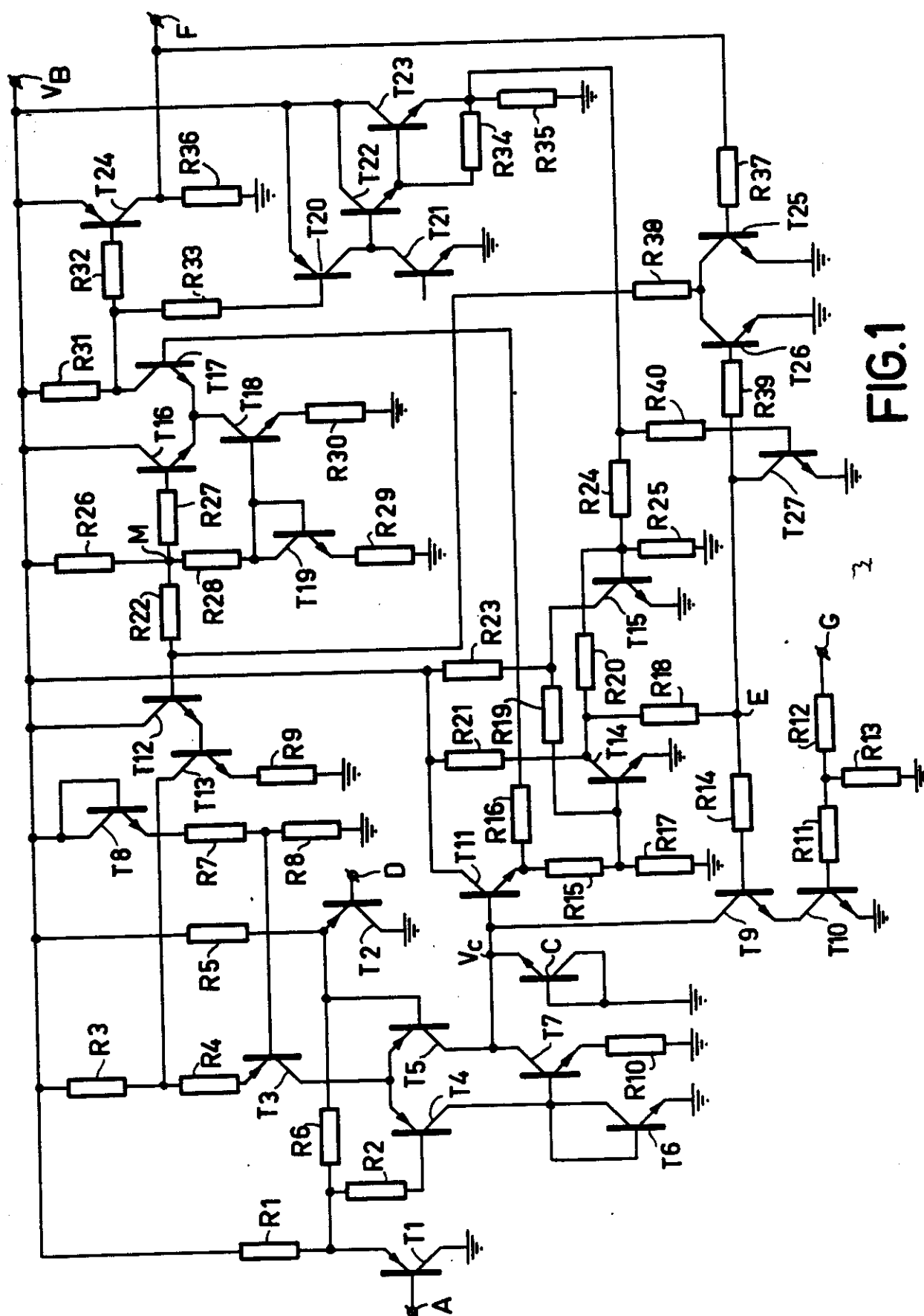.PSX

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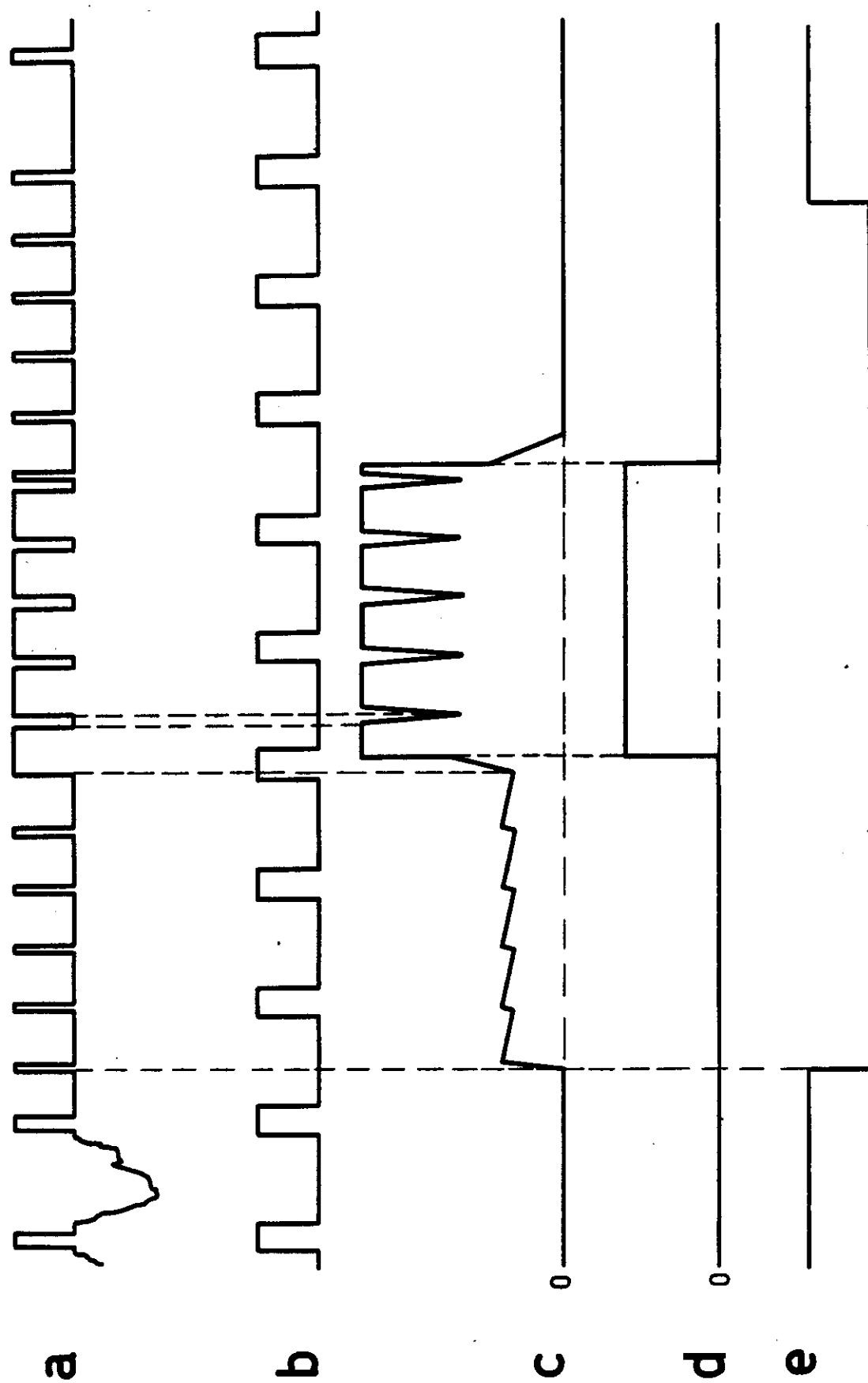
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FIG.1

2095066

a

b

c   0

d   0

e

FIG.2

"CIRCUIT ARRANGEMENT FOR DERIVING A FIELD SYNCHRONIZING SIGNAL FROM AN INCOMING SIGNAL"

The invention relates to a circuit arrangement for deriving a field synchronizing signal from an incoming signal which contains at least line synchronizing and field synchronizing pulses whose amplitude extends between a reference and a peak level, comprising

5 a signal generator for generating a signal for each pulse which has a value located between the reference and the peak level occurring in the incoming signal, said generated signal having a value which is representative of the duration of each pulse, and a comparator stage for comparing the generated signal with a threshold value.

10 Such a circuit arrangement is disclosed in United States Patent Application 3,678,199. The pulses causing the generation of a signal by the signal generator may be line synchronizing, field synchronizing and also interference pulses, the reference level of said pulses being usually only slightly different from the black level

15 of the video information. However, the threshold value has been chosen such that only the field synchronizing pulses are of a sufficiently long duration to produce a signal which exceeds the threshold value.

In this prior art circuit arrangement the threshold value must

20 be chosen to be rather high to enable a somewhat reliable distinction between a field synchronizing pulse and a different, shorter pulse. If the incoming signal contains much noise then the threshold value will, however, not always be reached, while the signal produced by the signal generator between two consecutive pulses is not zero. This

25 may cause the field synchronization to become lost. Furthermore, even in the event of little noise a hum voltage may be superposed on the television signal, which hum voltage may originate from, for example, an intermediate frequency amplifier, causing a direct current shift of the incoming signal, so that there is a risk that

30 the threshold value is not reached at the proper moment.

The invention has for its object to provide a circuit arrangement for more reliably generating the field synchronizing signal.

The invention provides a circuit arrangement of the type described in the opening paragraph which is characterized in that the circuit
5 arrangement also comprises a gate circuit for, in operation, inhibiting the generated signal from the signal generator during the occurrence of the line synchronizing pulses for which the threshold value is not reached by the generated signal from the signal generator, this gate circuit not inhibiting the generated signal when said threshold
10 value is reached by said generated signal, the circuit arrangement generating the field synchronizing signal when the generated signal from the signal generator reaches a second threshold value which is representative of a pulse duration which exceeds that corresponding to the first mentioned threshold value.
15 As with the above circuit arrangement the line synchronizing pulses have no influence during a long period on the signal produced by the signal generator, the first threshold value may be chosen rather low, that is to say corresponding to a comparatively short pulse duration, while the second threshold value, which initiates
20 the generation of the field synchronizing signal, may be chosen to be relatively high. This results in an improved reliability and an improved noise insensitivity.

The gate circuit may comprise a gate for the transmission outside the field blanking interval of pulses at the line frequency whose
25 periods of occurrence substantially include those of the line synchroniz- ing pulses and for inhibiting the transmission of said pulses at the line frequency after the generated signal from the signal generator has reached the first threshold value.

The circuit arrangement may further comprise a monostable element
30 for maintaining the gate circuit during a predetermined period after the second threshold value has been reached by the generated signal from the signal generator in the state in which the gate inhibits the transmission of the pulses at the line frequency.

The signal generator may generate during the occurrence of a
35 pulse in the incoming signal a substantially linear signal, the slope

of which is reduced after the first threshold value has been reached.

Preferably the circuit arrangement comprises a bistable element which is in a first state when the generated signal from the signal generator is lower than the first threshold value and in a second
5 state after the signal has reached the first threshold value, the second state being maintained until at least the end of the field synchronizing signal, in which second state the bistable element maintains the gate circuit in the state in which the gate inhibits the transmission of the pulses of the line frequency.
10 The features of invention will now be explained in detail, by way of non-limitative example, with reference to the accompanying drawings, in which:-

Figure 1 shows an embodiment of the circuit arrangement in accordance with the invention suitable for inclusion in an integrated
15 circuit for generating a field synchronizing signal in a television receiver, while Figure 2 shows waveforms present in the circuit arrangement of Figure 1 during operation.

An input terminal A of the circuit arrangement of Figure 1 is connected to the base of a pnp-transistor T1 the collector of which
20 is connected to ground, while the emitter is connected to the junction of a 8.2 k Ω resistor R1 and a 10k Ω resistor R2. The other end of resistor R1 is connected to the positive terminal of a supply voltage source V_B of 12 V, the negative terminal of which is connected to ground. The other end of resistor R2 is connected to the base of a
25 pnp-transistor T4 the first end of which is connected to a resistor R6 of 1.5 k Ω. The other terminal of resistor R6 is connected to the emitter of a pnp-transistor T2 and to the base of a pnp-transistor T5. The collector of transistor T2 is connected to ground, while the base is connected to an input terminal D of the circuit and the emitter to source
30 V_B via a resistor R5 of 4.3 k Ω. Terminal A is connected to a video circuit, not shown, and terminal D is connected to a d.c. voltage of 8 V.

The emitters of transistors T4 and T5 are interconnected and connected to the collector of a pnp-transistor T3, the emitter of which is connected to source V_B via two series-arranged resistors R4
35 of 22 k Ω and R3 of 1.5 k Ω, while the base is connected to the junction

of a resistor R7 of 1k Ω and a resistor R8 of 15k Ω. The other end
of resistor R7 is connected to the emitter of an npn-transistor T8,
the other end of resistor R8 being connected to ground. The collector
and the base of transistor T8 are both connected to source V_B.

5   The collector of transistor T4 is connected to the base and to
the collector of an npn-transistor T6 and to the base of an npn-
transistor T7. The emitter of transistor T6 and also a 30k Ω emitter
resistor R10 of transistor T7 are connected to ground. The collectors
of transistors T5 and T7 and also the collector of an npn-transistor

10   T9 and the emitter of a further pnp-transistor are interconnected.
The base and the collector of said further transistor are connected
to ground. As is known, during operation such a transistor behaves
as a small capacitance, in this example having a value of approximately
18pF, with respect to ground. For this reason, this transistor is

15   denoted in Figure 1 by the symbol C. In addition, the emitter of
transistor T9 is connected to the collector of an npn-transistor T10
whose emitter is connected to ground and whose base is connected to
an input terminal G via two series-arranged resistors R11 of 4.7k Ω
and R12 also of 4.7k Ω. A 4.3k Ω resistor R13 is connected between

20   the junction of said resistors and ground.

The junction point of transistors T5, T7 and T9 and of capacitor C
is also connected to the base of an npn-transistor T11. The collector
of transistor T11 is connected to voltage V_B, while the emitter is
connected to a 6.8k Ω resistor R15. The other end of resistor R15 is

25   connected to a 6.8k Ω resistor R17, to a resistor R19 also having a
value of 6.8k Ω and to the base of an npn-transistor T14. The other
terminal of resistor R17 and also the emitter of transistor T14 are
connected to ground. Via a 15k Ω resistor R18 and a 4.7k Ω resistor R14
arranged in series therewith the collector of transistor T14 is connected

30   to the base of transistor T9. This collector is also connected via
a 6.8k Ω resistor R20 to the base of an npn-transistor T15 the
emitter of which is connected to ground, while the base is connected
to the emitter of an npn-transistor T23 via a 4.7k Ω resistor R24
and to ground via a 6.8k Ω resistor R25. The collector resistors

35   R21 and R23 of transistors T14 and T15 both have a value of

12 kΩ and are both connected to source V_B. The terminal of resistor R19 which is not connected to the base of transistor T14 is connected to the collector of transistor T15. From the foregoing it will be clear that transistors T14 and T15 with associated resistors from a bistable element (flip-flop).

A resistor R16 having a value of 1 kΩ is arranged between the emitter of transistor T11 and the base of an npn-transistor T17. The emitter of transistor T17 is connected to the emitter of an npn-transistor T16 and to the collector of an npn-transistor T18 whose emitter is connected via a 200 Ω resistor R30 to ground and whose base is connected to the collector and to the base of an npn-transistor T19 and also to a resistor R28 having a value of 3.9 kΩ. The emitter of transistor T19 is connected to ground via a resistor R29 having a value of 200 Ω. The other terminal of resistor R28 is connected to the base of transistor T16 via a 1.5 kΩ resistor R27, to the base of an npn-transistor T12 via a 3 kΩ resistor R22 and to source V_B via a 9.1 kΩ resistor R26. The collectors of transistors T12 and T16 are both connected directly to source V_B and the collector of transistor T17 is connected to source V_B via a 4.7 kΩ resistor R31. The emitter of transistor T12 is connected to the base of an npn-transistor T13 the collector of which is connected to the junction of resistors R3 and R4 and the emitter is connected to ground via a 8.2 kΩ resistor R9.

Via a resistor R32 and R33 each having a value of 2 kΩ the collector of transistor T17 is respectively connected to the base of a pnp-transistor T24 and T20 the emitters of which are connected to voltage V_B. The collector of transistor T24 is connected to ground via a 12 kΩ resistor R36 and to the base of an npn-transistor T25 via a 11 kΩ resistor R37. The said collector is also connected to the output terminal F of the circuit. The collector of transistor T20 is connected to the collector of an npn-transistor T21 and to the base of an npn-transistor T22. The emitter of transistor T22 is connected directly to the base of transistor T23 and to the emitter thereof via a 16 kΩ resistor R34. The emitter of transistor T21 is directly connected to ground, while the emitter of transistor T23 is

connected to ground <u>via</u> a 10 kΩ resistor R35. The collectors of transistors T22 and T23 are connected to voltage V_B. The base of transistor T21 is not connected, so that during operation this transistor behaves as a small capacitance of 1 to 2pF.

5   A resistor R39 having a value of 4.7 kΩ is connected between the base of an npn-transistor T26 and the junction E of resistors R14 and R18. The collector of an npn-transistor T27 is also connected to the said junction. The collectors of transistors T25 and T26 are interconnected and <u>via</u> a resistor R38 having a value of 2.4 kΩ to

10 the base of transistor T12. A 4.7 kΩ resistor R40 is connected between the base of transistor T27 and the emitter of transistor T23. Finally, the emitters of transistors T25, T26 and T27 are connected to ground.

On terminal A there is a negative going video signal during

15 operation. By means of transistor T8 which acts as a diode, and resistors R7 and R8 the base of transistor T3 is adjusted to a substantially constant voltage. Transistor T3 forms a current source; the current thereof flows either through transistor T4 or through transistor T5. Transistors T4 and T5 form a differential

20 amplifier: if the voltage at terminal A exceeds the voltage on terminal D, that is to say if the voltage at the base of transistor T4 exceeds the voltage at the base of transistor T5, then transistor T5 is conductive while transistor T4 and also transistor T6, which acts as a diode, and consequently also transistor T7 which in combination

25 with transistor T6 forms a current mirror, are non-conductive. In these circumstances capacitor C is charged by the collector current of transistor T5. The direct current level on terminal A relative to the level on terminal D has been chosen so high that this charging operation can only be performed when the incoming signal increases

30 to above the reference level, for example during the occurrence of the line synchronizing pulses. Transistors T2 to T7 and C together form a signal generator.

However, on terminal G there are line flyback blanking pulses present coming from a line deflection circuit, not shown, and which

35 are processed in a portion, not shown, of the integrated circuit of

which the circuit of Figure 1 forms part. During each line period
(having a duration of approximately 64 /us) these pulses have a
positive value for approximately 12 /us. In this period, the line
flyback period, transistor T10 is driven to its conducting state,
5 while the pulses during the remaining portion of the line period,
the line trace period, have such a low value that transistor T10 does
not conduct.

If the voltage V_c across capacitor C is lower than a given
value, then transistor T11 does not conduct and consequently transistor
10 T14 is also non-conductive. The collector of transistor T14 then
carries voltage V_B and the voltage at point E is high. As long as
the voltage at terminal G is low, transistors T9 and T10 can not,
however, conduct. During the line flyback period transistor T5 as
well as transistors T9 and T10 are conductive. The voltage at the
15 collector of transistor T9 is kept very low so that the line
synchronizing pulses occurring in the line flyback period in the
signal of terminal A cannot cause charging of capacitor C. The same
holds for disturbing interference pulses occurring in the said period
of time at terminal A. During the line trace period the video voltage
20 at terminal A is always lower than 8V and capacitor C is discharged
by the collector current of transistor T7 which is conductive because
transistor T4 is conductive. Owing to the comparatively high value
of resistor R10 this discharging current is rather small so that
voltage V_c decreases slowly.
25 From the foregoing it appears that voltage V_c at the end of
the field trace period is substantially zero. During the field
blanking interval occurring thereafter, there first occur five pre-
equalizing pulses having a duration of approximately 2.3 /us with
a time difference of half a line period, i.e. approximately 32 /us.
30 These pulses are followed by five field synchronizing pulses the total
duration of which is also 2.5 line periods and between which field
serration pulses the duration of each of which is equal to the
duration of the line synchronizing pulses, namely approximately
4.7 /us occur. They are followed by five post-equalizing pulses.
35
This holds for the European television standard. Other television

standards, for example the United States standard deviate from this in a few details, which is of no importance for the invention.

Figure 2a illustrates the video signal present at terminal A, more specifically for a portion of one of the two fields which form a picture, in this case the field which ends with a full line. The line period which follows immediately after the post-equalizing interval is also shown. Thereafter there follow a number of line periods until the beginning of a new field trace. Figure 2b shows the signal applied to terminal G. From Figures 2a and 2b it will be seen that the first pre-equalizing pulse does not coincide with a line flyback pulse and so causes charging of capacitor C. Voltage V_c (see Figure 2c), which was substantially zero now increases substantially linearly.

By means of resistors R22, R26, R28. R29 and R38 as well as the transistor T19 which acts as a diode, the voltage at the junction M of resistors R22, R26, R27 and R28 is adjusted to a low value when transistor T26 conducts. Transistor T16 is conductive, while transistor T17, which forms in conjunction with transistor T16 and the transistor T18, which acts as a current source, a differential amplifier, is non-conductive. Since transistor T17 is non-conductive, the collector thereof carries voltage V_B, so that transistors T20 and T24, and consequently also transistors T22 and T23 are non-conductive, resulting in that the output voltage at terminal F (see Figure 2d) and also the voltage at the emitter of transistor T23 are zero. Also transistors T25 and T27 are non-conductive.

As long as the voltage at the base of transistor T11 is too low to render this transistor conductive, transistor T14 remains also non-conductive. The voltage at terminal E (see Figure 2e) is high but as the voltage at terminal G is low, transistor T9 cannot conduct. Transistor T15 whose base is connected to voltage V_B via resistor R20 is conductive. In a similar manner transistor T26 is conductive as the base resistor R39 thereof is connected to point E. A small collector current flows through transistor T12 whose base is connected to point M via resistor R22 and to ground via resistor R38, and consequently also through transistor T13. The emitter current of

transistor T3 and consequently also the charging current of capacitor C
have a high value, so that voltage V_c increases rather rapidly.

Transistor T11 operates as a level detector. As soon as voltage
V_c exceeds the value which is equal to twice the base-emitter
5 threshold voltage of a conductive transistor, i.e. approximately 1.5 V,
then transistor T11 and consequently also transistor T14 are rendered
conductive. The voltage at the collector of transistor T14
and the voltage at point E (see Figure 2e) become substantially zero.
This decrease in voltage is transferred by means of resistor R18
10 and R39 to the base of transistor T26 and by means of resistor R20
to the base of transistor T15, as a result of which these transistors
become non-conductive. The resulting increase of the voltage at
the collector of transistor T15 is transferred to the base of
·transistor T14 by means of resistor R19. So this transistor is held
15 conductive as a result of which the flip-flop formed by transistors
T14 and T15 will have changed to its other state.

As transistor T26 is non-conductive, the voltage at point M
assumes a higher value of approximatley 4.2 V, as a result of which
the emitter current of transistor T12 and consequently also the
20 emitter current of transistor T13 become larger. The collector
current of transistor T13 flows through resistor R3 and is subtracted
from the emitter current of transistor T3. This causes the charging
current of capacitor C to decrease to a lower value, namely approximately
one tenth, and voltage V_c increases less rapidly. As long as the
25 voltage at the emitter of transistor T11 is lower than approximately
4.2 V, transistor T17 remains in the non-conductive state. So the
state of transistors T20, T22, T23, T24, T25, and T27 does not
change and the output signal remains zero.

The second value of the charging current is so low and the value
30 of approximately 4.2 V has been chosen so high that the equalizing
pulse is too short to cause this value to be reached. At the end
of the occurrence of the pulse the voltage at terminal A decreases,
causing transistor T4 and T6 and consequently also transistor T7
to become conductive, while transistor T6 is cutoff. As a result
35 thereof capacitor C is discharged by a small current. Voltage V_c

decreases slowly.   Transistor T11 remains conductive but no change
occurs in the state of the remaining portion of the circuit, particular-
ly not in the state of flip-flop T14, T15. As the voltage at point E
remains low, transistor T9 cannot conduct. The line flyback pulse
occurring after the first pre-equalizing pulse at terminal G has
therefore no influence on voltage V_c. The same holds for the
subsequent line flyback pulses, while each one of the remaining pre-
equalizing pulses produce a slight increase of voltage V_c, so that
voltage V_c varies little.

As the field synchronizing pulse is of a longer duration than
the equalizing pulse the voltage at the emitter of transistor T11 is
able to reach the value of approximately 4.2 V after the occurrence
of the leading edge of said synchronizing pulse. The circuit, the
charging current in particular, is dimensioned such that this second
level is reached approximately 15 μs after the first level has been
reached, causing transistor T17 to become conductive and transistor T16
to become non-conductive. So these transistors form a second level
detector. The voltage at the collector of transistor T17 decreases,
in response to which transistors T20 and T24 become conductive. A
positive edge is now present at output terminal F and causes
transistor T25 to become conductive. Resistor R38 is now connected
to a low potential and the voltage at point M assumes a lower value.
As a result thereof transistors T12 and T13 conduct to a lesser extent
and the charging current of capacitor C assumes a higher value. Voltage
V_c increases rapidly until the Zener voltage, approximately 7 V, of
the semiconductor diode by which capacitor C is formed, is reached,
whereafter voltage V_c no longer increases. The high value of the
charging current ensures that this high level is reached by voltage V_c
before the first field serration pulse occurs.

The small capacitor formed by transistor T21 is charged rather
rapidly by the collector current of transistor T20. Transistors T22
and T23 become conductive, resulting in transistors T15 and T27 also
becoming conductive. The voltage at point E remains low and transistors
T9 and T26 remain in the non-conductive state. As the base of transistor
T14 and the base of transistor T15 are both connected to a positive
voltage flip-flop T14, T15 cannot change state.

During the occurrence of the field serration pulses the voltage
at terminal A again assumes the value of the reference level. This
causes capacitor C to be discharged and voltage V_c decreases. As
transistor T25 is conductive, that terminal of resistor R38 which
is not connected to resistor R22 is connected to ground, so that the
value of the second threshold voltage at point M is less than 4.2 V.
The voltage at the emitter of transistor T11 also decreases, but
owing to the short duration of the serration pulse this voltage
does not decrease below the value of the voltage at point M, so
that transistor T17 remains conductive and the voltage at terminal F
remains high. The line flyback pulses present at terminal G have
no influence, as transistor T9 is still non-conductive.

After the last field synchronizing pulse and the first post-
equalizing pulse which occurs shortly thereafter, capacitor C is
rapidly discharged. As the interval before the next equalizing
pulse is long enough, the voltage at the emitter of transistor T11
now decreases to below the new value of the second threshold voltage,
as a result of which transistor T17 is made non-conductive while
transistor T16 becomes conductive. Transistors T20 and T24 are
cut-off and the output voltage at terminal F becomes zero. The
capacitor formed by transistor T21 discharges to the base of
transistor T22. As this base is high-ohmic, the period of discharge
has a determined duration which can be adjusted by selecting the
value for resistor R34 and during which the transistors T22 and T23
remain conductive. The state of flip-flop T14, T15 does not change,
so that during this interval post-equalizing pulses and current pulses
cannot exercise any influence.

Owing to the fact that transistor T24 has been cut-off, transistor
T25 will also be cut-off which results in the voltage at point M
becoming high again. Capacitor C is now further slowly discharged.
At the instant at which transistor T11 is cut-off a positive
voltage is no longer applied to the base of transistor T14. The
flip-flop T14, T15 can now change state. Transistor T15 then conducts
while transistor T14 is non-conductive.

Approximately at the end of the post-equalizing interval the

capacitor formed by transistor T21 is discharged to such an extent that transistors T22 and T23 are cut-off, as a result of which transistor T27 is made non-conductive.

Since the voltage at the collector of transistor T14 is high
5 from the moment onwards at which the state of flip-flop T14, T15 has changed, the voltage at point E also becomes high which drives transistor T9 and T26 to conduction. The voltage at point M becomes low again and the current from transistors T12 and T13 returns to its low value, so that the emitter current from transistor T3 returns
10 to its high value. So capacitor C is discharged with absolute certainty. The circuit is now in the same state as at the end of the field trace period.

If a positive going interference pulse occurs in the signal at terminal A then this pulse may cause an increase of voltage V_c
15 and may even make transistor T11 conductive provided the pulse duration is sufficiently long, but generally the pulse will be too short, that is to say shorter than approximately 15 μs, to make transistor T17 conductive and consequently to cause the generation of an output signal. The next following line flyback pulse present
20 at terminal G, which makes transistor T10 conductive, short-circuits voltage V_c with respect to ground. If transistor T11 has been made conductive by the disturbing pulse then flip-flop T14, T15 has changed state at that moment, causing the voltage at point M and consequently the collector current of transistor T13 to become high. So a
25 subsequent interference pulse will only produce a low charging current of capacitor C. Voltage V_c remains low, more specifically until the occurrence of the next train of pre-equalizing pulses. In this situation the field terminates with half a line and the first pre-equalizing pulse coincides with a line flyback pulse. If the
30 circuit has not been set by an interference pulse to the preparatory state in which voltage V_c has attained the first threshold value, then this state is not initiated by the first but by the second pre-equalizing pulse. If the incoming signal contains so much noise that the first pre-equalizing pulse in the case of the field shown
35 in Figure 2, and the second pre-equalizing pulse in the case of the

subsequent field, does not initiate the preparatory state, then
this state will be initiated for one field by the third or the fifth
pre-qualizing pulse or for the subsequent field by the fourth pre-equal-
ising pulse. If also these pulses are "missed" then the first field
synchronizing pulse causes the first and thereafter the second
5 threshold value to be reached by voltage V_c. Only in the event
that this does not happen will the circuit of Figure 1 not
generate an output signal but then the television signal received
by the television receiver of which the circuit is part, contains
so much noise that it would not be possible anyway to obtain a
10 viewable picture.

From the foregoing it will be appreciated that the circuit of
Figure 1 generates a reliable pulse at terminal F, the leading edge
of which occurs a fixed period of time after the leading edge of
the first field synchronizing pulse and the trailing edge occurs a
15 fixed period of time after trailing edge of the last field synchronizing
pulse and which generated pulse is consequently suitable for application
as a field synchronizing signal to a field synchronizing circuit
connected to terminal F. This also holds in the event that the
incoming signal is a non-standard signal, that is to say a signal
20 not containing equalizing pulses. It should be noted that an interlace
error is prevented from occurring as the line flyback pulses applied
to terminal G do not have any influence at the occurrence of the first
field synchronizing pulse. Otherwise charging of capacitor C could
not start until after the trailing edge of the line flyback pulse
25 which occurs simultaneously with said pulse, which would imply a
shift of the leading edge of the pulse of Figure 2d. However, this
shift would not occur at the next field, namely because of the fact
that a line flyback pulse does then not coincide with the first field
synchronizing pulse, which results in that one field would start
30 approximately 12 /us too late and the other field at the correct
moment. It can also be seen that the video information in the signal
of Figure 2a plays no part in the generation of the field synchronizing
signal so that the signal applied to terminal A may be a composite
television synchronizing signal, that is to say a signal which does
35 not contain video information.

In the circuit of Figure 1 flip-flop T14, T15 acts as a memory element. As a result thereof the application of line flyback pulses to the circuit has no effect after the first threshold value has been reached while charging of capacitor C is performed slowly.

5 Without the flip-flop voltage V_c would rapidly decrease after the occurrence of the first pre-equalizing pulse, which entails the risk, especially when there is much noise and little impulsive interference, that the first threshold level would not be reached during the pre-equalizing interval. This could result in an interlace error.

10 It will be obvious that portions of the circuit shown in Figure 1 may be constructed in different ways. The portion comprising the transistors T20, T21, T22 and T23 may be replaced by, for example, a monostable element since it operates as such an element, while transistors T25, and T26 form an OR-gate and transistors T9 and T10

15 form an AND-gate. The change-over of the charging and discharging current, respectively of capacitor C may be performed in a different, known manner. Instead of the operation described, the capacitor itself may be switched to a different value. The duration of the pulses of the line frequency applied to terminal G is not critical:

20 the sole requirement to be satisfied is that these pulses must include the line synchronizing pulses of the signal applied to terminal A, but it is obvious that they must be shorter than 32 /us.

CLAIMS:-

1.   A circuit arrangement for deriving a field synchronizing
signal from an incoming signal which contains at least line
synchronizing and field synchronizing pulses whose amplitude extends
5 between a reference and a peak level, comprising a signal generator
for generating a signal for each pulse which has a value located
between the reference and the peak level occurring in the incoming
signal, said generated signal having a value which is representative
of the duration of each pulse, and a comparator stage for comparing
10 the generated signal with a threshold value, characterized in that
the circuit arrangement also comprises a gate circuit for, in
operation, inhibiting the generated signal from the signal generator
during the occurrence of the line synchronizing pulses for which
the threshold value is not reached by the generated signal from the
15 signal generator, this gate circuit not inhibiting the generated
signal when said threshold value is reached by said generated signal,
the circuit arrangement generating the field synchronizing signal
when the generated signal from the signal generator reaches a second
threshold value which is representative of a pulse duration which
20 exceeds that corresponding to the first mentioned threshold value.

2.   A circuit arrangement as claimed in Claim 1, characterized
in that the gate circuit comprises a gate for the transmission outside
the field blanking interval, of pulses at the line frequency whose
periods of occurrence substantially include those of the line synchronising
25 pulses and for inhibiting the transmission of said pulses at the line
frequency after the generated signal from the signal generator has
reached the first threshold value.

3.   A circuit arrangement as claimed in Claim 2, characterized in
that it further comprises a monostable element for maintaining the
30 gate circuit during a predetermined period after the second threshold
value has been reached by the generated signal from the signal generator

in the state in which the gate inhibits the transmission of the
pulses at the line frequency.

4. A circuit arrangement as claimed in one of the Claims 2
or 3, characterized in that the pulses at the line frequency are
5 line flyback blanking pulses originating from a line deflection
circuit.

5. A circuit arrangement as claimed in Claim 1, in which the
signal generator generates during the occurrence of a pulse in the
incoming signal a substantially linear signal, characterized in that
10 the slope of the substantially linear signal is reduced after the
first threshold value has been reached than it is before it.

6. A circuit arrangement as claimed in Claim 5, characterized
in that the slope of the substantially linear signal is steeper after
the second threshold value has been reached than it is before it.

15 7. A circuit arrangement as claimed in Claim 2, characterized
in that the circuit arrangement comprises a bistable element which
is in a first state when the generated signal from the signal generator
is lower than the first threshold value and in a second state after
the signal has reached the first threshold value, the second state
20 being maintained until at least the end of the field synchronizing
signal, in which second state the bistable element maintains the
gate circuit in the state in which the gate inhibits the transmission
of the pulses of line frequency.

8. A circuit arrangement as claimed in Claims 3 and 7, characterised
25 in that the monostable element is coupled to the bistable element
for setting it to its first state.

9. A circuit arrangement as claimed in Claim 3, characterized
is that it also comprises a second comparator stage for comparing
the signal of the signal generator with the second threshold value
30 and for setting the monostable element when said signal has reached
said second threshold value.

10. A circuit arrangement for deriving a field synchronizing
signal from an incoming signal substantially as herein described with
reference to the accompanying drawings.

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Circuit arrangement for deriving a field synchronizing signal from an incoming signal:

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R | Request for examination: 2 5 JUN 1982

R |

A | Application refused

A |

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