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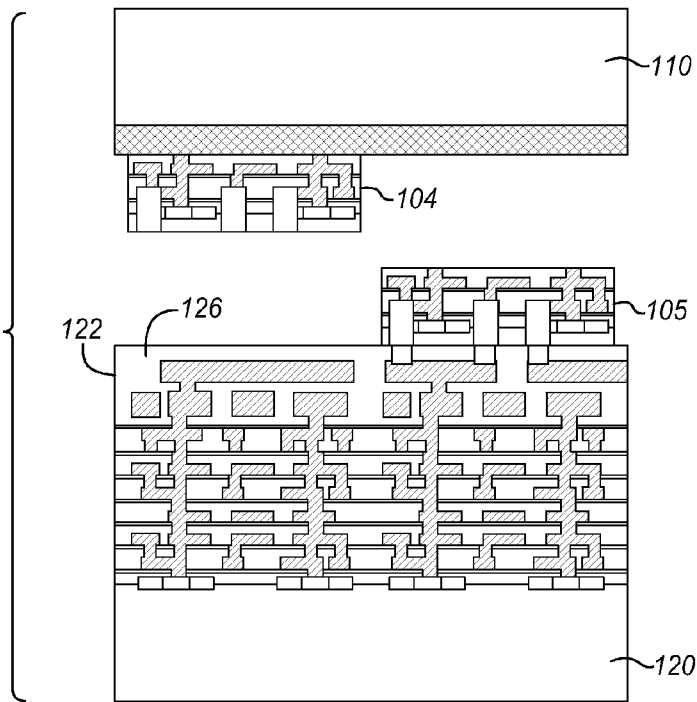
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(54) Title: COMBINATION OF SEMICONDUCTOR DIE WITH ANOTHER DIE BY HYBRID BONDING

FIG. 7



(57) Abstract: Hybrid bonding is described for combining one semiconductor die with another. Some embodiments include attaching small dies on a wafer to a temporary carrier, aligning the dies over a plurality of larger host dies on a host wafer using the temporary carrier, applying the small dies against the host dies using the temporary carrier so that a subset of the small dies bond to respective host dies, separating the temporary carrier so that the subset of bonded small dies are attached to a respective host die and the remaining small dies are separated with the temporary carrier, singulating the host dies, and packaging the host dies.

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COMBINATION OF SEMICONDUCTOR DIE WITH ANOTHER DIE BY HYBRID BONDING

FIELD

The present disclosure relates to assembling semiconductor dies for a package and in particular to an assembly with dies of different sizes connected together.

BACKGROUND

In order to increase speed and power efficiency and to reduce the size of electronic equipment, integrated circuit dies are made ever smaller. These dies are mounted closer together so that the connections between these dies are also made shorter. The shortest connection is a connection that is made within an integrated circuit package. In some cases dies are mounted side by side on a package substrate and connected together through the package substrate or directly with wires. In other cases, dies are mounted one on the other for a direct connection without any intervening wire or package substrate. This is sometimes called a stacked die package. One die can be placed over another using a pick and place machine or a variety of other types of equipment. The combination can be packaged as if it is a single die with double the height.

Combining multiple dies into a single package allows for two or more different types of dies to be placed into a single package. This may be referred to as heterogeneous integration of die-to-die connections. As one example, the dies may be made using different materials such as Si, Ge, III-V, SiC, etc.. As another example the dies may be made using different technology nodes such as 22 nm, 14 nm, 10 nm, etc.. These differences may be combined and combined with other types of differences so that different types of dies from different processes and different fabricators may be placed into a single compact package.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings in which like reference numerals refer to similar elements.

Figure 1 is a side cross-sectional view diagram of a portion of a device wafer carrying multiple small die with a scribe trench between each die according to an embodiment.

Figure 2 is a side cross-sectional view diagram of the device wafer with a temporary carrier attached to the front side of the small dies using temporary adhesive according to an embodiment.

Figure 3 is a side cross-sectional view diagram of the device wafer and temporary carrier after the device wafer is thinned to the level of the scribe trenches according to an embodiment.

Figure 4 is a side cross-sectional view diagram of the device wafer and temporary carrier after adding through die vias on the back side of the small dies according to an embodiment.

Figure 5 is a side cross-sectional view diagram of the device wafer and temporary carrier aligned over a portion of a host wafer carrying a host die with landing pads for one of the small dies according to an embodiment.

Figure 6 is a side cross-sectional view diagram of bonding the through die vias of one of the small dies to the landing pads of the host die according to an embodiment.

Figure 7 is a side cross-sectional view diagram removing the temporary carrier and the other of the small dies that was not bonded away from the host wafer according to an embodiment.

Figure 8 is a side cross-sectional view diagram of adding dielectric and metal routing layers over the small die to finish a package according to an embodiment.

Figure 9 is a side cross-sectional view diagram of a device wafer carrying multiple small die with a scribe trench between each die and through die vias from the die circuitry into the device wafer according to an embodiment.

Figure 10 is a side cross-sectional view diagram of the device wafer with through die vias with a temporary carrier attached to the front side of the small dies using temporary adhesive according to an embodiment.

Figure 11 is a side cross-sectional view diagram of the device wafer with through die vias and temporary carrier after the device wafer is thinned to the level of the scribe trenches and the through die vias according to an embodiment.

Figure 12 is a side cross-sectional view diagram of a device wafer and temporary carrier aligned over a portion of a host wafer carrying a host die with landing pads for one of the small dies in which a dielectric is formed around the landing pads but recessed to expose the landing pads according to an embodiment.

Figure 13 is a side cross-sectional view diagram of the device wafer and temporary carrier aligned over a portion of a host wafer carrying a host die with landing pads for one of the small dies in which a dielectric layer is recessed around the landing pads and also

recessed at the position of the second small die so that the second small die does not physically contact the dielectric according to an embodiment.

Figure 14 is a side cross-sectional view diagram of face-to-face bonding of the front side of a small die to the front side of host die so that the thinned substrate is on the opposite side of the small die from the landing pads according to an embodiment.

Figure 15 is a side cross-sectional view diagram of the face-to-face bonded small die after covering in dielectric and metal layers to connect the host die to external components and to finish the package according to an embodiment.

Figure 16 is a side cross-sectional view diagram of face-to-face bonding of the front side of a small die to the front side of host die using a small solder ball according to an embodiment.

Figure 17 is a side cross-sectional view diagram of the face-to-face solder ball bonded small die host die combination with a conventional C4 solder ball attached according to an embodiment.

Figure 18 is a side cross-sectional view diagram of the face-to-face solder ball bonded small die host die combination showing an attachment to a package substrate using the C4 solder ball to finish the package according to an embodiment.

Figure 19 is a block diagram of a computing device incorporating a hybrid bonded hybrid semiconductor die package according to an embodiment.

DETAILED DESCRIPTION

As described herein functional small dies or islands may be integrated into existing positions on a die that is constructed on a host wafer. Very small and thin dies may be handled in bulk by using wafer level handling. Instead of manipulating a single small die into a small location, a whole wafer may be handled at once but dies are only transferred to selected areas of the larger dies on the host wafer.

In some cases a hybrid bond may be used to reduce the amount of heat that is applied to attach an island to a die. This allows lower process temperatures to be used. The hybrid bonding, as described makes a strong bond at relatively low temperatures as compared to other types of permanent bonding. The hybrid bonding may be used to provide a lower overall thermal budget or a wider process window for detachment of the islands from a carrier wafer.

In some of the described examples, a carrier wafer containing small dies is bonded to a host wafer. Both small dies or islands and the formed dies on a host wafer have metallic

landing pads, through-die-vias or some other metallic connector. By placing the carrier wafer over the host wafer so that the landing pads are aligned and then applying mild heat and pressure, the metallic pads and vias form a strong bond. The areas without the metallic landing pads are attached together only very weakly.

After the mild heat and pressure is applied, the carrier and host wafers are separated to selectively transfer islands to the bonded areas of the large dies. If there are islands remaining on the carrier wafer, then the carrier wafer may then be positioned over another host wafer to transfer some of the islands to another set of large dies. This may be repeated until all of the islands are placed.

As described, the small dies are handled as a group on a wafer. When held on a carrier wafer, very small and thin dies can be transferred. The dies may be much smaller and thinner than can easily be manipulated by a die pick-and-place assembly. By forming interconnects on both the top and the bottom of the islands, more routing resources can be obtained. The small dies are applied against the host dies using the temporary carrier so that some of the small dies or a subset of the total dies on the carrier wafer bond to respective host dies on the host wafer. The application may be without substantial pressure or pressure may be applied to press the metal of the dies together. Heat may also be used instead of with the pressure.

Figures 1-8 show an example process for placing a small island die in a location so that it may be a fully embedded small island die inside a host die. Figure 1 is a side cross-sectional diagram of a set of small dies 104, 105 formed on a device wafer 102. The device wafer is the substrate on which the dies have been formed and securely carries the dies. The dies have been partially diced by sawing, scribing, or etching so that there is a scribe trench 106 or saw kerf between the dies and into the wafer 102.

In this example, the dies are referred to as small meaning only that they are smaller than the host die to which they will be attached. The small dies may be half the size of the host die, one tenth the size or any other relative size. The device wafer contains many small dies to be transferred to dies that have been formed on a host wafer. The dies may be functional materials which are beneficial to integrate with host wafer. Examples of such functional materials may include silicon, germanium, silicon carbide, III-V and III-nitride compound semiconductors. Because the small dies are formed independently on a separate wafer, they may be formed using a different technology, different materials, or different

process nodes than the host die. The small dies may be power, radio-frequency, optical, memory, or other types of devices that are best formed separate from the host wafer.

Figure 2 is a cross-sectional side view diagram of the device wafer 102 of Figure 1 inverted and attached to a temporary carrier 110 using a temporary adhesive 108. The front side of the dies 104, 105 is covered by the carrier and the back side of wafer 102 is exposed. This device wafer is bonded to the temporary carrier wafer so that the wafer may be handled by the carrier. The temporary adhesive is selected to withstand any mechanical forces that may be caused during grinding the wafer and any thermal or mechanical overburden during wafer thinning. These forces may include shear forces, compressive forces, tensile forces, etc. The temporary adhesive is also selected so that the dies may easily be debonded from the carrier when desired. One such class of adhesive is polymer adhesives. Polymer adhesives may include polymethacrylates, polyacrylates, polystyrenes, polysilsesquioxanes, polysiloxanes, polynorbornenes, polyimides, polybenzoxazoles, epoxies, novolac, benzocyclobutenes, and polycarbonates. Inorganic adhesives may include H-implanted silicon (or silicon implanted with other volatile species), or amorphous Si:H.

Figure 3 is a cross-section side view diagram of the device wafer and dies of Figure 2 after the device is thinned. This may be done by grinding or in any other way. Bulk micromachining techniques such as grinding, wet etching, dry etching and chemical-mechanical polishing may be used, among others. The amount of thinning or the thinning target varies upon the integration level. If the dies are to be embedded into an interconnect stack as shown in Figure 8, then the die requires no structural stability and the wafer can be made very thin, for example, less than 1 μ m thick. As another example, if the small die is to be embedded as a part of C4 or packaging as in Figure 18, then the die requires some mechanical reinforcement and stability but still may be only a few tens of a μ m thick.

In this example the scribe trenches extend into the device wafer. The scribe trenches are made deep enough so that the thinning of the device wafer meets the scribe trench. As a result in Figure 3, after thinning the dies are singulated by the scribe trenches. In this way, when the dies are attached to the temporary carrier, the dies are maintained in their original positions by the device wafer. After attachment and thinning the alignment is maintained by the temporary carrier. This precise alignment may be used to accurately place the small dies on the host wafer as shown in Figure 6.

Figure 4 is a side cross-sectional diagram of the dies 104, 105 of Figure 3 with the addition of vias 112. After thinning, "through-die-vias" may be fabricated. This is analogous

to through-silicon-vias (TSV) but are drilled, etched, or bored through the back side substrate or wafer to make contact with the front end circuitry of the dies. The drilled holes are then filled with a metal such as Cu, Ti, Ta to make the connection. The holes are overfilled so that the metallic surfaces at the tops of the vias are exposed.

Figure 5 is a diagram of the dies and temporary carrier inverted again so that the back side of the dies is face down. Figure 5 also shows a corresponding larger host die 122 formed on a host wafer 120. The host wafer also has an underlying stack. There are vertical conductive posts 114 that form landing pads to the through-die-vias of the small die 105. The large die has a conductive redistribution layer or other metal or conductive layer with conductive lines or traces 124 over the die. The landing pads 114 provide connections for the vias to these metal layers. As shown the two wafers, the host device wafer 120 and the carrier wafer 110 are aligned.

Figure 6 is a diagram of bonding the two wafers. After alignment, the two wafers are brought together for example by moving the carrier wafer and the two dies 105, 122 together. In the drawing figure, the two dies are bonded. The metallic top surfaces of the vias are applied to the landing pads so that they physically contact each other. Heat or pressure or both are applied to form a sufficient metallic bonding. For pressure, the vias are pressed against the landing pads. For heat the host wafer and the temporary carrier are placed in a heated chamber or heat is applied to assist the two dies in bonding together. The conditions may be adjusted to form strong metallic bonding. The rest of the area of the host wafer which, in this example is made primarily of ILD (Inter-Layer Dielectric) has only a very weak bond so that these areas will later separate.

A variety of different bonding mechanisms may be used to connect the small die to the host die. In some embodiments, metal inter-diffusion is used through the bonding boundary with grain growth. In this case, since the diffusion rate between the metals is temperature-dependent, higher temperatures may cause faster and stronger bonding. However, higher temperatures also affect the characteristics of other materials of the dies and even those near the inter-metal diffusion bonds, such as ILDs at the hybrid bonding interface. Using a lower temperature as described herein reduces or eliminates any negative impact on materials other than the bonding metals.

In some embodiments, no heating is applied and the metals are bonded at room temperature. In other embodiments, the temperature is elevated to 100°C or even to 200°C or to some temperature in between. This promotes diffusion between the metals without

damaging other materials. After the metals are bonded using the hybrid bonding described herein, the temporary carrier with the dies that are not bonded may be removed. In some embodiments, the bonded metal may be allowed to cool before separation. This will provide for an even stronger metal-to-metal bond. When the temporary carrier is removed as shown in Figure 7, the metal-to-metal bond is stronger than the temporary bond adhesive. The strength of the adhesive bond may be used in determining specifically how to control the hybrid metal-to-metal bond for any particular implementation.

Figure 7 is a diagram of separating the carrier wafer from the host wafer. This causes the two dies to be separated. The bonding on the temporary adhesive is weaker than the metal or hybrid bonding. In some embodiments, some external stimulation such as heat may be applied to weaken the bond between the island dies and the temporary carrier wafer. After the separation, the carrier wafer may be used to apply dies to another host wafer.

As shown, the host wafer has landing pads 114 in a position corresponding to only one of the small dies. Figure 5 shows two small dies over a surface of one large host die 122. While through die vias are formed on both small dies, only the vias of one of the dies contact landing pads on the host wafer. The vias of the other die contact a dielectric layer 126 of the host die. Therefore, the metal bonding occurs only for the small dies 105 that contact landing pads. The other dies 104 are not bonded and remain connected to the temporary carrier.

Upon separation in Figure 7, the metal thermal or compression bond is a stronger bond than the temporary adhesive. As a result, the die over the landing pads stays with the host die as the temporary carrier is removed. There is no significant bond between the through die vias and the dielectric. Since the temporary adhesive is stronger than this bond, the second die is lifted away from the host die by the temporary carrier. As noted above the dies have already been separated through a portion of the wafer as shown by the scribe trenches 106. Accordingly, after wafer thinning in Figure 3, only the carrier holds the dies together. The dies are already diced or singulated.

Figure 8 is a diagram with the temporary carrier and other small dies removed. The one attached small die remains metal bonded to the host die. The host wafer is further processed to embed the transferred small die fully into the interconnect stack. In the illustrated example, the further processing include additional dielectric 134, additional conductive posts or vias 130 and conductive contact pads or lines 132 to connect to other components. As shown, the smaller die 105 is fully embedded within the ILD of the host die.

This allows special functions and specialized dies to be incorporated into a larger die assembly without any change in packaging and other processing aspects of the host die.

In this example, only two small dies 104, 105 are shown on the device wafer 102. Typically there will be many more. These dies are formed on the device wafer together. They may then be tested. These functional dies may be carried on the wafer and manipulated as a group. Similarly, the host wafer 120 is only shown as having part of a single die 122, however, there will be many more. The transfer operation may be performed using wafer handlers so that many small dies are transferred to many host dies in one operation. The temporary carrier may then be moved to transfer more small dies to the same host wafer at a different location on the host dies or it may be moved to transfer small dies to the dies of a different host wafer.

Similar to other TSV (Through-Silicon Via) process, the through-die-via of Figure 4 may be fabricated either in a via-first or via-last manner. Figure 4 shows a via last approach in which the vias are formed on the back side of the die or wafer side after the dies are fully formed (Figure 1) and the wafer has been thinned (Figure 3). Figures 9-11 shows an alternative via-first process.

Figure 9 is cross-sectional side view diagram of an alternative to the device wafer of Figure 1. In this case the two dies 204, 205 are formed on the wafer 202 as in Figure 1, except that the through-die vias 212 are formed before the upper layers of the die are applied. These vias are therefore already formed before die thinning. The holes for the vias are drilled or bored to depth into the wafer so that they will be exposed after thinning. The dies are already separated and a scribe trench or saw kerf 206 is shown between the dies.

Figure 10 is a diagram of the same dies 204, 205 after a temporary carrier 210 is attached with an adhesive 208. Figure 11 is a diagram of the same device wafer 202 after the wafer has been thinned. As shown, the thinned wafer is taken down to below the level of the through die vias 212 which are now exposed. The structure is very similar to the structure of Figure 4 and can be used in the same process as shown in figure 5-8, or in other processes.

As another option, in order to improve the bonding and the release, the metallic landing pads may protrude above the adjacent ILD. Figure 12 is a cross-sectional side view diagram of a host wafer in which the ILD has been removed below the level of the landing pads. The host wafer 320 has many dies of which a portion of one die 322 is shown. After the wafer is formed there are many layers of metal and ILD 326 and landing pads 314 are formed to make connection with the metal layers 324 to connect with the circuitry of the die.

The ILD has been removed after the landing pads were formed. The landing pads now protrude above the ILD.

The island dies 304, 305 are formed in any of the ways described above and are adhered to a carrier 310. The dies are separated and have through die vias ready to make a metal connection with the landing pads 314. When the two are brought together in the manner described with respect to Figure 6 and 7. The through-die vias will make a more significant contact with the exposed landing pads 314 because the ILD has been removed and will not interfere. This may lead to a stronger and more secure metal compression bond. The dies 304 that are not over landing pads may not even make contact with the ILD. This will prevent any bonding with the host die so that, upon separation, there is even less stress on the bond with the temporary carrier.

Figure 13 shows another alternative. Instead of the metal landing pads protruding with all of the ILD recessed as in Figure 12, in Figure 13, mesa is formed that matches the size of the small die to be bonded. In other words, the ILD is recessed only where there is to be no die bonding.

Figure 13 is a cross-sectional side view diagram with similar small dies 404, 405 separated from each other and attached to a temporary carrier 410. Through die vias 412 in one of the dies are positioned directly over landing pads 414 of a large or host die 422 on its own host wafer 420. The landing pads are at the top of a multi-level ILD 426. The ILD 427 has been recessed under the die 405 that is not being attached. Under the die that is to be attached, the ILD 426 is not changed. As a result, when the small dies are brought together with the large dies as in Figure 6, the small die where there are no landing pads, where the ILD is recessed, will not make any physical contact with the host die. If there is any contact then it will be with less pressure than the small die over the landing contacts.

The small die 405 over the landing contacts 414 will bond to the host die 422 in the same way as described with respect to Figure 6. When the temporary carrier lifts the dies as in Figure 7, the small die over the landing contacts will be bonded to the host die. The small die over the recessed ILD will have little or no physical contact with the host die and will have little to no bond with the host die. This die will stay with the temporary carrier and be lifted off.

Figure 14 is a cross-sectional side view diagram of a further alternative in which the small dies are attached face-to-face with the host die. In the above example, through-die vias are used to attach the back side of the small dies to the front side or face of the host dies. If

the front side of the small dies is attached to the host dies, then the hybrid bonding can be achieved without through-die-vias.

In Figure 14, the host die 522 is formed on a host wafer 520 with multiple layers of metal lines and ILD. Landing posts 514 are formed at appropriate locations to make an electrical connection with a small die. A small die 505 is placed over the host die front side down or facing the host wafer. The small die has been formed on a wafer 502 which is opposite the host die. The small die also has metal layer and ILD and the top most metal layer has connection pads 515 to make contact with the landing posts. The top most layer in this example is the one closest to the host die.

When the small die carrier 110 (not shown) is applied to the host die, as in Figure 6, the landing pads 514 make a metal connection and bond to the small die. A hybrid bonding process may be used, as described above, using pressure or heat or both. Using metal contact layers instead of through-die vias provides a larger number of available connections between the small island die and the host die. This is at least in part because the front side connections may be made closer together for a higher pitch, than can through-die vias. The small die wafer may or may not be thinned, depending on the particular implementation.

Figure 15 shows an example of finishing the structure of Figure 14 by adding additional routing to the host die. The die is embedded in ILD 534 and additional vertical vias 530 and metal routing layers 532 are added to provide connections from the host die to external components. In this example and that of Figure 8, the small die is connected only to the host die, however, there may be additional vias and routing layers to provide a direct or indirect connection between the small die and external components.

This technique and structures described herein may be used not only on backend-level integration, but also on C4 (Controlled Collapse Chip Connection) or far-backend-level integration. Figure 16 is a cross-sectional side view diagram of an example of small die integration using a micro C4 bump. The host die 622 has been formed on a host wafer 620. The host die has connection pads 624 at a top metal layer and landing pads 614 formed over the connection pads. A small die 605 has been formed over a substrate 662 with a grid of metal connections. In this case, the small die front end is positioned facing the host die front end, however, the small die 605 may be reversed as in Figure 6. Rather than direct metal compression or heat bonding, a small or micro C4 bump 642 has been placed on each of the landing pads. When the small die is brought into contact with the host die, the contact layers do not directly contact the host die but contact the host die through the micro C4 bumps. The

assembly is reflowed so that the C4 bumps provide a connection between the two dies. This results in the finished assembly as shown.

The resulting structure may be finished as shown in Figure 8. Alternatively, the assembly may be finished using a standard C4 or solder bump attachment to a package substrate. In Figure 17 a regular C4 bump is applied to open areas and contacts on the host die 622. In Figure 18, the host die is attached to package substrate 648. The solder bump is applied to a contact pad 646 of the package. The assembly is then placed in a solder reflow oven so that the solder bump bonds to the package and the die.

While only one small die and one C4 bump is shown, there may be more dies and there will be more C4 bumps. As shown, the small die with the thinned wafer is able to be attached within an array of C4 or solder bumps. As a result, the additional small dies do not affect the size of the overall package. By forming the small dies in a separate process, the small dies may contain very different components than may be formed on the host die. Heterogeneously integrated devices are enabled such as silicon processing dies with a III-V voltage regulator, an optical waveguide, various passive devices, or RF modulators.

Figure 19 illustrates a computing device 11 in accordance with one implementation of the invention. The computing device 11 houses a board 2. The board 2 may include a number of components, including but not limited to a processor 4 and at least one communication chip 6. The processor 4 is physically and electrically coupled to the board 2. In some implementations the at least one communication chip 6 is also physically and electrically coupled to the board 2. In further implementations, the communication chip 6 is part of the processor 4.

Depending on its applications, computing device 11 may include other components that may or may not be physically and electrically coupled to the board 2. These other components include, but are not limited to, volatile memory (e.g., DRAM) 8, non-volatile memory (e.g., ROM) 9, flash memory (not shown), a graphics processor 12, a digital signal processor (not shown), a crypto processor (not shown), a chipset 14, an antenna 16, a display 18 such as a touchscreen display, a touchscreen controller 20, a battery 22, an audio codec (not shown), a video codec (not shown), a power amplifier 24, a global positioning system (GPS) device 26, a compass 28, an accelerometer (not shown), a gyroscope (not shown), a speaker 30, a camera 32, and a mass storage device (such as hard disk drive) 10, compact disk (CD) (not shown), digital versatile disk (DVD) (not shown), and so forth). These

components may be connected to the system board 2, mounted to the system board, or combined with any of the other components.

The communication chip 6 enables wireless and/or wired communications for the transfer of data to and from the computing device 11. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 6 may implement any of a number of wireless or wired standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, Ethernet derivatives thereof, as well as any other wireless and wired protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 11 may include a plurality of communication chips 6. For instance, a first communication chip 6 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 6 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

The processor 4 of the computing device 11 includes an integrated circuit die packaged within the processor 4. In some implementations of the invention, the integrated circuit die of the processor, memory devices, communication devices, or other components include or are packaged together and bonded on a host die as described herein. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

In various implementations, the computing device 11 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 11 may be any other electronic device that processes data including a wearable device.

Embodiments may be implemented as a part of one or more memory chips, controllers, CPUs (Central Processing Unit), microchips or integrated circuits interconnected

using a motherboard, an application specific integrated circuit (ASIC), and/or a field programmable gate array (FPGA).

References to “one embodiment”, “an embodiment”, “example embodiment”, “various embodiments”, etc., indicate that the embodiment(s) of the invention so described may include particular features, structures, or characteristics, but not every embodiment necessarily includes the particular features, structures, or characteristics. Further, some embodiments may have some, all, or none of the features described for other embodiments.

In the following description and claims, the term “coupled” along with its derivatives, may be used. “Coupled” is used to indicate that two or more elements co-operate or interact with each other, but they may or may not have intervening physical or electrical components between them.

As used in the claims, unless otherwise specified, the use of the ordinal adjectives “first”, “second”, “third”, etc., to describe a common element, merely indicate that different instances of like elements are being referred to, and are not intended to imply that the elements so described must be in a given sequence, either temporally, spatially, in ranking, or in any other manner.

The drawings and the forgoing description give examples of embodiments. Those skilled in the art will appreciate that one or more of the described elements may well be combined into a single functional element. Alternatively, certain elements may be split into multiple functional elements. Elements from one embodiment may be added to another embodiment. For example, orders of processes described herein may be changed and are not limited to the manner described herein. Moreover, the actions of any flow diagram need not be implemented in the order shown; nor do all of the acts necessarily need to be performed. Also, those acts that are not dependent on other acts may be performed in parallel with the other acts. The scope of embodiments is by no means limited by these specific examples. Numerous variations, whether explicitly given in the specification or not, such as differences in structure, dimension, and use of material, are possible. The scope of embodiments is at least as broad as given by the following claims.

The following examples pertain to further embodiments. The various features of the different embodiments may be variously combined with some features included and others excluded to suit a variety of different applications. Some embodiments pertain to a method that includes attaching small dies on a wafer to a temporary carrier, aligning the dies over a plurality of larger host dies on a host wafer using the temporary carrier, applying the small

dies against the host dies using the temporary carrier so that a subset of the small dies bond to respective host dies, separating the temporary carrier so that the subset of bonded small dies are attached to a respective host die and the remaining small dies are separated with the temporary carrier, singulating the host dies, and packaging the host dies.

In further embodiments applying further comprises pressing the small dies against the host dies.

In further embodiments applying further comprises heating the small dies while pressing the small dies, the heating being at a temperature less than a solder reflow temperature.

Further embodiments include scribing through the small dies so that the small dies have scribe trenches to separate the dies through a portion of the small die wafer and thinning the small die wafer after attaching the dies to the temporary carrier so that the dies are separated by the scribe trenches.

In further embodiments the temporary carrier is attached to the front side of the dies, the method further comprising forming vias through the back sides of the dies to connect to a respective host die.

In further embodiments the temporary carrier is attached to the back side of the dies, the method further comprising forming through silicon vias on the front sides of the dies to connect to a respective host die.

Further embodiments include forming landing pads on the host dies at locations to be bonded to a small die and wherein the small dies bond to the host dies at the landing pads.

In further embodiments the landing pads are formed over a dielectric layer, the method further comprising removing a portion of the dielectric layer surrounding the landing pads to expose the landing pads to a respective small die.

In further embodiments the landing pads are formed over a dielectric layer, the method further comprising removing a portion of the dielectric layer beside the landing pads to prevent a small die beside the small die to be bonded to the host die from contacting the host die.

Further embodiments include attaching a solder ball to each of the landing pads wherein the small dies bond to the host dies at the landing pad through the solder ball.

In further embodiments the bond is a metal compression bond.

In further embodiments packaging comprises covering the small die in a dielectric and forming metal routing layers in the dielectric to connect the host die to external components.

In further embodiments packaging comprises attaching a solder ball array to the host die around the small die and attaching the solder ball array to a package substrate.

Some embodiments pertain to a multiple die package that includes a host die, a plurality of small dies smaller than the host die formed on a wafer, attached to a temporary carrier, aligned over the host die while on a host wafer using the temporary carrier, and applied against the host die using the temporary carrier, the small dies having a hybrid bond to the host die, and a package to cover the host die and the small dies together.

Further embodiments include landing pads on the host die at locations to be bonded to a small die, the landing pads being formed over a dielectric layer, and metal contacts on the small die to bond to the landing pads.

Further embodiments include a dielectric covering the small die and the host die and metal routing layers in the dielectric to connect the host die to external components.

Some embodiments pertain to a method that includes forming a plurality of small dies on a wafer, the small dies having metal contacts to attach to host dies, attaching the small dies to a temporary carrier, forming a plurality of larger host dies on a host wafer, formed a dielectric layer on at least a portion of each of the host dies, forming landing pads on the host dies at locations to be bonded to a small die, removing a portion of the dielectric layer surrounding the landing pads to expose the landing pads to a respective small die, aligning the dies over the host using the temporary carrier, heating the small dies, pressing the metal contacts of the small dies against the landing pads of the host dies using the temporary carrier so that a subset of the small dies bond to respective host dies, separating the temporary carrier so that the subset of bonded small dies are attached to a respective host die and the remaining small dies are separated with the temporary carrier, singulating the host dies, and packaging the host dies.

In further embodiments forming a plurality of small dies comprises forming the small dies using a first fabrication technology and wherein forming a plurality of host dies comprises forming the host dies using a second fabrication technology different from the first fabrication technology.

In further embodiments attaching the small dies to the temporary carrier comprising attaching the front sides of the dies to the temporary carrier, thinning the back sides of the dies, forming vias through the back sides of the dies to connect to a respective host die and separating the small dies from each other while attached to the temporary carrier.

In further embodiments packaging comprises covering the small die in a dielectric after separating the temporary carrier and forming metal routing layers in the dielectric to connect the small die to external components.

CLAIMS

1. A method comprising:
attaching small dies on a wafer to a temporary carrier;
aligning the dies over a plurality of larger host dies on a host wafer using the temporary carrier;
applying the small dies against the host dies using the temporary carrier so that a subset of the small dies bond to respective host dies;
separating the temporary carrier so that the subset of bonded small dies are attached to a respective host die and the remaining small dies are separated with the temporary carrier;
singulating the host dies; and
packaging the host dies.
2. The method of Claim 1, wherein applying further comprises pressing the small dies against the host dies.
3. The method of Claim 2, wherein applying further comprises heating the small dies while pressing the small dies, the heating being at a temperature less than a solder reflow temperature.
4. The method of any one or more of claims 1-3, further comprising scribing through the small dies so that the small dies have scribe trenches to separate the dies through a portion of the small die wafer and thinning the small die wafer after attaching the dies to the temporary carrier so that the dies are separated by the scribe trenches.
5. The method of any one or more of claims 1-4, wherein the temporary carrier is attached to the front side of the dies, the method further comprising forming vias through the back sides of the dies to connect to a respective host die.
6. The method of any one or more of claims 1-5, wherein the temporary carrier is attached to the back side of the dies, the method further comprising forming through silicon vias on the front sides of the dies to connect to a respective host die.
7. The method of any one or more of claims 1-6, further comprising forming landing pads on the host dies at locations to be bonded to a small die and wherein the small dies bond to the host dies at the landing pads.
8. The method of Claim 7, wherein the landing pads are formed over a dielectric layer, the method further comprising removing a portion of the dielectric layer surrounding the landing pads to expose the landing pads to a respective small die.

9. The method of Claim 7 or 8, wherein the landing pads are formed over a dielectric layer, the method further comprising removing a portion of the dielectric layer beside the landing pads to prevent a small die beside the small die to be bonded to the host die from contacting the host die.

10. The method of Claim 7 or 8, further comprising attaching a solder ball to each of the landing pads wherein the small dies bond to the host dies at the landing pad through the solder ball.

11. The method of any one or more of claims 1-10, wherein the bond is a metal compression bond.

12. The method of any one or more of claims 1-11, wherein packaging comprises covering the small die in a dielectric and forming metal routing layers in the dielectric to connect the host die to external components.

13. The method of any one or more of claims 1-12, wherein packaging comprises attaching a solder ball array to the host die around the small die and attaching the solder ball array to a package substrate.

14. A multiple die package comprising:
a host die;
a plurality of small dies smaller than the host die formed on a wafer, attached to a temporary carrier, aligned over the host die while on a host wafer using the temporary carrier, and applied against the host die using the temporary carrier, the small dies having a hybrid bond to the host die; and
a package to cover the host die and the small dies together.

15. The package of Claim 14, further comprising landing pads on the host die at locations to be bonded to a small die, the landing pads being formed over a dielectric layer, and metal contacts on the small die to bond to the landing pads.

16. The package of Claim 14 or 15, further comprising a dielectric covering the small die and the host die and metal routing layers in the dielectric to connect the host die to external components.

17. A method comprising:
forming a plurality of small dies on a wafer, the small dies having metal contacts to attach to host dies;
attaching the small dies to a temporary carrier;
forming a plurality of larger host dies on a host wafer;

formed a dielectric layer on at least a portion of each of the host dies;
forming landing pads on the host dies at locations to be bonded to a small die;
removing a portion of the dielectric layer surrounding the landing pads to expose the landing pads to a respective small die;
aligning the dies over the host using the temporary carrier;
heating the small dies;
pressing the metal contacts of the small dies against the landing pads of the host dies using the temporary carrier so that a subset of the small dies bond to respective host dies;
separating the temporary carrier so that the subset of bonded small dies are attached to a respective host die and the remaining small dies are separated with the temporary carrier;
singulating the host dies; and
packaging the host dies.

18. The method of Claim 17, wherein forming a plurality of small dies comprises forming the small dies using a first fabrication technology and wherein forming a plurality of host dies comprises forming the host dies using a second fabrication technology different from the first fabrication technology.

19. The method of Claim 17 or 18, wherein attaching the small dies to the temporary carrier comprising attaching the front sides of the dies to the temporary carrier, thinning the back sides of the dies, forming vias through the back sides of the dies to connect to a respective host die and separating the small dies from each other while attached to the temporary carrier.

20. The method of Claim 17, 18, or 19, wherein packaging comprises covering the small die in a dielectric after separating the temporary carrier and forming metal routing layers in the dielectric to connect the small die to external components.

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FIG. 1

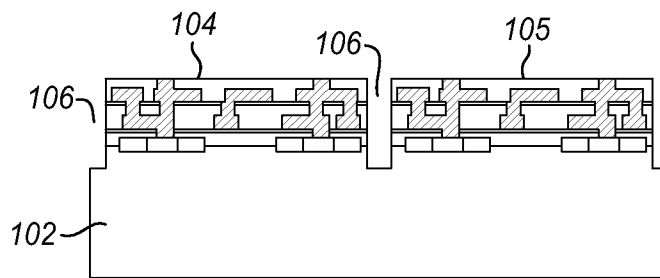


FIG. 2

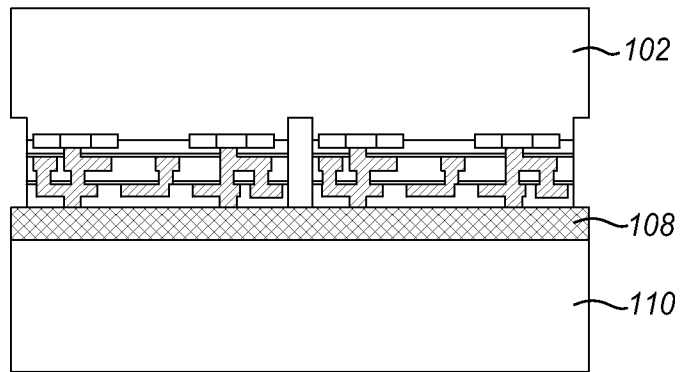


FIG. 3

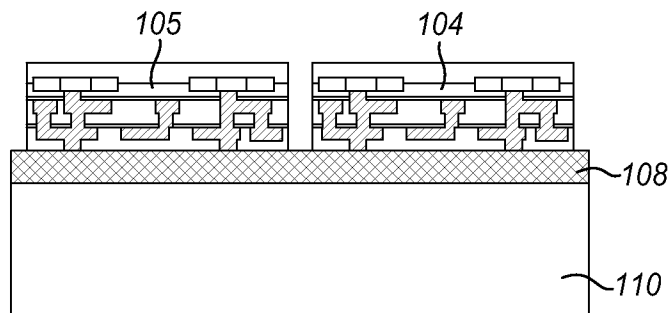


FIG. 4

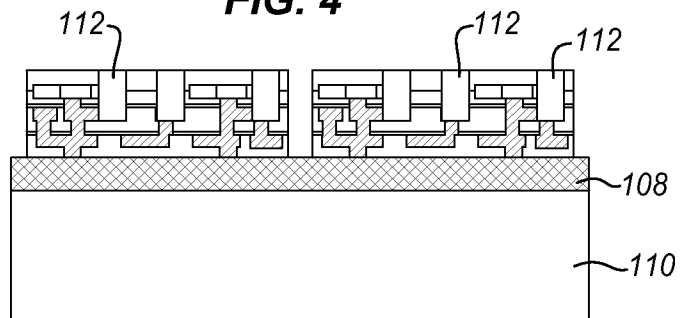


FIG. 5

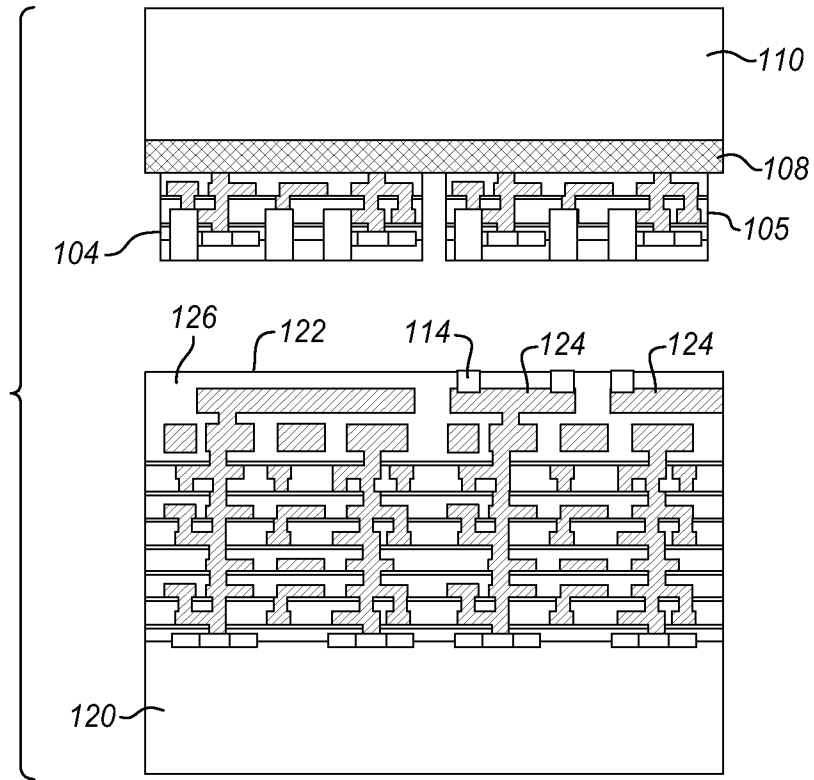


FIG. 6

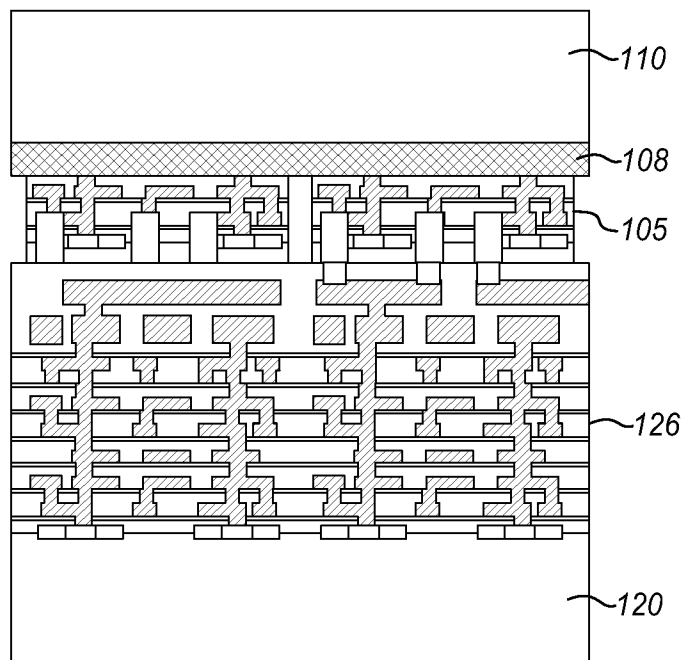


FIG. 7

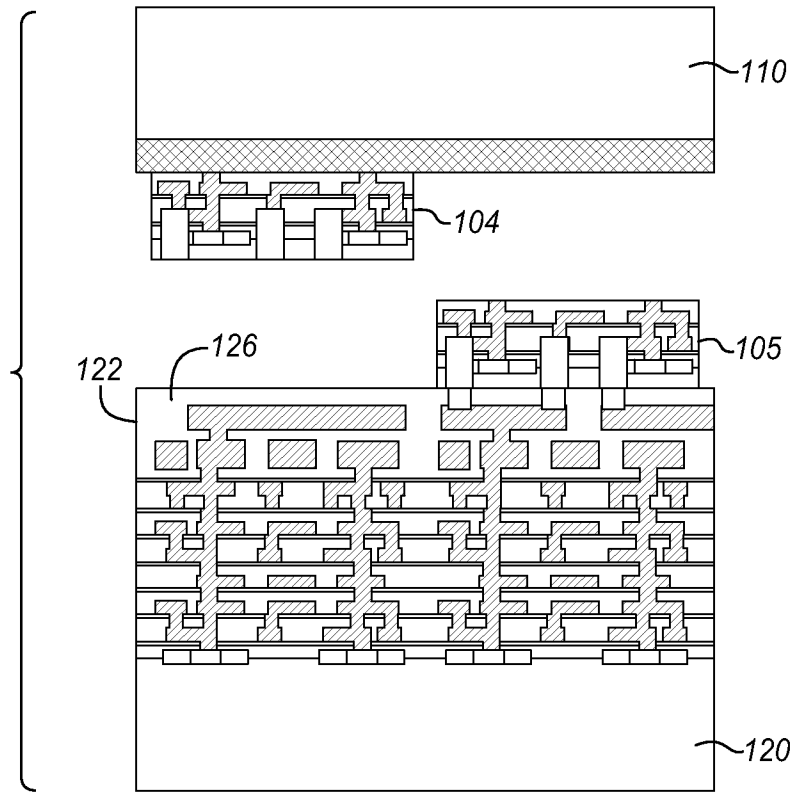


FIG. 8

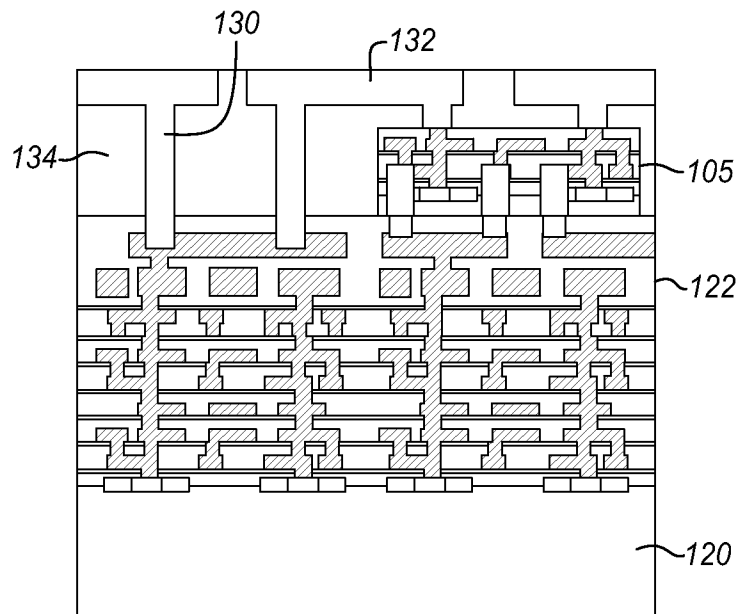


FIG. 9

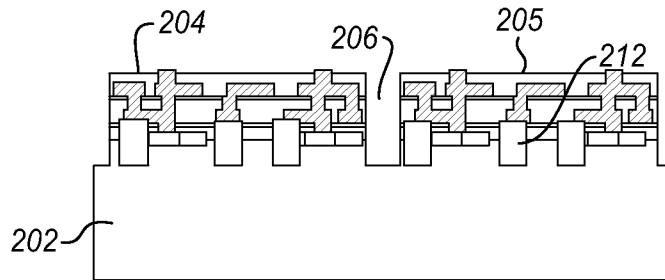


FIG. 10

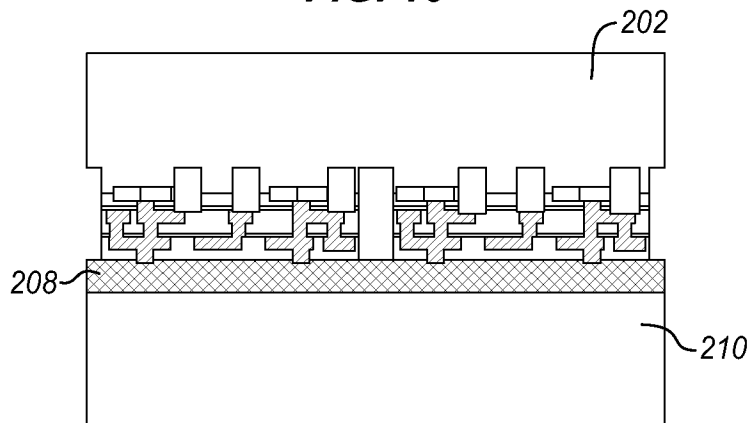


FIG. 11

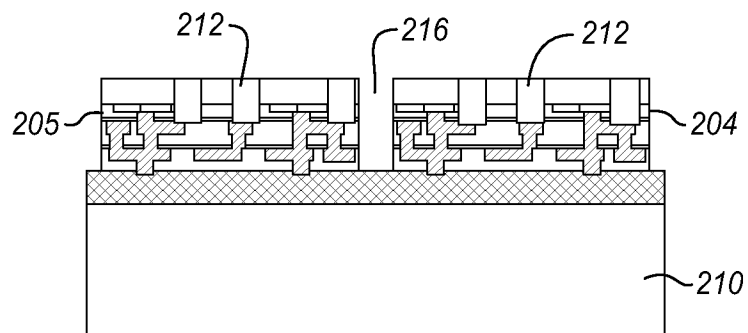


FIG. 12

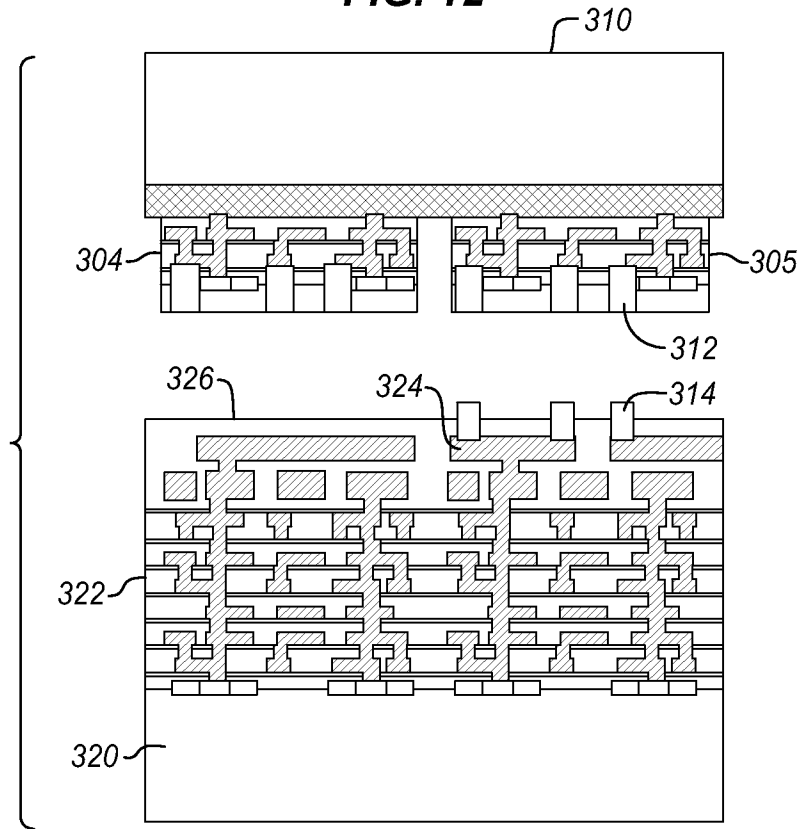


FIG. 13

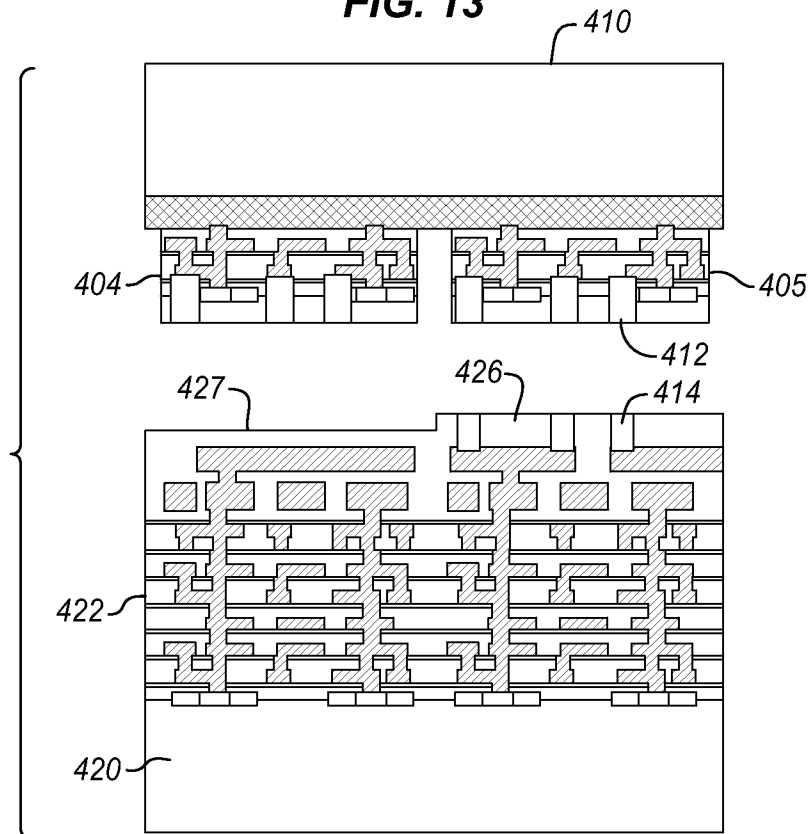


FIG. 14

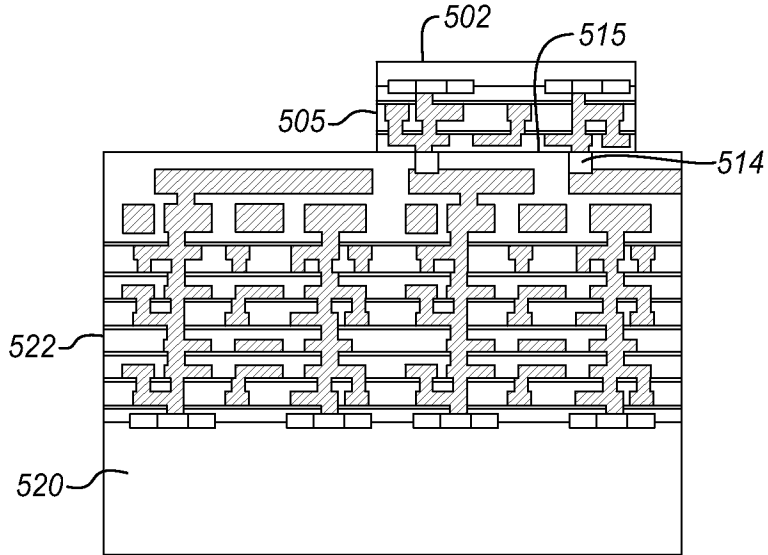


FIG. 15

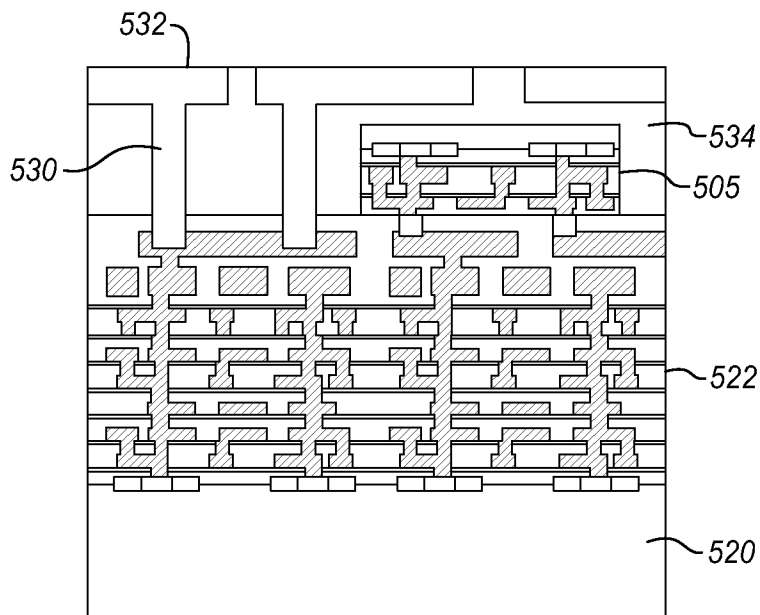


FIG. 16

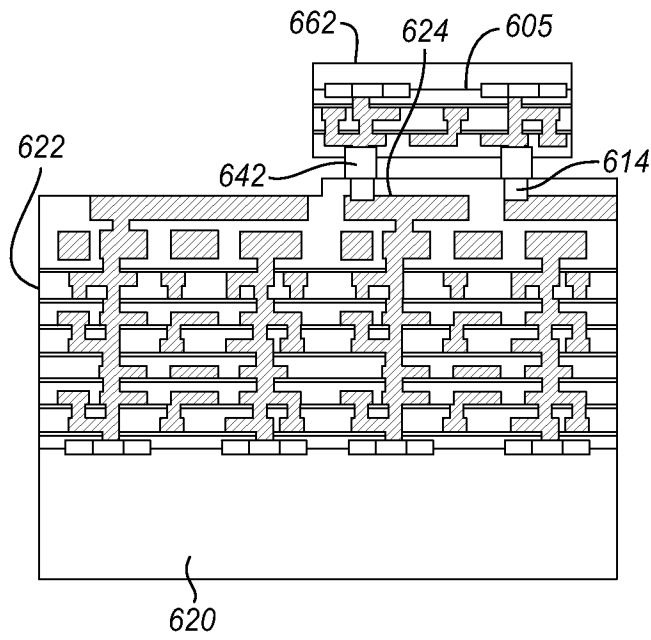


FIG. 17

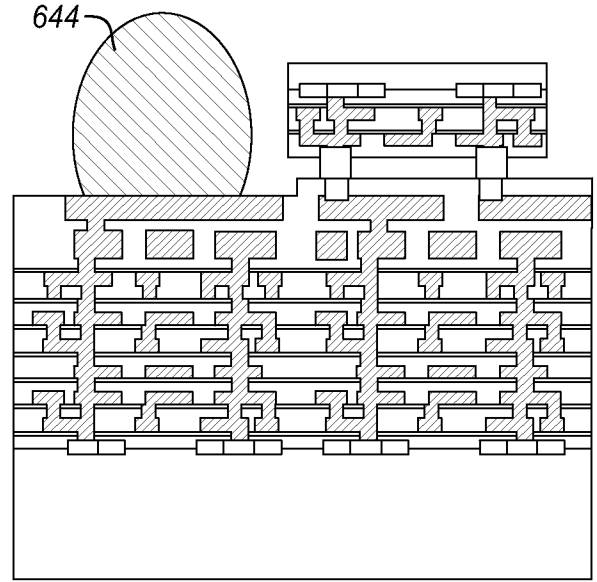


FIG. 18

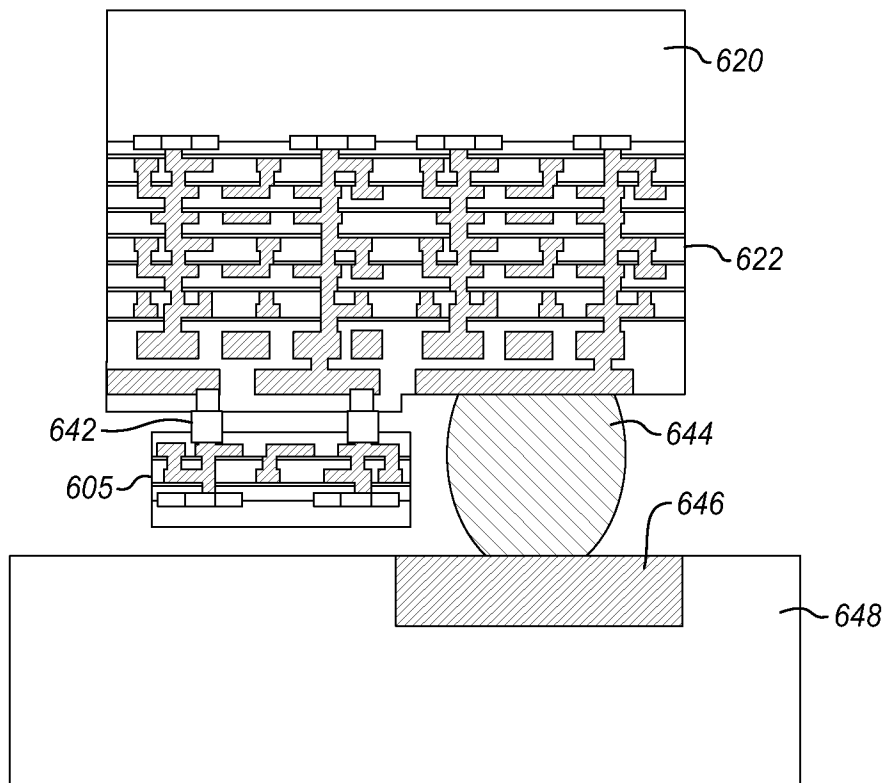
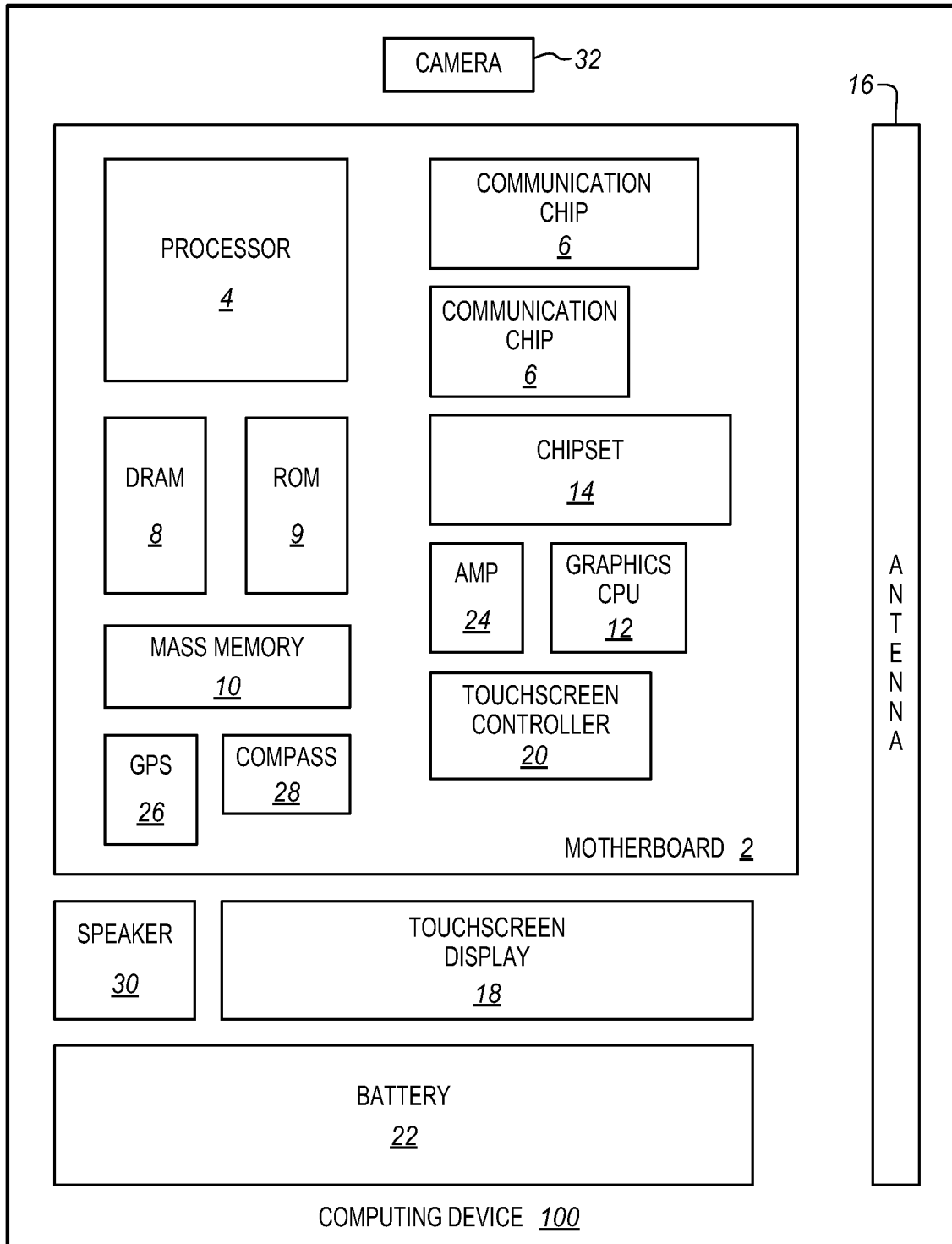


FIG. 19



A. CLASSIFICATION OF SUBJECT MATTER**H01L 25/065(2006.01)i, H01L 23/48(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; H01L 31/028; H05K 1/18; H01L 21/68; H05K 7/20; H01L 21/677; H01L 33/60; H01L 23/522; H01L 21/66; H01L 21/683; H01L 21/98; H01L 23/48

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: temporary carrier, small die, host die, separating, subset

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2013-0122617 A1 (CONNECTOR OPTICS LLC) 16 May 2013 See abstract, paragraphs [0070], [0075], [0076] and figures 10, 14.	1-2, 14
Y		3, 15-16
A		17-19
Y	US 2012-0027557 A1 (IAN ASHDOWN et al.) 02 February 2012 See abstract, paragraph [0032] and figures 5-7.	3
Y	US 2010-0290191 A1 (MOU-SHIUNG LIN et al.) 18 November 2010 See abstract, paragraphs [0149], [0175] and figures 18-21.	15-16
A	EP 2339614 A1 (IMEC) 29 June 2011 See abstract, paragraphs [0010]-[0011] and figures 1C-2.	1-3, 14-19
A	KR 10-2014-0098864 A (HARRIS CORPORATION) 08 August 2014 See abstract, claim 1 and figure 4.	1-3, 14-19

 Further documents are listed in the continuation of Box C. See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

22 June 2016 (22.06.2016)

Date of mailing of the international search report

22 June 2016 (22.06.2016)

Name and mailing address of the ISA/KR

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Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.: 8
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
Claim 8 was found unsearchable, because this claim refers to unsearchable multiple dependent claim, which is not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

3. Claims Nos.: 4-7, 9-13, 20
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.

3. As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2015/052475

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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