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(54) Title: METHODS OF MAKING AND USING TIN OXIDE FILM WITH SMOOTH SURFACE MORPHOLOGIES

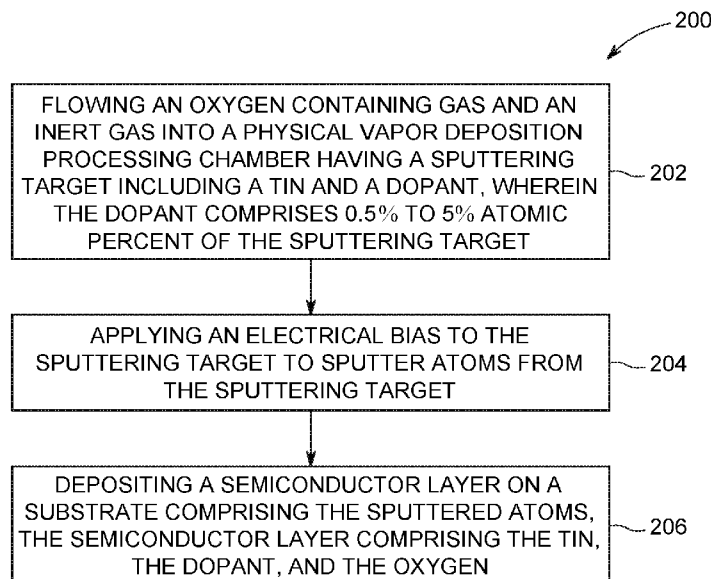


FIG. 2

(57) Abstract: The present disclosure generally relates to tin oxide films prepared by physical vapor deposition using a doped tin target. The semiconductor film may include tin and oxygen, and may be formed in a PVD chamber including a silicon doped tin target. Additionally, the semiconductor film may be smooth compared to similarly formed films without a doped target. The semiconductor film may be deposited by applying an electrical bias to a sputtering silicon doped tin target including the silicon in an amount of 0.5 to 5% by atomic weight of the total target. The semiconductor film has a smooth surface morphology compared to similarly formed tin oxide films formed without a doped target.

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METHODS OF MAKING AND USING TIN OXIDE FILM WITH SMOOTH SURFACE MORPHOLOGIES

FIELD

[0001] Embodiments of the present disclosure generally relate to a semiconductor material, and a method for depositing the semiconductor material.

BACKGROUND

[0002] Physical vapor deposition (PVD) is one of the most commonly used processes in fabrication of electronic devices. PVD is a plasma process performed in a vacuum chamber where a negatively biased target is exposed to a plasma of an inert gas having relatively heavy atoms (e.g., argon) or a gas mixture comprising such inert gas. Bombardment (or sputtering) of the target by ions of the inert gas results in ejection of atoms of the target material. The ejected atoms accumulate as a deposited film on a substrate placed on a substrate pedestal disposed underneath the target within the chamber.

[0003] The inventors have found that deposited film on the substrate, such as a tin oxide film, may have varied surface morphologies resulting in adverse effects in downstream processing such as lithography and etching. For example, during downstream photolithographic processing, a rougher surface of a deposited film may have a negative effect on the roughness of line sidewalls or cause higher line edge roughness (LER) or line width roughness (LWR) resulting in decreased device performance.

[0004] Therefore, the inventors have provided improved semiconductor processing methods and chamber components for forming one or more semiconductor layers such as tin oxide or tin rich tin oxide having substantially smooth surface morphologies.

SUMMARY

[0005] Methods and apparatus for depositing the semiconductor material are provided herein. In some embodiments, a method includes: flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin and a dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering

target to sputter atoms from the sputtering target; and depositing a semiconductor layer on a substrate comprising the sputtered atoms, the semiconductor layer comprising the tin, the dopant, and the oxygen.

[0006] In some embodiments, a method includes flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and depositing a semiconductor layer comprising the sputtered atoms on a substrate.

[0007] In some embodiments, a method includes forming a semiconductor layer including: flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target; and depositing a semiconductor layer on a substrate, the semiconductor layer comprising tin oxide composition or tin rich tin oxide composition.

[0008] Other and further embodiments of the present disclosure are described below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Embodiments of the present disclosure, briefly summarized above and discussed in greater detail below, can be understood by reference to the illustrative embodiments of the disclosure depicted in the appended drawings. However, the appended drawings illustrate only typical embodiments of the disclosure and are therefore not to be considered limiting of scope, for the disclosure may admit to other equally effective embodiments.

[0010] Figure 1 is a schematic cross sectional view of a sputtering chamber that may be used to deposit the semiconductor film according to one embodiment of the disclosure.

[0011] Figure 2 is a flow chart of a sputtering method in accordance with some embodiments of the present disclosure.

[0012] Figure 3 is a flow chart of a method of sputtering in accordance with some embodiments of the present disclosure.

[0013] Figure 4 is a flow chart of a method of forming a semiconductor layer in accordance with some embodiments of the present disclosure.

[0014] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. The figures are not drawn to scale and may be simplified for clarity. Elements and features of one embodiment may be beneficially incorporated in other embodiments without further recitation.

DETAILED DESCRIPTION

[0015] Embodiments of depositing a semiconductor layer are provided herein. For example the present disclosure relates to a sputtering method, including: flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including tin and a dopant, wherein the dopant includes 0.5% to 5% atomic weight of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and depositing a semiconductor layer on a substrate including the sputtered atoms. The methods and apparatus of the present disclosure are advantageous in that they provide very smooth surfaced semiconductor films such as tin oxide films deposited by a PVD process. The films are advantageous in providing smooth surface morphology and facilitating downstream processing such as lithography and etching. For example, during downstream photolithographic processing, a smoother surface of a deposited film may have a positive effect on reducing roughness of line sidewalls or cause lower line edge roughness (LER) or line width roughness (LWR) resulting in increased device performance, or lower lithographic dosing requirements.

[0016] In some embodiments, a reactive sputtering method is described and may be practiced in a PVD chamber for processing substrates, such as a PVD chamber, available from Applied Materials, Inc., of Santa Clara, California. However, because the semiconductor layer or film produced according to the method may be determined by the semiconductor layer structure and composition, the reactive sputtering method may

have utility in other system configurations, including systems produced by other manufacturers. While the present disclosure is illustratively described below as deposited by PVD, other methods including chemical vapor deposition (CVD), atomic layer deposition (ALD), or spin-on processes may be utilized to deposit the semiconductor layers or films of the present disclosure.

[0017] Figure 1 is a cross-sectional schematic view of a PVD chamber 100 according to one embodiment of the present disclosure. The PVD chamber 100 may be evacuated by a vacuum pump 114. Within the PVD chamber 100, a substrate 102 may be disposed opposite a target 104. In some embodiments, the substrate 102 may include plastic, paper, polymer, glass, stainless steel, silicon, germanium, silicon-germanium and combinations thereof. When the substrate is plastic, the reactive sputtering may occur at temperatures below about 180°C. In embodiments, substrate 102 may include silicon wafers, glass substrates, soda lime glass substrates, plastic substrates, etc. The substrate 102 may comprise any shape or size such as 200 mm wafers, 300 mm wafers, 400 mm wafers, flat panel substrates, polygonal substrates, roll-to-roll substrates, etc.

[0018] Still referring to Figure 1, the substrate 102 may optionally be disposed on a susceptor 106 within the PVD chamber 100. The susceptor 106 may be elevated and lowered as shown by arrows "A" by an actuator 112. The susceptor 106 may be elevated to raise the substrate 102 to a processing position and lowered so that the substrate 102 may be removed from the PVD chamber 100. Lift pins 108 elevate the substrate 102 above the susceptor 106 when the susceptor 106 is in the lowered position. Grounding straps 110 may ground the susceptor 106 during processing. The susceptor 106 may be raised during processing to aid in uniform deposition. The temperature of the susceptor 106 may be maintained within a range of about room temperature to about 400°C. In one embodiment, the temperature of the susceptor 106 may be maintained between about 25°C and about 250°C. In embodiments, the temperature of the PVD chamber 100 may be maintained within a range of about room temperature to about 400°C, or in embodiments, about 25°C to about 400°C. In one embodiment, the temperature of PVD chamber 100 may be maintained between about 25°C and about 250°C. In some embodiments, the PVD chamber 100 is at a

temperature of about 16°C to 25°C. In some embodiments, the PVD chamber 100 is at room temperature. In embodiments, an anode 124 may be placed between the target 104 and the substrate 102.

[0019] In some embodiments, the target 104 may include one or more targets 104 such as a sputtering target. In one embodiment, the target 104 may include a large area sputtering target. In another embodiment, the target 104 may comprise a plurality of tiles. In yet another embodiment, the target 104 may comprise a plurality of target strips. In still another embodiment, the target 104 may comprise one or more cylindrical, rotary targets. The target 104 may be bonded to a backing plate 116 by a bonding layer (not shown). One or more magnetrons 118 may be disposed behind the backing plate 116. In embodiments, the magnetrons 118 may scan across the backing plate 116 in a linear movement or in a two dimensional path. The walls of the chamber may be shielded from deposition by a dark space shield 120 and a chamber shield 122.

[0020] In embodiments, the target 104 such as a sputtering target may comprise, consists essentially of, or consist of tin and one or more dopants. The inventors have found the amount of dopant affects the morphology or surface roughness of the deposited film. In some embodiments, the ratio of a silicon dopant to the tin in the target may affect the smoothness and morphology of the semiconductor film. For example small amounts of silicon compared to tin in the target promotes smooth and substantially smooth semiconductor layer formation. For example, target 104 may comprise or consists essentially of tin and a silicon dopant. The dopant, such as silicon, may be present in an amount of between about 0.5% to 5% (atomic percentage) of the total target composition, or between about 0.5% to 5% (atomic percentage) of the total target composition, or between about 1% to about 5% (atomic percentage) of total target composition, or between 1% to about 5% (atomic percentage) of total target composition, or about 1%, 2%, 3%, 4% or 5% (atomic percentage) of target composition. Atomic percentage as expressed herein may be converted to percent by weight of the total target composition. In some embodiments where there is an atomic percentage of silicon, the remaining percentage of the target may be tin. In some embodiments, the present disclosure provides target 104 configured for use in a PVD

chamber as described herein. In some embodiments, the present disclosure provides a PVD chamber 100 including one or more targets 104 as described herein.

[0021] In some embodiments, to promote uniform sputtering deposition across a substrate 102, an anode 124 may be placed between the target 104 and the substrate 102. In one embodiment, the anode 124 may be bead blasted stainless steel coated with arc sprayed aluminum. In one embodiment, one end of the anode 124 may be mounted to the chamber wall by a bracket 130. The anode 124 provides a charge in opposition to the target 104 so that charged ions will be attracted thereto rather than to the chamber walls which are typically at ground potential. By providing the anode 124 between the target 104 and the substrate 102, the plasma may be more uniform, which may aid in the deposition. To reduce flaking, a cooling fluid may be provided through the one or more anodes 124. By reducing the amount of expansion and contraction of the anodes 124, flaking of material from the anodes 124 may be reduced. For smaller substrates and hence, smaller processing chambers, the anodes 124 spanning the processing space may not be necessary as the chamber walls may be sufficient to provide a path to ground and a uniform plasma distribution.

[0022] In embodiments, the reactive sputtering process may include disposing a sputtering target as described above opposite a substrate in a sputtering chamber. The sputtering target may substantially include tin, and comprise a dopant such as silicon in amounts sufficient to form a substantially smooth semiconductor layer. In embodiments, the semiconductor layer may also be annealed after depositing.

[0023] In some reactive sputtering embodiments, one or more gases such as a reactive gas may be provided into the PVD chamber 100. In embodiments, one or more gas introduction tubes 126 may span the distance across the PVD chamber 100 between the target 104 and the substrate 102. In embodiments, the gas introduction tubes 126 may introduce sputtering gases from a gas panel 132. The gas introduction tubes 126 may be coupled with the anodes 124 by one or more couplings 128. The coupling 128 may be made of thermally conductive material to permit the gas introduction tubes 126 to be conductively cooled. Additionally, the coupling 128 may be electrically conductive as well so that the gas introduction tubes 126 are grounded and function as anodes.

[0024] In some embodiments, during the sputtering process, inert gas such as argon, and an oxygen containing gas may be provided to the chamber for reactive sputtering of the target 104. In one embodiment, the oxygen containing gas comprises or consists of O_2 . In embodiments, the oxygen of the oxygen containing gas react with the sputtering target to form a semiconductor material comprising metal, oxygen, and optionally a dopant such as silicon on the substrate. In one embodiment, the inert gas such as argon and the oxygen containing gas are separate gases. In another embodiment, the inert gas such as argon and the oxygen containing gas include the same gas. In some embodiments, the inert gas such as argon gas is provided at a flow rate is between 1 to 200 sccm, 10 to 100 sccm, or 20 to 60 sccm. In some embodiments the oxygen containing gas or oxygen gas is provided at a flow rate is between 1 to 200 sccm, 10 to 100 sccm, or 20 to 60 sccm. In one embodiment, argon gas flow rate is about 60 sccm, and the oxygen flow rate is about 5 sccm. In one embodiment, inert gas such as argon gas flow rate is about 60 sccm, and the oxygen flow rate is about 5 sccm.

[0025] In some embodiments, the reactive sputtering process as described herein forms semiconductor layers on the surface of the substrate. In embodiments, a doped tin target is suitable for forming a semiconductor layer such as a tin oxide or tin rich tin oxide semiconductor layer. To produce a coating of the tin oxide or tin rich tin oxide on a substrate, the semiconductor layer typically formed by sputtered the target described above onto a substrate under the conditions described herein. In some embodiments, one or more semiconductor layers such as tin oxide layer or tin rich tin oxide layer is in the form of a sheet or foil having a suitable thickness, such as, a thickness of or less than 1 mm, 0.5 mm, 0.1 mm, 0.05 mm, 0.01 mm, or 0.001 mm, or 100 angstrom or 50 angstrom or a range between any two of these values. Alternatively, the foregoing thicknesses describe the thickness of a tin oxide or tin rich tin oxide coating on a substrate. In some embodiments, the semiconductor layer may include a mixture of silicon, tin and oxygen, or a mixture of silicon-doped tin oxide (TSO). Other non-limiting examples of semiconductor layers include layers deposited as films include SnO_x , tin oxide, tin rich tin oxide, tin dioxide, and combinations thereof. In some embodiments, the semiconductor deposited film may include a tin oxide or composition characterized as Sn_xO_y . In embodiments, x and y are numbers such as decimals, or integers. In

another embodiment, the semiconductor film may include a first tin oxide compound and a second tin oxide compound.

[0026] While the semiconductor layer or film is described as being deposited by sputtering a tin target including a dopant, other deposition methods may be utilized. In one embodiment, the sputtering target in accordance herewith may be biased with an RF current. In embodiments, DC current may be applied to the target. In some embodiments, power is applied to the sputtering target in an amount of about 1 to about 500 KW. In some embodiments, sputtering a tin target doped with silicon includes sputtering for about 20 to 360 seconds while a DC bias of 1 to about 400 KW was applied to the sputtering target. In some embodiments sputtering a tin target doped with silicon as described herein includes sputtering for up to 360 seconds while a DC bias of up to 500 KW was applied to the sputtering target. Argon may introduced to the processing chamber at a flow rate of up to about 100 sccm, and oxygen may be introduced at a flow rate of up to about 30 sccm. In embodiments, a semiconductor layer having a thickness of 100 angstroms may be formed by sputtering for a duration of 20 seconds to 2 minutes, or about 60 seconds, or 60 seconds.

[0027] In some embodiments, argon containing gas to oxygen containing gas flow ratios of about 1:1 to about 10:1 may produce semiconductor films with smoothness sufficient to reduce an EUV lithography dose by 5-10% during EUV lithographic patterning. In one embodiment, the argon containing gas to oxygen containing gas flow ratios may be between about 5:1 to about 10:1.

[0028] In embodiments, by controlling the proportionate amount of oxygen gas flow relative to the amount of inert gas such as argon, the RMS value and smoothness of the deposited semiconductor layer may be controlled. When increasing the amount of oxygen supplied relative to the inert gas such as argon, the RMS value may be increased. A lower RMS value may be desirable for the semiconductor layer of the present disclosure. In embodiments, the morphology of the deposited semiconductor layer in accordance with the present disclosure on a substrate can be tested using a multi-mode atomic force microscope (MM-AFM) and accompanying hardware. In embodiments, RMS output is a suitable indicator of roughness or smoothness. For

example, as described in ASME B46.1, RMS is the root mean square average of the profile height deviations from the mean line, recorded within the evaluation length. The deposited semiconductor film in accordance with the present disclosure may have an RMS value in the about of 0.1 to 0.4 nanometers at room temperature and a thickness of 100 angstrom. In embodiments, having an RMS value in the amount of 0.1 to 0.4 nanometers at room temperature and a thickness of 100 angstrom indicates the deposited material is substantially smooth in accordance with the present disclosure. In embodiments, having an RMS value in the amount of 0.2 to 0.3 nanometers at room temperature and a thickness of 100 angstrom indicates the deposited material is substantially smooth in accordance with the present disclosure. In embodiments, having an RMS value in the amount of 0.20 to 0.25 nanometers at room temperature and a thickness of 100 angstrom indicates the deposited material is substantially smooth in accordance with the present disclosure. However, other methods of measuring surface roughness may include roughness measured by manual comparison against a "surface roughness comparator" (a sample of known surface roughness).

[0029] Referring now to Figure 2, a sputtering method 200, includes: 202 flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin and a dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target; 204 applying an electrical bias to the sputtering target; and 206 depositing a semiconductor layer on a substrate, the semiconductor layer including or consisting of the tin, the dopant, and the oxygen.

[0030] In embodiments, the semiconductor layer comprises or consists of tin oxide, SnO_x , or tin dioxide. In some embodiments, the dopant comprises or consists of silicon. In some embodiments, at least a portion of the semiconductor layer comprises a tin oxide compound and a silicon compound. In some embodiments, the semiconductor layer has a substantially smooth surface morphology. In embodiments, the oxygen containing gas and the inert gas are separate gases. In some embodiments, the physical vapor deposition processing chamber is at a temperature of about 16°C to 25°C, and a pressure of about 3 to 6 milliTorr.

[0031] In embodiments, a sputtering method includes the method shown in Figure 3. In some embodiments, sputtering methods include at process sequence 310: flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target, and subsequently, at process sequence 320 applying an electrical bias to the sputtering target. In some embodiments, the methods include at process sequence 330, depositing a semiconductor layer on a substrate. In some embodiments, the silicon dopant comprises 0.5 to 4.0 atomic percent of the sputtering target. In some embodiments, the silicon dopant comprises 0.5 to 3.0 atomic percent of the entire sputtering target. In some embodiments, the silicon dopant comprises 0.5 to 2.0 atomic percent of the sputtering target. In some embodiments, the silicon dopant comprises 0.5 to 1.0 atomic percent of the sputtering target.

[0032] In some embodiments, a method of forming a semiconductor layer is provided as shown in Figure 4. The method 400 includes, at 410 flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target. Method 400 includes at process sequence 420 applying an electrical bias to the sputtering target. Method 400 includes at process sequence 430 depositing a semiconductor layer on a substrate, the semiconductor layer comprising tin oxide composition or tin rich tin oxide composition. In some embodiments, the semiconductor layer consists of tin oxide composition or tin rich tin oxide composition.

[0033] In some embodiments, a method includes: flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin and a dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the target; and depositing a semiconductor layer on a substrate comprising the sputtered atoms, the semiconductor layer comprising the tin, the dopant, and the oxygen.

[0034] In some embodiments, a method includes flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the target; and depositing a semiconductor layer comprising the sputtered atoms on a substrate. For example, referring to Figure 3, method 300 relating to a sputtering method includes at process sequence 310 flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target. The process sequence further includes at 320 applying an electrical bias to the sputtering target to sputter atoms from the sputtering target. The process sequence further includes at 330, depositing a semiconductor layer comprising the sputtered atoms on a substrate. In embodiments, the semiconductor layer has a substantially smooth surface morphology. In embodiments, the oxygen containing gas and the argon gas are separate gases. In embodiments, the physical vapor deposition processing chamber is at a temperature of about 16°C to 25°C. In embodiments, the physical vapor deposition processing chamber is at a pressure of about 3 to 6 milliTorr. In embodiments, power is applied to the sputtering target in an amount of about 1 to about 500 KW.

[0035] Referring back to Figure 1, the processing chamber can be controlled by a microprocessor controller (not shown). The microprocessor controller may be one of any form of general purpose computer processor or central processing unit (CPU) that can be used in an industrial setting for controlling various chambers and sub-processors. The computer processor may use any suitable memory, such as random access memory, read only memory, floppy disc drive, hard disk, or any other form of digital storage, local or remote. Various support circuits may be coupled to the CPU for supporting the processor in a conventional manner. Software routines, as required, may be stored in the memory or executed by a second CPU that is remotely located.

[0036] The software routines are executed after the substrate is positioned on the substrate support. The software routines, when executed, transform the general purpose computer into a specific process computer that controls the chamber operation

so that a chamber process is performed. Alternatively, the software routines may be performed in hardware as an application specific integrated circuit or other type of hardware implementation, or a combination of software and hardware.

[0037] In another embodiment, a non-transitory computer readable medium having instructions stored thereon that, when executed, cause a sputtering method such as e.g., a deposition in accordance with the present disclosure. For example, in embodiments, a non-transitory computer readable medium having instructions stored thereon that, when executed, cause a sputtering method, including flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin and a dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and depositing a semiconductor layer on a substrate comprising the sputtered atoms, the semiconductor layer comprising or consisting of the tin, the dopant, and the oxygen.

[0038] In embodiments, the present disclosure includes a non-transitory computer readable medium having instructions stored thereon that, when executed, cause a sputtering method, including flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and depositing a semiconductor layer comprising the sputtered atoms on a substrate.

[0039] In embodiments, the present disclosure includes a non-transitory computer readable medium having instructions stored thereon that, when executed, cause a method of forming a semiconductor layer, including: flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target; applying an electrical bias to the sputtering target; and depositing a semiconductor layer on a substrate, the semiconductor layer comprising tin oxide composition or tin rich tin oxide composition.

[0040] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof.

Claims:

1. A sputtering method, comprising:
flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin and a dopant, wherein the dopant comprises 0.5% to 5% atomic percent of the sputtering target;
applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and
depositing a semiconductor layer on a substrate comprising the sputtered atoms, the semiconductor layer comprising the tin, the dopant, and the oxygen.
2. The method of claim 1, wherein the semiconductor layer comprises tin oxide, SnO_x , tin rich tin oxide, or tin dioxide.
3. The method of claims 1 or 2, wherein the dopant is silicon.
4. The methods of any of claims 1-3, wherein at least a portion of the semiconductor layer comprises a tin oxide compound and a silicon compound.
5. The methods of any of claims 1-4, wherein the semiconductor layer has a substantially smooth surface morphology having an RMS value in an amount of 0.1 to 0.4 nanometers.
6. The methods of any of claims 1-5, wherein the oxygen containing gas and the inert gas are separate gases prior to mixing in the physical vapor deposition processing chamber.
7. The methods of any of claims 1-6, wherein the physical vapor deposition processing chamber is at a temperature of about 16°C to 25°C.

8. The methods of any of claims 1-7, wherein the physical vapor deposition processing chamber is at a pressure of about 3 to 6 milliTorr.
9. The methods of any of claims 1-8, wherein power is applied to the sputtering target in an amount of about 1 to about 500 KW.
10. A sputtering method, comprising:
 - flowing an oxygen containing gas and argon gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target;
 - applying an electrical bias to the sputtering target to sputter atoms from the sputtering target; and
 - depositing a semiconductor layer comprising the sputtered atoms on a substrate.
11. The method of claim 10, wherein the semiconductor layer has a substantially smooth surface morphology.
12. The method of claims 10 or 11, wherein the oxygen containing gas and the argon gas are separate gases.
13. The methods of any of claim 10-12, wherein the physical vapor deposition processing chamber is at a temperature of about 16°C to 25°C, at a pressure of about 3 to 6 milliTorr, and wherein power is applied to the sputtering target in an amount of about 1 to about 500 KW.
14. A method of forming a semiconductor layer, comprising:
 - flowing an oxygen containing gas and an inert gas into a physical vapor deposition processing chamber having a sputtering target including a tin metal and a silicon dopant, wherein the silicon dopant comprises 0.5% to 5% atomic percent of the sputtering target;

applying an electrical bias to the sputtering target; and
depositing a semiconductor layer on a substrate, the semiconductor layer comprising tin oxide composition or tin rich tin oxide composition.

15. The method of claim 15, wherein the semiconductor layer has a substantially smooth surface morphology.

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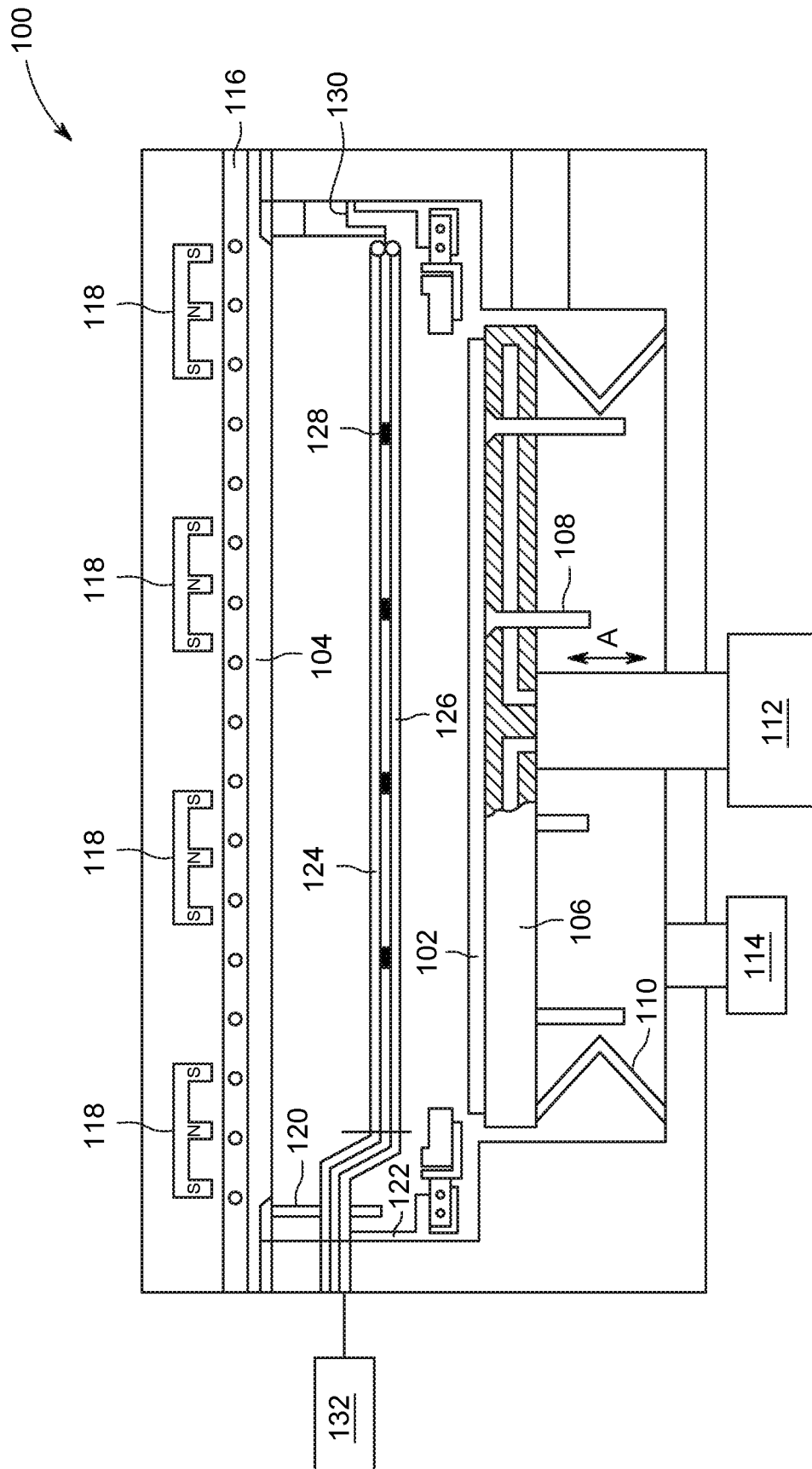


FIG. 1

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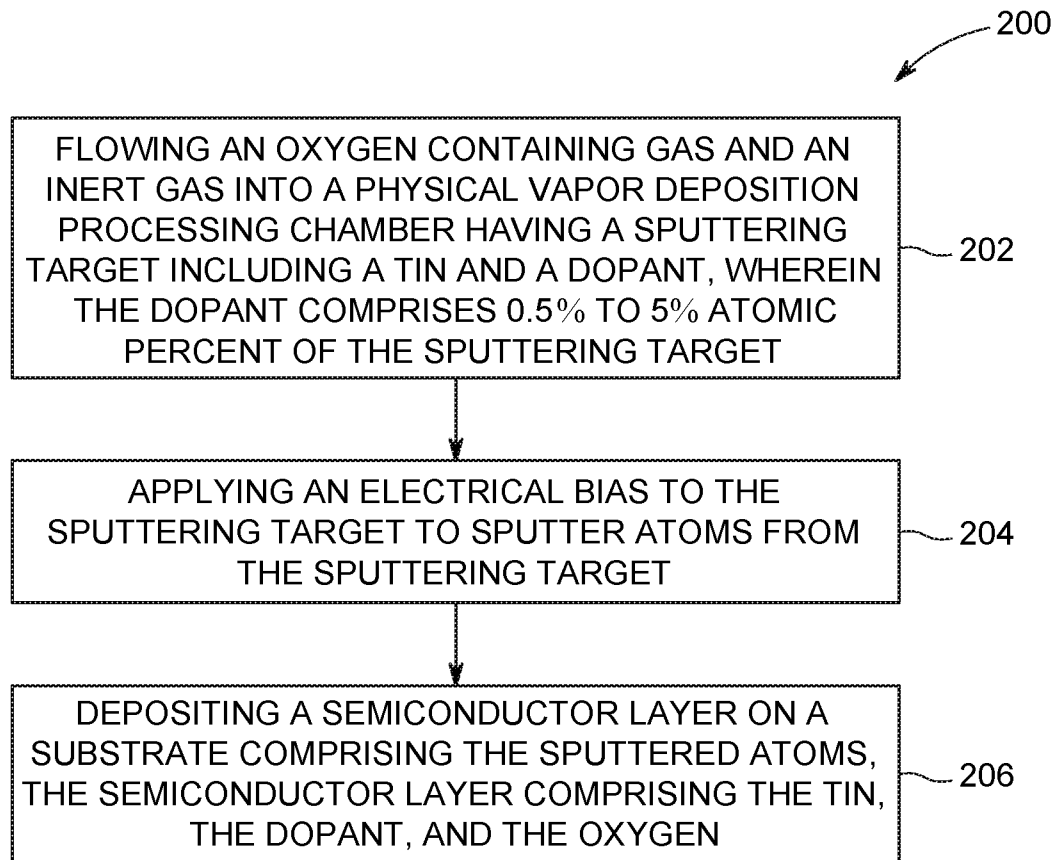


FIG. 2

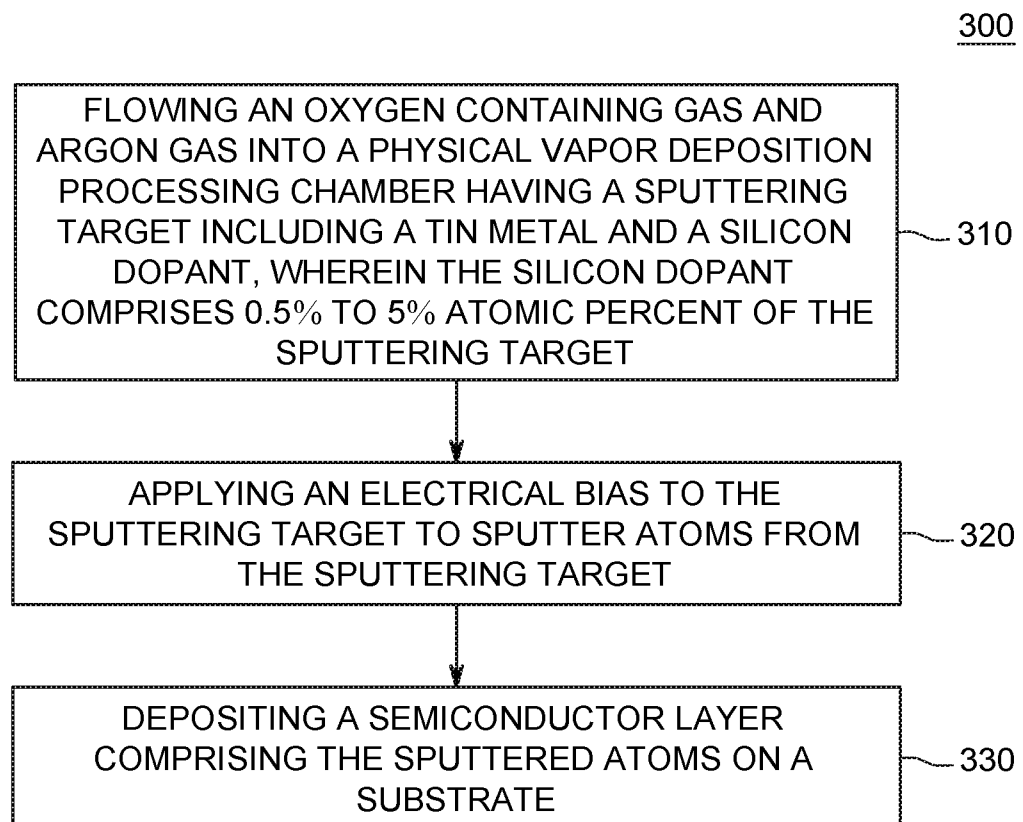


FIG. 3

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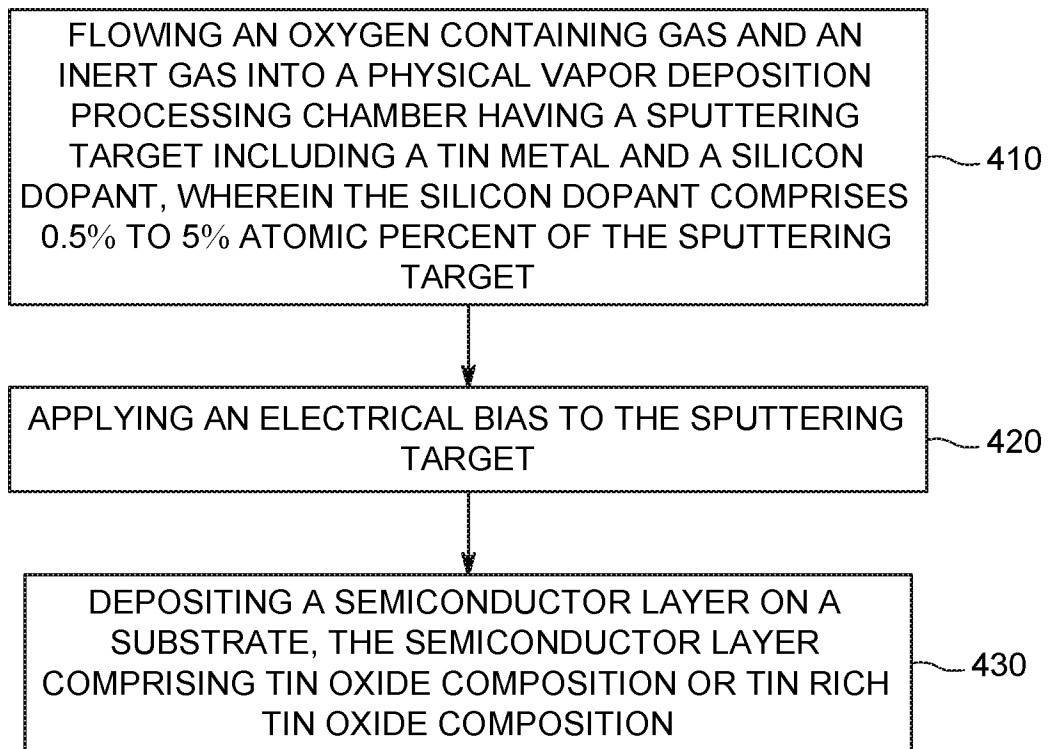
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FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2019/030303**A. CLASSIFICATION OF SUBJECT MATTER****H01L 21/28(2006.01)i, H01L 21/285(2006.01)i, H01L 21/02(2006.01)i, H01L 21/324(2006.01)i, C23C 14/34(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 21/28; B22F 3/14; B32B 17/06; B32B 5/00; C23C 14/00; C23C 14/34; C23C 16/06; C23C 16/40; H01L 21/363; H01L 21/285; H01L 21/02; H01L 21/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: sputtering, oxygen, tin, target, silicon, dopant, deposit, SnO

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 8980066 B2 (YAN YE) 17 March 2015 See column 3, line 33 - column 4, line 51, column 5, lines 60-62, column 6, lines 58-59 and claims 1, 3.	1-3, 10-12, 14-15
Y	US 2008-0261035 A1 (JEAN-MICHEL GRIMAL et al.) 23 October 2008 See paragraph [0055].	1-3, 10-12, 14-15
A	US 8097302 B2 (ROMAN Y. KOROTKOV et al.) 17 January 2012 See column 4, lines 35-52 and claim 1.	1-3, 10-12, 14-15
A	US 2008-0206923 A1 (CHANG-JUNG KIM et al.) 28 August 2008 See claims 1, 7 and figure 1.	1-3, 10-12, 14-15
A	M. KORMUNDA et al., "A single target RF magnetron co-sputtered iron doped tin oxide films with pillars", Vacuum, No.85, 2011, pages 871-874 See pages 872, 874.	1-3, 10-12, 14-15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

16 August 2019 (16.08.2019)

Date of mailing of the international search report

16 August 2019 (16.08.2019)

Name and mailing address of the ISA/KR

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INTERNATIONAL SEARCH REPORTInternational application No.
PCT/US2019/030303**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:
2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
3. ☒ Claims Nos.: 4-9,13
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2. ☐ As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of any additional fees.
3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- ☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- ☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- ☐ No protest accompanied the payment of additional search fees.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2019/030303

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 8980066 B2	17/03/2015	TW 200951235 A	16/12/2009
		TW 201428115 A	16/07/2014
		TW I435943 B	01/05/2014
		TW I519659 B	01/02/2016
		US 2009-0233424 A1	17/09/2009
		WO 2009-114362 A1	17/09/2009
US 2008-0261035 A1	23/10/2008	AT 227698 T	15/11/2002
		CZ 100999 A3	17/11/1999
		CZ 299869 B6	17/12/2008
		DE 69809385 T2	11/09/2003
		EP 0937013 A1	25/08/1999
		EP 0937013 B1	13/11/2002
		ES 2187052 T3	16/05/2003
		FR 2766174 A1	22/01/1999
		FR 2766174 B1	20/08/1999
		JP 2001-500813 A	23/01/2001
		PL 189624 B1	31/08/2005
		PL 332285 A1	30/08/1999
		PT 937013 E	31/03/2003
		US 2003-0235719 A1	25/12/2003
		US 7527868 B2	05/05/2009
		WO 99-05072 A1	04/02/1999
US 8097302 B2	17/01/2012	US 2008-0107893 A1	08/05/2008
		US 2010-0117035 A1	13/05/2010
		US 7662431 B2	16/02/2010
		WO 2005-106896 A1	10/11/2005
US 2008-0206923 A1	28/08/2008	CN 101657885 A	24/02/2010
		CN 101657885 B	20/06/2012
		KR 10-1275801 B1	18/06/2013
		KR 10-1509663 B1	06/04/2015
		KR 10-2008-0076747 A	20/08/2008
		US 8268194 B2	18/09/2012
		WO 2008-100039 A1	21/08/2008