(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
07 June 2018 (07.06.2018)

WIPO | PCT

(10) International Publication Number
WO 2018/102645 A1

(51) International Patent Classification:
G06K 19/077 (2006.01) *H01L 21/822* (2006.01)
H01L 21/78 (2006.01) *G08B 13/24* (2006.01)

(21) International Application Number:
PCT/US2017/064141

(22) International Filing Date:
01 December 2017 (01.12.2017)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/428,873 01 December 2016 (01.12.2016) US

(71) Applicant: **AVERY DENNISON RETAIL INFORMATION SERVICES, LLC** [US/US]; 8080 Norton Parkway, 22D, Mentor, Ohio 44060 (US).

(72) Inventor: **FORSTER, Ian J.**; 31 Great Cob, Chelmsford Essex CM1 6LA (GB).

(74) Agent: **RUIC, Amber C.**; Avery Dennison Corporation, 8080 Norton Parkway, 22D, Mentor, Ohio 44060 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH,

WO 2018/102645 A1

(54) Title: A MIXED STRUCTURE METHOD OF LAYOUT OF DIFFERENT SIZE ELEMENTS TO OPTIMIZE THE AREA USAGE ON A WAFER

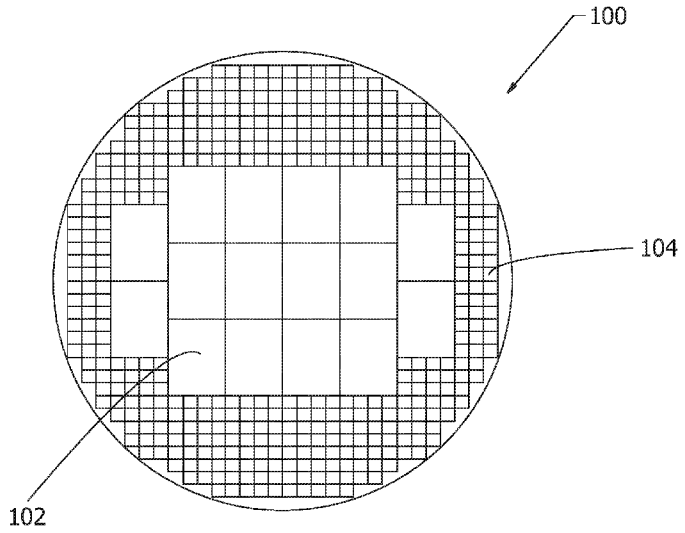

FIG. 1

(57) Abstract: A semiconductor wafer device that comprises a round wafer with a large surface area and a low cost per unit area is disclosed. The semiconductor wafer device comprises mixed size elements, such that a plurality of large devices are manufactured on the wafer, as well as a plurality of small devices are manufactured on the wafer. The small devices act as fill in elements for the wafer, as the plurality of large devices do not efficiently fill in the wafer. Typically, the large devices comprise strap or interposer devices and the small devices comprise chip devices. The chip devices attach to small RFID antennas and the interposer devices attach to larger structures, such as high frequency tags where the strap/interposer can act as a bridge from the center of an antenna coil to the outside.

[Continued on next page]

GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

— *with international search report (Art. 21(3))*

Title: A MIXED STRUCTURE METHOD OF LAYOUT OF DIFFERENT SIZE ELEMENTS TO OPTIMIZE THE AREA USAGE ON A WAFER

CROSS REFERENCE TO RELATED APPLICATION(S)

[0001] The present application claims priority to and the benefit of U.S. Provisional Utility Patent Application Number 62/428,873 filed December 1, 2016, which is incorporated herein by reference in its entirety.

BACKGROUND

[0002] The present invention relates generally to a semiconductor wafer device. Specifically, the semiconductor wafer device comprises a round wafer with a large surface area and a low cost per unit area. The semiconductor wafer device comprises mixed size elements, such that a plurality of large devices are manufactured on the wafer, as well as a plurality of small devices are manufactured on the wafer.

[0003] In the manufacture of semiconductor devices, a plurality of integrated circuits are simultaneously prepared in a semiconductor wafer through the use of conventional photolithographic techniques. It is also convenient to provide a plurality of secondary devices such as contact pads, test monitor devices, devices for measurement and alignment, etc. on the planar surface adjacent the outer perimeter of each integrated circuit or other semiconductor device.

[0004] Furthermore, based on the lower cost per unit area of the semiconductor wafer device, it is possible to create larger devices suitable for acting as strap interposers. However, the larger size of semiconductor wafer typically means that a user cannot efficiently use all of the area of a semiconductor wafer.

[0005] Accordingly, the present invention discloses a semiconductor wafer device comprising mixed size elements, such that small size devices can be utilized on the wafer device to act as fill in elements for the wafer, as the plurality of large size devices do not efficiently fill in the wafer.

SUMMARY

[0006] The following presents a simplified summary in order to provide a basic understanding of some aspects of the disclosed innovation. This summary is not an extensive overview, and it is not intended to identify key/critical elements or to delineate the scope thereof. Its sole purpose is to present some concepts in a simplified form as a prelude to the more detailed description that is presented later.

[0007] The subject matter disclosed and claimed herein, in one aspect thereof, comprises a semiconductor wafer device that comprises a round wafer with a large surface area and a low cost

per unit area. The semiconductor wafer device comprises mixed size elements, such that a plurality of large devices are manufactured on the wafer, as well as a plurality of small devices are manufactured on the wafer. The small devices act as fill in elements for the wafer, as the plurality of large devices do not efficiently fill in the wafer. Typically, the large devices are greater than 4 mm^2 and the small devices are less than 4 mm^2. Further, the large devices typically comprise strap or interposer devices and the small devices typically comprise chip devices. The chip devices attach to small RFID antennas and the interposer devices attach to larger structures, such as high frequency tags where the strap/interposer can act as a bridge from the center of an antenna coil to the outside.

[0008] In another embodiment, the semiconductor wafer device with mixed size elements further comprises a 3-D stack of devices. The 3-D stack of devices is created by picking up components and placing them on top of each other, increasing functionality in a given area. Typically, the smaller part or top component is a digital processor, and the larger part or bottom component is a sensor, photovoltaic or other device such as a display. In one embodiment, when there is insufficient area to have both a coil and a chip in the same area separately, the larger part or bottom component is a high density coil. Thus, the process of creating a 3-D stack of devices makes use of the thinness and flexibility of the chip devices to create an area efficient semiconductor wafer device.

[0009] To the accomplishment of the foregoing and related ends, certain illustrative aspects of the disclosed innovation are described herein in connection with the following description and the annexed drawings. These aspects are indicative, however, of but a few of the various ways in which the principles disclosed herein can be employed and is intended to include all such aspects and their equivalents. Other advantages and novel features will become apparent from the following detailed description when considered in conjunction with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 illustrates a top perspective view of the semiconductor wafer device with mixed size elements in accordance with the disclosed architecture.

[0011] FIG. 2 illustrates a top perspective view of the semiconductor wafer device with laser cut, mixed size elements in accordance with the disclosed architecture.

[0012] FIG. 3A illustrates a top perspective view of the semiconductor wafer device with a 3-D stack of mixed size elements in accordance with the disclosed architecture.

[0013] FIG. 3B illustrates a side perspective view of the semiconductor wafer device with a 3-D stack of mixed size elements in accordance with the disclosed architecture.

DETAILED DESCRIPTION

[0014] The innovation is now described with reference to the drawings, wherein like reference numerals are used to refer to like elements throughout. In the following description, for purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding thereof. It may be evident, however, that the innovation can be practiced without these specific details. In other instances, well-known structures and devices are shown in block diagram form in order to facilitate a description thereof.

[0015] New processes for creating chips can make relatively large flexible parts that can be used as straps which can be used on antennas but also as bridges for high frequency antennas. These larger devices do not efficiently fill the wafer area, so in this invention a smaller part is also created on the wafer. Thus, the present invention discloses a semiconductor wafer device that comprises a round wafer with a large surface area and a low cost per unit area. The semiconductor wafer device comprises mixed size elements, such that a plurality of large devices are manufactured on the wafer, as well as a plurality of small devices are manufactured on the wafer. The small devices act as fill in elements for the wafer, as the plurality of large devices do not efficiently fill in the wafer. Typically, the large devices comprise strap or interposer devices and the small devices comprise chip devices. The chip devices attach to small RFID antennas and the interposer devices attach to larger structures, such as high frequency tags where the strap/interposer can act as a bridge from the center of an antenna coil to the outside.

[0016] Referring initially to the drawings, FIG. 1 illustrates a first exemplary embodiment of a round semiconductor wafer device 100 with mixed size elements. Specifically, the semiconductor wafer device 100 can be any suitable size, shape, and configuration as is known in the art without affecting the overall concept of the invention. One of ordinary skill in the art will appreciate that the shape and size of the semiconductor wafer device 100 as shown in FIG. 1 is for illustrative purposes only and many other shapes and sizes of the semiconductor wafer device 100 are well within the scope of the present disclosure. Further, although dimensions of the semiconductor wafer device 100 (i.e., length, width, and height) are important design parameters for good performance, the semiconductor wafer device 100 may be any shape or size that ensures optimal performance and sensitivity during use.

[0017] Typically, the semiconductor wafer device 100 is inexpensive to manufacture, as such it has a low cost per unit area. Given the lower cost per unit area of the semiconductor wafer device 100, it is possible to create larger devices suitable for acting as strap interposers, and other

suitable devices as is known in the art. However, the larger size of wafer device 100 typically means a user cannot efficiently use all of the area of the wafer.

[0018] One way to efficiently use more of the area of the wafer, is to utilize mixed size elements on the wafer. Thus, a round wafer is shown in FIG. 1 with both large 102 and small 104 devices manufactured on the same sheet. The small devices 104 are typically components that are less than 4 mm^2, or any other suitable size as is known in the art. The large devices 102 are typically components that are greater than 4 mm^2, or any other suitable size as is known in the art. Further, the smaller devices 104, are analogous to chips and other suitable devices as is known in the art, and the large devices 102 are analogous to straps/interposers and other suitable devices as is known in the art. The chips (small devices 104) are ideal for attachment to small RFID antennas, and other suitable devices. The straps/interposers (large devices 102) are ideal for attachment to larger structures, including high frequency (HF) tags where the strap can act as a bridge from the center of an antenna coil to the outside, and other suitable devices as is known in the art.

[0019] Typically, utilizing mixed sized elements on the wafer device 100 is only applicable to semiconductor wafer devices 100 which have a low cost per unit area and that make a flexible chip. For example, a greater than 4 mm^2 device used as a strap/bridge in silicon would be comparatively expensive and also fragile. In contrast, the round wafer device 100 with a low cost per unit area shown in FIG. 1 discloses a plurality of large area straps/interposers 102 that do not efficiently fill in the wafer device 100. Further, as shown, the area that would otherwise not be used is filled in by smaller devices 104, such as chips.

[0020] Additionally, the large devices (strap devices) 102 and small devices (chip devices) 104 are typically used in different processes, but could be used in the same process as well. If used in different processes, laser cutting and ejection is done in two steps to separate the device stream. For example, as shown in FIG. 2, the strap devices 102 and chip devices 104 are released or ejected from the wafer device 100 at different times, as they are likely to be used in different processes. Typically, the strap devices 102 are laser cut and ejected first and the chip devices 104 are laser cut and ejected second, or the chip devices 104 can be laser cut and ejected first and the strap devices 102 laser cut and ejected second. Thus, the laser cutting and ejection of the devices 102 and 104 is performed in two steps to separate the device stream, but does not have to be and the laser cutting and ejection of the devices 102 and 104 can be performed at the same time as well.

[0021] FIGS. 3A-B illustrate another exemplary embodiment of a semiconductor wafer device 300 with mixed size elements, however this wafer device 300 also comprises a 3-D stack of devices 106. Typically, the 3-D stack of devices 106 is created by picking up parts or components and placing them on top of each other (one on top of the other), increasing functionality in a given area. For

example, the smaller part (or top component 108) maybe a chip or a digital processor or other suitable device as is known in the art, and the larger part (or bottom component 110) can be a sensor, photovoltaic or other device such as a display or other suitable large area device as is known in the art. In one embodiment, if there is insufficient area to have both the antenna coil and the chip in the same area separately, then the larger device (bottom component 108) would typically be a high density antenna coil. Furthermore, although the chips (top components 108) are shown as being different sizes, the process of creating the 3-D stack of parts 106, would make use of the thinness and flexibility of the chips 108 to create an area efficient device 300.

[0022] What has been described above includes examples of the claimed subject matter. It is, of course, not possible to describe every conceivable combination of components or methodologies for purposes of describing the claimed subject matter, but one of ordinary skill in the art may recognize that many further combinations and permutations of the claimed subject matter are possible. Accordingly, the claimed subject matter is intended to embrace all such alterations, modifications and variations that fall within the spirit and scope of the appended claims. Furthermore, to the extent that the term "includes" is used in either the detailed description or the claims, such term is intended to be inclusive in a manner similar to the term "comprising" as "comprising" is interpreted when employed as a transitional word in a claim.

CLAIMS

What is claimed is:

1. A semiconductor wafer device, comprising:
   a wafer with a large surface area;
   a plurality of large devices manufactured on the wafer; and
   a plurality of small devices manufactured on the wafer; and
   wherein the small devices act as fill in elements for the wafer, as the plurality of large devices do not efficiently fill in the wafer.

2. The semiconductor wafer device of claim 1, wherein the wafer is round in shape.

3. The semiconductor wafer device of claim 1, wherein the wafer has a low cost per unit area.

4. The semiconductor wafer device of claim 1, wherein the wafer functions as a strap interposer.

5. The semiconductor wafer device of claim 1, wherein the large devices comprise strap or interposer devices.

6. The semiconductor wafer device of claim 5, wherein the large devices are greater than 4 mm^2.

7. The semiconductor wafer device of claim 6, wherein the strap or interposer devices attach to high frequency tags.

8. The semiconductor wafer device of claim 7, wherein the strap or interposer devices act as a bridge from a center to an outside of an antenna coil.

9. The semiconductor wafer device of claim 1, wherein the small devices comprise chip devices.

10. The semiconductor wafer device of claim 9, wherein the small devices are less than 4 mm^2.

11. The semiconductor wafer device of claim 10, wherein the chip devices attach to small RFID antennas.

12. The semiconductor wafer device of claim 1, wherein the small and large devices are ejected from the wafer device at different times, as the small and large devices are used in different processes.

13. The semiconductor wafer device of claim 12, wherein the large devices are laser cut and ejected first from the wafer device and the small devices are laser cut and ejected second from the wafer device.

14. The semiconductor wafer device of claim 1, further comprising a 3-D stack of devices.

15. The semiconductor wafer device of claim 14, wherein a top device of the 3-D stack of devices comprises a digital processor and a bottom device of the 3-D stack of devices comprises a sensor.

16. A semiconductor wafer device, comprising:
a round wafer with a large surface area and a low cost per unit area;
a plurality of interposer devices manufactured on the wafer; and
a plurality of chip devices manufactured on the wafer; and
wherein the chip devices act as fill in elements for the wafer, as the plurality of interposer devices do not efficiently fill in the wafer; and
wherein the chip devices and the interposer devices are laser cut and ejected from the wafer device at different times.

17. The semiconductor wafer device of claim 16, wherein the interposer devices are greater than 4 mm^2.

18. The semiconductor wafer device of claim 16, wherein the chip devices are less than 4 mm^2.

19. The semiconductor wafer device of claim 16, further comprising a 3-D stack of devices manufactured on the wafer comprising a top device and a bottom device, wherein the top device comprises a digital processor and the bottom device comprises a high density coil.

20. A semiconductor wafer device, comprising:

a round wafer with a large surface area;

a plurality of interposer devices and a plurality of chip devices manufactured on the wafer;

wherein the chip devices act as fill in elements for the wafer, as the plurality of interposer devices do not efficiently fill in the wafer; and

a 3-D stack of devices manufactured on the wafer comprising a top device and a bottom device, wherein the top device comprises a digital processor and the bottom device comprises a high density coil.

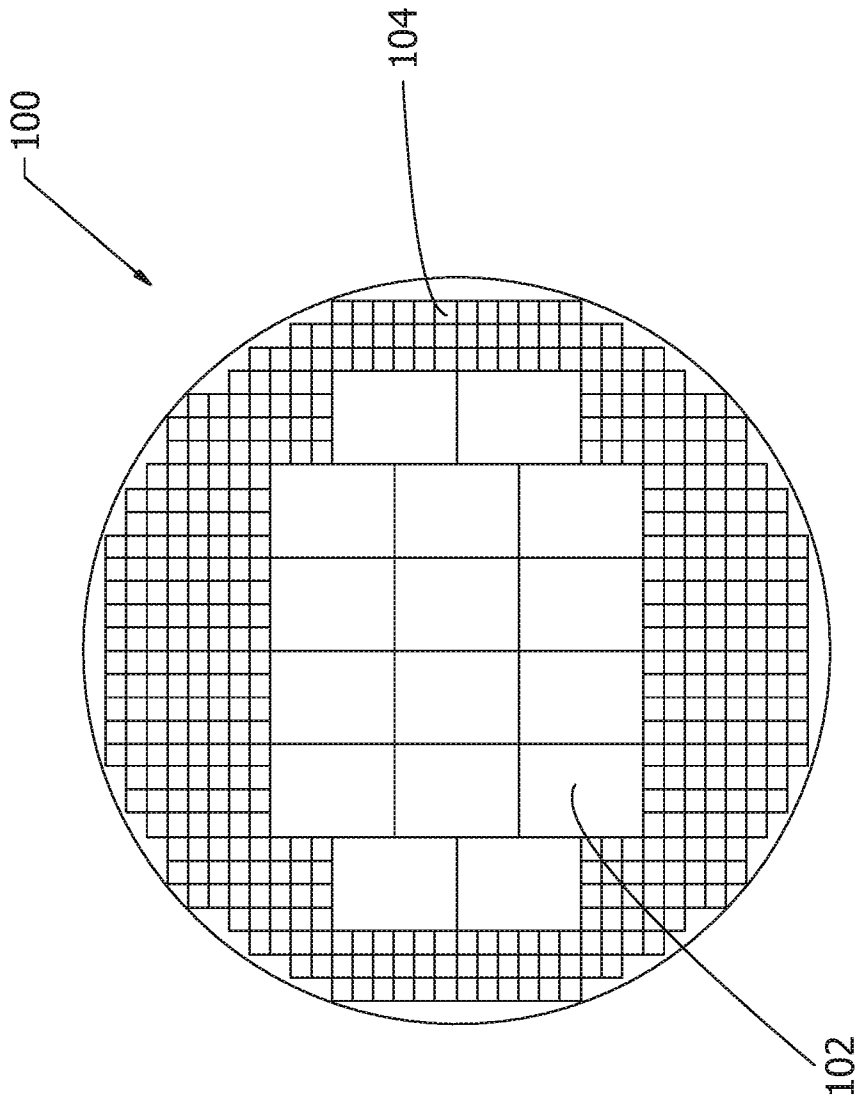

FIG. 1

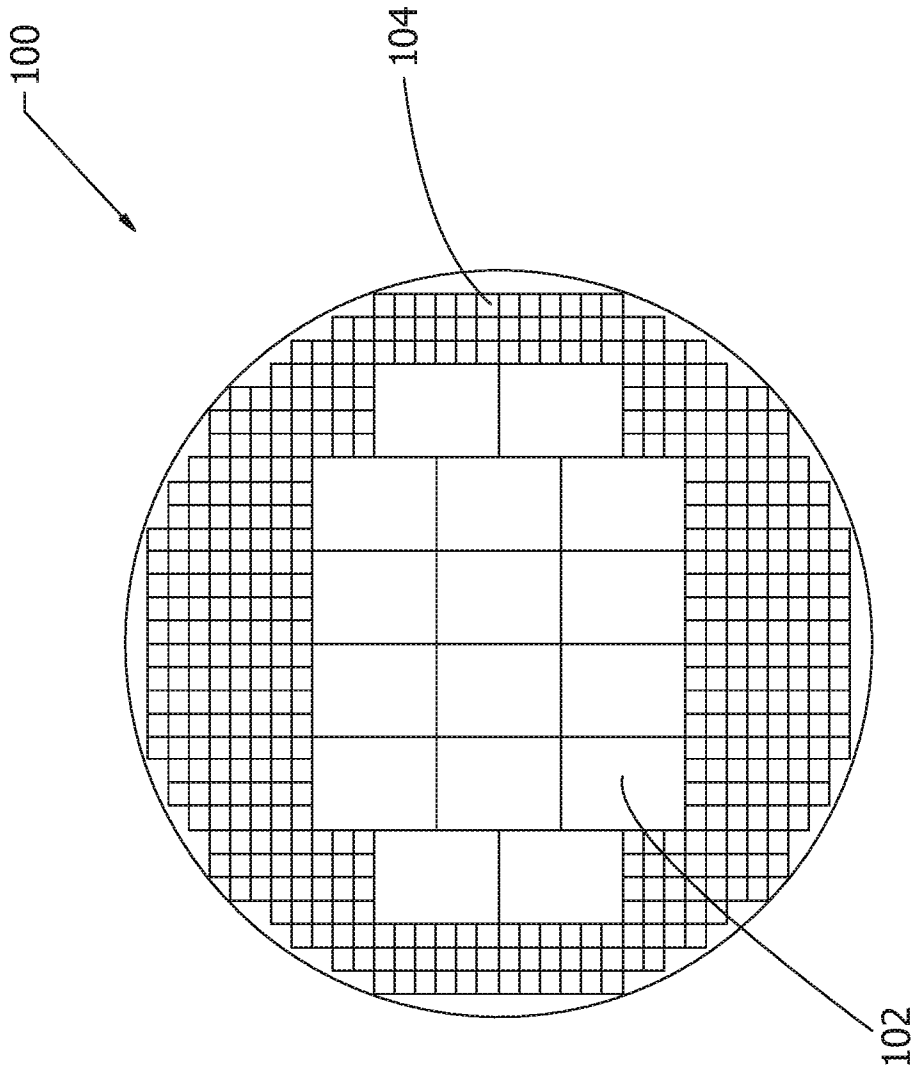

FIG. 2

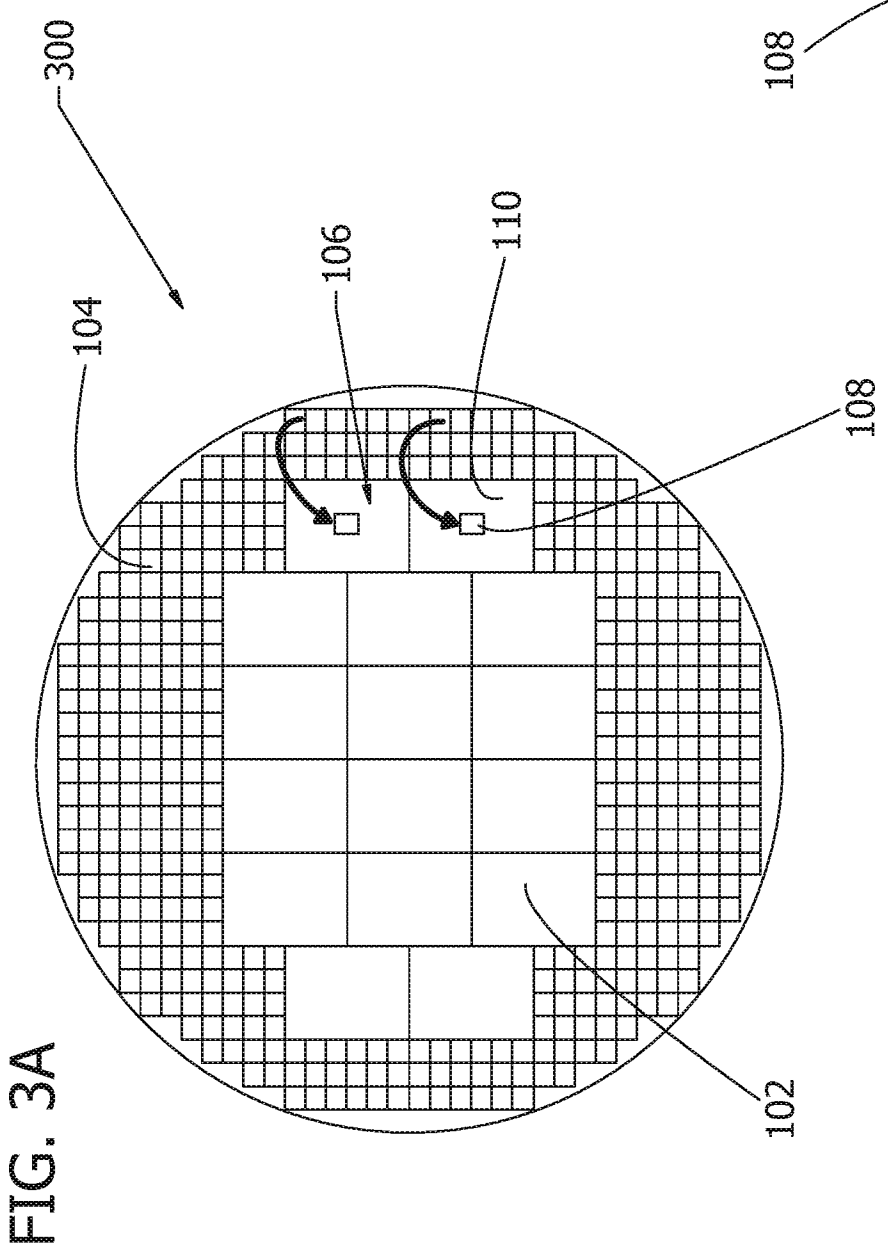

FIG. 3A

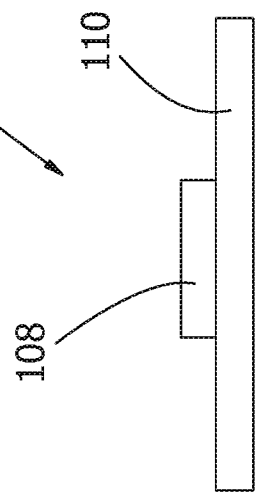

FIG. 3B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/064141

A. CLASSIFICATION OF SUBJECT MATTER
INV. G06K19/077 H01L21/78 H01L21/822 G08B13/24
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G08B G06K H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal, INSPEC, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2014/139259 A1 (CHOU YUNG-FA [TW] ET AL) 22 May 2014 (2014-05-22)	1-19
A	paragraph [0017] - paragraph [0022] figure 1	20

X	US 2007/007641 A1 (LEE KANG-WOOK [KR] ET AL) 11 January 2007 (2007-01-11) paragraph [0035] - paragraph [0048] figures 3, 4 paragraph [0006]	1-3,5-7, 9-11, 14-20

X	US 2009/095818 A1 (SMITH PATRICK [US] ET AL) 16 April 2009 (2009-04-16) paragraph [0060] paragraph [0075] - paragraph [0079] figures 6-8	1-3,5-13

	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
9 March 2018	22/03/2018

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Bruckmayer, Manfred

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2017/064141

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	ANDREW B. KAHNG ET AL: "Multi-project reticle design and wafer dicing under uncertain demand", PROCEEDINGS OPTICAL DIAGNOSTICS OF LIVING CELLS II, vol. 6281, 30 June 2006 (2006-06-30), page 628104, XP055455855, US ISSN: 0277-786X, DOI: 10.1117/12.692627 ISBN: 978-1-5106-1324-9 the whole document -----	1-3,9-15
X	US 2013/341783 A1 (ALFANO MICHAEL [US] ET AL) 26 December 2013 (2013-12-26) paragraph [0020] - paragraph [0038] figures 1, 3, 5 -----	1-4,6,9, 10,14,15
X	US 2010/051701 A1 (OGATA TETSUJI [JP] ET AL) 4 March 2010 (2010-03-04) paragraph [0007] - paragraph [0008] figure 1 -----	1-13,16

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2017/064141

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2014139259 A1	22-05-2014	TW 201421038 A	01-06-2014
		US 2014139259 A1	22-05-2014
US 2007007641 A1	11-01-2007	CN 1893053 A	10-01-2007
		DE 102006010085 A1	25-01-2007
		JP 2007019454 A	25-01-2007
		KR 20070006327 A	11-01-2007
		US 2007007641 A1	11-01-2007
US 2009095818 A1	16-04-2009	CA 2702399 A1	16-04-2009
		CN 101896947 A	24-11-2010
		EP 2201546 A1	30-06-2010
		JP 5881223 B2	09-03-2016
		JP 2011516932 A	26-05-2011
		JP 2014160515 A	04-09-2014
		KR 20100065186 A	15-06-2010
		US 2009095818 A1	16-04-2009
		WO 2009049264 A1	16-04-2009
US 2013341783 A1	26-12-2013	NONE	
US 2010051701 A1	04-03-2010	JP 5169832 B2	27-03-2013
		JP WO2008053702 A1	25-02-2010
		US 2010051701 A1	04-03-2010
		WO 2008053702 A1	08-05-2008