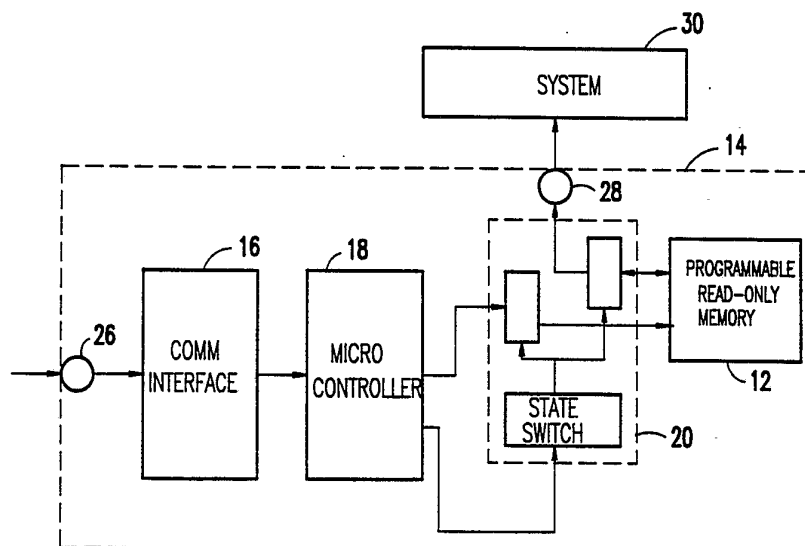




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(21) International Application Number: PCT/US92/11212 (22) International Filing Date: 15 December 1992 (15.12.92) (30) Priority data: 838,050 19 February 1992 (19.02.92) US (71) Applicant: MILSYS, LTD. [IL/IL]; Atidim Industrial Park, Bldg. No. 1, Neve Sharet, P.O.B. 58036, 61 580 Tel Aviv (IL). (72) Inventors: MORAN, Dov ; 20 Habaal-Shem-Tov St., 52 303 Ramat Gan (IL). MERGUI, Arie ; 17 Hofein St., 61 580 Tel Aviv (IL). FRIEDMAN, Amir ; 306 Weymouth St., Dix Hills, NY 11746 (US).		(74) Agent: MARHOEFER, Laurence, J.; Whitham & Marhofer, 11800 Sunrise Valley Drive, Suite 220, Reston, VA 22091 (US). (81) Designated States: AU, BR, CA, FI, HU, JP, KP, NO, RU, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published <i>With international search report.</i>

(54) Title: EXTERNALLY UPDATABLE ROM (EUROM)



(57) Abstract

An electronically programmable read-only memory module (12) has an embedded micro-controller (18) for program/data updating. Upon power up, the module (12) acts as a prior art ROM. The embedded micro-controller (18) in a standby mode is responsive to data arriving from a download communication interface (16) that is accessible by an external port (26) on the module (12). The external port (26) and download communication interface (16) is independent of the system of which the module (12) is an operating component. When a command is received from the download communication interface (16), the micro-controller (18) switches the memory device (12) to respond to micro-controller inputs that starts an update session. The micro-controller (18) receives download data from the download communication interface (16) and writes it into the memory device (12). When the download process terminates, the micro-controller (18) switches the memory device (12) back to its system interface.

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EXTERNALLY UPDATABLE ROM (EUROM)**DESCRIPTION**

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BACKGROUND OF THE INVENTION**Field of the Invention**

10 The present invention relates to electronically programmable read-only memories, and more particularly to memory with an embedded controller that allows the memory contents to be changed independently of, but without removal from, a system of which it is a component part.

15

Description of the Prior Art

20 Microprocessor-based systems and subsystems commonly employ a read-only memory (ROM) to store at least certain operating system routines. Within the last several years, new electronically programmable read-only memories (EPROMs) have been developed and are in commercial use. These memories include various device technologies. Most applications are
25 simply a non-volatile memory such as EEPROM, Flash, SRAM with battery backup or FRAM.

These new memory technologies offer a potential for in-system changes in the program stored in them. However, this potential has not been fully
30 commercially realized because of the system overhead needed to take advantage of this potential.

SUMMARY OF THE INVENTION

An object of this invention is the provision of an electronically programmable, memory module that
5 has an embedded controller to allow the contents of the memory to be altered independently of the system of which the module is a part and without removing the module from a system.

Briefly, the invention contemplates the
10 provision of an electronically programmable read-only memory module with an embedded micro-controller (i.e., controller, processor, or control logic) for program/data updating.

Upon power up, the module acts as a prior art
15 ROM. The embedded micro-controller in a standby mode is responsive to data arriving from a download communication interface that is accessible by an external port on the module. The external port and download communication interface is independent of
20 the system of which the module is an operating component. When a command is received from the download communication interface, the micro-controller switches the memory device to respond to micro-controller inputs that starts an update
25 session. The micro-controller receives download data from the download communication interface and writes it into the memory device. When the download process terminates, the micro-controller switches the memory device back to its system interface.

30 The memory device can be any standard memory component. Practically it should be non-volatile memory such as EEPROM, Flash memory, Static RAM with battery backup, Ferroelectric RAM, or any other non-

volatile memory technology or implementation leading to non-volatile storage of data.

Switching logic specifies which channel accesses the memory. In normal system operation, the memory is accessed from the standard memory interface. When the module is in a memory update state, the memory device is accessed by the embedded micro-controller.

The embedded download communication interface can be any suitable interface to the outside world. It can be a wired interface, which requires additional pins or an embedded connector in the module package. It also can be a wireless interface such as an RF channel, infra-red channel, or an optical channel.

One embodiment of the module incorporates pin sockets that allows insertion of an additional memory device on top of it. The additional memory device incorporates memory and decoding logic and may include pin sockets which will enable insertion of still another additional memory device.

The logic for programming a module with inserted add-on memories is the same as that without inserted modules. Therefore, an upgrade involves only stacking a memory device over the base module or over another memory upgrade device. The upgradeability feature allows combination of different types of memory technologies (e.g., CMOS, RAM and FLASH modules to be combined).

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of a preferred embodiment of the invention with reference to the drawings where like reference numerals designate like components in the various figures, and in which:

Figure 1 is a block diagram of one embodiment of a programmable memory with an embedded controller in accordance with the teachings of this invention.

Figure 2 is a block diagram of one embodiment of a embedded micro-controller suitable for the practice of this invention.

Figure 3 is a block diagram of one embodiment of an embedded RF communication interface suitable for the practice of this invention.

Figure 4 is a perspective block diagram of an embodiment of the invention illustrating the memory upgradeability feature.

Figure 5 is a block diagram illustrating the embodiment of the invention illustrated in Figure 4.

DETAILED DESCRIPTION OF A PREFERRED EMBODIMENT OF THE INVENTION

Referring now to Figure 1, in this preferred embodiment of the invention a programmable memory device 12 is formed in a single semiconductor chip 14 indicated by the dotted rectangle. Chip 14 also has formed integrally therein a download communication interface 16, and a micro-controller

18 along with appropriate interconnections among the various components. Also formed in the chip 14 is a state switching logic 20. Program data to alter the contents of memory device 12 is coupled to a data input port 26, and in normal operation, the memory 12 is connected to a system 30 (of which the memory module is a component part), through a system input/output port 28. It will be appreciated by those skilled in the art that the memory module shown in Figure 1 may be readily manufactured using well known semiconductor fabrication process steps such as those employed to manufacture very large-scale integrated circuits. For example, the module can be implemented by techniques such as, but not limited to, hybrids, large-scale silicon integration and packaged in plastic, ceramic, DIP, SIP, SOP, TSOP, TAB form, and in any standard or non-standard pin out.

The memory module 14 can be treated by a system designer as a regular memory component; it can have the same external pin-out (not shown), the same physical dimension and the same electrical interface characteristics.

Upon power up, the module acts as a prior art ROM. The embedded micro-controller 18 is in a standby mode, but is responsive to any data arriving from the download communication interface 16 coupled to port 26. The external port 26 is independent of the system 30 of which the module is an operating component. When a command is received via the download communication interface 16, the micro-controller 18 operates state switching logic 20 to switch the memory device 12 to respond to micro-

controller inputs, and an update session is started. The micro-controller 18 receives download data from the download communication interface 16 and writes it into the memory device 12. When the download
5 process terminates, the micro-controller switches the memory device back to system interface port 28.

Referring now to Figure 2, the embedded micro-controller 18 can be of any suitable design and will include a microprocessor 33 with its own stored
10 operating system program memory 35, a data memory 37, and an I/O buffers and logic section 39. The micro-controller controls the interface to the external port 26, monitors the input lines, controls the state switching logic 20 and programs the memory
15 12 in accordance to data arriving from the external port 26.

The memory device 12 can be any standard memory component. Practically it should be non-volatile memory such as EEPROM, Flash memory, Static RAM with
20 battery backup, Ferroelectric RAM, or any other non-volatile memory technology. The memory device 12 is accessed by the system 30 as a standard memory device. It has address lines which specify which address is accessed, and data lines which contain
25 the data to be written into memory during write accesses and the read data during read from memory cycles. It has control lines for selecting the device for access and specifying access type, i.e., read or write, and it includes power lines, usually
30 5V and sometimes 12V, used during write cycles to the memory component or any other voltage required by the memory technology.

State switching logic 20 specifies which channel accesses the memory. In normal system operation, the memory is accessed from the standard memory interface port 28. When the module is in a memory update state, the memory device 12 is accessed by the embedded micro-controller 18, which also controls the state switching logic 20. Here it should be noted that, if desired, during a memory update session, the switching logic can be programmed to respond to a memory access from the standard memory interface 28 as either tri-state or any data value on the data lines.

The embedded download communication interface can be any suitable interface to the outside world. The communication interface can include a modem for connecting to communication lines, such as telephone lines. It can be a wired interface, which requires additional or multiplexed pins or an embedded connector in the module package. A typical wired interface would be a serial interface such as an RS-232 interface. The additional pins can be arranged by either extending the package size of a standard memory device, or by adding the pins on any side of the package, i.e., on top, bottom or one of the four package walls to allow a connection from the module to the "external world" with wires which will serve as communication lines. The communication interface can also be a wireless interface such as an RF channel or an optical channel.

A wireless download interface allows an interface to the module without any wiring to the "external world". A module with wireless download interface can serve as a direct replacement to

existing memory component, with no need for a system designer to change his or her design.

5 A typical RF download communication interface is illustrated in Figure 3. It includes an antenna 40 to receive the data and an RF to micro-controller interface of a suitable design known in the art appropriate to the transmitted RF signal.

10 In general, the download protocol can be any interface protocol. It can be uni-directional, bi-directional, full duplex or half duplex protocol. The protocol can be any standard protocol such as XMODEM, KERMIT, XON/XOFF, SCSI. It also can be a proprietary protocol specially designed for the module.

15 Referring now to Figures 4 and 5, this embodiment of the invention incorporates pin sockets 50 that allows insertion of an additional memory device 52 on top of it by way of pins 51 on the module 50. The additional memory device
20 incorporates memory and decoding logic 54 and may itself include pin sockets 50 which will enable insertion of an additional memory module.

The logic for programming a module 14 with inserted memories 52 is the same as that without
25 additional memory. Therefore, an upgrade involves only stacking a memory module over the base module or over another memory upgrade module/modules. The upgradeability feature allows combination of
30 different types of memory (e.g., CMOS, RAM and FLASH modules).

While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be

practiced with modification within the spirit and scope of the appended claims.

CLAIMS

Having thus described our invention, what we
claim as new and desire to secure by Letters Patent
5 is as follows:

1. An electronically programmable memory module,
comprising in combination:

an electronically alterable memory device;

10 a first data channel for coupling said memory
device to a digital system in which said memory is a
component part;

a second data channel for coupling said memory
device to a data input port that is accessible
independently of said digital system;

15 said second data channel including a
communications interface, a controller, and a state
switch controlled by said controller;

said communications interface coupling data
from said data input port to said controller;

20 said controller switching said state switch to
a first state in response to a data input at said
data input port, and to a second state in the
absence of a data input at said data input port;

25 said state switch, in said first state,
coupling said memory device to said controller and,
in said second state, coupling said memory device to
said first data channel; and

30 said controller storing data received from said
communications interface in said memory device
independently of said digital system.

2. An electronically programmable memory module, comprising in combination:

a semiconductor substrate;

5 an electronically alterable memory device formed in said semiconductor substrate;

a first data channel for coupling said memory device to a digital system in which said memory is a component part;

10 a second data channel formed in said substrate for coupling said memory device to a data input port that is accessible independently of said digital system;

said second data channel including a communications interface, a controller, and a state switch controlled by said controller;

said communications interface coupling data from said data input port to said controller;

said controller switching said state switch to a first state in response to a data input at said data input port, and to a second state in the absence of a data input at said data input port;

20 said state switch, in said first state, coupling said memory device to said controller and, in said second state, coupling said memory device to said first data channel; and

said controller storing data received from said communications interface in said memory device independently of said digital system.

30 3. An electronically programmable memory module as in claim 1, wherein said controller includes a microprocessor, a programmable data storage means, and an input/output logic apparatus.

4. An electronically programmable memory module as in claim 1, wherein said communications interface includes a wireless communication interface.

5 5. An electronically programmable memory module as in claim 3, wherein said communications interface includes a wireless communication interface.

6. An electronically programmable memory module as in claim 1, further including a plurality of pin
10 sockets on said module for connection of an additional memory device to said module, means to couple at least one of said plurality pin sockets to said first channel, and means to couple at least one of said plurality of said pin sockets to said
15 controller.

7. An electronically programmable memory module as in claim 3, further including a plurality of pin sockets on said module for connection of an additional memory device to said module, means to
20 couple at least one of said plurality pin sockets to said first channel, and means to couple at least one of said plurality of said pin sockets to said controller.

8. An electronically programmable memory module as
25 in claim 4, further including a plurality of pin sockets on said module for connection of an additional memory device to said module, means to couple at least one of said plurality pin sockets to said first channel, and means to couple at least one

of said plurality of said pin sockets to said controller.

5 9. An electronically programmable memory module as in claim 5, further including a plurality of pin sockets on said module for connection of an additional memory device to said module, means to couple at least one of said plurality pin sockets to said first channel, and means to couple at least one
10 of said plurality of said pin sockets to said controller.

10. An electronically programmable memory module as in claim 2, wherein said controller includes a microprocessor, a programmable data storage means,
15 and an input/output logic apparatus.

11. An electronically programmable memory module as in claim 2, wherein said communications interface includes a wireless communication interface.

20 12. An electronically programmable memory module as in claim 2, further including a plurality of pin sockets on said module for connection of an additional memory device to said module, means to couple at least one of said plurality pin sockets to said first channel, and means to couple at least one
25 of said plurality of said pin sockets to said controller.

13. An electronically programmable memory module as in claim 10, further including a plurality of pin sockets on said module for connection of an

14

additional memory device to said module, means to couple at least one of said plurality pin sockets to said first channel, and means to couple at least one of said plurality of said pin sockets to said controller.

1/4

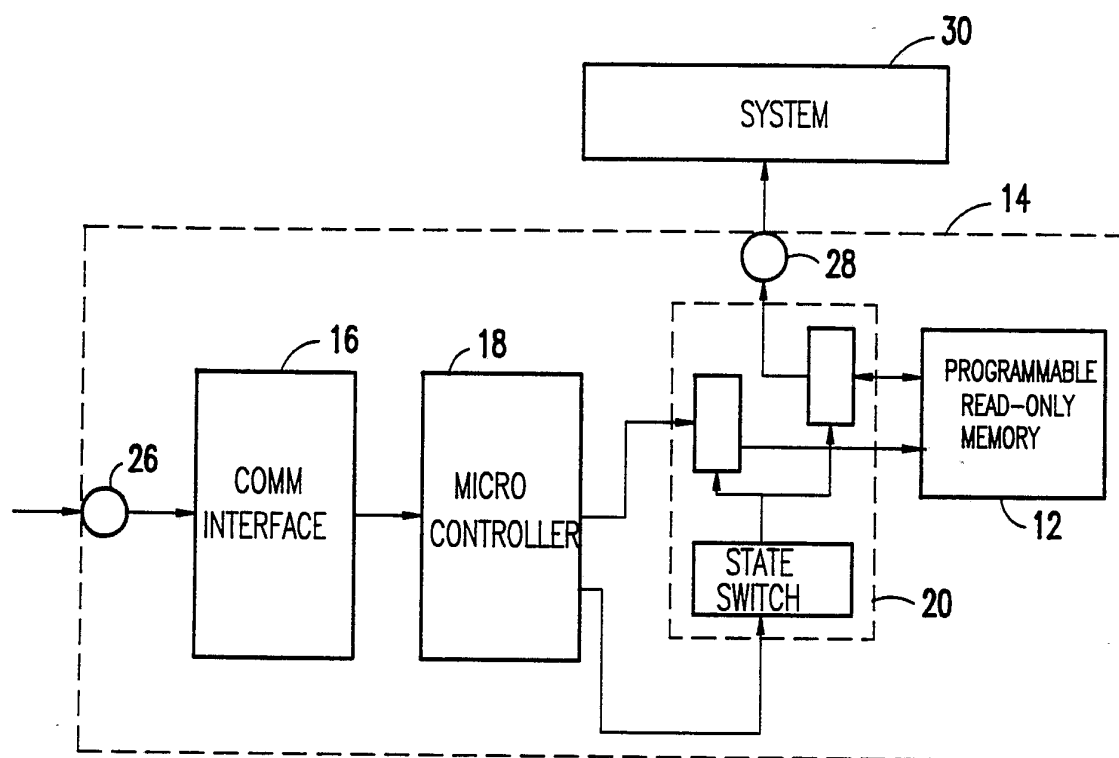


FIG. 1

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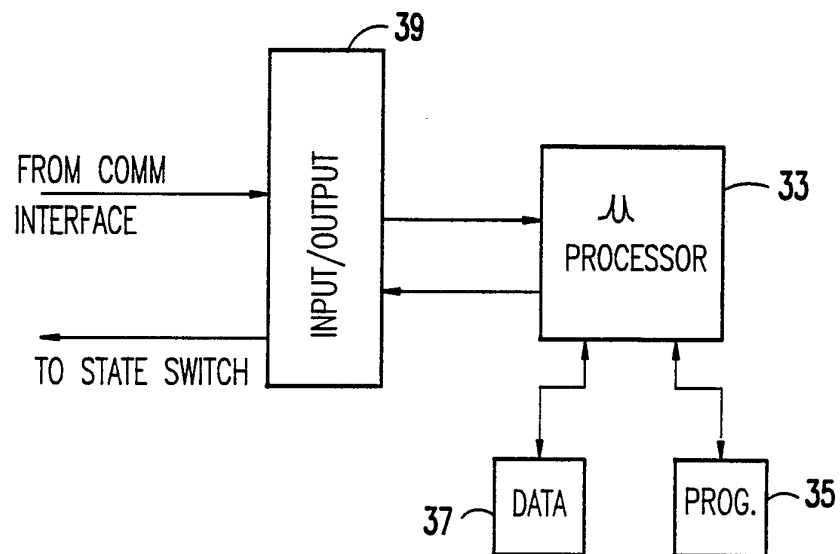


FIG.2

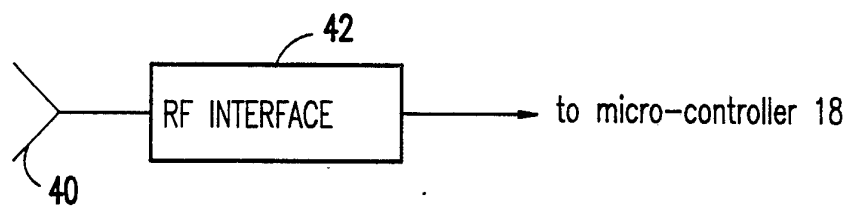


FIG.3

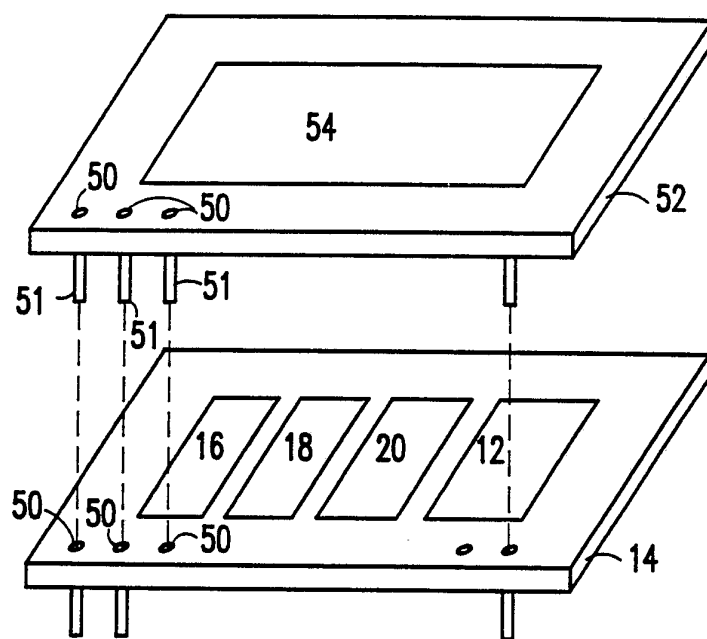


FIG. 4

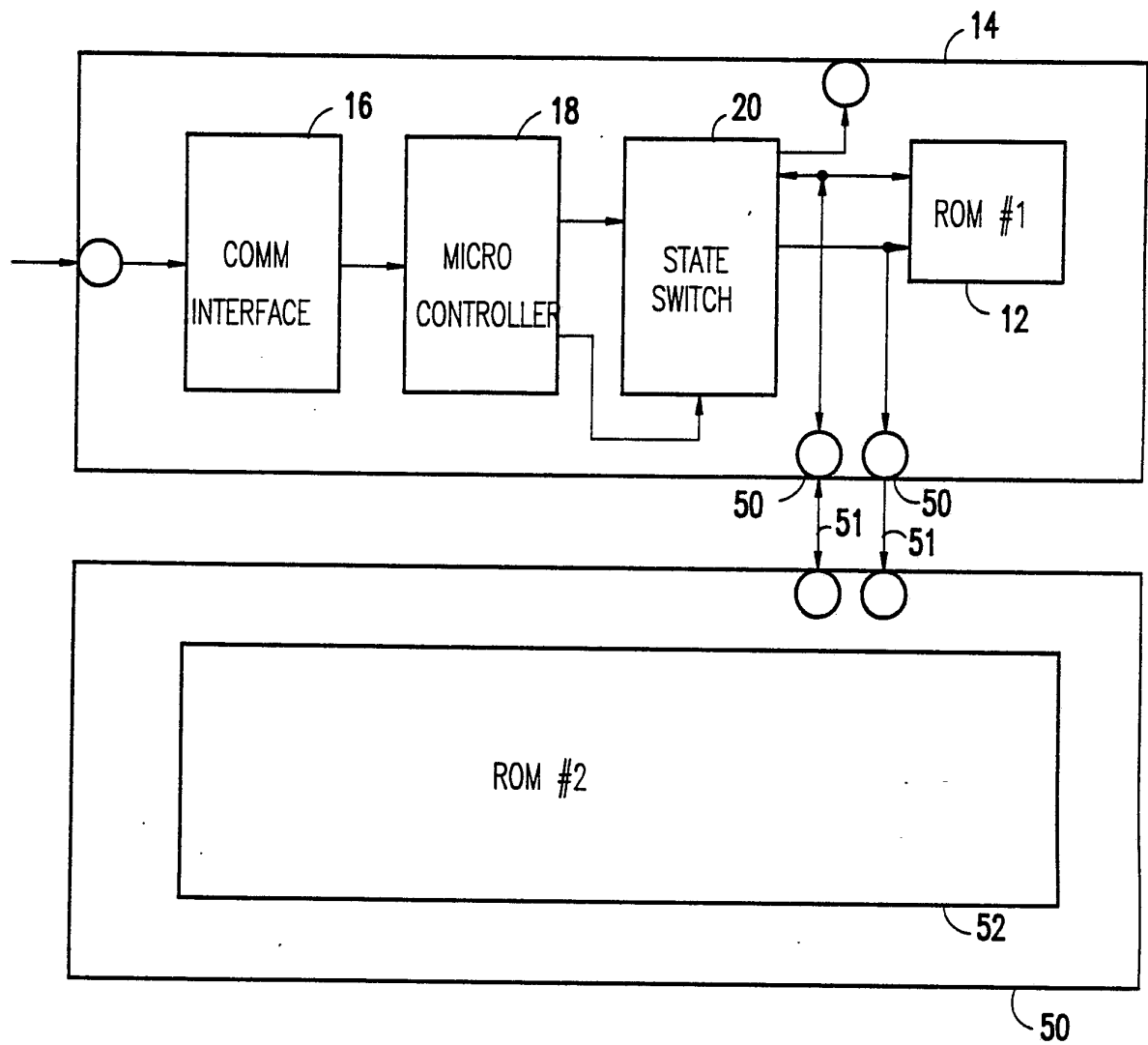


FIG.5

INTERNATIONAL SEARCH REPORT

PCT/US92/11212

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) : G06F 13/00

US CL : 395/275

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/275; 395/325, 425

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS - DATA, STORE, MEMORY, PROGRAM, REPROGRAM, SWITCH, PORT POWER-UP, POWER-ON

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,720,812 (KAO ET AL.) 19 January 1988. See the abstract.	ALL
A,P	US, A, 5,155,833 (CULLISON ET AL.) 13 October 1992. See the abstract.	ALL

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A" document defining the general state of the art which is not considered to be part of particular relevance	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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Date of the actual completion of the international search

17 FEBRUARY 1993

Date of mailing of the international search report

08 MAR 1993

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