

July 4, 1967

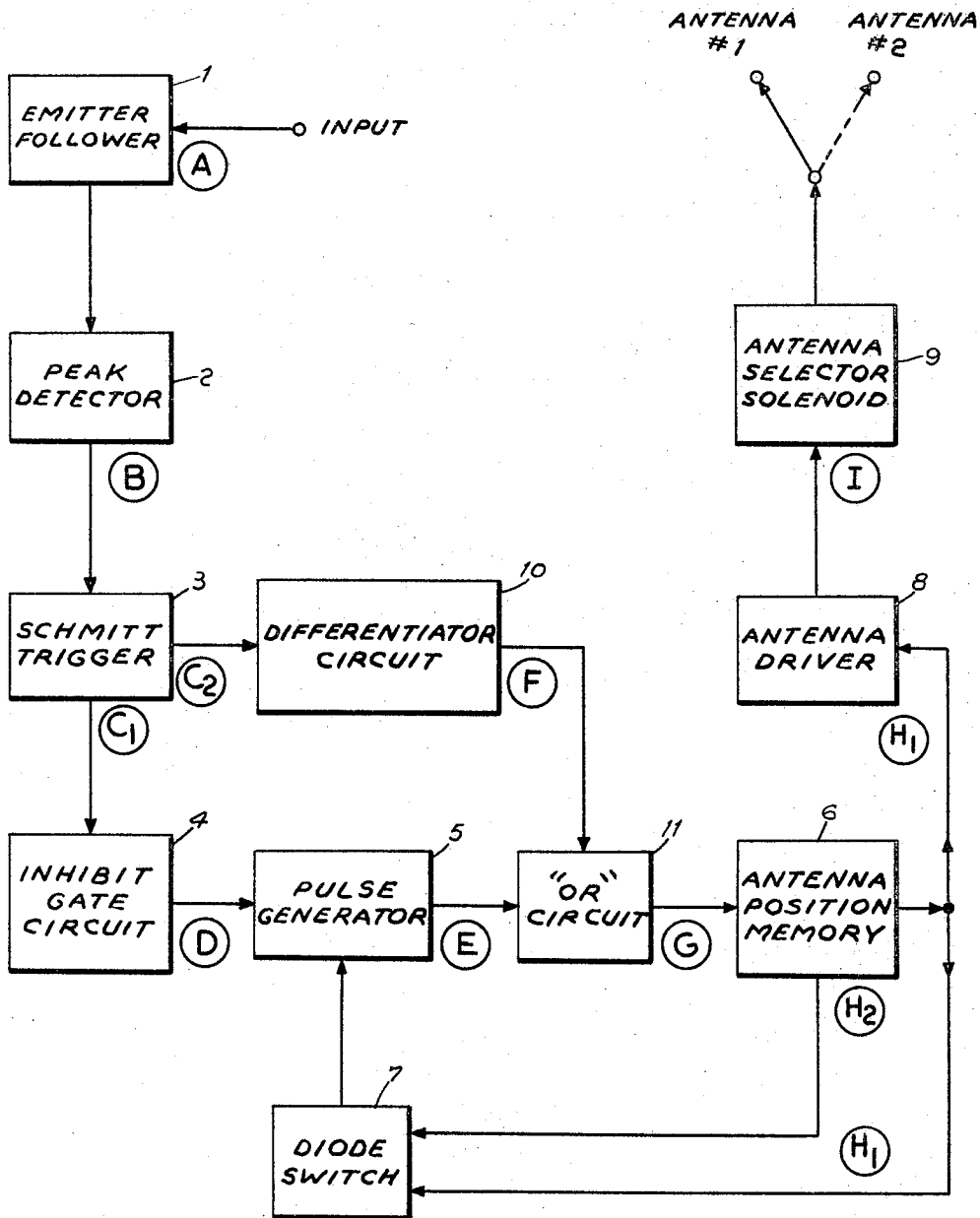
T. CASE
SELECTOR SYSTEMS FOR LOCKING ONTO ANTENNA RECEIVING
USABLE SIGNAL STRENGTH

3,329,901

Filed June 3, 1963

4 Sheets-Sheet 1

Fig. 1



INVENTOR

THOMAS CASE

BY *Joseph J. Littenberg*

AGENT

July 4, 1967

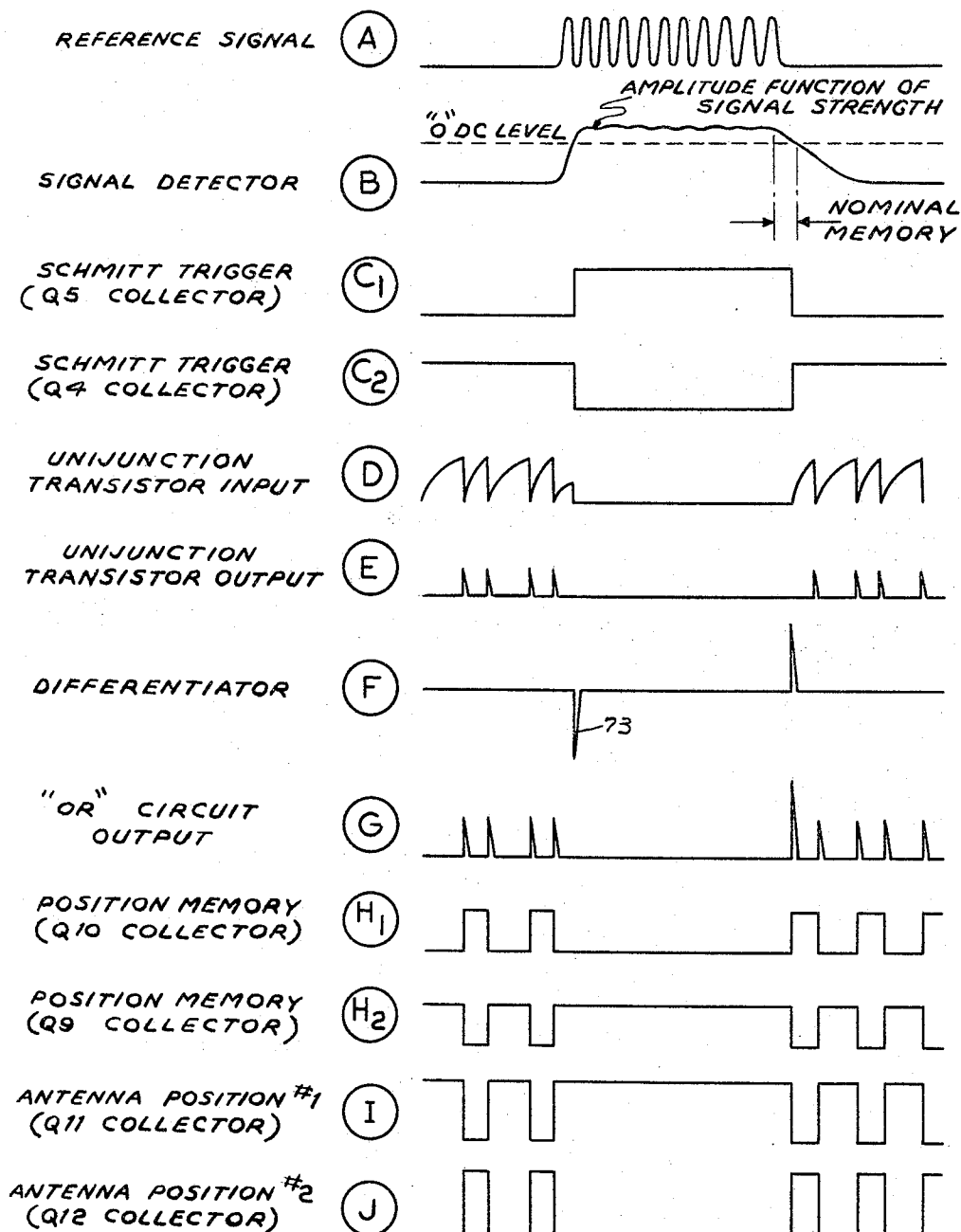
T. CASE
SELECTOR SYSTEMS FOR LOCKING ONTO ANTENNA RECEIVING
USABLE SIGNAL STRENGTH

3,329,901

Filed June 3, 1963

4 Sheets-Sheet 2

Fig. 2



INVENTOR

THOMAS CASE

BY *Joseph S. Littenberg*

AGENT

July 4, 1967

T. CASE
SELECTOR SYSTEMS FOR LOCKING ONTO ANTENNA RECEIVING
USABLE SIGNAL STRENGTH

3,329,901

Filed June 3, 1963

4 Sheets-Sheet 3

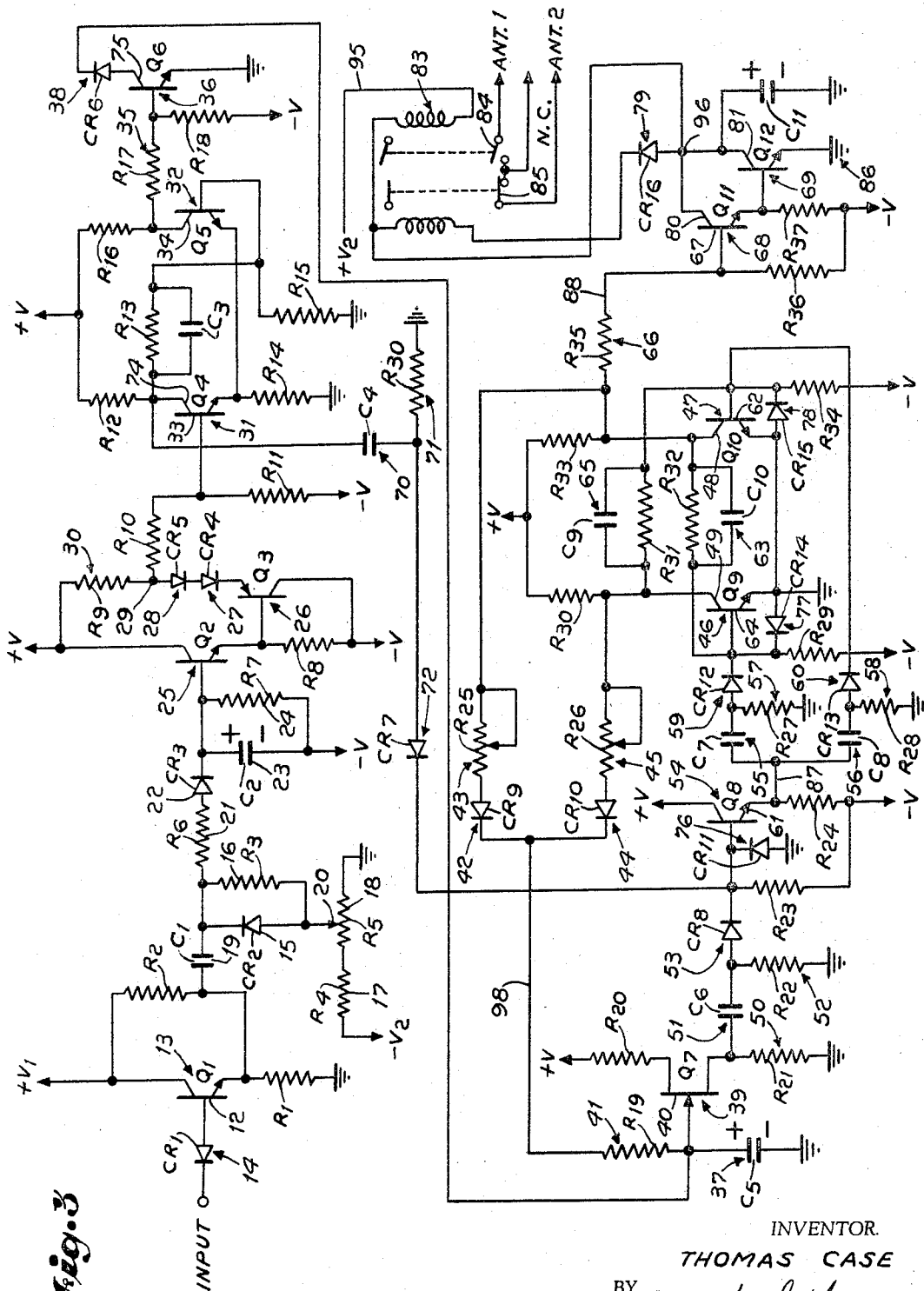


Fig. 3

INVENTOR.

THOMAS CASE

BY

Joseph S. Littenberg

AGENT

July 4, 1967

T. CASE
SELECTOR SYSTEMS FOR LOCKING ONTO ANTENNA RECEIVING
USABLE SIGNAL STRENGTH

3,329,901

Filed June 3, 1963

4 Sheets-Sheet 4

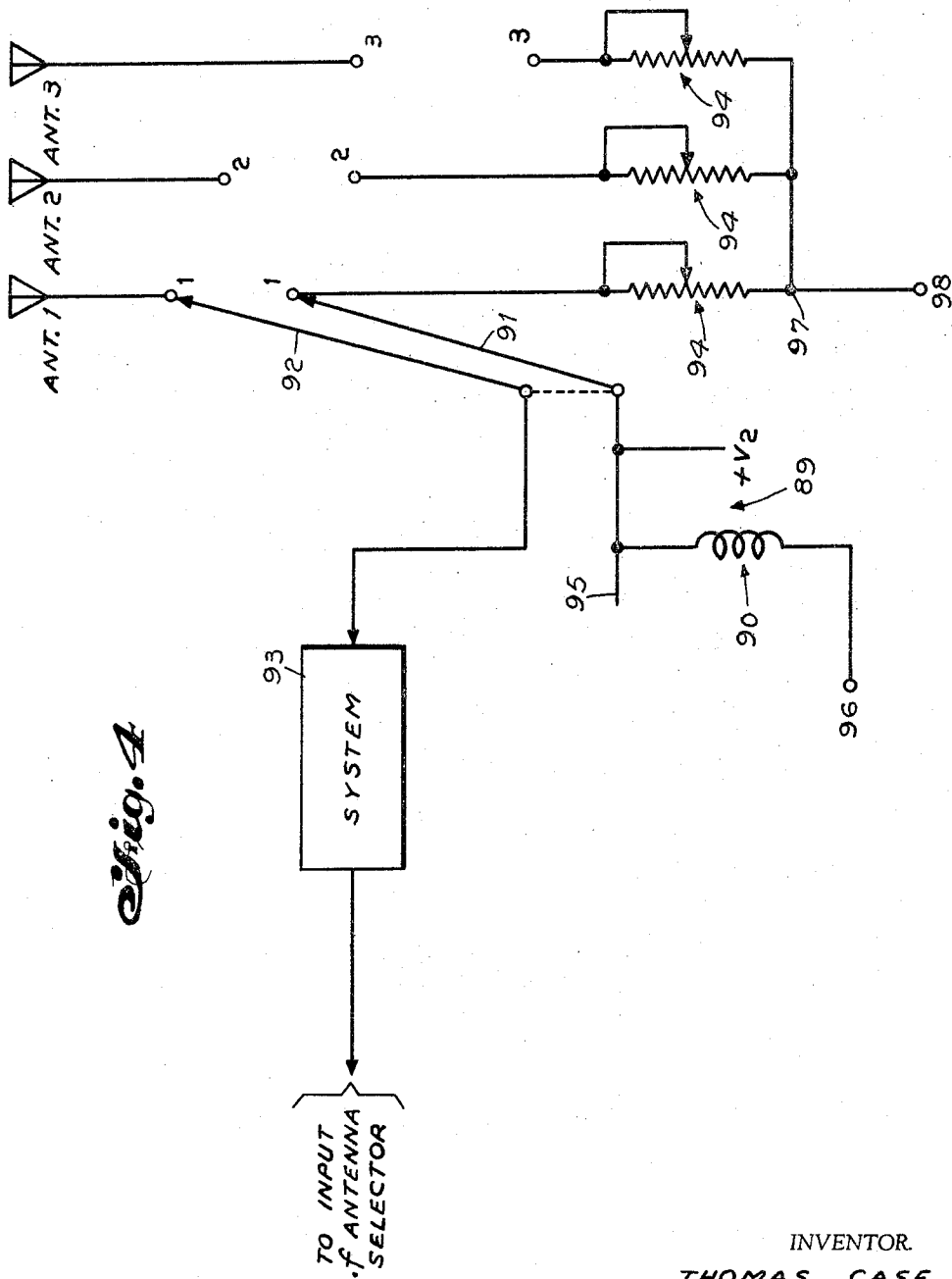


Fig. 4

INVENTOR

THOMAS CASE

BY

Joseph S. Littenberg

AGENT

1

3,329,901

SELECTOR SYSTEMS FOR LOCKING ONTO ANTENNA RECEIVING USABLE SIGNAL STRENGTH

Thomas Case, Tenafly, N.J., assignor to International Telephone and Telegraph Corporation, Nutley, N.J., a corporation of Maryland

Filed June 3, 1963, Ser. No. 284,959

23 Claims. (Cl. 325—370)

This invention relates to antenna selector systems and more particularly to solid state antenna selector systems.

Aircraft require more than one antenna for adequate signal reception. This is due to the movement of the aircraft towards and away from the transmitter. Because the aircraft is always moving, it often blocks its own antennas from receiving a usable signal. In radio navigation systems such as Tacan, it is desirable to maintain constant radio contact. For this purpose, antennas are placed above and below the aircraft so that when one antenna is blocked, the other one will receive the signal. Antenna selector systems are provided for "locking" onto an antenna receiving a usable signal and for searching for one receiving a usable signal. Antenna selector systems, heretofore known, have not been capable of high-speed switching due to the use of Miller integrators or other analog techniques for effecting switching. Also, due to the use of relays, prior art antenna selectors have been relatively inefficient and consume large amounts of power. Further, it was not possible to individually control the dwell time of the sampling means used on each antenna as the dwell time of each was usually determined by interrelated parameters such as capacitors when a bistable flip-flop is used to switch between two antenna positions.

It is therefore an object of this system to provide an improved antenna selector system for use in Tacan.

It is another object of this invention to provide an antenna selector system which is highly reliable and consumes very little power.

It is another object of this invention to provide an antenna selector system which receives an analog input and uses digital techniques in switching between antennas.

It is another object of this invention to provide an antenna selector system capable of high-speed switching.

It is a further object of this invention to provide an antenna selector system including means to individually adjust the dwell times of the separate antennas.

It is still a further object of this invention to provide an antenna selector system comprising means for effecting direct current temperature stabilization.

A feature of this invention is the provision of an antenna selector system which includes only solid state components.

Another feature of this invention is an antenna selector system for two antennas, the combination of a unijunction transistor serially coupled to a first diode and a first variable resistor, and also serially coupled with a second diode and a second variable resistor, the second diode and second variable resistor being in parallel with the first diode and first variable resistor, whereby the dwell time of the two antennas may be individually determined by adjustment of the first and second resistors.

Another feature of this invention is the combination of a clamping circuit comprising a first diode, a peak detector circuit including a second diode, and an isolation circuit including a PNP transistor, an NPN transistor, a third diode, and a fourth diode, the diodes and transistors being connected so that the first and second diodes compensate for temperature variations of the third and fourth diodes and the base emitter circuit of the NPN transistor compensates for temperature variations of the

2

base emitter circuit of the PNP transistor and vice versa, so that direct current temperature stabilization is effected.

The above-mentioned and other features and objects of this invention will become more apparent by reference to the following description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a block diagram which illustrates an antenna selector system in accordance with my invention;

FIGURE 2 illustrates the waveforms present in various parts of the system at specific periods;

FIGURE 3 is a circuit diagram of an antenna selector system in accordance with my invention; and

FIGURE 4 is a circuit diagram of an arrangement for connecting to a plurality of antennas.

Referring now to FIGURES 1 and 2, there is shown an embodiment of this invention and descriptive waveforms. Reference signal A (in Tacan this signal is 135 c.p.s.) is fed via emitter follower 1 to a peak detector circuit 2 having a nominal discharge time or memory. This memory or delay time insures uninterrupted operation in case signal A is temporarily lost. The output of the peak detector (waveform B) is fed to a Schmitt trigger circuit 3 which generates a gate (waveform C1) that is fed to gate circuit 4. The presence of this gate indicates that one of the two antennas has locked "on" to a usable signal. This gate or gating signal controls the free running operation of an astable pulse generator circuit 5 which utilizes a unijunction transistor. The unijunction transistor pulse output (waveform E) spacing is adjustable using two feedback gate signals (waveforms H1 and H2) derived from the antenna memory position circuit 6 so that the dwell time of each antenna can be independently adjusted. The dwell time of each can be independently adjusted as the adjustments of the timing circuits are independent of each other.

In the absence of the gating signal, the pulse generator 5 is free to generate pulses causing the antenna position memory circuit 6 to cycle between antennas at the above set dwell times. The gating action signal (H1) is fed to an antenna driver 8 (comprising transistors 68 and 69) which supplies the necessary power to the antenna selector switch or solenoid 9. When an insufficient signal prevents lock-on, the antenna position memory circuit provides the cycling process between the two antennas by causing antenna driver 8 to drive the antenna selector solenoid circuit 9 which switches between antennas 1 and 2.

Because of the gating action of the Schmitt trigger, one pulse from the unijunction transistor output is lost when this gate terminates. An auxiliary circuit is therefore provided consisting of the differentiator network 10 and a diode "OR" circuit 11 (including transistor 54) to supply an extra pulse. Without this extra pulse, the search time of either antenna would be lost for one cycle. With it, the sampling or search process will start immediately after the delay period by locking to the antenna which was not in use at the time when the signal was lost.

Referring now to FIGURE 3, a circuit diagram for a solid state antenna selector is shown. A reference signal is directly coupled to the base 12 of emitter follower transistor 13 through Zener diode 14. Zener diode 14 shifts the average DC level at the input to a DC level which maintains the reference signal in the linear operating range of transistor 13. Transistor 13, because it is connected in emitter follower fashion, prevents loading of the reference signal source and also provides the necessary low impedance to drive an input clamping circuit consisting of diode 15, resistor 16, and a sensitivity adjustment network comprising resistors 17 and 18. Capacitor 19 removes the input DC level so that an independent DC level can be set with the clamping circuit. Desired

levels can be chosen by adjusting the setting of contact 20 with respect to resistor 18.

The clamped reference signal is fed to a peak detector circuit consisting of resistor 21, diode 22, capacitor 23 and resistor 24. A nominal memory or delay is obtained from the discharge time constant of the combination of resistor 24 and capacitor 23. This discharge time constant determines the length of the delay period during which the antenna selector will remain locked "on" to an antenna receiving a usable signal after the loss of the usable signal.

Transistors 25 and 26 are connected in Darlington fashion (double emitter follower action) to prevent loading of the memory or delay circuit. Diodes 27 and 28 are provided to compensate for the direct current temperature drifts of diodes 15 and 22. The base emitter junctions of transistors 25 and 26 also compensate for each others direct current temperature drifts. Thus, an almost temperature drift free DC level is provided at junction 29 of diode 28 and resistor 30. The DC level at this junction is fed to a Schmitt trigger circuit comprising transistors 31 and 32. When the input reference signal is of sufficient magnitude, the DC level to the base 33 of transistor 31 will exceed the Schmitt trigger threshold level turning it "on." This turn-on process causes the collector 34 of transistor 32, which is normally at a low potential to jump to +V. This level supplies the necessary base current through resistor 35 to turn on transistor 36 which effectively shorts out timing capacitor 37. Zener diode 38 sets the lower charging level of capacitor 37. Thus the charging level of capacitor 37 can be varied by varying the value of diode 38.

During the time that transistor 36 remains turned on, no pulses can be generated by unijunction transistor 39 as the "on" signal from transistor 36 provides a blocking signal to the base 40 of unijunction transistor 39. If the DC level to the Schmitt trigger drops below the threshold level, the DC level at collector 34 of transistor 32 will drop back to its lower potential causing transistor 36 to turn off, as there will be an insufficient potential at its base 33, thus removing the short across capacitor 37. Capacitor 37 immediately starts to charge towards +V through resistor 41 in series with either diode 42 and resistor 43 or diode 44 and resistor 45 depending upon which collector of transistors 46 or 47 is more positive.

Assuming that collector 48 of transistor 47 is more positive then the charging time of capacitor 37 will be determined by the setting of resistor 43 in series with resistor 41 and capacitor 37. When the exponential voltage level across capacitor 37 exceeds the unijunction threshold level, a pulse is generated by unijunction transistor 39 which appears across resistor 50. This pulse is coupled through a network consisting of capacitor 51, resistor 52 and diode 53 to emitter follower transistor 54 which supplies a current pulse to alternately trigger the bistable antenna position memory circuit (comprising transistors 46 and 47) "on" and "off."

Capacitors 55 and 56, resistors 57 and 58, and diodes 59 and 60 form pulse steering networks. For instance, when transistor 46 is turned "on," then the next positive trigger pulse appearing at emitter 61 of transistor 54 will be steered through the network consisting of capacitor 56, resistor 58, and diode 60, to base 62 of transistor 47 causing 47 to turn "on." Collector 48 of transistor 47 will then fall to approximately a zero potential causing a negative pulse to be coupled through capacitor 63 over to base 64 of transistor 46 turning it "off." This process is repetitive, except the next pulse following will be steered through the network consisting of capacitor 55, resistor 57, and diode 59, turning transistor 46 on and causing transistor 47 to shut off due to the negative pulse coupled through collector 49 of transistor 46 through capacitor 65 to base 62 of transistor 47.

The DC level at collector 48 of transistor 47 determines which antenna is locked "on." If transistor 47 is

at its upper level +V, sufficient current is supplied through resistor 66 to base 67 of transistor 68 to turn on the power switching circuit comprising transistors 68 and 69. With transistor 69 thus in saturation, a low impedance path to ground 86 is provided from V2 through antenna solenoid 83 through the collector emitter junction of transistor 69. Solenoid 83 is part of the antenna array and not part of my antenna selector system itself. It is driven by my antenna selector system. Antenna 1 remains in this locked up position until the DC level at collector 48 of transistor 47 falls to its lower potential at which time the solenoid path to ground is broken, allowing antenna 1 to unlock and antenna 2 to lock "up." Connection 84 to antenna 1 is normally open while connection 85 to antenna 2 is normally closed.

The coupling network or differentiator network consisting of capacitor 70, resistance 71, and diode 72 couples a positive pulse via emitter follower 54 into the bistable position memory circuit whenever the Schmitt trigger turns off, due to a weak signal, (after the delay period determined by capacitor 23 and resistor 24 has elapsed) to start the antenna recycling at the proper time. The negative pulse emitted by the differentiator and shown in FIGURE 2 (waveform F) as a spike 73 below the line is eliminated by diode 72 and does not appear on the "OR" circuit output as can be seen by comparing waveforms F and G. The differentiator network causes the antenna selector to immediately lock onto the antenna which had not been receiving a usable signal at the end of the delay period, thus saving the time that would be required for capacitor 37 to be charged sufficiently to cause the pulse generator comprising unijunction transistor 39 to emit a pulse and cause the alternate antenna to be sampled.

Transistors 36 and 54 provide added stability and reliability. Capacitor 37 could be directly connected to collector 74 of transistor 31 instead of collector 75 of transistor 36. Unijunction 39 could pulse the bistable directly to eliminate transistor 54. By using 54, the bistable can be made harder to trigger so that it is less sensitive to noise. Clamping diodes 76, 77, and 78 are provided to keep the signal pulses above ground level. Diode 79 prevents negative feedback at the collectors 80 and 81 of transistors 68 and 69, respectively, due to the overshoot or solenoid action (inductive action in coil).

My antenna selector system may be used with a plurality of antennas. It can be modified for use by eliminating the bistable device or used essentially as is. Generally this would be done by using a commutation device such as a stepping relay as part of the antenna array. It could be made responsive directly to the unijunction pulses or to the step pulses out of the bistable device which is the output of the described circuit. The commutator would simultaneously connect each antenna back to the input of the system and the presence of a usable signal would stop the commutative action in the same manner as it is done now. That is, blocking the unijunction. Dwell times could be independently adjustable for each antenna by providing independent return circuit loops for each antenna.

A system for directly coupling a commutation device to the unijunction pulses will now be described with reference to FIGURES 3 and 4. Point 87 will be directly tied to point 88 thus eliminating the antenna memory circuit and related parameters. Stepping relay 89 has a coil 90 and ganged switches 91 and 92. The upper deck switch 92 connects a sampled antenna via the system 93 in which the selector is used, such as Tacan, to the input of the antenna selector system. Lower deck switch 91 connects +V2 to the timing capacitor via timing resistors 94 associated with the particular antenna which is being sampled. Switches 91 and 92 move in synchronism with each other. As many antenna positions as desired may be provided, and the dwell time of each can be independently set by the resistor 94 associated with it.

Stepping relay 89 is part of the antenna array and is connected to my antenna selector system by connecting one end of coil 90 to V2 at 95 (eliminating solenoid 83) and the other end of coil 90 to collectors 80 and 81 of transistors 68 and 69 respectively at 96. The timing resistors 94 are joined at 97 and are connected to my antenna selector system at 98. Relay 89 steps from one antenna to the next in response to the unijunction pulses. The locking means operate as described hereinbefore to deactivate the unijunction and the unlocking means such as a differentiator and OR circuit operate in the same manner to immediately cause relay 89 to step to the next antenna position as described hereinbefore with reference to solenoid 83.

The circuit in FIGURE 3 has been reduced to practice and successfully tested. The circuit parameters utilizing a 135 c.p.s. reference signal as in Tacan are as follows:

Diodes

CR1 Zener	volts	43
CR2, CR3, CR4, CR5, CR7, CR8, CR9, CR10, CR11, CR12, CR13, CR14, CR15, CR16	1N459	
CR6 Zener	volts	8.2

Resistors

R1, R17, R19, R31, R32	ohms	21.5K
R2	do	121K
R3	megohms	2.21
R4, R13	ohms	17.8K
R5, R24, R37	do	10K
R6	do	2.67K
R7	do	261K
R8	do	34.8K
R9	do	4.64K
R10	do	6.81K
R11, R22, R23, R27, R28, R36	do	909K
R12	do	1.96K
R14	do	442
R15	do	14.7K
R16	do	2.74K
R18	do	68.1K
R20	do	536
R21	do	383
R25	do	100K
R26	do	150K
R29, R34	do	249K
R30, R33	do	2.15K
R35	do	8.25K

Capacitors

C1	μfarads	0.022
C2, C11	do	22
C3, C4	μμfarads	390
C5	μfarads	100
C6	do	0.033
C7, C8, C9, C10	μμfarads	2200

Transistors

Q1, Q11	2N1893
Q2, Q4, Q5, Q6, Q8, Q9, Q10	2N338A
Q3	2N1132
Q7	2N491
Q12	2N1722

Potentials

+V	volts	22
+V1	do	120
+V2	do	28
-V	do	-22

While I have described above the principles of my invention in connection with specific apparatus, it is to be clearly understood that this description is made only by way of example and not as a limitation to the scope of my invention as set forth in the objects thereof and in the accompanying claims.

I claim:

1. An antenna selector system for locking onto one of a plurality of antennas which receives a usable signal comprising:

5 sampling means for alternately sampling the antennas for the presence of a usable signal;

locking means responsive to the presence of a usable signal for locking said sampling means on an antenna receiving a usable signal;

10 unlocking means responsive to the loss of a usable signal for causing said sampling means to immediately sample the previously unlocked antenna; and

means for individually and independently adjusting the dwell time of the sampling means on each of said antennas.

2. A system according to claim 1 wherein said sampling means includes triggering means and wherein said unlocking means includes:

an OR circuit coupled to the output of said triggering means; and

a differentiator circuit coupled between said OR circuit and said locking means for transmitting a pulse to said selector means upon the loss of a usable signal whereby said selector means immediately samples a previously unlocked antenna.

3. A system according to claim 2 wherein said locking means further comprises:

means for detecting the presence of a usable signal;

means coupled to said detecting means including a monostable device for indicating the presence or absence of a usable signal; and

a delay circuit serially coupled between said monostable device and said detecting means for causing the indication of the loss of a usable signal to be transmitted to said differentiator or said triggering means only after a predetermined delay time has elapsed between usable signals.

4. An antenna selector system for locking onto one of a plurality of antennas which receives a usable signal comprising:

40 sampling means including triggering means for alternately sampling the antennas for the presence of a usable signal; and

locking means responsive to the presence of a usable signal for deactivating said triggering means, thereby locking said sampling means onto an antenna receiving a usable signal.

5. A system according to claim 4 further comprising unlocking means responsive to the loss of a usable signal for causing said sampling means to immediately sample a previously unlocked antenna.

6. A system according to claim 5 wherein said unlocking means includes:

an OR circuit coupled to the output of said triggering means; and

a differentiator circuit coupled between said OR circuit and said locking means for transmitting a pulse to said selector means upon the loss of a usable signal whereby said selector immediately samples a previously unlocked antenna.

7. A device according to claim 6 wherein said locking means further comprises:

means for detecting the presence of a usable signal;

means coupled to said detecting means including a monostable device for indicating the presence or absence of a usable signal; and

a delay circuit serially coupled between said monostable device and said detecting means for causing the indication of the loss of a usable signal to be transmitted to said differentiator or said triggering means only after a predetermined delay time has elapsed between usable signals.

8. A system according to claim 4 wherein said triggering means includes a pulse generator.

9. A system according to claim 8 wherein said pulse generator includes a unijunction transistor.

10. A system according to claim 9 wherein said locking means includes means for coupling a blocking signal to the base electrode of said unijunction transistor for deactivating said pulse generator.

11. A system according to claim 9 further comprising means for individually and independently adjusting the dwell time of said sampling means on each of said antennas.

12. A system according to claim 11 wherein said pulse generator includes a timing capacitor coupled to the base electrode of said unijunction transistor and wherein said means for individually and independently adjusting the dwell time includes:

- a first variable resistor coupled in series with said capacitor; and
- a second variable resistor coupled in series with said capacitor, said resistors being so coupled that they are in parallel with each other and can be adjusted independently of each other to vary the charging rate of said capacitor.

13. A system according to claim 4 wherein said plurality of antennas comprises two antennas and wherein said sampling means includes a bistable device coupled to and activated by said pulse generator for alternately coupling said locking means to each of said two antennas.

14. A system according to claim 13 wherein said pulse generator includes a unijunction transistor and wherein said locking means comprises means for coupling a blocking signal to the base electrode of said unijunction transistor for deactivating said pulse generator.

15. A device according to claim 14 wherein said sampling means comprises a timing capacitor connected to the base of said unijunction transistor and further comprising a first variable resistor in series with said capacitor, and a second variable resistor in series with said capacitor, said resistors being so connected that they are in parallel with each other and can be adjusted independently of each other to vary the charging rate of said capacitor.

16. A device according to claim 14 further comprising locking means comprising an OR circuit connected serially between said pulse generator and said bistable device, and a differentiator circuit serially connected between said OR circuit and said locking means for transmitting a pulse to said bistable device upon the loss of a usable signal whereby said bistable device immediately samples the previously unlocked antenna.

17. A device according to claim 16 wherein said locking means further comprises means for detecting the presence of a usable signal, means connected to said detecting means including a monostable device for indicating the presence or absence of a usable signal, and a delay circuit serially connected between said monostable device and said detecting means for causing the indication of the loss of a usable signal not to be transmitted to said differ-

entiator or said pulse generator unless a desired delay time has elapsed between usable signals.

18. An antenna selector system for locking onto one of a plurality of antennas which receives a usable signal comprising:

- means including triggering means for alternately sampling the antennas for the presence of a usable signal;
- locking means responsive to the presence of a usable signal for deactivating said triggering means, thereby locking said sampling means on an antenna receiving a usable signal; and
- means for individually and independently adjusting the dwell time of said sampling means on each of said antennas.

19. A system according to claim 18 wherein said triggering means includes a pulse generator.

20. A system according to claim 19 wherein said pulse generator includes a unijunction transistor and said locking means includes means for coupling a signal to the base electrode of said unijunction transistor for deactivating said pulse generator.

21. A system according to claim 18 further comprising unlocking means responsive to the loss of a usable signal for causing said sampling means to immediately sample the previously unlocked antenna.

22. A system according to claim 21 wherein said unlocking means includes:

- an OR circuit coupled to the output of said triggering means; and

a differentiator circuit coupled between said OR circuit and said locking means for transmitting a pulse to said selector means upon the loss of a usable signal whereby said selector means immediately samples a previously unlocked antenna.

23. A system according to claim 22 wherein said locking means further comprises:

- means for detecting the presence of a usable signal;
- means coupled to said detecting means including a monostable device for indicating the presence or absence of a usable signal; and

a delay circuit serially coupled between said monostable device and said detecting means for causing the indication of the loss of a usable signal to be transmitted to said differentiator or said triggering means only after a predetermined delay time has elapsed between usable signals.

References Cited

UNITED STATES PATENTS

2,729,741	1/1956	Chapman	325—370
2,937,268	5/1960	Downie et al.	325—370 X
3,037,114	5/1962	Bier et al.	325—370
3,182,263	5/1965	Gossard	325—370

KATHLEEN H. CLAFFY, *Primary Examiner*.

R. S. BELL, *Assistant Examiner*.