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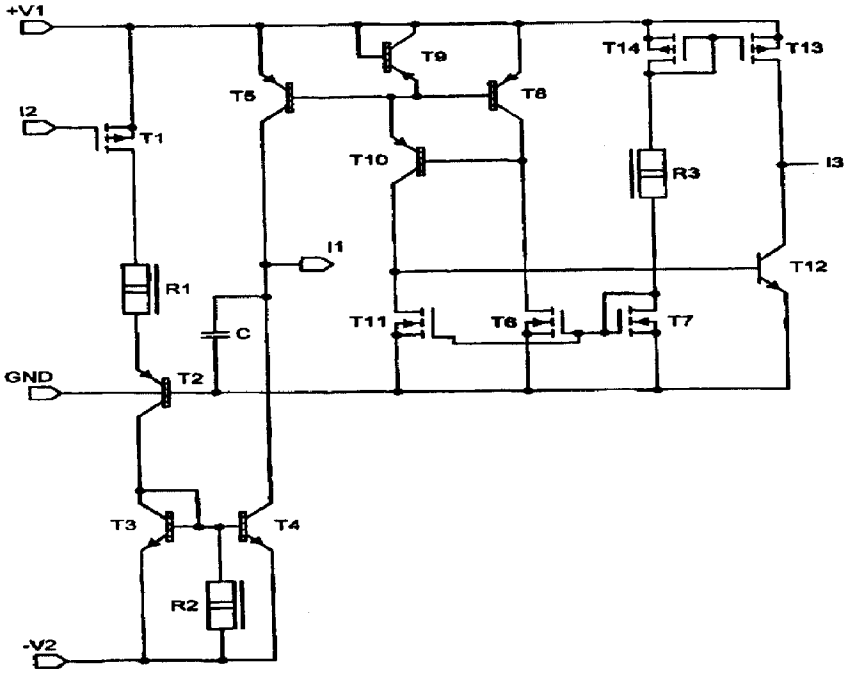
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(54) **CIRCUIT D'AJUSTAGE**
(54) **TRIMMING CIRCUIT**



(57) Afin de pouvoir surveiller l'état d'un condensateur antifusible, on a connecté à ce condensateur un transistor, afin que ce transistor ne sature que si le condensateur n'a pas claqué. La surveillance du courant de base du transistor permet la surveillance de l'état du condensateur, sans avoir à utiliser de comparateur haute tension classique.

(57) To monitor the state of an antifuse capacitor, a transistor is connected to the capacitor such that it saturates only when the capacitor is not blown. Monitoring the base current of the transistor allows the state of the capacitor to be monitored without needing to use a conventional high-voltage comparator.

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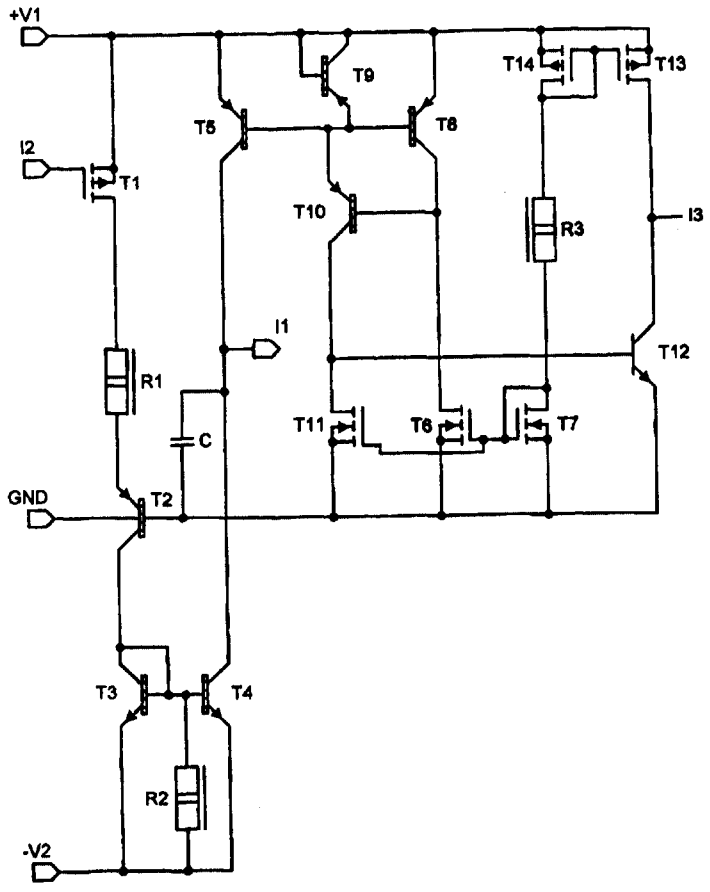
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(57) Abstract

To monitor the state of an antifuse capacitor, a transistor is connected to the capacitor such that it saturates only when the capacitor is not blown. Monitoring the base current of the transistor allows the state of the capacitor to be monitored without needing to use a conventional high–voltage comparator.



TRIMMING CIRCUIT

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a trimming circuit, and in particular to a circuit which includes an antifuse, and means for detecting whether or not the antifuse has blown.

DESCRIPTION OF RELATED ART

Trimming circuits are known which include at least one antifuse, that is a fuse which, when blown, presents a short circuit across its terminals.

For example, in order to blow an antifuse capacitor, it may be necessary to apply a zapping voltage of several tens of volts across the terminals of the capacitor, whilst limiting the current. There is then a problem in sensing that the capacitor has blown. This arises because the sensing circuitry will then need to be able to distinguish between two voltages several volts apart and survive the zapping voltage of several tens of volts. Although high voltage comparator circuits are available, they are not easily incorporated into integrated circuit designs, because they require a relatively large area. This is a particular problem because a trimming circuit will typically include several antifuses, each requiring its own comparator, and so problems of size are multiplied accordingly.

SUMMARY OF THE INVENTION

The present invention seeks to overcome the problem of sensing when an antifuse capacitor has blown, by connecting a transistor to the capacitor, and relying on the fact that, in one state, the transistor will be saturated, and then detecting when saturation occurs. Specifically, the transistor may be connected to the antifuse capacitor such that, when the antifuse capacitor is not blown, the transistor is saturated and draws a large base current, whereas, when the antifuse

capacitor is blown, the transistor is not saturated and draws a smaller base current. There is then provided means for monitoring the base current of the transistor, to determine whether the transistor is saturated, and hence to determine whether the antifuse capacitor is blown.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram of a trimming circuit in accordance with the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 shows a trimming circuit, based on an antifuse capacitor C, which is a poly1 to poly2 capacitor, with a value of 13.8fF. The capacitor acts as an antifuse, which means that, when it blows, which is when a voltage in the region of 45-55V is applied across its plates, it forms an essentially short circuit resistance of typically 80Ω. The capacitor C is connected between a ground rail GND of the circuit and a node I1. Before the capacitor C is blown, this node is pulled up towards the positive supply voltage +V1 by a transistor T5. In order to blow the capacitor, a voltage of at least about -50V must be applied at the node I1, and thereafter the node I1 is essentially at earth voltage, 0V.

The circuit used to blow the capacitor consists of transistors T1, T2, T3 and T4 and resistors R1 and R2. The transistor T1 is connected in series with a resistor R1, and with the base-emitter junction of a transistor T2, between a positive voltage supply rail +V1 and the ground rail GND. The positive supply rail +V1 supplies a voltage in the region of +5V. The collector of transistor T2 is connected to a current mirror circuit comprising transistors T3 and T4 and resistor R2, the emitters of the transistors and one end of the resistor being connected to the negative supply voltage -V2, which is greater than 60V below

GND, for example -70V. The collector of transistor T4 is connected to the node I1.

Thus, with I2 at GND, transistor T1 is conducting, and there is a voltage drop across the resistor R1. The resulting current flows through transistor T2 to the current mirror circuit, resulting in a corresponding current flowing through transistor T4, which pulls the node I1 down towards -V2.

With the current flowing through T4, and I1 approaching -V2, there is a sufficient voltage across the antifuse capacitor C to blow it.

Once blown, the capacitor is equivalent to an 80Ω resistor, i.e. effectively a short circuit. The node I1 is thus pulled to GND. The current through T4 is then switched off by switching I2 to +V1.

Thus, before the capacitor C blows, the node I1 is at a potential close to +V1, during zapping it is several tens of volts below GND, and, after the capacitor C has blown, it is at GND, zero volts. The remainder of the circuitry is for the purpose of detecting this difference. Although this could be achieved using a conventional high voltage comparator, such comparators have considerable surface areas, and are thus unsuitable for integration, particularly since a device may include several such trimming circuits.

Therefore, in order to sense that the capacitor C has blown, the transistor T5, which is a PNP transistor connected at its collector terminal to the node I1, and at its emitter terminal to the positive supply voltage +V1, is used.

Resistor R3 has a voltage of approximately 3V applied across it, which, with suitable component values, causes a current of approximately 5μA to flow through it. A current mirror circuit comprising transistors T6 and T7 causes a similar current of 5μA to flow through transistor T8, and this current then

acts as a reference current. Transistors T5 and T8 form a further current mirror circuit, with their emitters connected to the positive supply rail +V1, and their bases connected together. The bases of transistors T5 and T8 are also connected to the emitter of a transistor T9, which acts as a protection diode, with its base and collector terminals connected to the positive supply rail +V1. This prevents the bases of transistors T5 and T8 from being pulled much above the positive supply voltage +V1, which might otherwise happen when the terminal I1 is pulled down to the negative supply voltage -V2, and the capacitor C suddenly blows and pulls the terminal I1 up to GND. In the absence of the protection diode T9, this would run the risk that the voltage change at I1 would be coupled through the collector-base capacitance of T5, and similarly through T8, and damage the transistor T6.

The bases of transistors T5 and T8 are also connected to the emitter of a transistor T10. Thus, the base currents of transistors T5 and T8 flow through transistor T10, and then normally flow through transistor T11 to GND, T11 being configured as a 0.5μA current sink. The collector of transistor T10 is connected to the base of a further transistor T12, which has its emitter connected to the ground rail GND. Transistor T13 is connected between transistor T12 and the positive supply rail +V1, and its gate is connected to the gate of transistor T14, which is connected between the resistor R3 and the positive supply rail +V1.

When the capacitor C is blown, and the node I1 is at GND, the transistor T5 is unsaturated, and has a relatively small base current, which is able to flow through transistor T10 and the current sink T11 to GND. With the combined base currents of transistor T5 and T8 flowing through transistor T11 to GND, the collector of

the transistor T10 is pulled close to GND. Thus, in this situation, transistor T12 is turned off. With transistor T12 switched off, current flows through transistor T13, and an output terminal I3 is pulled up towards the positive supply voltage.

By contrast, if the capacitor C is not blown, it will be charged by transistor T5, such that I1 is pulled close to +V1 and therefore T5 will be saturated, and will therefore draw a much larger base current, for example up to 5μA. This is much larger than can flow through the current sink T11. The excess current therefore flows into the base of the transistor T12, which is therefore turned on, and so the output terminal I3 is pulled low towards the ground rail.

It is therefore possible to monitor the voltage at terminal I3 to determine whether transistor T5 is saturated, and hence whether antifuse capacitor C has blown. This allows the state of the antifuse capacitor to be monitored in a simple way, using a relatively small number of components, so that the circuitry can be included in an integrated circuit design.

CLAIMS

1. A trimming circuit, comprising an antifuse capacitor, the antifuse capacitor having a first terminal connected to a ground rail, and a second terminal to which a voltage may be selectively applied to blow the capacitor, the circuit further comprising:

a first transistor, with its collector-emitter path connected between a first supply voltage rail and the second terminal of the capacitor;

a current source, connected to the second terminal of the capacitor, such that, when the antifuse capacitor is not blown, the first transistor is saturated and draws a large base current, whereas, when the antifuse capacitor is blown, the first transistor is not saturated and draws a smaller base current; and

means for monitoring the base current of the first transistor to determine when the first transistor is saturated.

2. A trimming circuit as claimed in claim 1, wherein the current source comprises a first current mirror circuit comprising a first pair of transistors, a first transistor of the pair having its collector-emitter path connected between the second terminal of the capacitor and a second supply voltage which is sufficient to blow the antifuse capacitor, and a second transistor of the pair having its collector-emitter path connected between the first supply voltage and a second supply voltage through a further transistor which is controlled from an input terminal of the circuit.

3. A trimming circuit as claimed in claim 1 or 2, wherein the base terminal of the first transistor is connected to a current sink, and to the base terminal of a second transistor, such that, when the first transistor is unsaturated, its base current flows through the current sink, and the second transistor is

switched off, and, when the first transistor is saturated, the second transistor is switched on.

4. A trimming circuit as claimed in claim 3, wherein the first transistor forms a current mirror circuit with a third transistor, the bases of the first and third transistors being connected together, and the circuit comprises means for drawing a reference current through the third transistor.

5. A trimming circuit, comprising an antifuse capacitor, and means for selectively applying a suitable voltage thereto to blow the antifuse capacitor, and further comprising:

a first current mirror circuit, comprising first and second transistors, the first transistor being connected between one terminal of the antifuse capacitor and a supply voltage rail;

a third transistor, connected to the bases of the first and second transistors, such that the base currents of the first and second transistors flow therethrough;

a current sink, connected to receive the current flowing through the third transistor;

a fourth transistor, with its collector-emitter path connected in series with a load element between the supply voltage rail and a ground rail, and with its base terminal connected to the connection of the third transistor and the current sink; and

an output terminal located between the load element and the fourth transistor.

6. A trimming circuit as claimed in claim 5, wherein, when the antifuse capacitor is not blown, the first transistor is saturated and therefore has a large base current, which causes the base terminal of the fourth transistor to receive a current which switches the fourth transistor on, and therefore causes the voltage at the output terminal to approach ground

voltage,

whereas, when the antifuse capacitor is blown, the first transistor is not saturated, and therefore has a smaller base current, which flows through the current sink, so that the base terminal of the fourth transistor receives no current, so that the fourth transistor is switched off, and therefore causes the voltage at the output terminal to go high.

7. A method of monitoring the state of an antifuse capacitor, the antifuse capacitor having a first terminal connected to a ground rail, and a second terminal to which a voltage may be selectively applied to blow the capacitor, the circuit further comprising a current source, connected to the second terminal of the capacitor, the method comprising:

connecting a transistor with its collector-emitter path between a first supply voltage rail and the second terminal of the capacitor, such that, when the antifuse capacitor is not blown, the first transistor is saturated and draws a large base current, whereas, when the antifuse capacitor is blown, the first transistor is not saturated and draws a smaller base current; and

monitoring the base current of the first transistor to determine when the first transistor is saturated.

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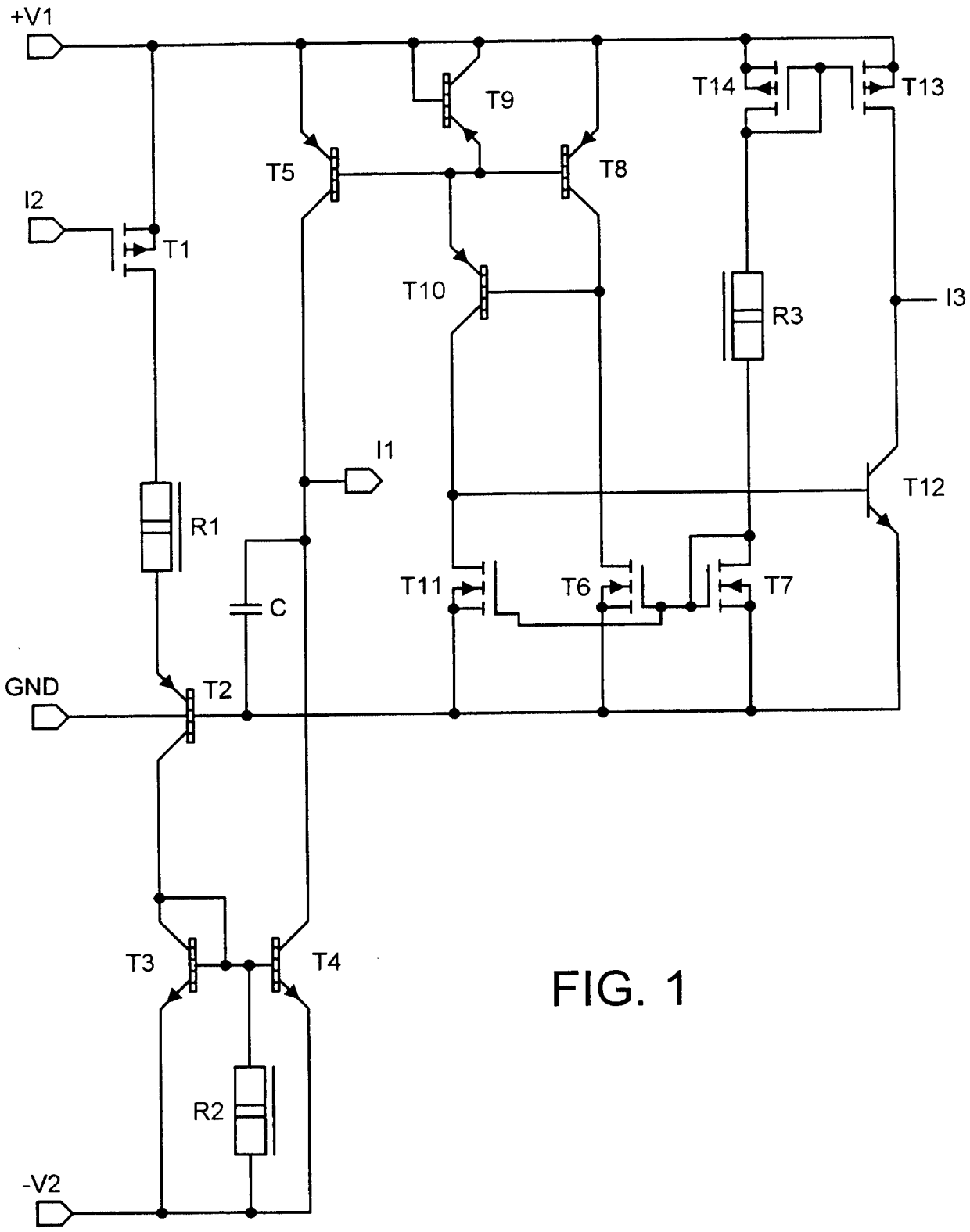
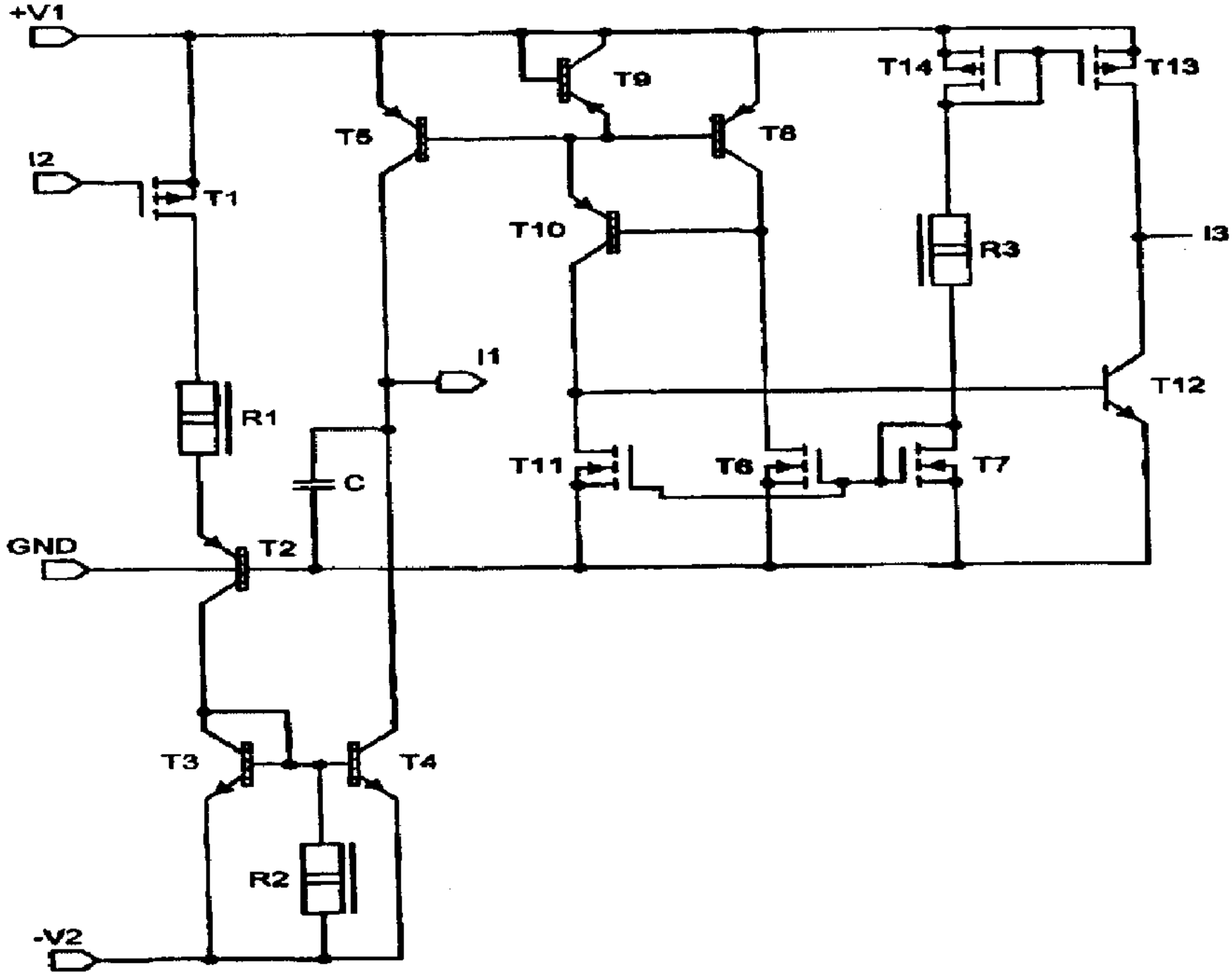


FIG. 1


+V1
I2
T1
T5
T9
T8
T14
T13
T10
R3
I3
I1
R1
T12
C
T11
T6
T7
GND
T2
T3
T4
R2
-V2