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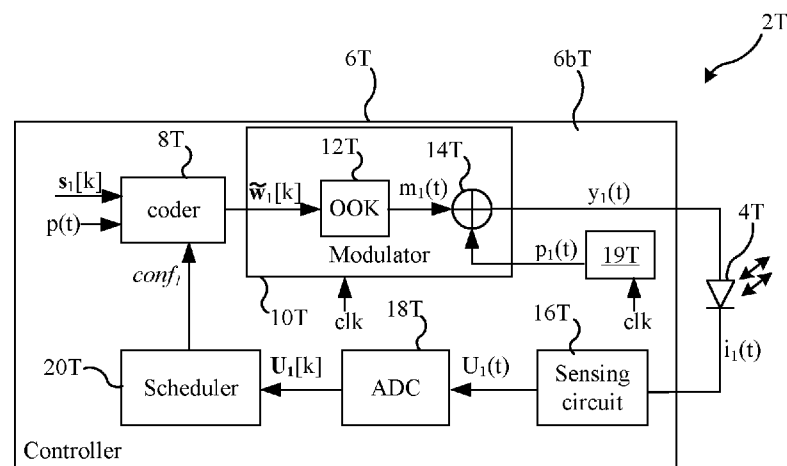


FIG. 1A

(57) **Abstract:** A light source for use in a visible light communications system is driven in the following manner. On-off key modulation is applied to a data sequence to embed it in a data signal as on-off keyed amplitude modulations of the data signal. A pulse width modulation dimming signal. The data signal and the dimming signal are synchronized with each other. A drive signal is generated by summing the data signal with the dimming signal. The drive signal is supplied to the light source to vary an intensity of light emitted by the light source according to the drive signal, thereby transmitting the embedded data sequence to a receiving device whilst simultaneously providing dimmable illumination.



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Controlling a Light Source

TECHNICAL FIELD

The present invention pertains to visible light communication, wherein a data sequence is modulated into light (i.e. visible radiation) emitted by a light source.

5 BACKGROUND

Visible light communications (VLC), also referred to herein as "coded light", is drawing increasing interest as a means of communication, particularly with recent developments in solid-state lighting, e.g. using modern forms of light-emitting diodes (LEDs), such as semiconductor LEDs, organic LEDs or polymer LEDs. VLC refers to a
10 scheme whereby information is embedded in visible light using suitable modulation, for example in the illumination output of a luminaire(s) of a lighting system whose primary function is one of illuminating all or part of an environment. The visible light from LEDs is modulated such that the information is embedded in a manner that is imperceptible to users. VLC enables a wide range of applications. For instance, it has applications for intelligent
15 lighting systems, such as remote lighting control and lamp status monitoring, etc. Other applications based on light interaction and actuation are becoming viable as the technology develops.

Modern LED-based lighting systems are particularly suitable for coded light applications. Different forms of modulation and access schemes such as FDMA, CDMA etc.
20 may be used to achieve this. For a low cost driver implementation, the fundamental frequency of communication may be restricted to around 2 kHz. This in turn limits the data rate that can be supported on a visible light communication link between two luminaires maximally to the order of a few kbps, which in turn limits the network throughput.

A coding scheme which may be used for coded light is Manchester coding,
25 which means any coding scheme in which each bit of a sequence is encoded as either a high-to-low transition or a low-to-high transition of a modulated characteristic over a bit transmission interval having a duration T_b ("bit duration"). A clock signal having a period T_b may be used to this end. Manchester-coded data can be modulated into visible illumination in a number of different ways. For example it may be amplitude modulated where "high" and

"low" are represented by different amplitudes, e.g. by transitioning an emitting state (denoted an "ON cycle" herein) and a non-emitting state ("OFF cycle") of the luminaire at a frequency that is sufficiently high that the transitions are imperceptible to a human eye. That is, in which the modulated characteristic is the intensity of the illumination.

Manchester coding has certain properties that make it particularly suitable for coded light applications. For example, for amplitude modulation based on Manchester coding, provided the frequency of the modulations is sufficiently high that they are imperceptible to the human eye, the perceived intensity of the illumination from a luminaire will be proportional to the DC component of the modulated illumination (as the human visual system effectively averages out the high-frequency AC components to zero). A benefit of Manchester coding is that the DC component is independent of the coded data, which in turn means the perceived intensity of the illumination is independent of the coded data. This is because Manchester coding is DC-balanced. As such, the primary illumination function of the system is not negatively affected by the addition of coded light capability. Moreover, the DC component and hence the perceived intensity of the illumination can be varied by varying the duty cycle of the modulation independently of the coded data, the duty cycle being the fraction Q of each bit transmission interval for which the luminaire is in the emitting state, i.e. the duration of the ON cycle relative to T_b . This is a form of dimming, referred to as pulse width modulation ("PWM"), with which Manchester coding is compatible. The perceived intensity of the illumination will be $Q \cdot I$, where I is the (actual) intensity of the illumination when emitting during the ON cycle, and the duty cycle Q constitutes a dimming level in this context. Manchester coding is a DC-balanced, run-length limited (RLL) coding scheme and other forms of DC-balanced RLL coding may be similarly applicable to VLC communications.

SUMMARY

In practical contexts, there can be a trade-off between data rate and dimming levels. For example, in some VLC systems incorporating PWM dimming, it is not possible to achieve reasonable communication rates when the ON or OFF period of a PWM cycle is close to unity (i.e. a duty cycle close to one or zero respectively).

Various aspect of the present invention relate to a data transmission scheme, to achieve VLC while providing illumination from a transmitting light source over a large dimming range.

A first aspect of the present invention is directed to a drive system for a light source for use in a visible light communication system, the drive system comprising:

a data input configured to receive a data sequence to be transmitted;

a modulator configured to apply on-off key modulation to the data sequence to embed it in a data signal as on-off keyed amplitude modulations of the data signal;

a dimming signal generator configured to generate a pulse width modulation dimming signal;

a signal combiner having a data signal input connected to receive the data signal and a dimming input connected to receive the dimming signal;

wherein the data signal and the dimming signal are synchronized with each other;

wherein the signal combiner is configured to generate a drive signal by summing the data signal with the dimming signal; and

wherein the signal combiner has a drive output configured to supply the drive signal to the light source to vary an intensity of light emitted by the light source according to the drive signal, thereby transmitting the embedded data sequence to a receiving device whilst simultaneously providing dimmable illumination.

The dimming level can be adjusted by adjusting the duty cycle of the pulse width modulation dimming signal. Note that changing the dimming level in this manner does not change the duty cycle of the data signal i.e. in contrast to existing pulse width modulation dimming systems, changing the dimming level does not change the duration over which each bit is represented. This is beneficial as it means that the dimming level can be increased without reducing the maximum rate at which the data sequence can be transmitted, even for a duty cycle close or equal to one.

The drive system implements a two-stage modulation process. In the first stage, the coded data is modulated into a data signal as on-off keyed (OOK) amplitude modulations, i.e. each bit is represented over an equal duration as a presence of a first carrier, i.e. a non-zero level (data signal "ON"), or an absence, i.e. zero-level, of that carrier (data signal "OFF"), e.g. a voltage or current carrier. In the second stage, the OOK data signal is summed with a pulse-width modulation (PWM) dimming signal to generate a composite drive signal, e.g. a drive voltage or drive current, which drives the transmitting LED lamp. This simultaneously provides data transmission and illumination, thus achieving dimming over a wide range where the dimming level is adjustable by adjusting the duty cycle of the PWM dimming signal.

The pulse width modulation signal is a periodic rectangular waveform i.e. which varies between a zero and a non-zero level of a second carrier (e.g. a voltage or current carrier), having an adjustable duty cycle Q. The drive signal thus varies between four levels, corresponding to:

- 5 1. data and dimming signals OFF
2. data signal OFF, dimming signal ON
3. data signal ON, dimming signal OFF
4. data and dimming signals ON

The data signal and the pulse width modulation signal are synchronized with
10 each other, i.e. so that transitions in the data signal and the dimming signal are synchronized with each other. In the described embodiments, each on and off cycle of the pulse width modulation signal has a duration that is an integer multiple of a "bit duration" of the data signal, and at least one transition in the pulse width modulation signal occurs simultaneously with a transition in the data signal. The bit duration means the duration over which one bit is
15 represented in the data signal, after any coding has been applied, i.e. corresponding to one transmission symbol carrying one bit of (coded) data.

In embodiments, the drive system may further comprise a coder configured to code the data sequence and output the coded data sequence to the modulator, said modulation being applied to the coded data sequence.

20 The coder may be configured to generate a plurality of redundant marker bits in the coded data sequence so as to mark a plurality of successive transitions in the pulse width modulation dimming signal. An advantage of the marker bits is that they allow decoding at the receiver to be simplified. For example, the coder may be configured to generate a DC-balanced pair of redundant marker bits in the coded data sequence to mark
25 each of the transitions.

The coding may be a DC-balanced, run-length limited coding. This ensures flicker-free illumination, at a perceived intensity that is independent of the data embedded in the light.

30 The drive system may also comprise a scheduler configured to detect a clear channel condition during an off cycle of the pulse width modulation dimming signal occurring prior to said transmission, and to instigate said transmission in response to the detection of the clear channel condition.

The scheduler may be configured to use at least one LED of the light source as a sensor to detect the clear channel condition. Alternatively, the scheduler may use a radiation sensor collocated with the light source to perform this detection.

A second aspect of the present invention is directed to a transmitter comprising a drive system according to the first aspect, and a light source connected to the drive output of the drive system.

In embodiments of the second aspect, the drive system of the transmitter may be configured according to any embodiment of the first aspect.

The drive signal may be a voltage applied across the light source, and the light source may have a maximum rated voltage $V_{f,max}$ and a nominal voltage $V_{f,norm}$. The drive signal may be a weighted sum of the data and dimming signals, in which a first weighting factor is applied to the data signal and a second weighting factor is applied to the pulse width modulation signal, wherein the second weight factor divided by the first weight factor is no more than $\frac{V_{f,max}}{V_{f,norm}} - 1$. This optimizes the drive voltage for the light source, as described in further detail below.

A third aspect of the present invention is directed to visible light communications system comprising a transmitter according to the second aspect or any embodiment thereof, and a receiver, wherein the receiver comprises: a light source configured to emit light exhibiting periodic intensity variations thereby providing illumination; and a decoder configured to determine the transmitted data sequence from light emitted by the transmitter and sensed at the receiver during off cycles of the period intensity variations.

The decoder may be configured to use the light source of the receiver as a sensor to sense the light during the off cycles of periodic intensity variations. Alternatively, the receiver may comprise a radiation sensor collocated with the light source which is used to perform this sensing.

As noted, the coder of the transmitter-side drive system may generated marker bits into the coded data sequence. Preferably, the marker bits are inserted so as to cause, for each of the plurality of successive transitions in the pulse width modulation dimming signal, a matching transition in the data signal independently of the data sequence, thereby marking that transition.

Advantageously, this allows the receiver to implement a particularly simple decoding scheme, wherein the decoder of the receiver is configured to decode the sensed

light applying the following decoding operations for each off cycle of the periodic intensity variations:

- if a high-to-low intensity transition is detected in the sensed light in that off cycle, generating a pair of non-matching bits;

5 - if a low-to-high intensity transition is detected in the sensed light in that off cycle, generating a different pair of non-matching bits;

- if no intensity transition is detected in the sensed light in that off cycle:

- generating a pair of matching bits if the intensity is below a threshold, and

10 - generating a different pair of matching bits if the intensity is above a threshold.

A fourth aspect of the present invention is directed to a method of driving a light source for use in a visible light communication system, the method comprising:

- receiving a data sequence to be transmitted;

15 applying on-off key modulation to the data sequence to embed it in a data signal as on-off keyed amplitude modulations of the data signal;

- receiving a pulse width modulation dimming signal, wherein the data signal and the dimming signal are synchronized with each other;

- generating a drive signal by summing the data signal with the dimming signal;

20 and

- supplying the drive signal to the light source to vary an intensity of light emitted by the light source according to the drive signal, thereby transmitting the embedded data sequence to a receiving device whilst simultaneously providing dimmable illumination.

25 In embodiments of the fourth aspect, any feature of the first second or third aspect or any embodiment thereof may be implemented.

A fifth aspect of the present invention is directed to a method of receiving a light signal, the method comprising implementing by a receiving device the following steps:

- receiving at the receiver a light signal in which a sequence of bits is embedded as amplitude modulations;

30 controlling a light source of the receiving device to emit a periodic sensing signal having regular off cycles, wherein the period of the sensing signal is twice a bit duration of the light signal, and wherein the sensing signal and the light signal have a non-zero phase offset; and

decoding the light signal by generating, for each off cycle of the sensing signal, a pair of bits from a portion of the light signal received during that off cycle.

In embodiments, the light signal may vary between four intensity levels Y0, Y1, Y2, Y3, and only exhibit transitions between Y0 and Y1, Y2 and Y3 and Y0 and Y3. In this case, the decoding step may be performed by applying the following operations for each off cycle of the sensing signal:

- if a high-to-low intensity transition is detected in the sensed light in that off cycle, generating a pair of non-matching bits;
- if a low-to-high intensity transition is detected in the sensed light in that off cycle, generating a different pair of non-matching bits;
- if no intensity transition is detected in the sensed light in that off cycle:
- generating a pair of matching bits if the intensity is below a threshold, and
- generating a different pair of matching bits if the intensity is above a threshold.

A sixth aspect of the present invention is directed to a computer program product comprising code stored on a computer readable storage medium and configured when executed to implement the method of the fourth aspect or any embodiment thereof.

BRIEF DESCRIPTION OF FIGURES

For a better understanding of the present invention, and to show how the same may be carried into effect, reference is made to the following figures in which:

Fig. 1A shows a schematic block diagram of a VLC transmitter;

Fig. 1B shows a schematic block diagram of a VLC receiver;

Fig. 1C shows a schematic block diagram of a VLC communication system;

Fig. 2A shows an example data frame and timeslot structure for a VLC transmission scheme;

Fig. 2B shows an example of a data signal, a pulse width modulation dimming signal, and a composite drive signal generated by a VLC transmitter;

Figs. 3A and 3B demonstrates how exemplary optical signaling waveforms may be detected for decoding at a receiver;

Fig. 3C shows an example of a VLC signal received during an OFF cycle at a VLC receiver;

Fig. 3D shows a flow chart for a method of decoding a VLC signal received during OFF cycles at a VLC transmitter;

Fig. 4 illustrates principles on which a medium access control protocol is based, to allow multiple VLC transmitted to communicate with a single VLC receiver;

Fig. 5 shows an example architecture of a VLC modulator;

Fig. 5A shows an alternative architecture preferred for large-scale LED lamps;

Fig. 6 shows an alternative sensor architecture for a VLC transmitter or VLC receiver, in which a dedicated sensor is used;

Fig. 7A shows an exemplary lighting system comprising a plurality of luminaires;

Fig. 7B-E illustrate various ways in which a VLC transmitter or VLC receiver can be incorporated into a lighting system;

Fig. 8A illustrates a broadcast network topology with multiple receivers having non-overlapping field of views; and

Fig. 8B illustrates a broadcast network topology with multiple receivers having overlapping field of views.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

In the described embodiments, a VLC communications system, in the form of a lighting system, is described below in which a pair of LED lamps (luminaires) are driven by a physical layer protocol, wherein information, encoded using run-length limited (RLL) coding, is modulated into the light output of one LED lamp thereby transmitting it to, so that it can be detected at, the other. The transmitting LED is configured in the manner described above. The receiving LED lamp is similarly configured, however it emits a predetermined sensing sequence, such that its one or more LEDs exhibit period intensity variations having OFF cycles at regular intervals. During those regular OFF cycles, it senses the light emitted by the transmitting lamp – using either those one or more LEDs themselves, or a radiation sensor collocated with the one or more LEDs. The receiving LED lamp decodes the transmitted bit sequence, for example by applying a discrete wavelet analysis or a first-order time differential analysis on collected measurements at each OFF cycle of its own PWM signal.

To allow multiple LED lamps to transmit to the same receiving lamp, a medium access control (MAC) layer protocol is provided, for use in a visible light communication network having a star topology. This is based on clear-channel assessment (CCA) measurements performed by each transmitting lamp during the OFF cycles of their PWM signals, in a similar fashion to the data sensing at the receiving lamp.

Figure 1A shows a block diagram of a VLC transmitter 2T, which comprises a first light source 4T. The first light source 4T is an LED light source, comprising at least one LED for emitting illumination. The VLC transmitter 2T also comprises a first drive system 6T, configured to operate as a data transmission controller. The data transmission controller 6T is able to control at least an intensity of light emitted by the first light source 4T.

Figure 1B shows a block diagram of a VLC receiver 2R, which comprises a second light source 4R. The second light source 4R is also an LED light source, comprising at least one LED for emitting illumination. The VLC receiver 2R also comprises a second drive system 6R, which is configured to operate as a data reception controller. The data reception controller 6R is able to control at least an intensity of the light emitted by the second light source 4R.

As illustrated in Figure 1C and described in further detail below, a data sequence $s_1[k]$ is modulated into the illumination output by the first light source 4T of the transmitter 2T and thereby transmitted via a free-space channel where it may be received by the receiver 2R. When it is received at the receiver 2R, via the second light source 4R of the receiver 2R. That is, the second light source 4R itself is used as a sensor, during intervals when it is in a non-emitting state.

This exploits the fact that LEDs can be used not only as radiation emitters but also as radiation detectors: when an LED is itself in a non-emitting state, a small but detectable voltage is induced across the non-emitting LED when exposed to a certain type of radiation (visible light, non-visible electromagnetic radiation or a combination of both depending on the physical characteristics of the LED). In the present context, "non-emitting state" means that the LED is emitting no radiation or a negligible amount of radiation itself i.e. an amount that is sufficiently small for this small induced voltage to be detectable. The idea of exploiting this effect to use LEDs as both receivers and transmitters (i.e. as communication transceivers) to provide two-way communication to has been explored, for example, in S. Schmid et al., "LED-to-LED visible light communication networks" ACM MobiHoc 2013. This however requires timeslot synchronization and LEDs that are completely OFF during the consecutive symbol duration of the 2-PPM (pulse position modulation) transmission.

The first light source 4T of the transmitter 2T may also be used as a sensor in a similar fashion, to facilitate an appropriate scheduling of the transmission of the data sequence $s_1[k]$ by a scheduler 20T of the transmitter 2T, in a scenario in which multiple transmitters are communicating with receiver 2R: as described in further detail below,

scheduler 20T generates a confirmation signal $conf_1$ if and when it detects a clear channel condition on the free-space channel, triggering the transmission of $s_1[k]$.

To this end, each of the controllers 6T, 6R comprises a respective sensing circuit 16T, 16R connected to its respective light source 4T, 4R. Each light source 4T, 4R is connected to its respective sensing circuit 16T, 16R and operates in a short-circuit mode, i.e. such that a voltage induced across it causes a respective current $i_1(t), i_2(t)$ (photocurrent) to flow, each of which can vary as a function of time.

Each sensing circuit 16T, 16R detects the respective photocurrent $i_1(t), i_2(t)$ and comprises a respective trans-impedance amplifier (TIA), which converts it to a respective voltage signal $U_1(t), U_2(t)$.

The transmission and reception controllers 6T, 6R each comprise a respective analogue-to-digital converter (ADC) 18T, 18R, which samples the respective voltage signal $U_1(t), U_2(t)$ to convert it to a digital form, denoted $U_1[k], U_2[k]$ respectively.

The transmission and reception controllers 6T, 6R each comprise a respective data coder 8T, 8R and a respective modulator 10T, 10R having an output connected to an input of the coder 8T, 8R.

The coder 8T of the transmitter 2T has an input connected to receive the data sequence $s_1[k]$ to be transmitted to the receiver 2R. The coder 8T codes the data sequence $s_1[k]$.

The coding applied by the coder 8T is a two-stage coding.

In the first coding stage, $s_1[k]$ is coded according to a DC-balanced, run-length limited (RLL) code – the resulting coded-bit sequence is denoted $w_1[k]$ (Figure 2A).

As is well known in the art, RLL code is a line coding, wherein a maximum and a minimum on the number of 0s that can occur between consecutive 1s in the coded data is imposed. The run-length limiting prevents flicker, which could otherwise occur in the illumination outputted by the light source due to long runs of 1s and 0s.

A DC-balanced code means a code defined for a set of data units (each data unit being one bit or a sequence of bits of pre-determined length), wherein each of the data units is coded as a respective code word having an equal number of 1s and 0s.

In the following example, the DC-balanced RLL code is 4B6B RLL code. Alternatively, other standard RLL codes like Manchester code or 8B10B can be used and give different code redundancies.

The notation xByB means that each x-bit sub-sequence of the input sequence $s_1[k]$ is coded as a y-bit sequence, e.g. for 4B6B every four bits of unencoded data in $s_1[k]$ are represented as 6 bits of encoded data in $w_1[k]$.

In the second coding stage, additional redundancy bits ("marker bits") are added to $w_1[k]$ based on a PWM dimming signal $p_1(t)$, which is a pulse width modulation signal – the resulting sequence is denoted $\tilde{w}_1[k]$. This additional redundancy is described in further detail below; for now, suffice-it to say that the additional redundancy bits are such that $\tilde{w}_1[k]$ is also DC-balanced and run-length limited, and function as markers of transitions in the PWM dimming signal $p_1(t)$ for the benefit of the receiver 2R.

The modulator 10T of the transmitter 2T comprises an on-off key (OOK) modulator 12T connected to receive the coded sequence $\tilde{w}_1[k]$, and a summing amplifier 14T having a data signal input connected to an output of the OOK modulator 12T and dimming input connected to receive the PWM dimming signal $p_1(t)$.

The OOK modulator 12T modulates the coded sequence $\tilde{w}_1[k]$ using on-off-keying, i.e. such that $\tilde{w}_1[k]$ is represented as transitions between a zero-value (OFF) and a non-zero value (ON) of a data signal $m_1(t)$.

As illustrated in Figure 2A, bits of $\tilde{w}_1[k]$ are represented by respective portions of $m_1(t)$ of equal duration ("bit duration"), over which $m_1(t)$ remains constant (either zero or non-zero, depending on the bit being represented). The bit duration is denoted T_b , and corresponds to one timeslot TS of a physical layer transmission frame $F[t]$. Accordingly, $\tilde{w}_1[k]$ is represented by a sequence of binary values of $m_1(t)$ in a sequence of timeslots, i.e. one-bit per timeslot TS. The bit duration T_b is defined by a clock signal clk , received at the modulator 10.

As all of the timeslots TS have equal duration T_b , which means the data signal $m_1(t)$ has an inherent dimming level fixed at 50%. To allow the dimming level to be varied, $m_1(t)$ is not used to drive the light source 4T directly. Instead, $m_1(t)$ is combined with the PWM signal $p_1(t)$ in the following manner.

As shown in Figure 2A, the PWM signal $p_1(t)$ is a periodic signal having a period $T_p = M \cdot T_b$, where M is an integer greater than one. During each period T_p , the PWM signal $p_1(t)$ has one ON-cycle (of duration $Q \cdot T_p$) and one OFF-duration $((1-Q) \cdot T_p)$. Both $Q \cdot T_p$ and $(1-Q) \cdot T_p$ are respective integer multiples of T_b and $p_1(t)$ is synchronized with $m_1(t)$, such that every ON-to-OFF and OFF-to-ON transition of $p_1(t)$ coincides in time with a boundary between a pair of adjacent timeslots TS. The transmission controller 6T

comprises a dimming signal generator (19T, Figure 1A) configured to generate the dimming signal $p_1(t)$ using a matching clock signal clk to achieve this synchronization. Here, Q is the duty cycle of $p_1(t)$ and constitutes a dimming level as will become apparent. As T_p , $Q \cdot T_p$ and $(1-Q) \cdot T_p$ can all be expressed as multiples from T_p , this establishes a minimum and a maximum dimming level.

The OOK signal $m_1(t)$ is added to the PWM signal $p_1(t)$ to generate a composite drive signal, which is a (weighted) sum of $m_1(t)$ and $p_1(t)$:

$$y_1(t) = A * m_1(t) + B * p_1(t)$$

where A and B are weighting factors determined by the architecture of summing amplifier 14T (see below). In this example, both $m_1(t)$ and $p_1(t)$ vary between a voltage of 0 (OFF) and V_{pp} (ON).

An example is shown in Figure 2B. As can be seen, during OFF-cycles of $p_1(t)$, $y_1(t)$ varies between a first pair of values:

$$(Y0, Y1) = (0, A * V_{pp})$$

During ON-cycles of $p_1(t)$, $y_1(t)$ varies between a second, different pair of values:

$$(Y2, Y3) = (B * V_{pp}, (A + B) * V_{pp})$$

both of which are greater than both of the first pair of values.

The portion of $y_1(t)$ within one timeslot TS constitutes one symbol, representing one bit of coded data. Each type of bit (i.e. 0 or 1) is represented by one of two different symbols (0 by $Y0$ or $Y2$; 1 by $Y1$ or $Y3$) depending on whether it occurs during an ON or OFF cycle of $p_1(t)$.

In this example, $m_1(t)$, $p_1(t)$ and $y_1(t)$ are time-varying voltages, such that $y_1(t)$ varies between four voltage levels (one of which – $Y0$ – is zero). The output voltage $y_1(t)$ is applied accords the light source 4T, thereby driving the light source 4T, such that each of the four possible levels of $y_1(t)$, i.e. ($Y0$, $Y1$, $Y2$, $Y3$) causes the light source to output a light 4T of a different intensity ($Y0$ corresponding to zero-intensity, i.e. non-emitting). That is, each of ($Y0$, $Y1$, $Y2$, $Y3$) constitutes a different illumination level, corresponding to a different intensity of light emitted by the light source 4T.

However $y_1(t)$ has a frequency high enough that these are not perceptible individually to a human eye, i.e. such that there is no perceived flicker. PWM dimmed LED light source are most prone to visible flicker and stroboscopic flicker. For each of these types of flicker, there is a widely accepted lower bound of PWM frequency that is around 200 Hz

and 800 Hz respectively. Accordingly, an upper bound can be imposed on the period T_p of $p_1(t)$ as:

$$T_p \leq 1/f_0$$

where f_0 equals 200 Hz or 800 Hz depending on the application.

5 Signal $y_1(t)$ is able to control illumination level at a range of $[\epsilon_1, 1 + \epsilon_1]$ with a constant ϵ_1 determined by the power of signal $m_1(t)$. By changing Q, the perceived intensity of the emitted light is reduced, as the time-averaged amplitude of $y_1(t)$ is changed as a result.

10 The redundant bits added to $w_1[k]$ in the second coding step to generate $\tilde{w}_1[k]$ can also be seen in Figure 2A. The redundancy bits are added in DC-balanced pairs, based on the PWM signal $p_1(t)$, independently of the data sequence $s_1[k]$ itself. As shown, a (0,1) pair of redundancy bits is added to $w_1[k]$ at adjacent positions corresponding to the timeslots TS either side of every ON-to-OFF transition of $p_1[k]$; a (1,0) pair of redundancy bits is added to $w_1[k]$ at adjacent positions corresponding to the timeslots TS either side of every OFF-to-ON transition of $p_1[k]$. Accordingly, for every ON-to-OFF transition of $p_1[k]$, $m_1(t)$ is guaranteed to transition from Y4 to Y0 (i.e. ON-to-OFF also); for every OFF-to-ON transition, $m_1(t)$ is guaranteed to transition from Y0 to Y4 (i.e. OFF-to-ON also). As such, for every transition in $p_1[k]$ $m_1(t)$ exhibits a matching transition. As explained below, this allows the decoding by receiver 2R to be simplified.

20 By way of example, table 1 shows a standard 4B6B code that may be used by the coder 8T.

Hex value	4-bit input	6-bit output
0x0	0000	001110
0x1	0001	001101
0x2	0010	010011
0x3	0011	010110
0x4	0100	010101
0x5	0101	100011

0x6	0110	100110
0x7	0111	100101
0x8	1000	011001
0x9	1001	011010
0xA	1010	011100
0xB	1011	110001
0xC	1100	110010
0xD	1101	101001
0xE	1110	101010
0xF	1111	101100

Table I: Standard 4B6B code.

As highlighted in Table I, 4B6B code gives a maximum run number of $R_n=4$, i.e. a maximum of four consecutive 0s or 1s (e.g. when transmitting a hex data '0x0' after '0xF'). Consequently, there is a long OFF slot in signal $m_1(t)$. To prevent flicker, the following constraint is imposed on the bit duration T_b

$$\frac{1}{R_n \times T_b} \geq 200 \text{ Hz} \Rightarrow T_b \leq 1.5 \text{ ms}$$

for $R_n = 4$. This also holds for other maximum run numbers R_n .

Receiver 2R has an architecture similar to the transmitter 2T but with different inputs. The data reception controller also comprises a data coder 8R and a modulator 10R (itself comprising an OOK modulator 12R and summing amplifier 14R), which correspond to those of the transmitter 2T. Accordingly, all description pertaining to components 8T, 10T, 12T and 14T of the transmitter 2T apply equally to components 8R, 10R, 12R, 14R of the receiver 2R. The modulator 10 has access to a matching clock signal clk , such that the transmitter 4T and receiver 4R can define timeslots TS of the same duration T_b .

However, the coder 8R of the receiver 2R receives a dedicated sensing sequence $s_2[k]$, which is also coded using xByB coding to generate a coded sensing sequence $w_2[k] = \{0,1,0,1,0,1,0,1,\dots\}$ i.e. a repeating sequence of single 1s and single 0s.

Accordingly, $m_2(t)$ is dedicated sensing signal in the form of a square wave. Moreover, for the receiver 2R, a constant zero signal $p_2(t) = 0$ is applied to the dimming input of the summing amplifier 12R. Accordingly, the voltage $y_2(t)$ used to drive the light source 4R is remains equal to $m_2(t)$ at all times. As such, the intensity of the light emitted by the light source 4R simply varies as a square wave, between 0 and a single non-zero value such that light source 4R is in a non-emitting state every other timeslot TS. Following the 4B6B example, for $s_2[k] = (0, 1, 0, 0)$, $w_1 = (0, 1, 0, 1, 0, 1)$ and hence causes signal $m_2(t)$ to alternate regularly between OFF and ON. No redundancy bits are added to w_2 , because there are no transitions of $p_2(t) = 0$.

This allows the light source 4R of the receiver 2R to provide illumination, whilst still being able to receive the modulated data sequence $\tilde{w}_1[k]$ from the transmitter 2T using the light source 4R as a sensor during the regular OFF cycles of $y_2(t) = m_2(t)$ that occur every other timeslot TS.

Note that it is not necessary for the receiver 2R to generate square wave intensity variations in this manner – there are simpler ways in which this can be achieved. However, an advantage of the above scheme is that the same architecture is used for both the transmitter 2T and receiver 2R – a device incorporating this architecture can therefore switch between from a transmitting mode, in which it operates as a transmitter 2T, to a receive mode, in which it operates as a receiver 2R simply by setting the data and dimming inputs accordingly.

When operating as a receiver 2R, as noted, the signal applied to the dimming input of the receiver's summing amplifier 12R remains fixed at zero in this example. Thus, it is only possible to vary the dimming level using this dimming input when operating as a transmitter 2T example.

However, as an alternative to fixing $p_2(t) = 0$, the receiver The receiver can also reach four dimming levels: 0, $m_2(t)$, $p_2(t)$, $m_2(t) + p_2(t)$, providing that $p_2(t)$ is generated at the same frequency and duty cycle as $m_2(t)$ i.e. so that $p_2(t)$ remains OFF for every OFF cycle of $m_2(t)$ such that regular sensing intervals are still provided. This provides greater dimming flexibility at the receiver side and is preferably implemented purely in software executed at the receiver 2R.

A mechanism by which the receiver 2R can receive the data is illustrated in Figures 3A, for a simplified example of $p_1(t) = 0$, and in Figure 3B for an example in which $p_1(t)$ is varying. These figures illustrate exemplary signaling waveforms depicting

asynchronous communication between LED light sources 4T (transmitter) and 4R (receiver). The transmitter 2T and receiver 2R are out of phase by an amount θ i.e. the receiver's timeslots are offset from the transmitter's timeslots in time, such that they are out of sync with one another.

5 Hz
 T

The decoder 22R of the receiver 2R implements a decoding scheme, which makes use of the phase offset θ between two LED light sources.

10 In the simplified example of figure 3A, the top-most of the two waveforms corresponds to the modulation signal $m_1(t)$, and the middle waveform to the dedicated sensing signal $m_2(t)$. During the OFF cycles of $m_2(t)$, sensing circuit 16T of the receiver 2T measures the photocurrent $i_2(t)$ that is proportional to the power of signal $m_1(t)$, and which is conveyed to voltage $U_2(t)$ shown as a dashed curve at the bottom of Figure 3A. As noted above, ADC 18T convert this voltage to a digital form $U_2[k]$.

15 Decoder 22R performs decoding in two stages, as illustrated in the flowchart of Figure 3D. For each OFF cycle of $m_2(t)$, the decoder decodes two bits from $U_2[k]$ – which is possible due to the phase offset θ as is evident in Figures 3A and 3B.

20 At step S2, decoder 22R detects whether there is a discontinuity in discontinuity in the digital voltage samples $U_2[k]$ (caused by a transition in $y_1(t)$ during a current OFF cycle of $m_2(t)$). An example is shown in Fig. 3C, which shows about 100 ADC measurements of $U_2[k]$ distorted by additive Gaussian noise.

25 If so, the decoder determines (S4) whether the transition is falling, i.e. from a higher value of $y_1(t)$ to a lower value of $y_1(t)$, or rising, i.e. *vice versa*. This can for example detected by decoder 22R generating first level and second level Daubechies 4 wavelet coefficients, as illustrated in Figure 3C. Each of these has peaks presenting only around the discontinuity. The decoder outputs two binary values depending on the sign of peak coefficients listed in table II

Decoder output	Sign of global peak coefficient (level-1)	Sign of global peak coefficient (level-2)
01	-	+
10	+	-

Table II: Decoder output determined by wavelet analysis.

Alternatively, the discontinuity can be detected by estimating a first order derivative $\mathbf{D}[k]$ of $\mathbf{U}_2[k]$ with respect to time, which can be approximated as the difference between two subsequent samples of $\mathbf{U}_2[k]$ (current sample minus the previous one). A scalar variable $d[k]$ is assigned with the derivative that has the maximum absolute value, from which we derive two received bits are generated as follows:

$$d[k] > \Gamma \rightarrow (0,1) \text{ as this indicates a rising edge in } \mathbf{U}_2[k];$$

$$d[k] < -\Gamma \rightarrow (1,0) \text{ as this indicates a falling edge in } \mathbf{U}_2[k]$$

where Γ is an appropriately chosen value defining a band gap $[-\Gamma, \Gamma]$.

In the case where no discontinuity is detected at step S2, for example if decoder 22R determines that there are no Daubechies peaks or that $\Gamma > d[k] > -\Gamma$, decoding for the current OFF cycle of $m_2(t)$ is performed based on a voltage threshold V_θ (S6):

If $\sum \mathbf{U}[k] < V_\theta$, decoder 22R outputs 00;

Otherwise, decoder 22R outputs 11.

Returning to Figure 3B, recall that, at the transmitter 2T, a pair of redundant marker bits is added to $\mathbf{w}_1[k]$ to mark every transition of $p_1(t)$. The reason for this is so that the simple decoding scheme described above can still be applied in the case that $p_1(t)$ is not fixed at zero. Without the redundancy bits, a more complex analysis of $\mathbf{U}_2[k]$ would be needed around transitions of $p_1(t)$, as the decoding could not be performed based on its gradient alone or wavelet coefficients alone – for example, without the redundancy bits, a (0,1) bit pair could occur either side of a transition of $p_1(t)$ from p to 0, i.e. a 0,1 bit pair could coincide with a falling edge in $\mathbf{U}_2[k]$, leading to an error in the decoder output at step S4 if not corrected.

The threshold $V_\theta = \gamma(t)$ is time varying, and is derived in a calibration phase as follows. The calibration phase may, for example, be a manual or partly-manual process, that need only be performed once, for example as part of a commissioning process.

During the calibration phase, a frame of data is communicated to the receiver 2R from a known distance d from the transmitter 2T. Two voltage levels y_{HI}, y_{LO} are determined at the transmitter side as follows:

$$y_{HI} = \frac{1}{QT_p} \int_0^{QT_p} y_1(t) dt$$

$$y_{LO} = \frac{1}{(1-Q)T_p} \int_{QT_p}^{T_p} y_1(t) dt$$

where $y_1(t)$ is known at the transmitter 2T.

Two threshold values γ_{HI}, γ_{LO} are then calculated as follows:

$$\gamma_{HI} = \theta(y_{HI}, d) \times R_\lambda \times R_s,$$

$$\gamma_{LO} = \theta(y_{LO}, d) \times R_\lambda \times R_s$$

where $\theta(y, d)$ relates the forward voltage y applied to light source 4T to the intensity of light observed from it distance d away; R_λ is the responsivity of light source 4R when operating as a sensor, and R_s is the resistance a feedback resistor within the sensing circuit 16R of the receiver 2R (see Figure 5, and accompanying description below). Once calculated, these threshold values can be stored in memory at the receiver 2R for use by the decoder 22R.

The threshold voltage signal $\gamma(t)$ applied by decoder 22R in the decoding process described above is:

$$\gamma(t) = \begin{cases} \gamma_{HI}, & 0 < t < QT_p \\ \gamma_{LO}, & QT_p \leq t < T_p \end{cases}$$

That is, γ_{HI} is used as the threshold during ON cycles of $p_1(t)$ and γ_{LO} is used as the threshold during OFF cycles of $p_1(t)$.

To implement this scheme, decoder 22R identifies $p_1(t)$ signal edges, i.e. its OFF-to-ON and ON-to-OFF transitions, so that it knows which threshold to apply. To this end, decoder 22R may implement edge detection as follows:

Rising edge detection: decoder 22R detects a rising edge of $p_1(t)$ if

$d[k] > \gamma_{HI}$ or if and when an element in $U_2[k]$ exceeds γ_{HI} ;

Falling edge detection: decoder 22R detects a falling edge if $d[k] < -\gamma_{HI}$ or if and when an element an element in $U_2[k]$ drops close to zero.

This simple edge detection scheme also makes use of the redundancy bits added by transmitter 2T, as can be readily verified from Figure 3B.

5 Knowing where the edges lie also allows decoder 22R to remove the redundant marker bits from the decoded signal.

The above described coding and decoding schemes can be used to provide peer-to-peer asynchronous communication between a single transmitter and receiver.

10 It can also be used to provide communication within a network having a broadcast topology that includes one transmitter and multiple receivers. The transmitter in a broadcast mode can transmit a signal to other receivers in a same way as the peer-to-peer topology. The transmitter and multiple receivers are asynchronous. The receivers can stay asynchronous or synchronized, depending on their relative location and field-of-view (FoV) of their receiving LEDs.

15 Figure 8A, illustrates a scenario wherein a transmitter 1T broadcast frames to three receivers 2R1, 2R2 and 2R3. The relative positions and FoVs (highlighted in dashed lines) of receivers 2R1, 2R2, 2R3 are such that there is no cross-talk between any of them. With this setup, receivers 2R1, 2R2, 2R3 can stay asynchronous and decode the broadcast frames in a same manner as the peer-to-peer topology.

20 By contrast Figure 8B, shows a setup wherein cross-talk does occur among receivers 2R1, 2R2, 2R3. Correct decoding requires symbol-level synchronization between receivers. Since receivers are transmitting a predetermined sensing sequence ‘...0101...’, a symbol-level synchronization scheme can be implemented by the receivers to align their matching, predetermined sensing sequences, which can be mutually sensed in the same
25 manner as light received from transmitter 2T.

It can also be used to provide communication within a network having a star topology and which includes multiple transmitters and a single receiver.

For correct decoding, a transmitter implements a carrier sensing mechanism and applies clear channel assessment (CCA) during OFF interval of the PWM signal $p_1(t)$ with $m_1(t) = 0$, i.e. such that $y_1(y) = p_1(t)$. The channel is determined to be idle (i.e. clear) if the transmitter measures no discontinuity during the OFF cycle. Transmission is then
30 executed at the next PWM cycle in that event. With $m_1(t) = 0$, a resulting drop in dimming level can be preventing by tuning the pulse width of $p_1(t)$.

Figure. 4 shows an exemplary star network comprising a first and a second transmitter 2T1 and 2T1, each configured as in Figure 1A. Each transmits a respective data sequences $s_{11}[k]$, $s_{12}[k]$ to receiver 2R.

Two OFF cycles of second transmitter 2T2's PWM signal $p_{12}(t)$ are shown by way of example. During the first of these, first transmitter 2T is shown transmitting data, leading to non-zero bits in $m_{11}[k]$ and hence changes in $y_{11}(t)$. During this OFF cycle of $p_{12}(t)$, the scheduler of the second transmitter 2T1 measures at least one discontinuity in its sensed voltage $U_{12}(t)$ and thereby determines that the channel is occupied and causes transmission of $s_{12}[k]$ to be postponed as a result. During the next OFF cycle in $p_{12}(t)$, first transmitter 2T1 is not transmitting. Therefore the scheduler of the second transmitter 2T2 detects an idle channel and transmits $s_{12}[k]$ at the beginning of the next PWM cycle (not shown).

Although only two transmitters are shown in Figure 4, the scheduling technique can be applied with a greater number of transmitters. As the transmitters are asynchronous, the free channel is occupied following a first-come-first-service manner, i.e. the first transmitter that claims a free channel will transmit a frame. The other transmitters will detect a busy channel as a result and back off.

A constraint may be placed on the duration of the off cycle, i.e. $(1-Q)T_b$, to capture the maximum run length of RLL code:

$$(1 - Q)T_b > Rn \times T_b$$

where Rn is the maximum run number as defined above, and equals 4 for 4B6B coding.

Figure 5 shows an example circuit architecture for the transmitter 2T and receiver 2R of Figures 1A and 1B. The circuit architecture may, for example, be embodied in an implication specific integrated circuit, or using programmable hardware such as an FPGA, or any suitable combination of application-specific and programmable hardware.

A summing amplifier circuit 14 (14T/14R) comprises a first op-amp A1, having a differential input pair and an output. Resistors R1 and R2 are connected to a ground terminal and to a first of the differential inputs of A1 (+), in parallel to one another, wherein PWM voltage $p(t)$ is applied across R1 and output voltage $m(t)$ is applied across R2 to as to gate a total voltage $y(t)$ at between the output of A1 and the ground terminal. The second differential input of A1 is connected to the ground terminal via resistor R4, and to the output of A1 via resistor R3. Multiplexor 32 is controlled by $y(t)$ so as to connect light source 4 (4T/4R) across the output of A1 and the ground terminal at times when $y(t) \neq 0$. At the

remaining times, when $y(t)=0$, multiplexor 32 instead connects light source 4 to sensing circuit 16, which operates as described above. The sensing circuit 16 comprises an op-amp A2, that is selectively connected to light source 4, via multiplexor 32, during OFF cycles of $y(t)$ via input (-), and a feedback resistor R5 connecting its output to that input (-). A noise reducing capacitor C1 is connected across the feedback resistor R5 to provide improved stability.

As indicated above:

$$y(t) = A * m(t) + B * y(t)$$

The constants A and B relate to the architecture of summing amplifier 12 as follows:

$$y(t) = \frac{R3 + R4}{R4} \cdot \frac{\frac{m(t)}{R1} + \frac{p(t)}{R2}}{\frac{1}{R1} + \frac{1}{R2}} =: G_{A1} \cdot \left(\frac{1}{1 + \alpha} m(t) + \frac{\alpha}{1 + \alpha} p(t) \right)$$

where G_{A1} denotes the gain of op-amp A1, and

$$\alpha = \frac{B}{A} = \frac{R1}{R2}$$

constitutes a modulation depth of the modulation.

PWM and output voltage signals $p(t)$ and $m(t)$ are generated by general input/output pins with equal peak-to-peak amplitude V_{pp} . They have different frequencies f_p and f_m respectively ($f_p < f_m$ and both are above the main frequency for flicker-free illumination, as indicated above).

There are two constraints that are beneficial to place on $y(t)$. First, the maximum amplitude of $y(t)$ (occurring when both $m(t)$ and $p(t)$ are simultaneously ON) should not exceed a maximum rated forward voltage $V_{f,max}$ of LED light source 4. Secondly, the amplitude of $y(t)$ in the OFF cycle of $p(t)$ and ON cycle of $m(t)$ should at least approximately match a nominal forward voltage $V_{f,norm}$ of the LED light source 4. To meet these two constraints, it can be shown that the modulation depth should be constrained as follows:

$$\alpha = \frac{B}{A} \leq \frac{V_{f,max}}{V_{f,norm}} - 1$$

For most LEDs, $V_{f,max}$ is about 10% above $V_{f,norm}$, giving $R2 > 10 * R1$.

In practice, we set α as large as possible, i.e. such that it substantially matches and does not exceed the right-hand term:

$$\alpha = \frac{B}{A} = \frac{V_{f,max}}{V_{f,norm}} - 1$$

such that $\max \{y(t)\} = V_{f,max}$, in order to achieve the longest possible communication distance range: since the light emitted from a point source obeys the inverse square law, a large α allows reliable decoding of $m(t)$ carried in ON cycles of $p(t)$ at the greatest distances.

Figure 5A shows an alternative architecture for a drive system 6 (e.g. 6T/6R), for large-scale LED luminaires, based instead on current regulation. The drive system 6 of Figure 5A comprises an LED controller 40, which is a microcontroller, and a power converter 42. Under the control of the microcontroller 40, the power converter generates output current $y(t) = i_y(t)$, which is selectively provided to drive LED light source 4 via switch S2. The power converter 42 is a current-mode regulator, such as a dimmable buck converter. A sensing path SP and a control path CP are shown. Sensing path SP selectively connects light source 4 to microcontroller 40 via switch S1 for sensing. Switch S3 is controlled via control path CP, to selectively short-circuit light source 4 for sensing.

The microcontroller 40 comprises peripheral components, which include a PWM wave generator, amplifiers and analog-to-digital converter etc. (not shown), which may for example be integrated in a single chip. A combination of these peripherals can be used to directly control the power converter 42. Microcontroller 40 is shown receiving data and dimming signals $m(t)$, $p(t)$, which are current signals and may be received in analogue or digital form. Alternatively, these signals may be generated on the microcontroller 40, i.e. the OOK modulator and dimming signal generator may be implemented as part of the microcontroller 40.

Output current $i_y(t)$ is regulated using a feedback control algorithm implemented by microcontroller 40, which calculates a difference between a desired LED current $C * m(t) + D * p(t)$ (with C and D two weighting factors) and an LED current $\frac{u_f(t)}{R_{sense}}$ measured using a sensing resistor R_{sense} (e.g. $R_{sense} = 1 \Omega$), and minimizes an absolute value of this difference by tuning a dimming control signal $i_d(t)$ outputted to power converter 42 for controlling $i_y(t)$.

The control path CP is added to improve the power efficiency of the driver. When $m[k]=p[k]=0$ (with k the bit duration index) the microcontroller 40 closes the switch S3, which bypasses light source 4 without shutting down the power converter 42. Meanwhile, the LED(s) of light source 4 are switched OFF for sensing. The microcontroller 40 activates the sensing path SP by closing switches S1, S3 and opening S2. Photocurrent $i_{ph}(t)$ is

converted by TIA 12 into a photovoltage signal $U_{ph}(t)$ and is measured by microcontroller 40.

For a data signal $m(t)$ and a dimming signal $p(t)$ that are with equal amplitude, the modulation depth has an upper bound

$$\alpha = \frac{D}{C} \leq \frac{I_{f,max}}{I_{f,norm}} - 1$$

, which is determined by the maximum rated forward current $I_{f,max}$ and the nominal forward current $I_{f,norm}$ of the LED light source 4.

Figure 6 shows an alternative sensing architecture that can be applied to the transmitter 2T, the receiver 2R or both. Rather than using the LED light source 4 (4T/4R) as a sensor for data reception or clear channel assessments, a dedicated radiation sensor 5 collocated with the LED light source is used instead. The radiation sensor 5 may for example be a photo sensor or photo transistor.

The advantage of using the LEDs light source 4 for sensing is that there is no need for a separate radiation sensor. The advantage of using a separate radiation sensor is that there is no need to add a switching mechanism for switching the (illumination) LEDs from an illumination mode to a sensing mode. The latter not only is beneficial when the LEDs in question are high power LEDs, but also facilitates retrofits in modular LED illumination systems. E.g. by providing a new LED driver, comprising the claimed drive system and a radiation sensor in the form of a photodiode or a phototransistor, a modular LED illumination system may be upgraded with visible light communication functionality.

Figure 7A illustrates an exemplary lighting system incorporating the techniques of the present invention. The lighting system comprises a plurality of luminaires 16 installed in an environment 15, arranged to emit illumination in order to illuminate that environment 15. In the illustrated example, the environment 15 is an indoor space within a building, such as one or more rooms and/or corridors (or part thereof). The luminaires 16 are ceiling-mounted, so as to be able to illuminate a surface below them (e.g. the ground or floor, or a work surface). However, in other arrangements one or more of the luminaires 16 could be mounted on the wall, or embedded in the floor or items of furniture; and/or the luminaires 16 need not be arranged in a regular grid; and/or the environment 15 may comprise an outdoor space such as a garden or park, or a partially-covered space such as a stadium or gazebo (or part thereof), or a combination of such spaces. At least two of the luminaires 16 in the lighting system are configured respectively as a coded light transmitter 2T and receiver 2R in accordance with the above described techniques, such that one is able to modulate data

into its illumination output that is received at the other. As shown, in Figures 5B-5E, each of these luminaires 16 supports an LED lamp 18 in which the one or more LEDs 4 are integrated. The luminaire 16 comprises any associated socket, housing or support for the lamp 18. Usually, the lamp 18 is a replicable component, though modern LED lamps may have working lifetimes of several years and thus require only occasional replacement.

A drive system 6 (e.g. 6T/6R) may be integrated in the lamp 18 itself (Figure 7B), which means that the present techniques can be incorporated into existing, non-specialized luminaires. Alternatively, drive system 6 may be supported by the luminaire 16 itself (Figure 7C), for example it may be integrated in the luminaire or it may be, say, a detachable module that can be incorporated in the luminaire 16 if the luminaire 16 has the necessary infrastructure. Alternatively, at least part of the drive 6 may be external to the luminaire, and connect to it via a suitable external interface. For example, a coder 8 and modulator 12 of the drive system 6 may be external to the luminaire 16, with the summing amplifier 14 integrated in or otherwise supported by the luminaire 16 (Figure 7D) or lamp 18 (Figure 7E).

Figure 7A also shows a system controller 21, for controlling the transceiver systems 2(1), 2(2). The system controller 21 may, for example, set the dimming level Q i.e. the duty cycle of the pulse width modulation signal $p_1(t)$ at the transmitter 2T, and allow Q to be varied to change the dimming level. The system controller 21 may communicate with the transmitter 2 in any suitable manner, e.g. using wireless technology, wired technology or a combination of both. The system controller 21 may for example comprise a user interface mechanism, such as a switch or wall panel, by which a user can set the dimming level Q . Alternatively, the system controller may comprise an interface by which it can communicate with a separate user device (based on wired and/or wireless technology), such as a smartphone, tablet or other computer device, with which the user can set the dimming level Q . The system controller 21 may be a single device, or it may be formed of multiple devices. The dimming signal generator 19T may, for example, be incorporated in the system controller, which communicates $p_1(t)$ to the relevant luminaire(s) 16. Alternatively, system controller 21 may communicate the duty cycle Q to a luminaire 16 incorporating the dimming signal generator 19T, i.e. the dimming signal $p_1(t)$ may be generated locally at the luminaire based on a received indication of the duty cycle Q .

It will be appreciated that the processing steps in embodiments as performed by the various components of the transmitter 2T and receiver 2R respectively could be implemented partially or in full on a general purpose computer and/or using dedicated

hardware or a mix thereof. In fact part of the functional behavior e.g. the data coding at the transmitter 2T and conversely the decoding at the receiver 2R may be implemented as computer software running on one or more data processors and/or digital signal processors.

Notably the same functionality could also be realized using a dedicated hardware in the form of an application specific integrated circuit or using programmable hardware such as a FPGA. Notably other tasks such as the control and coordination of various operations by the ADCs may also be partially implemented using software, hardware or a mix thereof.

Moreover, whilst a circuitry architecture of the modulator 10 is described, above, some or all of the functionality of the modulator 10 may instead be implemented in software executed on one or more processors. In this case, the OOK modulator 12 and/or the signal combiner 14T may instead be code modules that are executed on the processing modules. In addition it is noted that the elements and components used in the transmitter or receiver may all be incorporated in a singular device such as a luminaire, but within the luminaire may still be distributed over a plurality of units or as part of other functional units. For example, in case of an LED luminaire having a LED driver with an on-board microcontroller, it may be advantageous to integrate the functionality in the LED driver so as to reduce the number of components. Alternatively if the luminaire comprises a luminaire controller that e.g. also provides a Power over Ethernet or Radio Frequency communication unit, then it may be beneficial to include the visible light modulator/decoder functionality therein.

It will be appreciated that the above embodiments have been described by way of example only. Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims. In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single processor or other unit may fulfil the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measures cannot be used to advantage. A computer program may be stored/distributed on a suitable medium, such as an optical storage medium or a solid-state medium supplied together with or as part of other hardware, but may also be distributed in other forms, such as via the Internet or other wired or wireless telecommunication systems. Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. A drive system (6T) for a light source (4T) for use in a visible light communication system, the drive system comprising:
 - a data input configured to receive a data sequence to be transmitted;
 - a modulator (12T) configured to apply on-off key modulation to the data
 - 5 sequence to embed it in a data signal as on-off keyed amplitude modulations of the data signal;
 - a dimming signal generator (19T) configured to generate a pulse width modulation dimming signal;
 - a signal combiner (12T) having a data signal input connected to receive the
 - 10 data signal and a dimming input connected to receive the dimming signal;
 - wherein the data signal and the pulse width modulation dimming signal are synchronized with each other;
 - wherein the signal combiner (12T) is configured to generate a drive signal by summing the data signal with the pulse width modulation dimming signal; and
 - 15 wherein the signal combiner (12T) has a drive output configured to supply the drive signal to the light source to vary an intensity of light emitted by the light source according to the drive signal, thereby transmitting the embedded data sequence whilst simultaneously providing dimmable illumination.
- 20 2. A drive system according to claim 1, further comprising:
 - a coder (8T) configured to code the data sequence and output the coded data sequence to the modulator (12T), said modulation being applied to the coded data sequence.
3. A drive system according to claim 2, wherein the coder (8T) is configured to
- 25 generate a plurality of redundant marker bits in the coded data sequence so as to mark a plurality of successive transitions in the pulse width modulation dimming signal.

4. A drive system according to claim 3, wherein the coder (8T) is configured to generate a DC-balanced pair of redundant marker bits in the coded data sequence to mark each of the transitions.

5. A drive system according to claim 3 or 4, wherein the marker bits are inserted so as to cause, for each of the plurality of successive transitions in the pulse width modulation dimming signal, a matching transition in the data signal independently of the data sequence, thereby marking that transition.

6. A drive system according to any of claims 2 to 5, wherein said coding is a DC-balanced, run-length limited coding.

7. A drive system according to any preceding claim, further comprising:
a scheduler (20T) configured to detect a clear channel condition during an off cycle of the pulse width modulation dimming signal occurring prior to said transmission, and to instigate said transmission in response to the detection of the clear channel condition.

8. A drive system according to claim 7, wherein the scheduler (20T) is configured to use at least one LED of the light source as a sensor to detect the clear channel condition.

9. A transmitter (2T) comprising a drive system (6T) according to any preceding claim, and a light source (4T) connected to the drive output of the drive system.

10. A transmitter according to claim 9, wherein in the drive signal is a weighted sum of the data and dimming signals, in which a first weighting factor is applied to the data signal and a second weighting factor is applied to the pulse width modulation signal, and:

wherein the drive signal is a drive voltage, the light source has a maximum rated voltage $V_{f,max}$ and a nominal voltage $V_{f,norm}$, and the second weight factor divided by the first weight factor is no more than $\frac{V_{f,max}}{V_{f,norm}} - 1$, or

wherein the drive signal is a drive current, the light source has a maximum rated current $I_{f,max}$ and a nominal current $I_{f,norm}$, and the second weight factor divided by the first weight factor is no more than $\frac{I_{f,max}}{I_{f,norm}} - 1$.

11. A visible light communication system comprising a transmitter (2T) according to claims 9 or 10 and a receiver (2R), wherein the receiver comprises:

a light source (4R) configured to emit light exhibiting periodic intensity

5 variations thereby providing illumination; and

a decoder (22R) configured to determine the transmitted data sequence from light emitted by the transmitter and sensed at the receiver during off cycles of the period intensity variations.

10 12. A visible light communication system according to claim 11, wherein the decoder (22R) is configured to use the light source (4R) of the receiver (2R) as a sensor to sense the light during the off cycles of periodic intensity variations.

13. A visible light communication system according to claim 11 or 12, wherein
15 the drive system (6T) of the transmitter (2T) is configured according to claim 5 or any claim dependent thereon, and wherein the decoder (22R) of the receiver (2R) is configured to decode the sensed light applying the following decoding operations for each off cycle of the periodic intensity variations:

if a high-to-low intensity transition is detected in the sensed light in that off
20 cycle, generating a pair of non-matching bits;

if a low-to-high intensity transition is detected in the sensed light in that off cycle, generating a different pair of non-matching bits;

if no intensity transition is detected in the sensed light in that off cycle:
generating a pair of matching bits if the intensity is below a threshold, and
25 generating a different pair of matching bits if the intensity is above a threshold.

14. A method of driving a light source (4T) for use in a visible light communications system, the method comprising:

30 receiving a data sequence to be transmitted;

applying on-off key modulation to the data sequence to embed it in a data signal as on-off keyed amplitude modulations of the data signal;

receiving a pulse width modulation dimming signal, wherein the data signal and the pulse width modulation dimming signal are synchronized with each other;

generating a drive signal by summing the data signal with the pulse width modulation dimming signal; and

supplying the drive signal to the light source to vary an intensity of light emitted by the light source according to the drive signal, thereby transmitting the embedded data sequence whilst simultaneously providing dimmable illumination.

5

15. A computer program product comprising code stored on a computer readable storage medium and configured when executed to implement the method of claim 14.

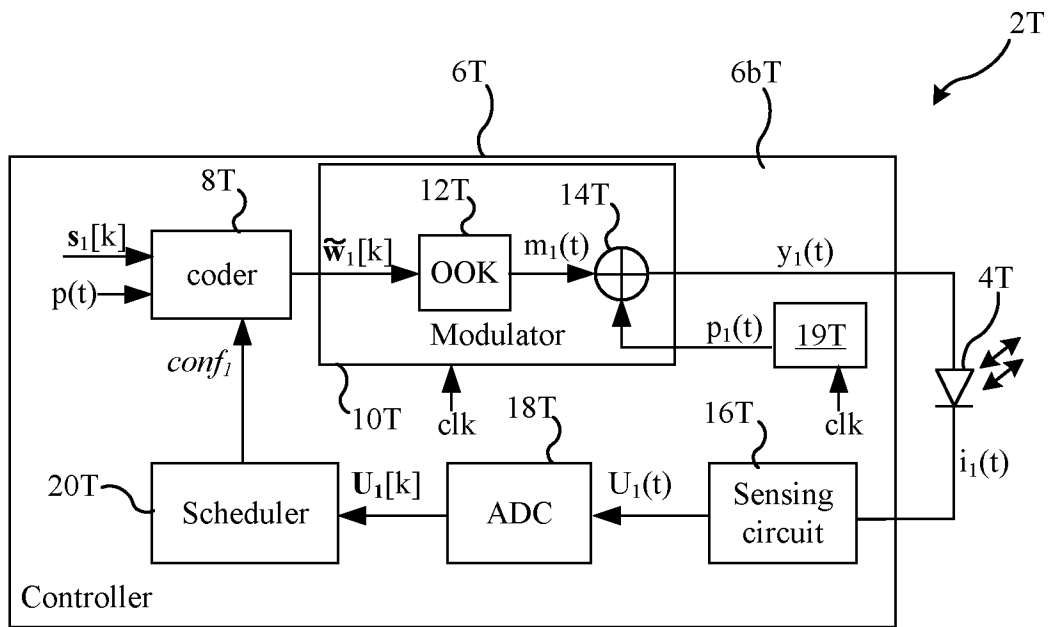


FIG. 1A

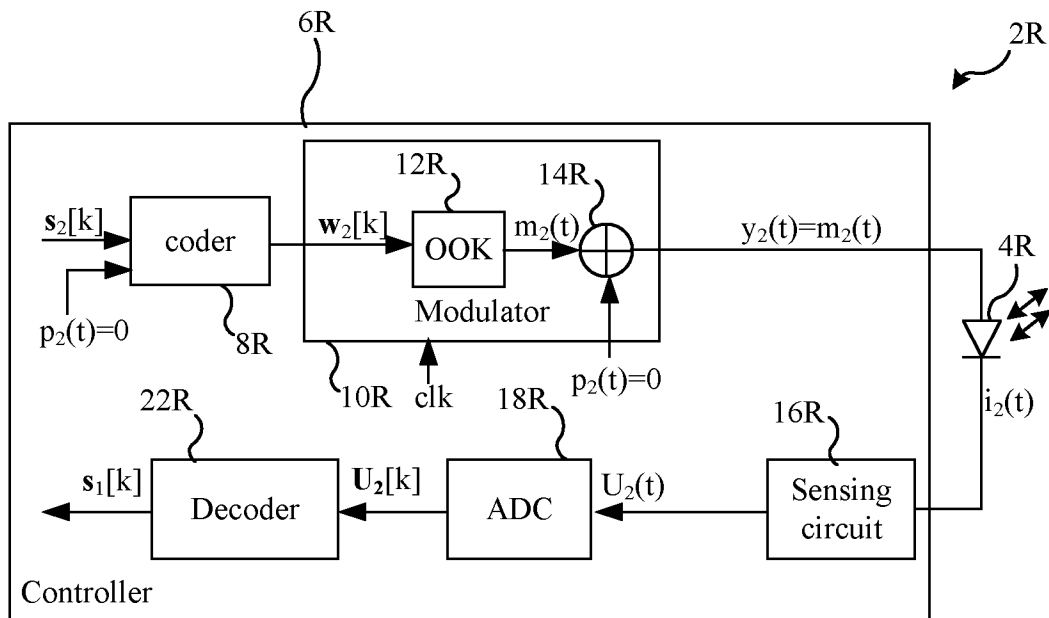


FIG. 1B

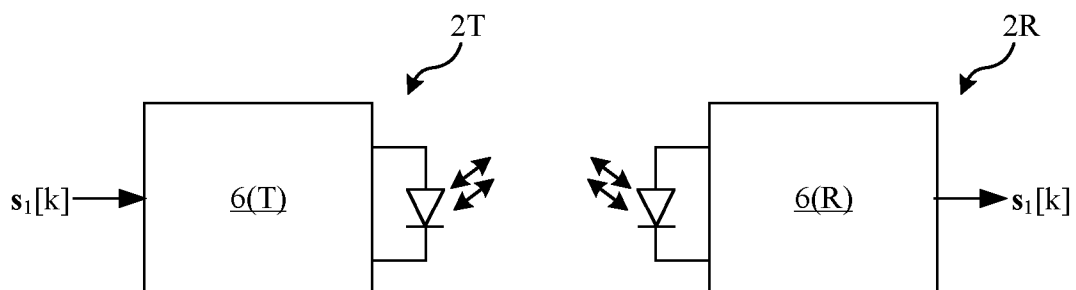


FIG. 1C

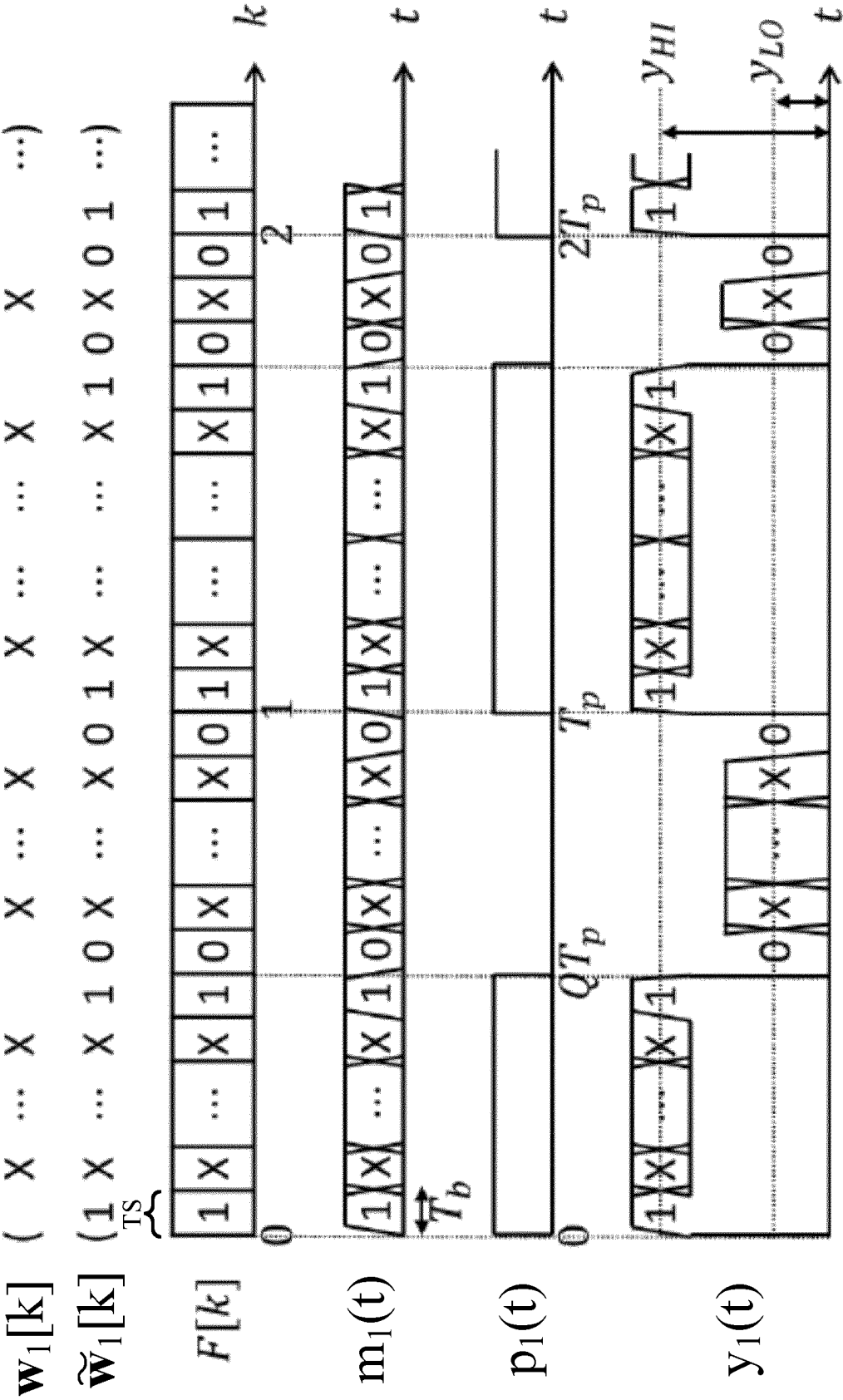


FIG. 2A

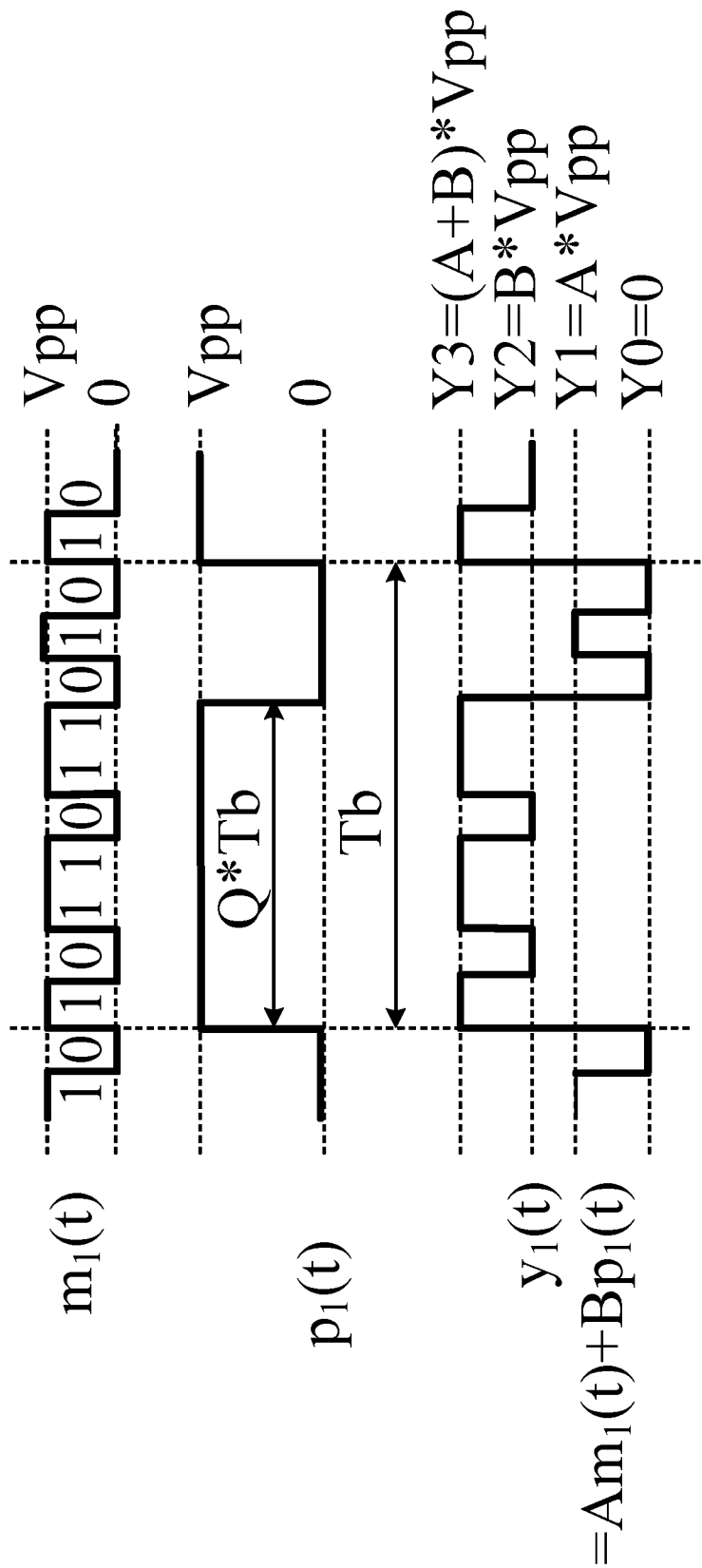


FIG. 2B

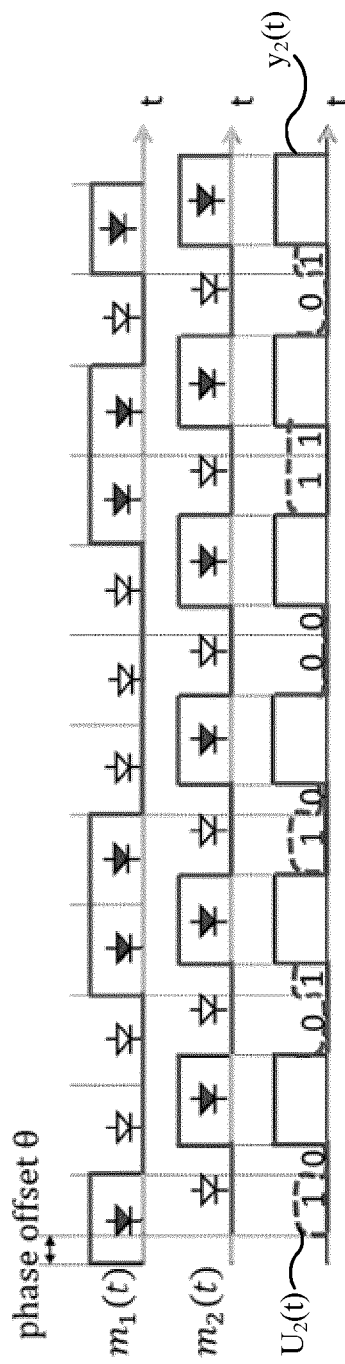


FIG. 3A

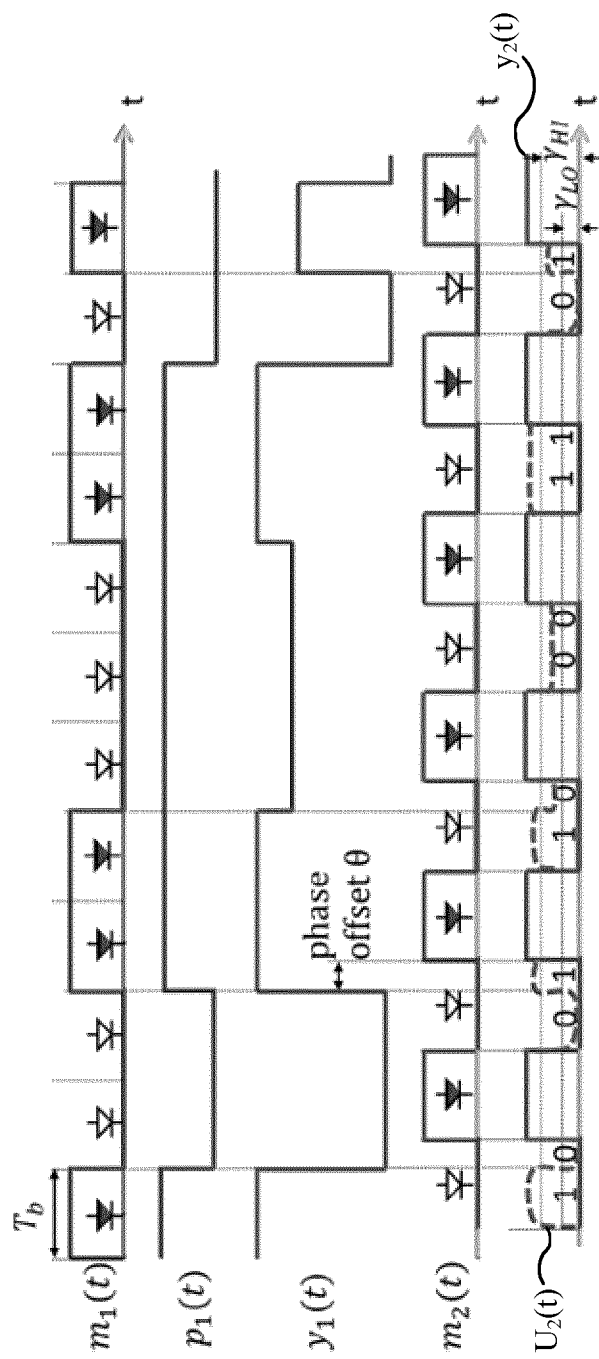


FIG. 3B

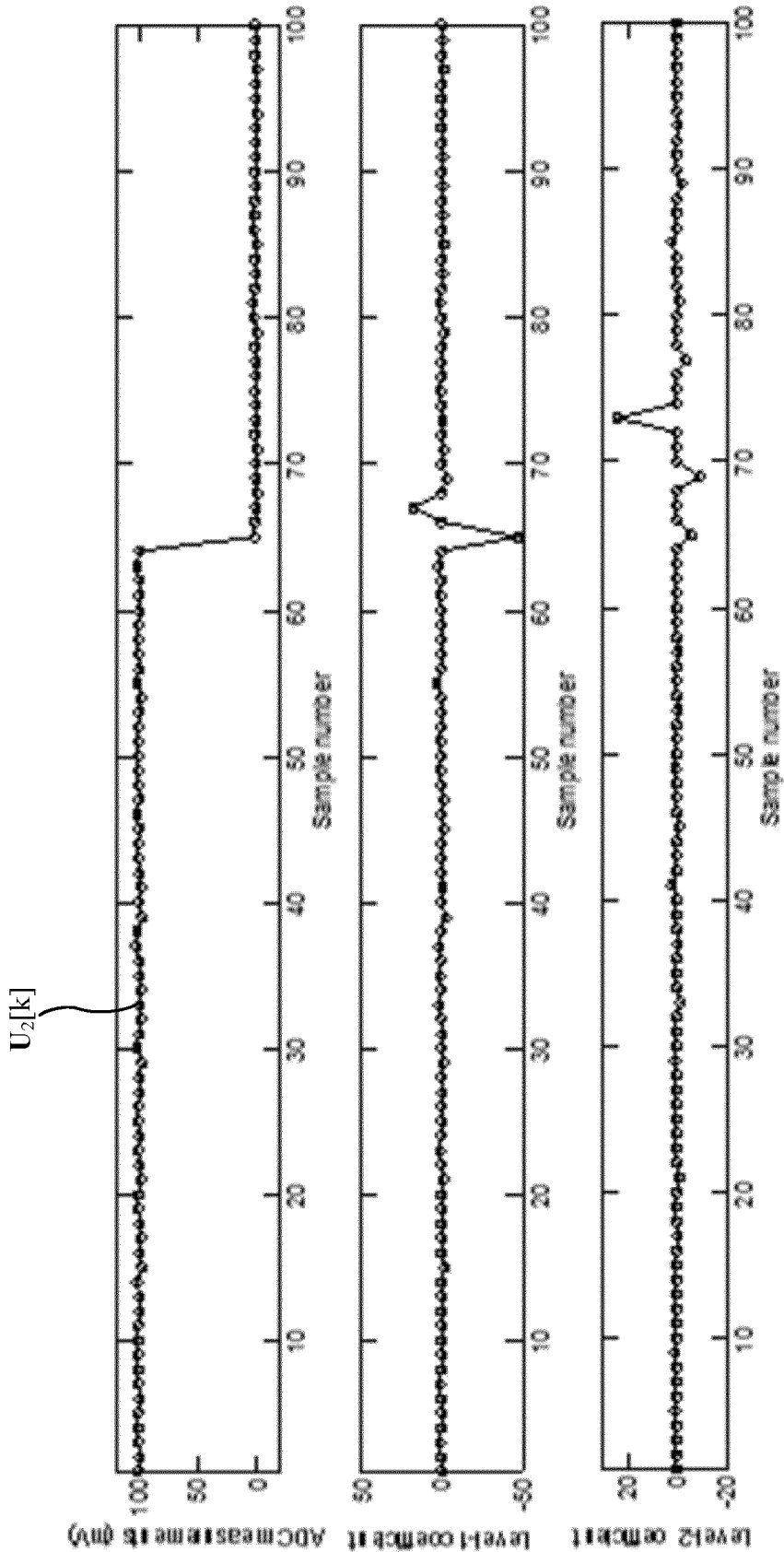


FIG. 3C

6/11

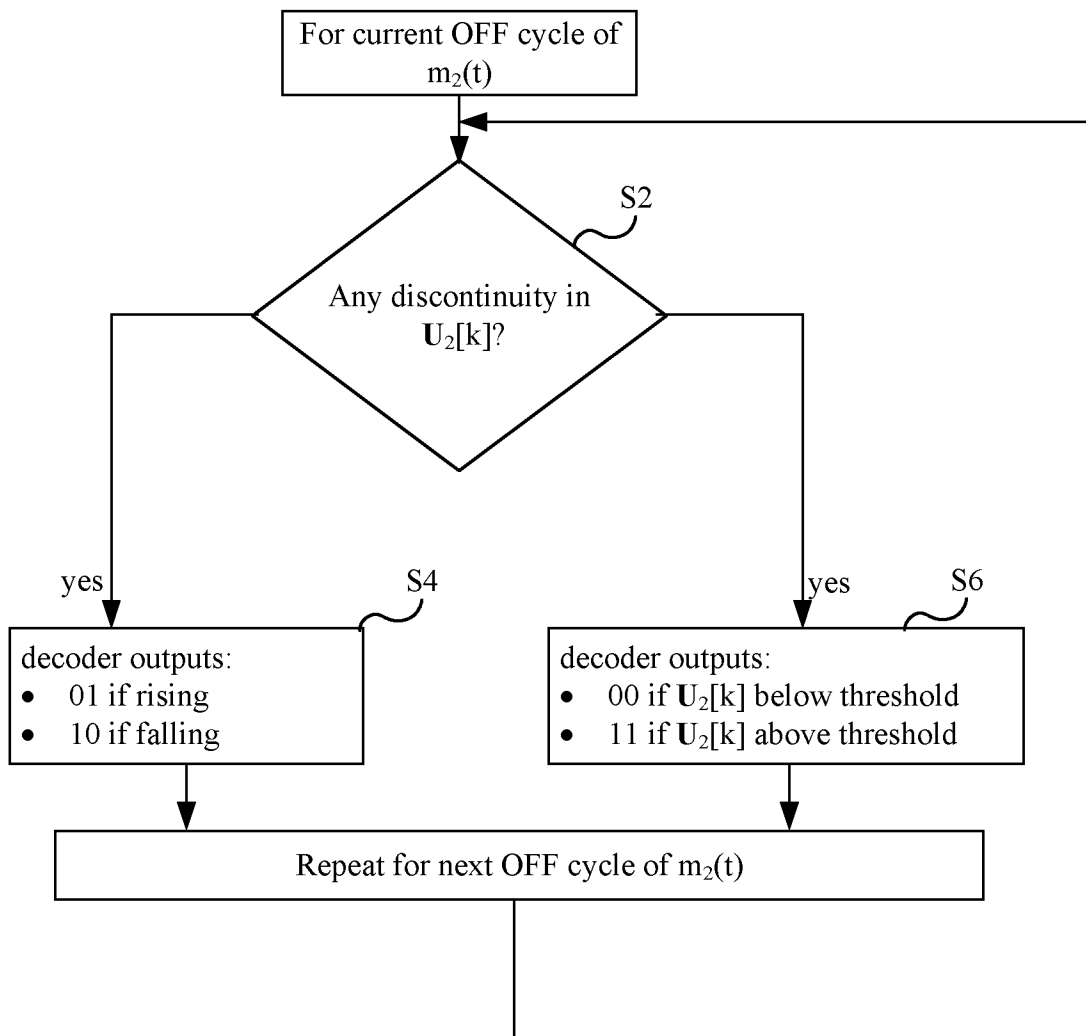
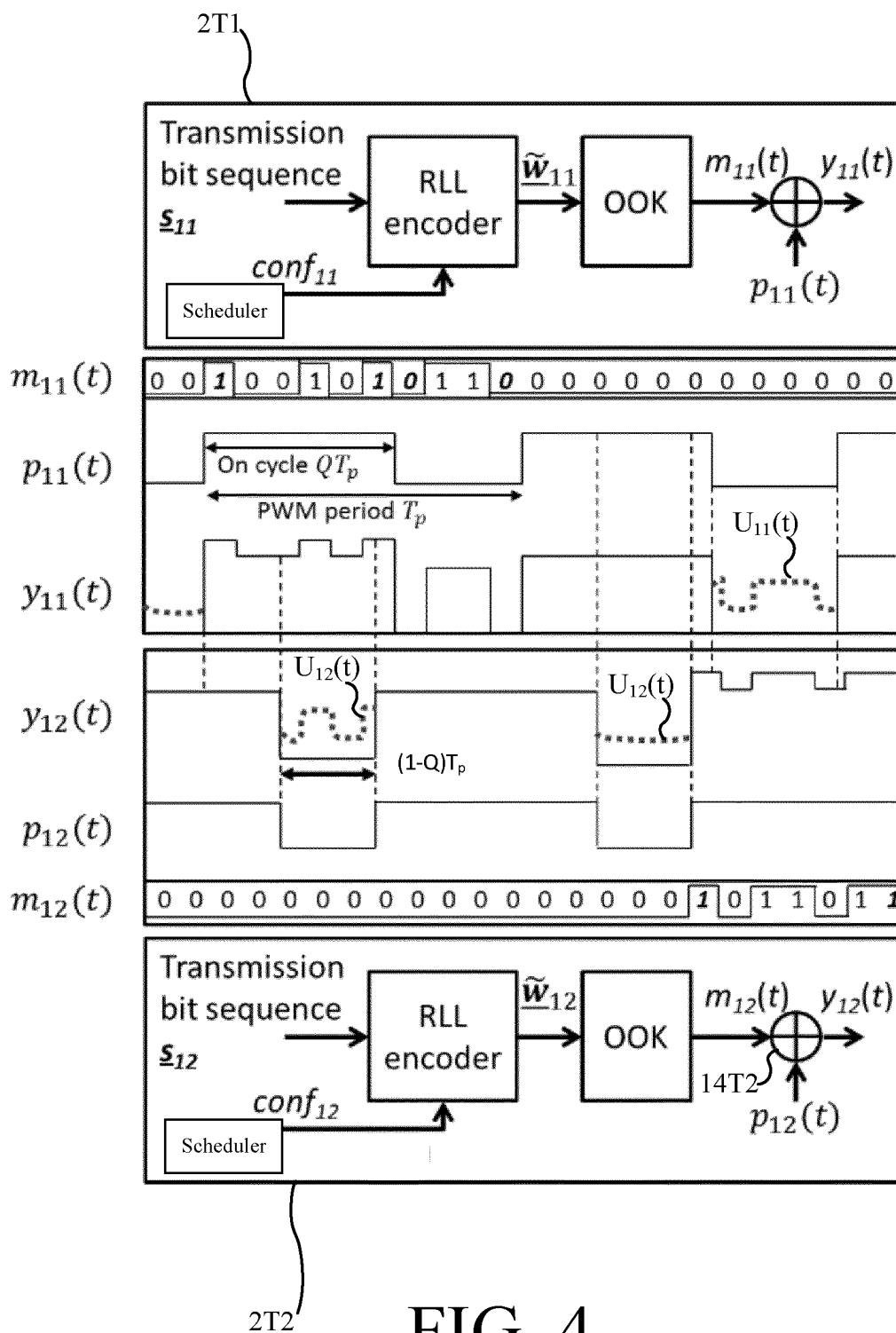


FIG. 3D



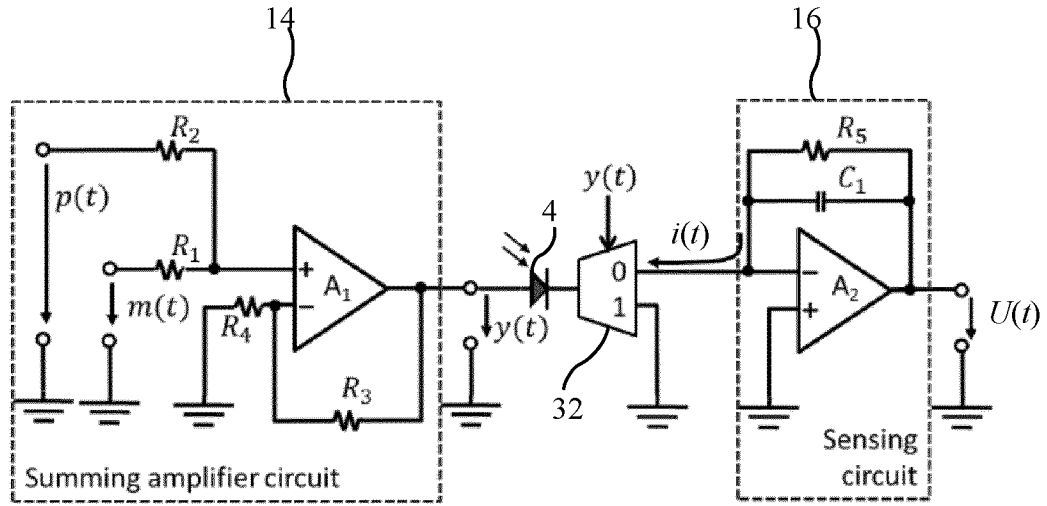


FIG. 5

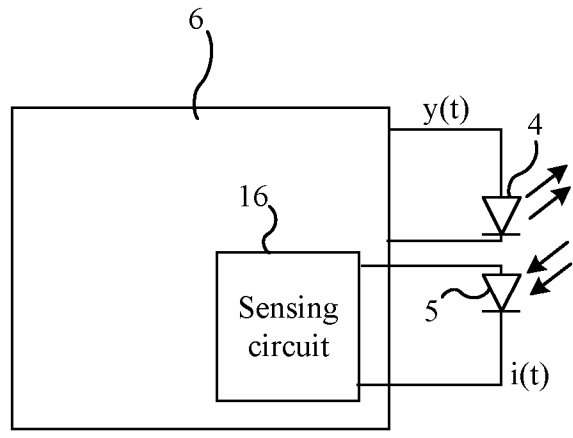


FIG. 6

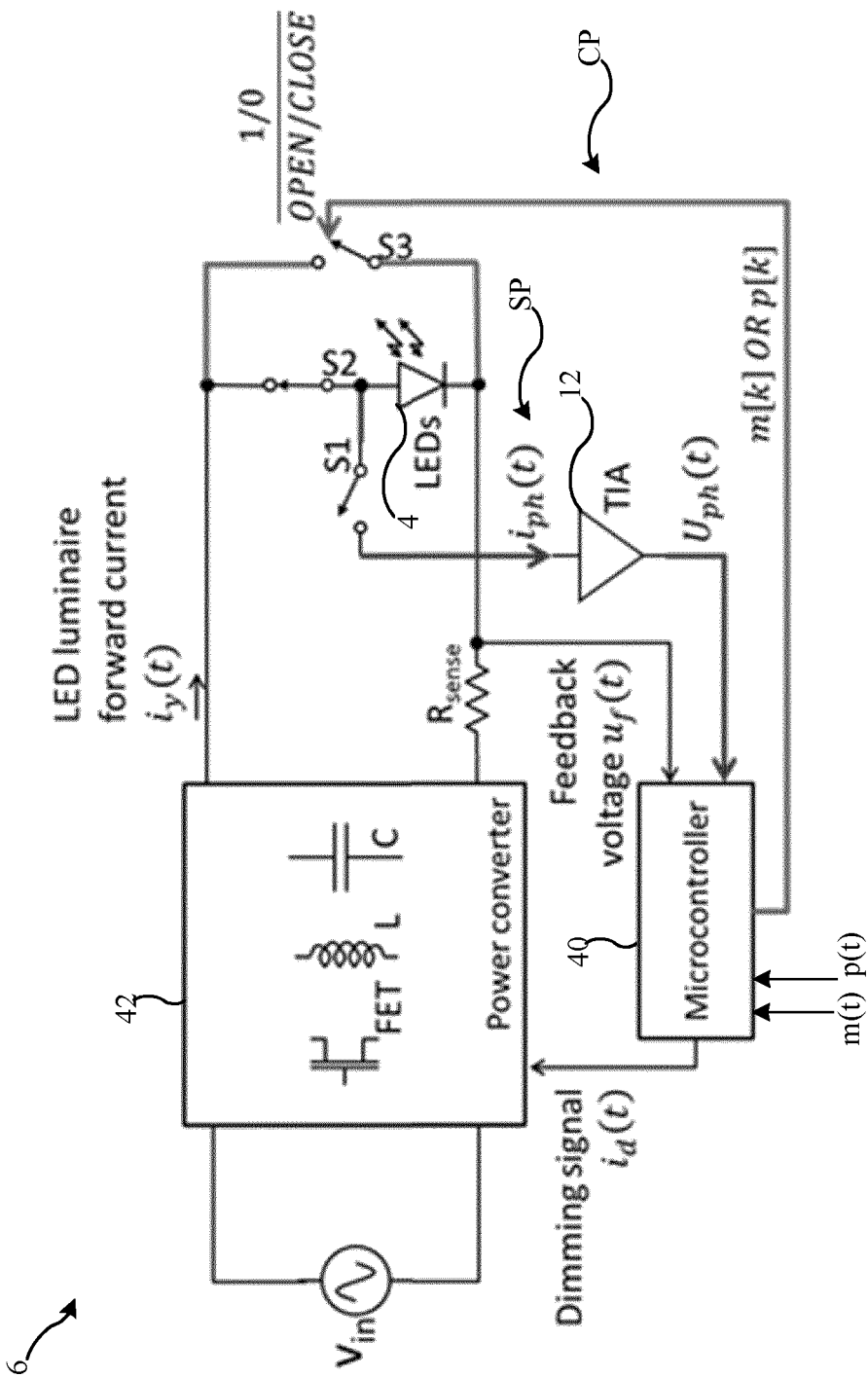


FIG. 5A

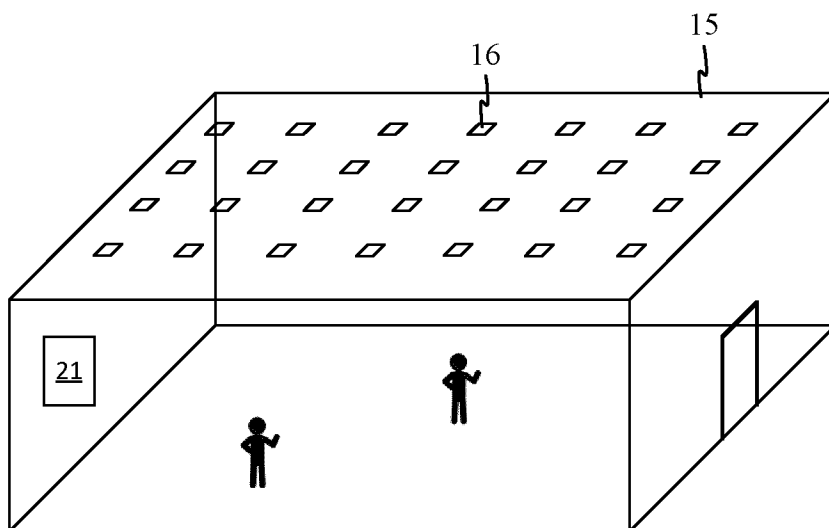


FIG. 7A

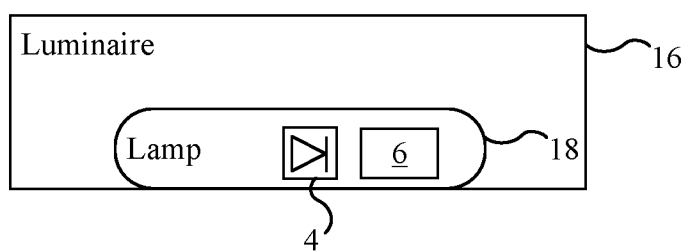


FIG. 7B

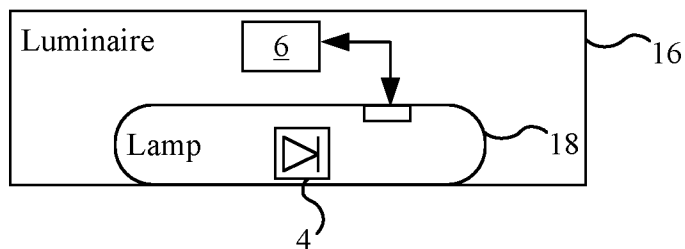


FIG. 7C

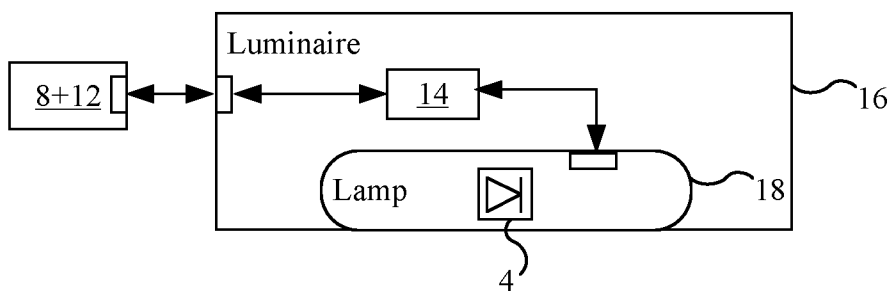


FIG. 7D

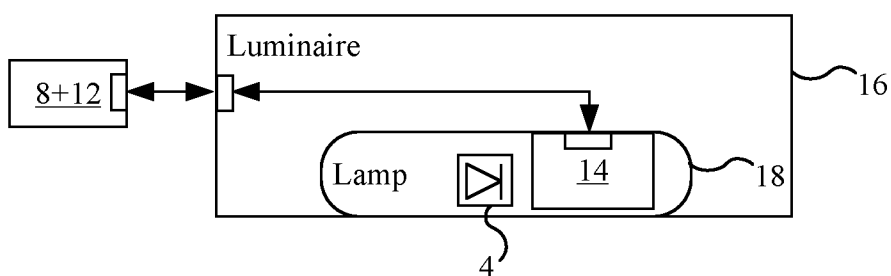


FIG. 7E

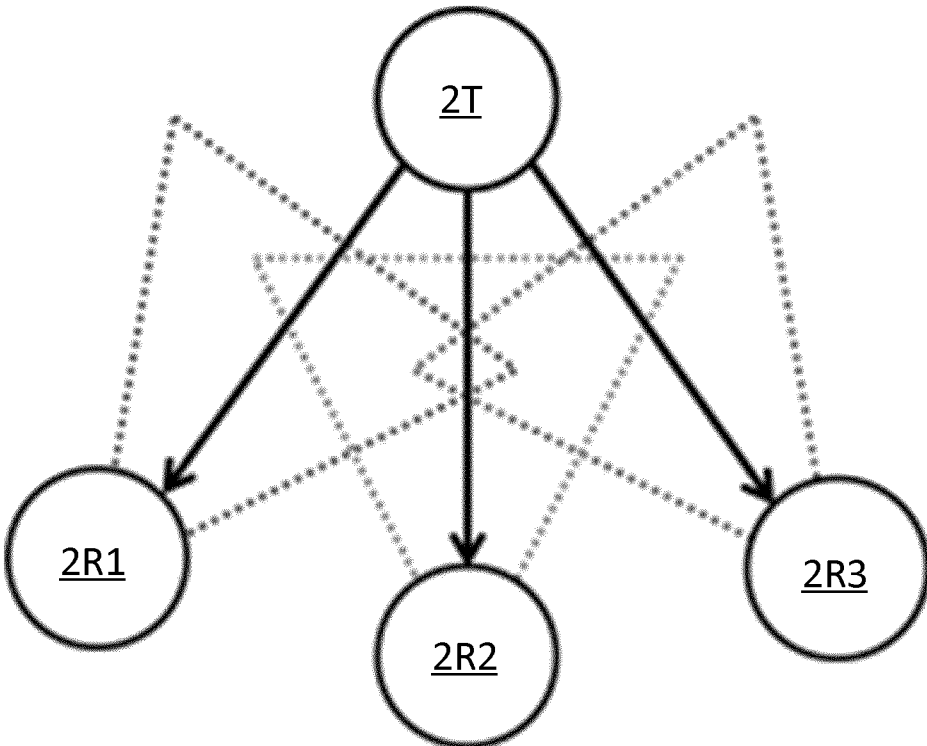


FIG. 8A

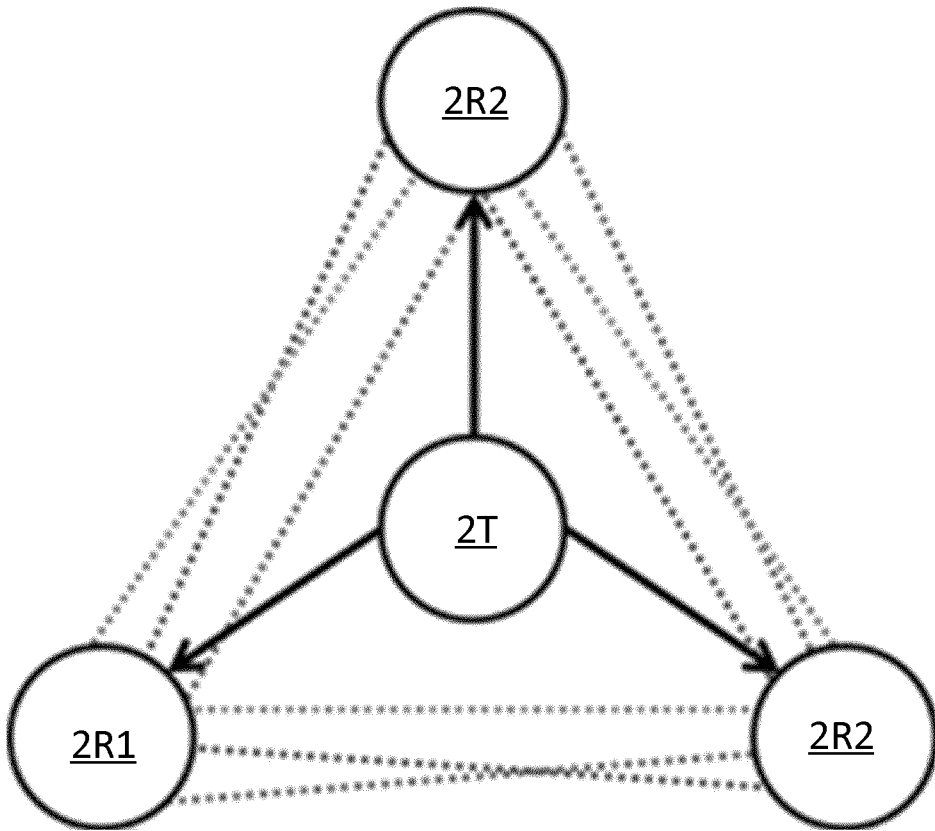


FIG. 8B

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2017/059874

A. CLASSIFICATION OF SUBJECT MATTER

INV. H04B10/116 H05B33/08
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H04B H05B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2007/092264 A1 (SUZUKI SHUUJI [JP] ET AL) 26 April 2007 (2007-04-26) paragraph [0052] - paragraph [0059]; claim 1; figure 2 -----	1-15
A	WO 2015/047497 A2 (UNIV BOSTON [US]) 2 April 2015 (2015-04-02) page 8, line 5 - page 11, line 2; figure 3 -----	1-15
Y	WO 2012/153220 A1 (KONINKL PHILIPS ELECTRONICS NV [NL]; YANG HONGMING [NL]; SCHENK TIM CO) 15 November 2012 (2012-11-15) page 6, line 7 - page 9; figures 1, 3 ----- -/--	1,2, 6-12,14, 15



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents :

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

21 July 2017

Date of mailing of the international search report

31/07/2017

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Authorized officer

Plamann, Tobias

INTERNATIONAL SEARCH REPORT

International application No

PCT/EP2017/059874

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Information on patent family members

International application No

PCT/EP2017/059874

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		EP 2547173 A2	16-01-2013
		JP 5891393 B2	23-03-2016
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		US 2013015784 A1	17-01-2013
