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(54) **Title**: INTEGRATED NITRIDE AND SILICON CARBIDE-BASED DEVICES AND METHODS OF FABRICATING INTEGRATED NITRIDE-BASED DEVICES

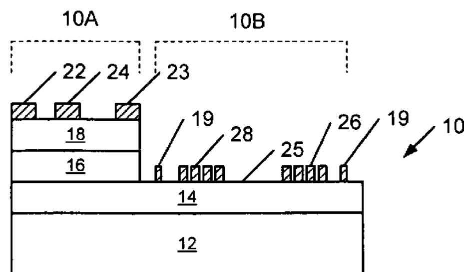

FIG. 1A

(57) **Abstract**: Monolithic electronic devices including a common nitride epitaxial layer are provided. A first type of nitride device is provided on the common nitride epitaxial layer including a first at least one implanted n-type region on the common nitride epitaxial layer. The first at least one implanted n-type region has a first doping concentration greater than a doping concentration of the common nitride epitaxial layer. A second type of nitride device, different from the first type of nitride device, including a second at least one implanted n-type region is provided on the common nitride epitaxial layer. The second at least one implanted n-type region is different from the first at least one implanted n-type region and has a second doping concentration that is greater than the doping concentration of the common nitride epitaxial layer. A first plurality of electrical contacts are provided on the first at least one implanted n-type region. The first plurality of contacts define a first electronic device of the first type of nitride device. A second plurality of electrical contacts are provided on the second at least one n-type implanted region. The second plurality of contacts define a second electronic device of the second type of electronic device. Corresponding methods are also disclosed.

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INTEGRATED NITRIDE AND SILICON CARBIDE-BASED DEVICES AND METHODS OF FABRICATING INTEGRATED NITRIDE-BASED DEVICES

CLAIM OF PRIORITY

[001] This application claims priority under 35 U.S.C. § 120 as a continuation-in-part application of United States Patent Application No. 10/378,331, filed on March 3, 2003 and United States Patent Application No. 11/410,768, filed April 25, 2006, the disclosures of which are hereby incorporated by reference herein as if set forth in its entirety.

FIELD OF THE INVENTION

[002] The present invention relates to nitride-based devices. In particular, the present invention relates to the monolithic integration of different types of nitride-based devices on a common substrate, and resulting devices.

BACKGROUND

[003] Wide bandgap semiconductor materials, including Group III-nitrides, such as gallium nitride, aluminum gallium nitride, indium nitride and alloys thereof, and silicon carbide, are desirable materials for the fabrication of high power, high temperature and/or high frequency devices. These wide bandgap materials have high electric field breakdown strengths and high electron saturation velocities as compared to other semiconductor materials such as gallium arsenide and silicon.

[004] Electrical circuits requiring high power handling capability (>20 watts) while operating at high frequencies such as radio frequencies, including for example, S-band (2-4 GHz) and X-band (8-12 GHz), have in recent years become more prevalent. Because of the increase in high power, high frequency circuits there has been a corresponding increase in demand for transistors that are capable of reliably operating at radio frequencies and above while still being capable of handling higher power loads. Previously, bipolar transistors and power metal-oxide semiconductor field effect transistors (MOSFETs) have been used for high power applications but the power handling capability of such devices may be limited at higher operating frequencies. Junction field-effect transistors (JFETs) were commonly used

for high frequency applications but the power handling capability of previously known JFETs may also be limited.

[005] Recently, metal-semiconductor field effect transistors (MESFETs) have been developed for high frequency applications. The MESFET construction may be preferable for high frequency applications because only majority carriers carry current. The MESFET design may be preferred over current MOSFET designs because the reduced gate capacitance permits faster switching times of the gate input. Therefore, although all field-effect transistors utilize only majority carriers to carry current, the Schottky gate structure of the MESFET may make the MESFET more desirable for high frequency applications.

[006] In addition to the type of structure, and perhaps more fundamentally, the characteristics of the semiconductor material from which a transistor is formed also affects the operating parameters. Of the characteristics that affect a transistor's operating parameters, the electron mobility, saturated electron drift velocity, electric breakdown field and thermal conductivity may have the greatest effect on a transistor's high frequency and high power characteristics.

[007] Electron mobility is the measure of the ease of electron motion within a semiconductor media and is defined as the rate of change of electron drift velocity with respect to electric field at a given electric field. In the past, semiconductor materials which have a high electron mobility were preferred because more current could be developed with a lesser field, resulting in faster response times when a field is applied. Saturated electron drift velocity is the maximum velocity that an electron can obtain in the semiconductor material. Materials with higher saturated electron drift velocities are preferred for high frequency applications because the higher velocity may translate to shorter transition times from source to drain.

[008] Electric breakdown field is the field strength at which breakdown of the Schottky junction and the current through the gate of the device suddenly increases. A high electric breakdown field material may be preferred for high power, high frequency transistors because larger electric fields generally can be supported by a given dimension of material. Larger electric fields may allow for faster transients as the electrons can be accelerated more quickly by larger electric fields than by smaller.

[009] Thermal conductivity is the ability of the semiconductor material to dissipate heat. In typical operations, all transistors generate heat. In turn, high power and high frequency transistors usually generate larger amounts of heat than low power transistors. As the temperature of the semiconductor material increases, the junction leakage currents

generally increase and the current through the field effect transistor generally decreases due to a decrease in carrier mobility with an increase in temperature. Therefore, if the heat is dissipated from the semiconductor, the material may remain at a lower temperature and may be capable of carrying larger currents with lower leakage currents. Reliability physics also predicts a longer lifetime for a device that operates at lower operating temperature.

[010] In the past, high frequency MESFETs have been manufactured of n-type III-V compounds, such as gallium arsenide (GaAs) because of their high electron mobilities. Although these devices provided increased operating frequencies and moderately increased power handling capability, the relatively low breakdown voltage and the lower thermal conductivity of these materials have limited their usefulness in high power applications.

[011] Silicon carbide (SiC) has been known for many years to have excellent physical and electronic properties which should theoretically allow production of electronic devices that can operate at higher temperatures, higher power and higher frequency than devices produced from silicon (Si) or GaAs. The high electric breakdown field of about 4×10^6 V/cm, high saturated electron drift velocity of about 2.0×10^7 cm/sec and high thermal conductivity of about 4.9 W/cm-K indicate that SiC would be suitable for high frequency, high power applications.

[012] SiC-based MESFET structures and their fabrication are described in U.S. Patent No. 5,270,554 to Palmour et al. and U.S. Patent No. 5,925,895 to Sriram et al., both of which are incorporated herein by reference as if fully set forth herein. SiC MESFET structures and fabrication are also described in U.S. Application Ser. No. 09/567,717 filed May 10, 2000 by Allen, et al., the disclosure of which is incorporated herein by reference as if fully set forth herein.

[013] In the III-nitride material system, a device of particular interest for high power and/or high frequency applications is the high electron mobility transistor (HEMT), which is also known as a heterostructure field effect transistor (HFET). These devices may offer operational advantages under a number of circumstances because a two-dimensional electron gas (2DEG) is formed at the heterojunction of two semiconductor materials with different bandgap energies, and where the smaller bandgap material has a higher electron affinity. The 2DEG is an accumulation layer in the undoped, smaller bandgap material and can contain a very high sheet electron concentration in excess of, for example, 10^{13} carriers/cm^2. Additionally, electrons that originate in the wider-bandgap semiconductor transfer to the 2DEG, allowing a high electron mobility due to reduced ionized impurity scattering.

[014] This combination of high carrier concentration and high carrier mobility can give the HEMT a very large transconductance and may provide a strong performance advantage over metal-semiconductor field effect transistors (MESFETs) for high-frequency applications.

[015] High electron mobility transistors fabricated in the gallium nitride/aluminum gallium nitride (GaN/AlGaN) material system have the potential to generate large amounts of RF power because of the combination of material characteristics that includes the aforementioned high breakdown fields, their wide bandgaps, large conduction band offset, and/or high saturated electron drift velocity.

[016] In electronic communication systems, it is usually desirable to amplify signals before transmission (power amplifier) or after reception (low noise amplifier). It is also often desirable to filter such signals immediately before or after amplification. Directing the RF signal to specific portions of a multifunction chip can be accomplished with a monolithic RF switch that is low-loss and can provide high isolation. Other types of non-power-amplifier circuits that would benefit from monolithic integration with the power amplifier circuits are limiter circuits and phase shifters. In high frequency communication systems, such amplification may be performed efficiently using an amplifier circuit incorporating a SiC MESFET or a Group III-nitride based transistor. Filtering may be efficiently performed using a SAW filter.

[017] In order to minimize the number of circuit elements required to implement a communication system and simplify its design, it is desirable to integrate as many components as possible on a single chip. Attempts to integrate SAW devices with other devices have been made. However, such devices have typically required that the piezoelectric crystal be bonded onto a semiconductor substrate (such as silicon) on which active electronic components are formed.

[018] Acoustic wave devices form a class of electronic devices that process signals that exist as acoustic (i.e. sound or compression) waves traveling in piezoelectric crystals. Piezoelectric crystals are characterized by the fact that when the material is mechanically stressed (i.e. compressed or placed under tension), an associated electric field is induced. Likewise, when an electric field is applied to a piezoelectric crystal, the material becomes mechanically stressed in a predetermined manner. It is possible to exploit these characteristics to perform many different functions with a piezoelectric crystal.

[019] For example, piezoelectric microphones convert acoustic waves traveling though air into electronic signals. Piezoelectric speakers and buzzers perform the opposite

function. Piezoelectric sensors detect changes in pressure, temperature, torque, humidity and/or a wide range of other phenomena.

[020] Common piezoelectric materials include quartz (SiO_2), zinc oxide (ZnO), barium titanate ($BaTiO_3$), lithium tantalate ($LiTaO_3$) and lithium niobate ($LiNbO_3$). However, other materials, most notably silicon carbide (SiC) and the Group III-nitride materials such as aluminum nitride (AlN) and Gallium Nitride (GaN) are piezoelectric and may be used to form acoustic wave devices.

[021] When a time-varying electric field is applied to a portion of a piezoelectric crystal, the applied electric field induces an acoustic wave that propagates through the crystal. Acoustic waves may travel through a piezoelectric material in a number of modes. For example, acoustic waves may travel through the body of the material - so-called "bulk" waves - or on the surface of the material. Waves that travel along the surface of the piezoelectric material are generally referred to as surface acoustic waves (or SAWs), and devices that process surface acoustic waves are referred to as surface acoustic wave devices, or SAW devices.

[022] A simple surface acoustic wave device comprises a piezoelectric crystal or a thin film of piezoelectric material on a substrate. Interdigitated metal stripes on the surface of the crystal form transmitting and receiving electrodes. The metal electrodes convert electrical energy into mechanical stress in the crystal and vice versa. Hence, the interdigital electrodes formed on a piezoelectric material are referred to as interdigital transducers, or IDTs.

[023] A simple surface acoustic wave device is illustrated in perspective in **FIG. 10**. The SAW device comprises a piezoelectric film **2** formed on a substrate **1**. A metal (usually aluminum) is deposited on the film and patterned using standard photolithographic or liftoff techniques to form the input IDT **3** and the output IDT **4**. The thickness of the piezoelectric film is generally on the order of one SAW wavelength.

[024] In operation, an electric signal may be applied to the input IDT **3**. The input signal causes a surface acoustic wave to be induced in the piezoelectric film **2** and propagate along the surface of the film **2** towards the output IDT **4**. The shape of the generated wave depends on the electric signal applied to the input IDT, the design and orientation of the IDT fingers, and the piezoelectric material used. When the wave reaches the output IDT **4**, a voltage is induced across the fingers of the IDT **4** which is then output from the device. The shape of the output wave is affected by the design of the output IDT **4**.

[025] **FIG. 11** illustrates some design parameters for IDTs. The finger period **D** determines the wavelength λ of the SAW generated by the IDT. The linewidth **L** and space **S** of the fingers are generally equal to λ/4. The number of fingers determines the coupling efficiency of the IDT, and the width W of the overlap of fingers affects the frequency response of the finger pair. By changing the overlap of finger pairs within an IDT, various filter functions can be realized.

[026] Surface acoustic wave devices have many different applications in digital and analog electronics. For example, surface acoustic wave devices may be used as bandpass or bandstop filters, duplexers, delay lines, resonators and/or impedance elements among other things. They may also be used to perform digital functions such as convolution, correlation, pulse compression and/or digital filtering (for example in spread-spectrum communication systems) depending on the design of the device, and in particular depending on the layout of the interdigital transducers. The design and fabrication of surface acoustic wave devices are described in Chapter 66 of K. Ng, Complete Guide to Semiconductor Devices, McGraw Hill (1995).

[027] The velocity of surface acoustic waves in a device depends on the material from which the device is constructed and the mode of propagation of the SAW. For example, the propagation velocity (also called the SAW velocity) of first order Rayleigh-mode acoustic waves in GaN is around 3600 m/s, while the corresponding SAW velocity in AlN is about 5800 m/s, and over 6800 m/s in SiC. For RF devices, the SAW velocity determines the bandwidth of signals that can be processed by the device. The fundamental operating frequency (f_0) of a SAW device is given by the formula:

a. $$f_0 = \frac{v}{\lambda}$$

[028] where v is the SAW velocity and λ is the wavelength. As discussed above, the wavelength of the device is determined by the finger period of the IDT. The width and spacing of IDT fingers (and thus the finger period) is limited by the resolution of photolithographic techniques. Thus, for a given finger period, increasing the SAW velocity increases the fundamental operating frequency of the device. Stated differently, having a higher SAW velocity permits a device to process higher-frequency signals for a given device geometry. Accordingly, the Group III-nitrides and SiC may be desirable piezoelectric materials for the fabrication of SAW devices.

[029] In addition to integrating SAW devices with nitride devices, it may be desirable to integrate other types of nitride devices together on a single substrate for more

efficient manufacturing and/or operation. However, in the past it has proved difficult to provide multiple device types on a common substrate due to the different epitaxial semiconductor structures required for different types of devices.

SUMMARY OF THE INVENTION

[030] Some embodiments of the invention provide a monolithic electronic device including a common nitride epitaxial layer, a first type of nitride device including a first epitaxial nitride structure on the common nitride epitaxial layer, and a second type of nitride device, different from the first type of nitride device, including a second epitaxial nitride structure on the common nitride epitaxial layer. A first plurality of electrical contacts is on the first epitaxial nitride structure and defines a first electronic device of the first type of nitride device, and a second plurality of electrical contacts is on the second epitaxial nitride structure and defines a second electronic device of the second type of electronic device.

[031] The first epitaxial nitride structure may include a nitride channel layer, a nitride barrier layer on the nitride channel layer, the nitride barrier layer having a higher bandgap than the nitride channel layer. The nitride barrier layer and the nitride channel layer are configured to cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer.

[032] The monolithic electronic device may further include a high bandgap layer on the barrier layer and a silicon nitride layer on the high bandgap layer.

[033] The second nitride epitaxial structure may include a layer of $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) having a thickness of about 300 Å to about 1000 Å.

[034] The first electronic device may include a high electron mobility transistor. The second electronic device may include a surface acoustic wave device, a diode, and/or a field effect transistor. In particular, the second electronic device may include source, drain and gate contacts, and the gate and drain contacts of the second electronic device may be electrically coupled to form an anode.

[035] The second epitaxial nitride structure may include a first layer of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) on the first epitaxial nitride structure and a second layer of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) on the first layer of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$). The first layer of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) may have a surface charge density of about 1×10^{14} cm^{-2}, and the

second layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$) may have a doping concentration of less than about $1x10^{16}$ cm^{-3}.

[036] The common epitaxial layer may include a layer of semi-insulating $Al_xGa_{1-x}N$ ($0 \le x \le 1$).

[037] A monolithic electronic device according to further embodiments of the invention includes a nitride epitaxial structure including a nitride channel layer, and a nitride barrier layer on the nitride channel layer. The nitride barrier layer has a higher bandgap than the nitride channel layer, and the nitride barrier layer and the nitride channel are configured to cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer. An $Al_xGa_{1-x}N$ ($0 \le x \le 1$) layer is on the barrier layer, and a first gate electrode is recessed through the $Al_xGa_{1-x}N$ ($0 \le x \le 1$) layer, the first gate electrode defining a first transistor device. A second gate electrode, defining a second transistor device, is on the $Al_xGa_{1-x}N$ ($0 \le x \le 1$) layer.

[038] The monolithic electronic device may further include a silicon nitride layer on the $Al_xGa_{1-x}N$ ($0 \le x \le 1$) layer. The first gate electrode and the second gate electrode may both be recessed through the silicon nitride layer. The silicon nitride layer may include a high purity silicon nitride layer.

[039] The monolithic electronic device may further include a source/drain electrode between the first gate electrode and the second gate electrode. The source/drain electrode is recessed through the $Al_xGa_{1-x}N$ ($0 \le x \le 1$) layer and provides a source/drain contact for both the first electronic device and the second electronic device.

[040] A monolithic electronic device according to still further embodiments of the invention includes a bulk semi-insulating silicon carbide substrate, source and drain regions in a surface of the silicon carbide substrate, a channel region in the silicon carbide substrate between the source and drain regions, and a nitride epitaxial structure on the surface of the silicon carbide substrate. The source and drain regions and the channel regions may include implanted regions.

[041] The monolithic electronic device may further include a first passivation layer on the implanted channel region and the implanted source and drain regions of the silicon carbide substrate, and a first gate contact on the silicon carbide substrate between the implanted source and drain regions, and a second gate contact on the nitride epitaxial layer. The first gate contact extends through the passivation layer.

[042] The first passivation layer may extend onto the nitride epitaxial layer, and the second gate contact may extend through the first passivation layer.

[043] The monolithic electronic device may further include a second passivation layer on the nitride epitaxial structure, the second passivation layer including a material different from the first passivation layer. The second gate contact may extend through the second passivation layer.

[044] The first gate contact may be a control contact for a silicon carbide-based transistor device and the second gate contact may be a control contact for a nitride-based transistor device, and the electronic device may further include an interconnect metallization connecting the silicon carbide-based transistor device and the nitride-based transistor device.

[045] Methods of forming a monolithic electronic device according to some embodiments of the invention include forming a first nitride epitaxial structure including a plurality of nitride epitaxial layers including at least one common nitride epitaxial layer, forming a second nitride epitaxial structure on the common nitride epitaxial layer of the first nitride epitaxial structure, forming a first plurality of electrical contacts on the first epitaxial nitride structure, the first plurality of contacts defining a first electronic device in the first nitride epitaxial structure, and forming a second plurality of electrical contacts on the first epitaxial nitride structure, the second plurality of contacts defining a second electronic device in the second nitride epitaxial structure.

[046] Forming the first nitride epitaxial structure may include forming a nitride channel layer, forming a nitride barrier layer on the nitride channel layer, the nitride barrier layer having a higher bandgap than the nitride channel layer. The nitride barrier layer and the nitride channel are configured to cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer.

[047] The methods may further include forming a high bandgap layer on the barrier layer, and forming a nitride layer, such as silicon nitride and/or gallium nitride, on the high bandgap layer.

[048] Forming the second epitaxial structure may include forming a first layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$) on the first epitaxial structure, and forming a second layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$) on the first layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$). The first layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$) may have a surface charge density of about 1×10^{14} cm^{-2}, and the second layer of n-type $Al_xGa_{1-x}N$ ($0 \le x \le 1$) may have a doping concentration of less than about 1×10^{16} cm^{-3}.

[049] Methods of fabricating a monolithic electronic device according to further embodiments of the invention include implanting source and drain regions in a surface of a bulk semi-insulating silicon carbide substrate, implanting a channel region in the silicon carbide substrate between the implanted source and drain regions, and forming a nitride epitaxial structure on the surface of the silicon carbide substrate.

[050] The methods may further include forming a first passivation layer on the implanted channel region and the implanted source and drain regions of the silicon carbide substrate, and forming a first gate contact on the silicon carbide substrate between the implanted source and drain regions, and forming a second gate contact on the nitride epitaxial layer. The first gate contact extends through the passivation layer.

[051] The first passivation layer may extend onto the nitride epitaxial layer, and the second gate contact may extend through the first passivation layer.

[052] The methods may further include forming a second passivation layer on the nitride epitaxial structure, the second passivation layer including a material different from the first passivation layer. The second gate contact may extend through the second passivation layer.

[053] The first gate contact may be a control contact for a silicon carbide-based transistor device and the second gate contact may be a control contact for a nitride-based transistor device, and the methods may further include forming an interconnect metallization to connect the silicon carbide-based transistor device and the nitride-based transistor device.

[054] Some embodiments of the present invention provide monolithic electronic devices including a common nitride epitaxial layer. A first type of nitride device is provided on the common nitride epitaxial layer including a first at least one implanted n-type region on the common nitride epitaxial layer. The first at least one implanted n-type region has a first doping concentration greater than a doping concentration of the common nitride epitaxial layer. A second type of nitride device, different from the first type of nitride device, including a second at least one implanted n-type region is provided on the common nitride epitaxial layer. The second at least one implanted n-type region is different from the first at least one implanted n-type region and has a second doping concentration that is greater than the doping concentration of the common nitride epitaxial layer. A first plurality of electrical contacts are provided on the first at least one implanted n-type region. The first plurality of contacts define a first electronic device of the first type of nitride device. A second plurality of electrical contacts are provided on the second at least one n-type implanted region. The

second plurality of contacts define a second electronic device of the second type of electronic device.

[055] In further embodiments of the present invention, the first at least one implanted n-type region may include source and drain regions for the first electronic device. The first plurality of electrical contacts may include a source contact on the source region, a drain contact on the drain region and a gate contact between the source and the drain contacts.

[056] In still further embodiments of the present invention, the second at least one implanted n-type region may include a highly conductive n-type region. The second plurality of electrical contact may include source and drain contacts and gate contact between the source and drain contacts on the highly conductive n-type region.

[057] In some embodiments of the present invention, the highly conductive n-type region may have a doping concentration of from about 5.0×10^{18} to about 6.0×10^{18} cm^{-3} and a depth of from about 0.1 to about 1.0μm.

[058] In further embodiments of the present invention, the gate and drain contacts of the second electronic device may be electrically coupled to form an anode.

[059] In still further embodiments of the present invention, the common nitride epitaxial structure may include a nitride channel layer. A nitride barrier layer may be provided on the nitride channel layer. The nitride barrier layer may have a higher bandgap than the nitride channel layer, wherein the nitride barrier layer and the nitride channel cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer.

[060] In some embodiments of the present invention, a high bandgap layer may be provided on the barrier layer and a silicon nitride layer on the high bandgap layer.

[061] In further embodiments of the present invention, the highly conductive n-type region may be an implanted region of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) in the high bandgap layer. The second electronic device may include a layer of n-type $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) on the highly conductive n-type region having a doping concentration of less than about 1×10^{16} cm^{-3}.

[062] In still further embodiments of the present invention, the first electronic device may be a high electron mobility transistor. The second electronic device a surface acoustic wave device, a diode, a field effect transistor or a MISHFET.

[063] Some embodiments of the present invention provide monolithic electronic devices including a nitride epitaxial structure comprising a nitride channel layer and a nitride barrier layer on the nitride channel layer. The nitride barrier layer has a higher bandgap than the nitride channel layer. The nitride barrier layer and the nitride channel cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer. First and second n-type implanted regions are provided on the barrier layer defining source and drain regions, respectively. A first gate electrode is provided between the source and drain regions, the first gate electrode defining a first transistor device. A third n-type implanted region is provided on the barrier layer defining an implanted highly conductive n-type region. A second gate electrode is provided on the implanted highly conductive n-type region, the second gate electrode defining a second transistor device.

DESCRIPTION OF THE DRAWINGS

[064] **FIGs. 1A-1C** are schematic drawings illustrating embodiments of the present invention along with device precursors that may be an intermediate step in the fabrication of a device as illustrated.

[065] **FIGs. 2A-2B** are schematic drawings illustrating embodiments of the present invention along with a device precursor that may be an intermediate step in the fabrication of a device as illustrated.

[066] **FIGs. 3A-3B** are schematic drawings illustrating embodiments of the present invention along with a device precursor that may be an intermediate step in the fabrication of a device as illustrated.

[067] **FIG. 4** is a schematic drawing illustrating embodiments of the present invention.

[068] **FIG. 5** is a schematic drawing illustrating embodiments of the present invention.

[069] **FIGs. 6A-6C** are schematic drawings illustrating embodiments of the present invention along with a device precursor that may be an intermediate step in the fabrication of a device as illustrated.

[070] **FIG. 7** is a schematic drawing illustrating embodiments of the present invention.

[071] **FIG. 8** is a schematic drawing illustrating embodiments of the present invention.

[072] **FIG. 9** is a schematic drawing illustrating embodiments of the present invention.

[073] **FIG. 10** is a perspective drawing illustrating a conventional surface acoustic wave device.

[074] **FIG. 11** is a schematic drawing illustrating the layout of an interdigital transducer of a conventional surface acoustic wave device.

[075] **FIGs. 12A-12B** are schematic illustrations of two device epitaxial structures.

[076] **FIG. 13A** is a schematic drawing illustrating embodiments of the present invention.

[077] **FIG. 13B** is an equivalent circuit diagram of two devices formed on a common substrate according to some embodiments of the invention.

[078] **FIG. 14A-14B** are schematic drawings illustrating embodiments of the present invention.

[079] **FIG. 15** is a schematic drawing illustrating embodiments of the present invention.

[080] **FIG. 16** is a schematic drawing illustrating embodiments of the present invention.

[081] **FIGs. 17A-17B** are schematic drawings illustrating embodiments of the present invention.

[082] **FIG. 18** is a schematic drawing illustrating some embodiments of the present invention along with device precursors that may be an intermediate step in the fabrication of a device as illustrated.

[083] **FIG. 19** is a schematic drawing illustrating some embodiments of the present invention along with device precursors that may be an intermediate step in the fabrication of a device as illustrate

[084] **FIGs. 20A** through **20C** are schematic drawings illustrating processing steps in the fabrication of devices in accordance with some embodiments of the present invention.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[085] The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which various embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the

scope of the invention to those skilled in the art. Like numbers refer to like elements throughout. Furthermore, the various layers and regions illustrated in the figures are illustrated schematically. Accordingly, the present invention is not limited to the relative size and spacing illustrated in the accompanying figures. As will also be appreciated by those of skill in the art, references herein to a layer formed "on" a substrate or other layer may refer to the layer formed directly on the substrate or other layer or on an intervening layer or layers formed on the substrate or other layer. Moreover, it will be understood that when a first element or layer is described as "in electrical contact" with a second element or layer, the first and second elements or layers need not be in direct physical contact with one another, but may be connected by intervening conductive elements or layers which permit current flow between the first and second elements or layers.

[086] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" "comprising," "includes" and/or "including" when used herein, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[087] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms used herein should be interpreted as having a meaning that is consistent with their meaning in the context of this specification and the relevant art and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[088] Embodiments of the present invention are schematically illustrated as an integrated SAW device/transistor **10** in the cross-sectional view of **FIG. 1A**. In the embodiment illustrated in **FIG. 1A**, a transistor structure **10A** of a device **10** comprises a high electron mobility transistor (HEMT); however, it will be appreciated by those skilled in the art that the transistor structure **10A** (as well as the transistor structures illustrated in connection with other embodiments of the invention described below) may comprise one or more other types of devices instead of or in addition to a HEMT. For example, the transistor structure **10A** may comprise a MESFET, MOSFET, JFET or other device.

[089] The integrated device **10** includes a substrate **12** that may, for example, be silicon carbide (SiC), such as semi-insulating silicon carbide of the 4H polytype. Other silicon carbide candidate polytypes include the 3C, 6H, and 15R polytypes. The term "semi-insulating" is used descriptively rather than in an absolute sense. In particular embodiments of the present invention, the silicon carbide bulk crystal has a resistivity equal to or higher than about 1×10^5 Ω-cm at room temperature.

[090] An aluminum nitride buffer layer **14** on the substrate **12** provides an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the device. In the embodiments illustrated in **FIG. 1A**, the aluminum nitride buffer layer **14** also forms a piezoelectric film on which a SAW device **10B** is fabricated as described in more detail below. The buffer layer **14** and subsequent GaN-based layers may be formed by MOCVD, MBE, or any other suitable growth technique for forming high-quality epitaxial layers.

[091] Silicon carbide has a much closer crystal lattice match to Group III nitrides than does sapphire (Al_2O_3), which is a very common substrate material for Group III nitride devices. The closer lattice match may result in Group III nitride films of higher quality than those generally available on sapphire. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is, typically, not as limited by thermal dissipation of the substrate as in the case of the same devices formed on sapphire. Also, the availability of semi-insulating silicon carbide substrates may provide for device isolation and reduced parasitic capacitance.

[092] Although silicon carbide is the preferred substrate material, embodiments of the present invention may utilize any suitable substrate, such as sapphire, aluminum nitride, aluminum gallium nitride, gallium nitride, silicon, GaAs, LGO, ZnO, LAO, InP and the like. In some embodiments, an appropriate buffer layer also may be formed.

[093] As used herein, the term "Group III nitride" refers to those semiconducting compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and/or indium (In). The term also refers to ternary and quaternary compounds such as AlGaN and AlInGaN. As is well understood by those in this art, the Group III elements can combine with nitrogen to form binary (e.g., GaN), ternary (e.g., AlGaN, AlInN), and quaternary (e.g., AlInGaN) compounds. These compounds all have empirical formulas in which one mole of nitrogen is combined with a total of one mole of the

Group III elements. Accordingly, formulas such as $Al_xGa_{1-x}N$ where $0 \leq x \leq 1$ or $In_yAl_xGa_{1-x-y}N$ where $0 \leq x \leq 1$, $0 \leq y \leq 1$ and $x+y \leq 1$ are often used to describe them.

[094] Appropriate semi-insulating SiC substrates are manufactured by, for example, Cree, Inc., of Durham, N.C., the assignee of the present invention, and the methods for producing are described, for example, U. S. Patent Nos. Re. 34,861; 4,946,547; 5,200,022; 6,218,680; 6,403,982; and 6,396,080, the contents of which are incorporated herein by reference in their entirety. Similarly, techniques for epitaxial growth of Group III nitrides have been described in, for example, U. S. Patent Nos. 5,210,051; 5,393,993; 5,523,589; and 5,292,501, the contents of which are also incorporated herein by reference.

[095] Suitable structures for GaN-based HEMTs are described, for example, in commonly assigned U.S. Patent 6,316,793 and U.S. application serial no. 09/904,333 filed July 12, 2001 for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME," U.S. provisional application serial no. 60/290,195 filed May 11, 2001 for "GROUP III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" and United States Patent Application Serial No. 10/102,272, to Smorchkova et al., entitled "GROUP-III NITRIDE BASED HIGH ELECTRON MOBILITY TRANSISTOR (HEMT) WITH BARRIER/SPACER LAYER" the disclosures of which are hereby incorporated by reference.

[096] Continuing with the description of **FIG. 1A**, a channel layer **16**, which in some embodiments is GaN, is formed on the buffer layer **14**. The channel layer **16** is preferably undoped, but may be doped with various substances in order to modify the electron concentration in the sheet charge region or the behavior of the conduction band E_c and valence band E_v in the area below the sheet charge region. In some embodiments, the channel layer **16** is about 1 to 5 μm thick. In some embodiments, the channel layer **16** may comprise a thick (1 to 5 μm) GaN-based buffer layer with a thin (approximately 100 Å) high-quality channel region formed thereon.

[097] The barrier layer **18** is formed on the channel layer **16**. In some embodiments, the barrier layer **18** may comprise AlGaN, thereby forming a heterojunction between the channel layer **16** and the barrier layer **18**. The barrier layer **18** preferably has an aluminum composition of between 20% and 40% and may be doped with silicon at a doping

concentration of about $2x10^{18}$ cm^{-3}. The barrier layer **18** may be between about 15 nm and 40 nm in thickness, and is preferably about 25 nm thick.

[098] As described above, because of the AlGaN/GaN heterobarrier at the interface between the channel layer **16** and the barrier layer **18**, a two dimensional electron gas is induced at the interface. An ohmic source electrode **22** and an ohmic drain electrode **23** are formed on the surface of the barrier layer **18**. The source **22** and drain **23** ohmic electrodes may be Ti/Si/Ni, Ti/Al/Ni, Ti/Al/Ni/Au or any other suitable material that forms an ohmic contact to n-type AlGaN. Appropriate ohmic contacts for AlGaN/GaN HEMT devices are described in S. T. Sheppard, W. L. Pribble, D. T. Emerson, Z. Ring, R. P. Smith, S. T. Allen and J. W. Palmour, "High Power Demonstration at 10 GHz with GaN/AlGaN HEMT Hybrid Amplifiers," Presented at the 58th Device Research Conference, Denver, CO June 2000, and S. T. Sheppard, K. Doverspike, M. Leonard, W. L. Pribble, S. T. Allen and J. W. Palmour, "Improved 10-GHz Operation of GaN/AlGaN HEMTs on Silicon Carbide," Mat. Sci. Forum, Vols. 338-342 (2000), pp. 1643-1646.

[099] The distance between the source electrode **22** and the drain electrode **23** is typically about 2-4 μm.

[0100] In some embodiments, a thin (20-40 Å), undoped GaN cap layer (not shown) may be formed on the surface of the barrier layer **18** between the source **22** and the drain **23** ohmic electrodes. The design and effect of such cap layers is described in detail in U.S. Application Ser. No. 09/904,333 to Smith for "ALUMINUM GALLIUM NITRIDE/GALLIUM NITRIDE HIGH ELECTRON MOBILITY TRANSISTORS HAVING A GATE CONTACT ON A GALLIUM NITRIDE BASED CAP SEGMENT AND METHODS OF FABRICATING SAME" the disclosure of which is hereby incorporated by reference.

[0101] The gate electrode **24** is formed between the source **22** and the drain **23** electrodes. In certain embodiments, the gate electrode **24** is formed of platinum, nickel or any other suitable metal that forms a non-ohmic contact to n-type $Al_xGa_{1-x}N$. The gate electrode **24** may be capped with an additional metal layer in a T-gate configuration, or a T-gate may be formed in one process step. As is known in the art, T-gate configurations are particularly suitable for RF and microwave devices.

[0102] The barrier layer **18** may also be provided with multiple layers as described in the above-referenced United States Patent Application Serial No. 10/102,272, to Smorchkova et al. Thus, embodiments of the present invention should not be construed as limiting the barrier layer to a single layer but may include, for example, barrier layers having

combinations of GaN, AlGaN and/or AlN layers. For example, a GaN, AlN structure may be utilized to reduce or prevent alloy scattering.

[0103] As illustrated in **FIG 1A**, a portion of the surface **25** of the buffer layer **14**, such as an AlN buffer layer, is exposed. A first plurality of metal fingers **26** forms an input IDT on the exposed surface **25**, while a second plurality of metal fingers **28** forms an output IDT. The input IDT **26**, the output IDT **28** and the AlN buffer layer **14** form a surface acoustic wave device **10B** integrated on the same substrate as the transistor **10A**. The IDTs **26, 28** may be formed of aluminum or any other suitable metal. Since the IDTs **26, 28** do not have to form an ohmic or other electrical contact with the buffer layer **14**, many different metals may be employed (including for example the same metals used for the gate **24**, the source **22** and drain **23** ohmic contacts and/or metal interconnections to reduce the number of metallization steps required).

[0104] The thickness of the buffer layer **14** affects the SAW propagation characteristics of SAW structure **10B**. In general, a surface acoustic wave propagating in a device extends for a distance of about one wavelength into the structure. In some embodiments, the buffer layer is about 250 nm or less. In that case, the SAW velocity of the propagating wave may be dominated by the SiC substrate, which has a higher SAW velocity than AlN. Also, the orientation of the SAW IDT fingers **26, 28** may be chosen so as to optimize the performance of the device. Although it has been reported that SAW propagation is isotropic in the c-plane of AlN and SiC, it is possible to fabricate devices using off-axis cut SiC substrates, which may make the propagation of surface acoustic waves dependent on orientation. For example, SiC MESFETs are typically manufactured using 8° off-axis wafers.

[0105] The input IDT **26** or the output IDT **28** may be connected to the source **22**, the drain **23** and/or the gate **24** of transistor **10A** via an overlayer metal (not shown), or via wire bonding or any other suitable technique so that electrical signals can be communicated from transistor **10A** to SAW device **10B** and vice versa.

[0106] To reduce and/or minimize undesired reflections and interference from the transistor **10A**, the die may be cut at an angle different from the orientation of the IDT fingers **26, 28** as illustrated in **FIG. 9**. In addition, SAW reflectors and/or absorbers **19** may be formed on the device adjacent the input IDT **26** and/or the output IDT **28** to minimize undesired interference. The design of SAW reflectors and absorbers is well known to those skilled in the design of SAW devices.

[0107] Precursor structures illustrating alternative methods of fabricating the device **10** are illustrated in **FIGs 1B** and **1C**. As illustrated in **FIG. 1B**, a precursor device **11** may

be formed by depositing epitaxial layers on a substrate **12** to form the buffer layer **14**, the channel layer **16** and the barrier layer **18**. Prior to metallization, an etch mask **32** is formed on the surface of the barrier layer **18**. The etch mask **32** may comprise photoresist, silicon dioxide, silicon nitride, or any other suitable mask that permits selective etching of the underlying nitride epitaxial layers. The etch mask **32** is patterned using standard photolithography techniques and partially removed. A typical photolithography process can include the steps of adding a layer of photoresist (typically a polymer resin sensitive to light) to a semiconductor structure, positioning a mask over the photoresist, exposing the photoresist to a frequency of light to which it responds (by undergoing a chemical change; usually its solubility in a particular solvent), etching the photoresist to remove the exposed or unexposed pattern (depending upon the resist selected), and then carrying out the next desired step on the remaining pattern.

[0108] The barrier and channel layers **16, 18** are then etched away to reveal a portion of the AlN buffer layer **14** on which the IDTs **26, 28** may be formed. The etch mask **32** is then removed and metallization steps are performed to form the contacts **22, 23, 24** and the IDTs **26, 28**.

[0109] The barrier **16** and the channel **18** layers may be etched using a dry etch process such as reactive ion etching (RIE). Suitable conditions for dry etching the mesa may include dry etching in an Ar environment using BCl_3 etchant. For example, a typical process may include flowing Ar at 20-100 sccm and BCl_3 at 10-20 sccm in an RIE reactor at a pressure of 5-50 mTorr and an RF power at 50-300W. Actual parameters will depend on the system used and may be determined by those skilled in the art. The etch should be highly selective to etch GaN but not AlN.

[0110] An alternative method of fabricating device **10** may be understood with reference to the precursor structure **13** shown in **FIG. 1C**. The device **10** may be fabricated by placing the substrate **12** into a growth reactor and depositing the AlN buffer layer **14** on the substrate **12** as described above. After formation of the buffer layer **14,** the substrate **12** is removed from the growth reactor and a growth mask **34** (which may comprise silicon dioxide, silicon nitride or another suitable material) is formed on the surface of the buffer layer. The mask layer **34** is patterned using standard photolithographic techniques as described above to reveal a portion of the surface of the buffer layer **14**. After formation and patterning of the mask layer **34**, the substrate **12** is placed back into a growth reactor for the regrowth of channel and the barrier layer **16** and the channel layer **18** (and any other layers

that may be present in the device). The contacts **22, 23, 24** and the IDTs **26, 28** may then be formed on the structure after removal of the mask layer **34**.

[0111] As illustrated in **FIGs. 2A** and **2B**, the device **20** includes a SAW structure **20B** that is isolated from a transistor structure **20A** by forming a trench **36** between the structures that extends through buffer layer **14**. The trench **36** may extend into the substrate **12** depending on the thickness of the buffer layer **14** and the wavelength of the device. As discussed above, a SAW extends for a distance of about one wavelength into the propagating medium. Thus, the trench **36** may extend for a distance of at least about one wavelength in order to provide physical isolation of SAW device **20B**.

[0112] As illustrated in **FIG. 2A**, the trench **36** may be formed before, during or after formation of the transistor. For example, an etch mask **38** may be formed on the structure and patterned to reveal a portion of the buffer layer **14** adjacent the transistor mesa. The exposed region is then etched in the manner described above to provide device isolation. After etching, the etch mask is removed and metallization is performed as illustrated in **FIG 2B.FIGs. 3A-3B** illustrate other embodiments of the invention. As **FIG. 3A** schematically illustrates, a device **30** includes a transistor structure **30A** and a SAW device structure **30B** formed on a common substrate. However, in this embodiment, the IDTs **26, 28** of the SAW device **30B** are formed on the surface of the same epitaxial layer as the transistor electrodes, thus avoiding the need for regrowth or mesa etching.

[0113] In order to electrically isolate the SAW device **30B** from the transistor structure **30A** and reduce loss in the SAW device itself, ions **43**, such as nitrogen or phosphorus, are implanted into a region **42** of the device to render the region **42** sufficiently highly resistive as to be electrically inactive.

[0114] As illustrated in **FIG. 3B**, after growth of the epitaxial layers of the transistor structure **30A** to form an epitaxial precursor structure **31**, a patterned implant mask **44** (which may comprise photoresist) is formed on the surface of the precursor structure **31** and nitrogen ions **43** are implanted into the exposed surface **45** so as to implant the nitrogen ions **43** into the region **42.** Other ions can be used to increase the resistivity of the region via implantation, including hydrogen, helium, aluminum, nitrogen, magnesium, zinc and/or calcium.

[0115] The implantation can be carried out in a conventional fashion and at room temperature. As presently best understood (and without being limited by a particular theory), the implanting ions create damage within the GaN to produce deep levels within the bandgap. These in turn trap free carriers in the GaN, thus rendering the material more resistive than a

GaN layer or region without such an implant. In a HEMT structure, the implanted ions effectively neutralize the conductive 2DEG channel at the interface between the barrier and channel layers.

[0116] In certain embodiments, nitrogen atoms are implanted into the exposed region at an energy of 10-400 keV and a dosage of 10^{13}-10^{14} ions per square centimeter (cm^{-2}). Such a dose may be sufficient to neutralize the region **42** or otherwise make the region 42 sufficiently non-conductive such that the transistor structure **30A** is electrically isolated from the SAW device **30B** such that the electrical performance of either the transistor structure **30A** or the SAW device **30B** are not substantially impaired by the other device.

[0117] **FIG. 4** illustrates a device **40** according to further embodiments of the present invention. As with the embodiments described in connection with **FIGs. 3** and **3A**, a SAW device **40B** is formed on the same epitaxial surface as the transistor structure **40A**. However, in addition to the implant neutralization of the layers forming the SAW device **40B**, an isolation trench **56** is formed between the SAW structure **40B** and the transistor structure **40A** using the masking and etching techniques described above in connection with **FIGs. 2A** and **2B**. As discussed above, the depth of the trench **56** may be equal to at least one SAW wavelength.

[0118] Further embodiments of the present invention are illustrated in **FIG. 5**. In the embodiments illustrated in **FIG. 5**, the barrier and the channel layers of the transistor structure **50A** are etched down into the thick GaN layer **16** to remove the 2DEG region between the barrier and channel layers. The SAW IDTs are formed on the exposed surface of the GaN layer, which is semi-insulating as grown. An optional isolation trench **66** may be etched between the transistor structure **50A** and the SAW device structure **50B** using the techniques described above.

[0119] In the embodiments illustrated in **FIGs. 6A-6C**, an AlN-based SAW structure **60B** is integrated on the same substrate as a SiC MESFET structure **60A**. Techniques for growing epitaxial layers of silicon carbide are disclosed in U.S. Patent Nos. U.S. 6,063,186; 6,297,522; 6,217,662; 5,155,062; 4,946,547; 4,912,063; 4,912,064; and 5,011,549, the disclosures of which are incorporated herein by reference. Techniques for growing epitaxial layers of silicon carbide are also disclosed in U.S. Application Serial No. 09/715,576 filed November 17, 2000 for "SUSCEPTOR DESIGNS FOR SILICON CARBIDE THIN FILMS"; U.S. Application Serial No. 09/790,169 filed February 21, 2001 for "SUSCEPTOR DESIGNS FOR SILICON CARBIDE THIN FILMS"; U.S. Publication No. 2001/0170491 published November 21, 2002 for "SEED CRYSTAL HOLDERS AND SEED CRYSTALS

FOR FABRICATING SILICON CARBIDE CRYSTALS AND METHODS OF FABRICATING SILICON CARBIDE CRYSTALS"; U.S. Publication No. 2002/0090454 published July 11, 2002 for "GAS-DRIVEN ROTATION APPARATUS AND METHOD FOR FORMING SILICON CARBIDE LAYERS"; U.S. Application Serial No. 10/017,492 filed October 30, 2001 for "INDUCTION HEATING DEVICES AND METHODS FOR CONTROLLABLY HEATING AN ARTICLE"; and U.S. Application Serial No. 10/117,858 filed April 8, 2002 for "GAS-DRIVEN PLANETARY ROTATION APPARATUS AND METHODS FOR FORMING SILICON CARBIDE LAYERS" the disclosures of which are incorporated herein by reference.

[0120] The SiC epitaxial layers **72** may be grown using techniques described in the foregoing patents and applications to form a precursor structure **61** as illustrated in **FIG. 6B**. An etch mask **73** is formed on the surface of the SiC epitaxial layers **72** and patterned to reveal a portion of the surface **74** of the SiC epitaxial layers **72**. The precursor structure **61** is then etched to reveal a portion of the semi-insulating SiC substrate. The remaining SiC epitaxial layers are then masked with a growth mask **77** illustrated in **FIG. 6C** that extends just past the edge of the SiC epitaxial layers **72** by a predetermined distance that may depend on the thickness of the growth mask **77**. The etch mask **73** may or may not be removed prior to formation of the growth mask **77**.

[0121] A layer of crystalline AlN **14** is regrown on the exposed substrate and the mask **77** is removed. Because the regrown AlN layer **14** is separated from the SiC epitaxial layer **72**, the SAW structure **60B** and the MESFET structure **60A** are isolated as grown. The metal contacts **22, 23, 24** are formed on the SiC epitaxial layers **72** and the SAW IDTs **26, 28** are then formed on the AlN layer to complete the device.

[0122] As illustrated in **FIG. 7**, the foregoing techniques can be extended to integrate more than one type of device on the same substrate as one or more SAW devices. For example, the device **70** includes a transistor structure **70A**, a SAW device **70B** and a photodetector structure **70C** integrated on the same substrate **12**. Such a device may, for example, be used as a monolithic element capable of receiving, amplifying, and filtering an optical information signal. Likewise, the embodiments illustrated in **FIG. 8** include a transistor structure **80A**, a SAW device **80B**, a photodetector structure **80C**, and an emitter structure **80D** integrated on the same substrate **12**. Such devices may, for example, be used as a monolithic element capable of receiving, amplifying, and filtering an optical information signal and transmitting an information signal. The design of GaN-based emitters and photodetectors is well known to those skilled in the art. Examples of GaN-based

photodetectors are illustrated in U.S. Patents 6,495,852 and 6,265,727, which are incorporated herein by reference. Examples of GaN-based emitters are illustrated in U.S. Patents 5,523,589 and 5,739,554, which are incorporated herein by reference.

[0123] Other circuit elements may be integrated onto the same substrate as the SAW device and the electronic device. For example, capacitors, inductors, resistors, delay lines and the like may be integrated into the device as well.

[0124] Integration of different types of nitride devices on a common substrate poses challenges, because many types of devices, such as transistors, emitters, limiters, etc., have complex epitaxial structures which are tailored to the operation of a particular type of device. Embodiments of the present invention arise from a recognition that while certain devices have different epitaxial structures, some aspects of those structures may be similar, and may be used in different types of devices formed on a common substrate.

[0125] For example, **FIG 12A** and **FIG. 12B** show exemplary epitaxial precursor structures that may be used to form two different types of devices. The epitaxial structure shown in **FIG. 12A** (Type I) may be used to fabricate a low-noise amplifier or a power amplifier, while the epitaxial structure shown in **FIG. 12B** (Type II) may be used as a basis for a limiter or an RF switch transistor. In particular, the Type I epitaxial structure of **FIG. 12A** includes a substrate **100** on which a buffer layer **102** and channel layer **104** are formed. The substrate **100** may include a semi-insulating 6H or 4H silicon carbide substrate. The buffer layer **102** may include an aluminum nitride layer, which may provide an appropriate crystal structure transition between the silicon carbide substrate **100** and the remainder of the device. In particular, the buffer layer **102** may be formed by metal-organic chemical vapor deposition and may have a thickness of about 100 Å to about 10,000 Å. In particular embodiments, the buffer layer 102 may have a thickness of about 1000 Å.

[0126] A channel layer **104**, which in some embodiments is semi-insulating $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$), is formed on the buffer layer **102**. In some embodiments, the channel layer **104** is undoped, but in other embodiments may be doped with various impurities in order to modify the electron concentration in the sheet charge region or the behavior of the conduction band Ec and valence band Ev in the area below the sheet charge region. In some embodiments, the channel layer **104** is about 1 to 5 μm thick. In some embodiments, the channel layer **104** may include a 2 μm thick GaN-based buffer layer with a thin (approximately 100 Å) high-quality channel region (not shown) formed thereon.

[0127] A barrier layer **106** is formed on the channel layer **104**. In some embodiments, the barrier layer **106** may include AlN, thereby forming a heterojunction between the channel layer **104** and the barrier layer **106**. A high bandgap layer **108** is on the barrier layer **106**. The high bandgap layer **108** may include $Al_xGa_{1-x}N$ ($0 \leq x \leq 1$) having an aluminum composition of between 20% and 40%. The high bandgap layer **108** may have a higher bandgap than the channel layer **104**. The high bandgap layer **108** may be doped with silicon at a doping concentration of about 2×10^{18} cm^{-3}. The high bandgap layer **108** may be between about 15 nm and 40 nm in thickness, and in some embodiments is about 25 nm thick.

[0128] As discussed above, because of the AlGaN/GaN heterobarrier at the interface between the channel layer **104** and the barrier layer **106**, a two-dimensional electron gas may be induced at the interface.

[0129] A high purity silicon nitride layer **110** may be formed on the high bandgap layer **108**. High purity silicon nitride may be formed as described in commonly-assigned U.S. Patent Application Serial No. 11/286,805 filed November 23, 2005 and entitled "GROUP III NITRIDE SEMICONDUCTOR DEVICES WITH SILICON NITRIDE LAYERS AND METHODS OF MANUFACTURING SUCH DEVICES" the disclosure of which is hereby incorporated by reference as if fully set forth herein.

[0130] The Type I epitaxial structure of **FIG. 12A** may be useful for forming a HEMT device for a low noise and/or high power amplifier. For example, the Type I epitaxial structure may provide appropriate peak current, transconductance, and/or breakdown voltage characteristics useful for high power amplifier output transistors. The thickness and/or the aluminum percentage of the high bandgap layer **108** may be adjusted to provide appropriate characteristics for a low noise amplifier.

[0131] The epitaxial structure shown in **FIG. 12B** (Type II) is similar to the Type I epitaxial structure shown in **FIG. 12A**, except that the Type II epitaxial structure includes an additional epitaxial layer **112** between the high bandgap layer **108** and the high purity silicon nitride layer **110**. In particular, the high bandgap layer **108**, the barrier layer **106** and the channel layer **104** may be the same as in the Type I epitaxial structure. The additional epitaxial layer **112** may include a layer of doped GaN and/or graded AlGaN having a thickness of about 300 Å to about 1000 Å. For an RF switch device and/or a limiter device, the additional epitaxial layer **112** may increase the distance between the top surface of the device and the charge in a 2DEG channel induced at the interface between the channel layer

104 and the barrier layer 106. This may reduce the gate-to-source capacitance of the device, while maintaining a low channel resistance.

[0132] A device having a Type I epitaxial structure and a device having a Type II epitaxial structure may be integrated on a common substrate as illustrated in FIG. 13A. As shown therein, a Type II epitaxial structure may be formed using, for example, conventional MOCVD growth techniques. Source/drain ohmic contacts 122, 124, 128 may be recessed through the high purity silicon nitride layer 110 and the additional epitaxial layer 112. While not illustrated in FIG. 13A, the source/drain ohmic contacts 122, 124, 128 may be fully and/or partially recessed into/through the high bandgap layer 108 and/or the barrier layer 106.

[0133] A first transistor Q1 is defined by a gate 120 positioned between adjacent source/drain contacts 122, 124. The first transistor Q1 may be, for example, a high power or low-noise transistor. Thus, in the first transistor Q1, the gate contact 120 is recessed through both the high purity silicon nitride layer 110 and the additional epitaxial layer 112, as shown in FIG. 13A.

[0134] Accordingly, for the first transistor Q1, the gate etch is used to remove a portion, or all, of the additional epitaxial layer 112 underneath the high purity silicon nitride layer 110. A low channel or access resistance may be maintained in the non-gated regions of the first transistor Q1 due to the presence of the additional epitaxial layer 112, which, as explained above, may be a relatively thick GaN cap and/or graded/doped AlGaN as described in Journal of Electronic Materials, Vol. 33, No. 5, 2004, or IEEE Electron Device Letters, Vol. 25, No. 1, January 2004 or Journal Of Applied Physics Volume 94, Number 8, 15 October 2003..

[0135] A second transistor Q2 is defined by a second gate contact 126 positioned between source/drain contacts 124, 128. The second transistor Q2 may be configured, for example, as a limiter and/or an RF switch. The second gate contact 126 may be recessed only through the high purity silicon nitride layer, and is not recessed through, or is only partially recessed through, the additional epitaxial layer 112. The presence of the additional epitaxial layer 112 may reduce the gate capacitance of the second transistor Q2. Thus, two transistors Q1 and Q2, having different epitaxial structures and/or different operational characteristics, may be provided on the same substrate by forming a single epitaxial structure and etching the structure appropriately.

[0136] A schematic diagram of a possible circuit formed by the first and second transistors Q1 and Q2 is ilustrated in FIG. 13B. As shown therein, the first and second transistors may share a common source/drain contact 124.

[0137] Further methods and structures according to embodiments of the invention are illustrated in **FIGs. 14A** and **14B**. As shown therein, a Type I epitaxial structure similar to the structure illustrated in **FIG. 12A** is provided. In particular, the structure shown in **FIG. 14A** includes a buffer layer **102** on a substrate **100**. A channel layer **104**, a barrier layer **106**, a high bandgap layer **108** and a high purity silicon nitride layer **110** are formed on the buffer layer **102**. A photoresist mask **210** is formed on a portion of the high purity silicon nitride layer **110**, and a portion of the high purity silicon nitride layer exposed by the mask **210** (i.e. not covered by the mask **210**) may be etched away using, for example, conventional dry etching techniques. The exposed portions of the high purity silicon nitride layer **110** may be etched away, for example, to reveal the high bandgap layer **108** beneath the high purity silicon nitride layer **110**.

[0138] Following the selective etching of the high purity silicon nitride layer, the photoresist mask **210** may be removed, and a epitaxial layer **125** may be epitaxially regrown on the exposed high bandgap layer **108**. The epitaxial layer **125** may be similar to the epitaxial layer **112** shown in **FIG. 13A**. For example, the epitaxial layer **125** may include doped GaN and/or graded AlGaN, and may have a thickness of about 30 Å to about 10,000 Å.

[0139] The high purity silicon nitride layer **110** may act as a growth mask for the growth of the epitaxial layer **125**. That is, when the epitaxial layer **125** is regrown, for example using MOCVD, crystalline material may not nucleate and/or grow on the high purity silicon nitride layer **110**, as the high purity silicon nitride layer **110** may not provide a suitable template for epitaxial growth.

[0140] In some embodiments, however, it may be desirable to provide a separate growth mask on the high purity silicon nitride layer **110** when the epitaxial layer **125** is regrown in order to reduce and/or prevent stray nucleation on the silicon nitride layer **110**. The photoresist mask **210** used as an etch mask when the high purity silicon nitride layer **110** is etched may not be useful as a growth mask, because the polymer-based material used in photoresist may not withstand the high temperatures required for epitaxial growth of nitride materials. Thus, a separate growth mask may be provided on the high purity silicon nitride layer **110**. For example, referring to **FIG. 14B**, a growth mask **160** may be formed on the high purity silicon nitride layer **110**. The growth mask may include, for example, silicon dioxide and/or aluminum nitride. The growth mask may be formed on the high purity silicon nitride layer **110** prior to etching the high purity silicon nitride layer **110**, and may be

patterned using conventional lithographic techniques. For a silicon dioxide growth mask, the silicon dioxide should have a thickness greater than 1000 Å.

[0141] In some embodiments, the same etch mask **210** may be used to pattern both the etch mask **160** and the high purity silicon nitride layer **110**. In other embodiments, the etch mask **210** may be used to pattern the growth mask **160**, and the growth mask **160** may be used as an etch mask for etching the high purity silicon nitride layer **110**, as well as for preventing and/or reducing unwanted nucleation on the high purity silicon nitride layer **110** during epitaxial regrowth of the epitaxial layer **125**.

[0142] As shown in **FIG. 14B**, during epitaxial regrowth of the epitaxial layer **125**, some random crystallite and/or polycrystalline material **163** may nucleate and/or grow on the growth mask **160**. The unwanted material **163** may be removed by removing the growth mask **160** from the high purity silicon nitride layer **110**, which may be done, for example, by performing a buffered oxide etch (BOE) if the growth mask **160** is silicon dioxide. A BOE may etch silicon dioxide but may not etch high purity silicon nitride **110**.

[0143] Following regrowth of the epitaxial layer **125**, a plurality of devices may be defined in the epitaxial structure by forming one or more electrical contacts on the structure. For example, as shown in **FIG. 15**, a first transistor **Q3**, which may be a low noise amplifier and/or a high power amplifier, may be defined by forming source/drain contacts **132**, **134** on the high bandgap layer **108**. The source/drain contacts **132**, **134** may be partially and/or fully recessed through the high bandgap layer **108**. A gate contact **130** for the first transistor **Q3** is recessed through the high purity silicon nitride layer **110**. In some embodiments, the transistor Q3 may have an insulating gate structure (e.g. a metal-insulator-semiconductor heterojunction field effect transistor, or MISHFET) as shown in any of U.S. Pre-grant Publication No. 2003/0020092 entitled "Insulating Gate AlGaN/GaN HEMT", U.S. Pre-grant Publication No. 2005/0170574 entitled "Nitride-based Transistors with a Protective Layer and Low-damage Recess and Method of Fabrication Thereof," U.S. Patent Application No. 11/185,398, filed July 20, 2005 and entitled " Nitride-Based Transistors and Fabrication Methods With an Etch Stop Layer" and/or U.S. Patent Application No. 11/187,171, filed July 21, 2005 and entitled "Switch Mode Power Amplifier using MIS-HEMT with Field Plate Extension," the disclosures of which are incorporated herein by reference as if fully set forth herein.

[0144] A second transistor **Q4** may be formed in the region of the structure in which the epitaxial layer **125** was regrown. In particular, the second transistor **Q4** may be defined by a gate contact **140** that is recessed through a silicon nitride layer **170** that may be formed

on the epitaxial layer **125**. Source and drain contacts **142, 144** complete the second transistor **Q4**.

[0145] It will be appreciated that the second transistor **Q4** may be configured as a two terminal device, such as a limiter diode, by electrically connecting the source contact **142** and the drain contact **144**. When so configured, the source and drain contacts **142, 144** together function as a device cathode, while the gate contact **140** may function as a device anode. A limiter diode may be used, for example, as an input to an amplifier transistor, such as the first transistor **Q3**.

[0146] It will be further appreciated that the epitaxial layers of the first transistor **Q3** may serve as the substrate on which the epitaxial layers of the second transistor **Q4** are formed. Accordingly, some embodiments of the invention provide a first nitride based electronic device including a first nitride based epitaxial structure, and a second nitride based electronic device having a second nitride based epitaxial structure formed on the first nitride based epitaxial structure. In the case of the structure shown in **FIG. 15**, the buffer layer **102**, channel layer **104**, barrier layer **106** and high bandgap layer **108** form a first epitaxial structure for a first transistor **Q3**, while the epitaxial layer **125** forms a second epitaxial structure, formed on the first epitaxial structure, for a second transistor **Q4**.

[0147] Referring to **FIG. 16**, In some embodiments in which a limiter diode is formed, it may be desirable to provide a first epitaxially regrown layer **127** of n+ GaN on the high bandgap layer **108** and a second epitaxially regrown layer **129** of n- GaN on the first regrown layer **127**. The first regrown layer **127** may have a thickness of about 0.5 μm and a doping concentration of about 2×10^{18} cm^{-3} or more, which provides a surface charge density of at least about 1×10^{14} cm^{-2}. The second regrown layer **129** may have a thickness of at least 1000 Å, and may be doped lightly enough that it is fully depleted at zero bias. In particular, the second regrown layer **129** may have a doping concentration of less than about 1×10^{16} cm^{-3}.

[0148] Embodiments of the present invention may provide both enhancement and depletion mode nitride-based transistor devices on a common substrate. For example, a depletion mode device may be formed by providing an epitaxial structure, such as the Type I epitaxial structure shown in **FIG. 12A**, and forming ohmic contacts thereto as described in connection with **FIG. 14C**. An enhancement mode device may be formed using the same epitaxial structure, but by recessing the gate contact into the underlying high bandgap layer **108** or performing a threshold-voltage shift using negative ions and introducing them into the device by ion implantation or plasma immersion doping.

[0149] Some embodiments of the invention provide for the integration of both silicon carbide devices and nitride devices on a common substrate. For example, as illustrated in **FIG. 6A**, a silicon carbide MESFET device and a nitride based SAW device may be integrated on a common substrate. As discussed above in connection with **FIG. 6A**, it may be possible to form an epitaxial layer **72** of silicon carbide on a substrate on which a layer **14** of aluminum nitride is also formed.

[0150] However, it may be difficult to form both silicon carbide epitaxial layers and gallium nitride-based epitaxial layers on a common substrate, since gallium nitride based epitaxial layers are conventionally grown on on-axis substrates, while silicon carbide epitaxial layers are conventionally grown on off-axis substrates, although it is possible to grow relatively thin (<100 nm) epitaxial layers of silicon carbide on an on-axis substrate.

[0151] According to some embodiments of the invention, a silicon carbide MESFET may be formed on an on-axis substrate by implanting source/drain regions as well as a channel region in an on-axis semi-insulating silicon carbide substrate, as illustrated in **FIGs. 17A** and **17B**. As shown therein, one or more implant regions may be formed in an on-axis, semi-insulating 4H-SiC substrate by means of ion implantation. For example, as shown in **FIG. 17A**, an n-type channel region **216** may be formed in the substrate **200** by selective implantation of nitrogen and/or phosphorus ions. Furthermore, n+ source/drain regions **212**, **214** may be formed in the substrate **200** by ion implantation. Multiple implantation steps with different implant energies/doses may be performed in order to provide a desired doping profile. Implantation of dopants into bulk silicon carbide layers is known in the art. After implantation, the dopants may be activated by annealing the implanted structure at a temperature of about 1400 °C to about 1700 °C for about 5 minutes to about 30 minutes. In particular, it may be desirable to activate the implanted dopants prior to epitaxial growth of nitride layers on the substrate **200**, as the temperatures required to activate dopants implanted in silicon carbide may be detrimental to nitride-based epitaxial layers.

[0152] As further illustrated in **FIG. 17A**, The implanted regions of the substrate **200** may then be masked with a growth mask **205**. The growth mask **205** may include, for example, a SiN and/or SiO_2 pattern formed on the surface of the substrate **200**. An epitaxial structure **210** may be grown on the exposed portions of the substrate **200** using conventional epitaxial growth techniques. For example, the epitaxial structure **210** may include a buffer layer, a channel layer, a barrier layer, and a high bandgap layer, which may have structures similar to the corresponding layers shown, for example, in **FIG. 12A**, in order to provide an

epitaxial precursor for a HEMT device. However, it will be appreciated that other epitaxial structures could be formed, depending on the type/characteristics of nitride device desired.

[0153] Referring to **FIG. 17B**, the growth mask **205** may be removed, and a passivation layer **228**, such as silicon dioxide and/or silicon nitride, may be formed on exposed portions of the substrate **200** and the epitaxial structure **210**. Alternatively, the growth mask may be left on the substrate as a passivation layer, and a second passivation layer may be formed on the nitride epitaxial layers. Accordingly, while a single passivation layer **228** is illustrated in **FIG. 17B**, the passivation layer on the nitride epitaxial structure **210** may be different from the passivation layer on the silicon carbide substrate **200**. Furthermore, the passivation layer **228** may include multiple passivation layers of the same and/or different types of materials stacked on one another.

[0154] A first gate contact **230** and corresponding source/drain contacts **232, 234** may be formed on the epitaxial structure **210** to define a HEMT transistor device **Q5**, and a second gate contact **240** may be formed on the implanted channel region **216** along with corresponding source/drain contacts **242, 244**, to define a silicon carbide MESFET device **Q6** in the substrate **200**. The nitride device **Q5** and the silicon carbide device **Q6** may be interconnected on the common substrate **200** by one or more levels of interconnect metallization. For example, a dielectric layer **260** may be formed on the nitride device **Q5** and the silicon carbide device **Q6**. Metal contact plugs **261, 262** may be formed through the dielectric layer **260** to contact electrical contacts of the nitride device **Q5** and the silicon carbide device **Q6**, respectively. The contact plugs **261, 262** may be electrically connected, for example, by an overlayer metal **266** formed on the dielectric layer **260**. Other connections between the nitride device **Q5** and the silicon carbide device **Q6** are possible.

[0155] Accordingly, in some embodiments of the invention, a silicon carbide transistor device may be formed on the same substrate as a nitride-based transistor device to form a monolithically integrated device structure. Monolithically integrated nitride devices, and monolithically integrated silicon carbide/nitride devices, may have particular applications in monolithic microwave integrated circuits, in which it may be desirable to carefully control the orientation, placement and/or interconnection of devices, due to the high frequency and/or high power of signals processed by such devices. For example, when devices are not monolithically integrated, it may be necessary to interconnect such devices using electrical traces and/or wires, which may add unwanted inductance, capacitance and/or resistance to the circuit. Such interconnections may also increase the difficulty of circuit design, since the

circuit designer must take into account additional signal delays and/or signal dispersion associated with chip-to-chip interconnections.

[0156] As discussed above, some embodiments of the present invention provide monolithic integration of two or more semiconductor device types when a highly conductive, buried layer is required for one of the device types. In other words, a first device having a first epitaxial structure (Type I), for example, a low noise and/or high power amplifier (LNA) can be integrated with a second device having a second epitaxial structure (Type II), for example, a limiter diode, according to some embodiments of the present invention discussed above. In particular, if the Type II structure including a full n^+/n^- GaN epitaxial structure as discussed above can be selectively grown on top of the Type I epitaxial structure, it may be possible to screen areas of the wafer to maintain the Type I structure while growing the extra layers in the regions of the wafer that require Type II as discussed in detail above.

[0157] In further embodiments of the present invention, devices that include buried, high-conductive regions can be formed by first forming a highly conductive region by selective ion implantation as will be discussed below with respect to **FIGs. 18** through **20C**. Thus, according to some embodiments of the present invention discussed below with respect to **FIGs. 18** through **20C**, it may not be necessary to grow a thick n^+ layer, for example, layer **127** of **FIG. 16**, on the high bandgap layer **108**, thus, possibly reducing the total regrowth thickness. Accordingly, higher quality materials and shorter growth times may be achieved.

[0158] Referring now to **FIG. 18**, integrated devices having an implanted highly conductive region according to some embodiments of the present invention will be discussed. Like numerals refer to like elements throughout, thus, details with respect to layers discussed above will not be repeated in the interest of brevity. As illustrated in **FIG. 18**, a buffer layer **102** is provided on a substrate **100**. A channel layer **104**, a barrier layer **106**, a high bandgap layer **108** are sequentially provided on the buffer layer **102**.

[0159] As further illustrated in **FIG. 18**, implanted source and drain regions **801** and **802**, respectively, are provided in the high bandgap layer **108** on the Type I side of the integrated device. In some embodiments of the present invention, the source and drain regions **801** and **802** may be implanted n^+ source and drain regions. Details of doping concentrations for these regions are discussed in commonly assigned United States Patent Application No. 11/302,062 to Sheppard et al., filed on December 13, 2005 entitled "SEMICONDUCTOR DEVICES INCLUDING IMPLANTED REGIONS AND PROTECTIVE LAYERS AND METHODS OF FORMING THE SAME," the disclosure of which is hereby incorporated herein by reference as if set forth in its entirety.

[0160] As further illustrated in **FIG. 18**, an implanted highly conductive region **805** in accordance with some embodiments of the present invention is provided in the high bandgap layer **108** on the Type II side of the integrated device. The highly conductive region **805** may be an implanted n^+ region having a peak doping concentration of about $5.0X10^{20}$ cm^{-3}.

[0161] As further illustrated in **FIG. 18**, an epitaxially regrown layer **129** of n- GaN is provided on the n^+ implanted region **805**. The regrown layer **129** may have a thickness of at least 1000 Å, and may be doped lightly enough that it is fully depleted at zero bias. In particular, the second regrown layer **129** may have a doping concentration of less than about $1x10^{16}$ cm^{-3}.

[0162] Following regrowth of the epitaxial layer **129**, a plurality of devices may be defined in the epitaxial structure by forming one or more electrical contacts on the structure. For example, as shown in **Fig.18**, a first transistor, for example, a low noise amplifier and/or a high power amplifier, may be defined by forming source/drain contacts **132, 134** on the implanted n^+ source and drain regions **801** and **802**, respectively, in high bandgap layer **108**. A gate contact **130** for the first transistor is recessed through the high purity silicon nitride layer **110**.

[0163] A second transistor may be formed in the region of the structure in which the epitaxial layer **129** was regrown. In particular, the second transistor may be defined by a gate contact **140** that is recessed through a silicon nitride layer **170** that may be formed on the epitaxial layer **129**. Source and drain contacts **142, 144** complete the second transistor.

[0164] It will be appreciated that the second transistor may be configured as a two terminal device as illustrated in **FIG. 19**, such as a limiter diode, by electrically connecting the source contact **142** and the drain contact **144**. When so configured, the source and drain contacts **142, 144** together function as a device cathode, while the gate contact **140** may function as a device anode.

[0165] Thus, according to embodiments of the present invention illustrated in **Fig.18**, inclusion of the n^+ implanted region **805** in the bandgap layer **108** allows the regrown region **127** illustrated in **FIG. 16** to be reduced. As discussed above, the device illustrated in **FIG. 18** may be configured as a two terminal device as illustrated in **FIG. 19**. Without the n^+ implanted region **805** in accordance with some embodiments of the present invention, the anode contact (**140**) would be placed on a regrown n^+ layer, which may cause hexagonal pit defects.

[0166] Referring now to **FIG. 19**, some embodiments of the present invention including a two terminal device will be discussed. Like reference numerals refer to like

elements throughout, thus, details with respect to like elements will not be repeated herein with respect to **FIG. 19**. As illustrated in **FIG. 19**, the anode **901** is provide on the epitaxially regrown layer **129** of n^- GaN, which is provided on the n^+ implanted region **805**. As further illustrated in **FIG. 19**, the cathode **902** of the two terminal device is provided on the n^+ implanted region **805**.

[0167] Processing steps in the fabrication of integrated devices in accordance with some embodiments of the present invention will be discussed with respect to **FIGs. 20A** through **20C**. The discussion with respect to Figures will be limited to the formation of the implanted source and drain regions **801** and **802**, the n^+ region **805** and the n^- GaN layer **129** as the formation of the remaining elements of **FIGs. 20A** through **20C** have been thoroughly discussed herein.

[0168] Referring first to **FIG. 20A**, a mask **1000**, for example, SiO_2 may be deposited and patterned on the high bandgap layer **108**. Ions are implanted into the portion of the high bandgap layer exposed through the mask **1000** to implant the n^+ source and drain regions drain regions **801** and **802**, respectively.

[0169] As illustrated in **FIG. 20B**, the mask **1000** is removed and a second mask **1010**, for example, SiO2 may be deposited and patterned on the high bandgap layer **108**. Ions are implanted into the portion of the high bandgap layer exposed through the mask **1010** to implant the highly conductive region **805** in accordance with some embodiments of the present invention. The highly conductive region **805** may be an implanted n^+ region may have peak doping concentration of about $5.0\text{x}10^{20}\ \text{cm}^{-3}$.

[0170] As illustrated in **FIG. 20C**, the mask **1010** may be removed and a third mask **1020**, for example, SiO2, may be deposited and patterned on the high bandgap layer **108**. The growth mask **1020** may be formed on the high purity silicon nitride layer **108** and may be patterned using conventional lithographic techniques. For a silicon dioxide growth mask, the silicon dioxide may have a thickness greater than about 1000 Å. Although the mask **1010** has been removed in **FIG. 20C**, in some embodiments of the present invention the growth mask **1020** may be formed with the mask **1010** still in place without departing form the scope of the present invention.

[0171] An epitaxially regrown layer **129** of n^- GaN is provided on the n^+ implanted region **805**. The regrown layer **129** may have a thickness of at least about 1000 Å, and may be doped lightly enough that it is fully depleted at zero bias. In particular, the regrown layer **129** may have a doping concentration of less than about $1.0\text{x}10^{16}\ \text{cm}^{-3}$ in some embodiments.

The masks **1020** and **1010**, if present, may be stripped and the device may be finished using conventional techniques.

[0172] It will be appreciated that the device structures illustrated herein may be representative unit cell structures that are replicated in larger devices, which may have multiple gate fingers on multiple active regions. Furthermore, while some embodiments of the invention employ semi-insulating silicon carbide substrates, other types and/or conductivities of substrates may be utilized.

[0173] While embodiments of the present invention have been described with reference to isolation of the device(s) from other devices on a common substrate through the use of etching and/or selective growth processes, other techniques of trench formation such as sawing, laser ablation or other techniques known to those of skill in the art may be utilized to provide such isolation trenches. Device isolation may also be provided by isolation implants or other means.

[0174] Embodiments of the invention have been set forth in the drawings and specification, and although specific terms have been employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being defined in the claims.

THAT WHICH IS CLAIMED IS:

1. A monolithic electronic device, comprising:

a common nitride epitaxial layer;

a first type of nitride device on the common nitride epitaxial layer including a first at least one implanted n-type region on the common nitride epitaxial layer, the first at least one implanted n-type region having a first doping concentration greater than a doping concentration of the common nitride epitaxial layer;

a second type of nitride device, different from the first type of nitride device, including a second at least one implanted n-type region on the common nitride epitaxial layer, the second at least one implanted n-type region being different from the first at least one implanted n-type region and having a second doping concentration that is greater than the doping concentration of the common nitride epitaxial layer;

a first plurality of electrical contacts on the first at least one implanted n-type region, the first plurality of contacts defining a first electronic device of the first type of nitride device; and

a second plurality of electrical contacts on the second at least one n-type implanted region, the second plurality of contacts defining a second electronic device of the second type of electronic device.

2. The monolithic electronic device of Claim 1, wherein the first at least one implanted n-type region comprises source and drain regions for the first electronic device and wherein the first plurality of electrical contacts comprise a source contact on the source region, a drain contact on the drain region and a gate contact between the source and the drain contacts.

3. The monolithic electronic device of Claim 2, wherein the second at least one implanted n-type region comprises a highly conductive n-type region and wherein the second plurality of electrical contact comprises source and drain contacts and gate contact between the source and drain contacts on the highly conductive n-type region.

4. The monolithic device of Claim 3, wherein the highly conductive n-type region has a doping concentration of from about 5.0×10^{18} to about 6.0×10^{18} cm^{-3} and a depth of from about 0.1 to about 1.0μm.

5. The monolithic device of Claim 3, wherein the gate and drain contacts of the second electronic device are electrically coupled to form an anode.

6. The monolithic electronic device of Claim 3, wherein the common nitride epitaxial structure comprises:

a nitride channel layer;

a nitride barrier layer on the nitride channel layer, the nitride barrier layer having a higher bandgap than the nitride channel layer, wherein the nitride barrier layer and the nitride channel cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer.

7. The monolithic electronic device of Claim 6, further comprising a high bandgap layer on the barrier layer and a silicon nitride layer on the high bandgap layer.

8. The monolithic electronic device of Claim 7, wherein the highly conductive n-type region comprises an implanted region of n-type $Al_XGa_{1-X}N$ ($0 \le x \le 1$) in the high bandgap layer, the second electronic device comprising a layer of n-type $Al_XGa_{1-X}N$ ($0 \le x \le 1$) on the highly conductive n-type region having a doping concentration of less than about 1×10^{16} cm^{-3}.

9. The monolithic electronic device of Claim 1, wherein the first electronic device comprises a high electron mobility transistor.

10. The monolithic electronic device of Claim 9, wherein the second electronic device comprises a surface acoustic wave device.

11. The monolithic electronic device of Claim 9, wherein the second electronic device comprises a diode.

12. The monolithic electronic device of Claim 9, wherein the second electronic device comprises a field effect transistor.

13. The monolithic electronic device of Claim 9, wherein the second electronic device comprises a MISHFET.

14. A monolithic electronic device, comprising:

a nitride epitaxial structure comprising:

a nitride channel layer;

a nitride barrier layer on the nitride channel layer, the nitride barrier layer having a higher bandgap than the nitride channel layer;

the nitride barrier layer and the nitride channel cooperatively inducing a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer;

first and second n-type implanted regions on the barrier layer defining source and drain regions, respectively;

a first gate electrode between the source and drain regions, the first gate electrode defining a first transistor device;

a third n-type implanted region on the barrier layer defining an implanted highly conductive n-type region; and

a second gate electrode on the implanted highly conductive n-type region, the second gate electrode defining a second transistor device.

15. A method of forming a monolithic electronic device, comprising:

forming a common nitride epitaxial layer;

forming a first type of nitride device on the common nitride epitaxial layer including a first at least one implanted n-type region on the common nitride epitaxial layer, the first at least one implanted n-type region having a first doping concentration greater than a doping concentration of the common nitride epitaxial layer;

forming a second type of nitride device, different from the first type of nitride device, including a second at least one implanted n-type region on the common nitride epitaxial layer, the second at least one implanted n-type region being different from the first at least one implanted n-type region and having a second doping concentration that is greater than the doping concentration of the common nitride epitaxial layer;

forming a first plurality of electrical contacts on the first at least one implanted n-type region, the first plurality of contacts defining a first electronic device of the first type of nitride device; and

forming a second plurality of electrical contacts on the second at least one n-type implanted region, the second plurality of contacts defining a second electronic device of the second type of electronic device.

16. The method of Claim 15, wherein forming the first at least one implanted n-type regions comprises implanting source and drain regions for the first electronic device and wherein forming the first plurality of electrical contacts comprises forming a source contact on the source region, a drain contact on the drain region and a gate contact between the source and the drain contacts.

17. The method of Claim 16, wherein forming the second at least one implanted n-type region comprises implanting a highly conductive n-type region and wherein forming the second plurality of electrical contact comprises forming source and drain contacts and gate contact between the source and drain contacts on the highly conductive n-type region.

18. The method of Claim 17, wherein forming the highly conductive n-type region comprises forming the highly conductive n-type region having a doping concentration of from about 5.0×10^{18} to about 6.0×10^{18} cm^{-3} and a depth of from about 0.1 to about 1.0μm.

19. The method of Claim 16, wherein forming the gate and drain contacts of the second electronic device comprises forming the gate and drain contacts such that the gate and drain contacts are electrically coupled to form an anode.

20. The method of Claim 19 wherein forming the common nitride epitaxial structure comprises:

forming a nitride channel layer;

forming a nitride barrier layer on the nitride channel layer, the nitride barrier layer having a higher bandgap than the nitride channel layer, wherein the nitride barrier layer and the nitride channel cooperatively induce a two-dimensional electron gas at an interface between the nitride channel layer and the nitride barrier layer.

21. The method of Claim 20, further comprising forming a high bandgap layer on the barrier layer and a silicon nitride layer on the high bandgap layer.

22. The method of Claim 21, wherein forming the highly conductive n-type region comprises implanting a region of n-type $Al_xGa_{1-x}N$ ($0\leq x\leq 1$) in the high bandgap layer, the method further comprising forming a layer of n-type $Al_xGa_{1-x}N$ ($0\leq x\leq 1$) on the highly conductive n-type region having a doping concentration of less than about $1x10^{16}$ cm^{-3}.

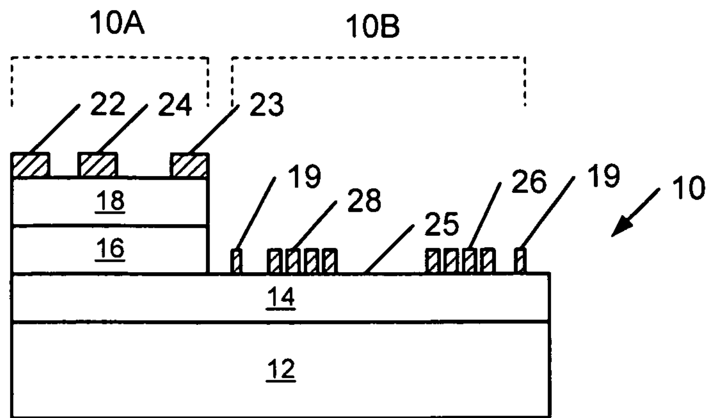

FIG. 1A

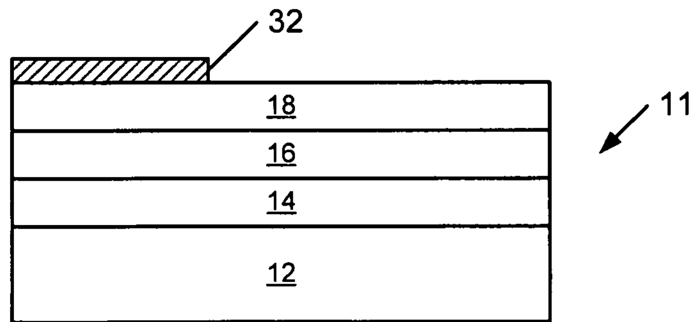

FIG. 1B

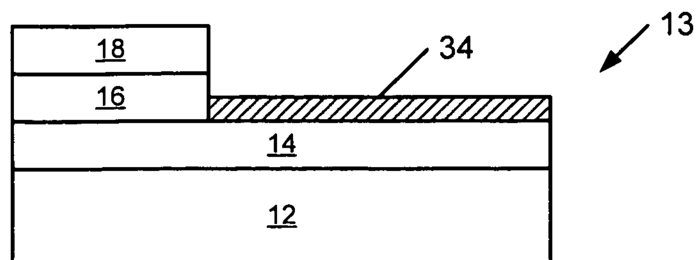

FIG. 1C

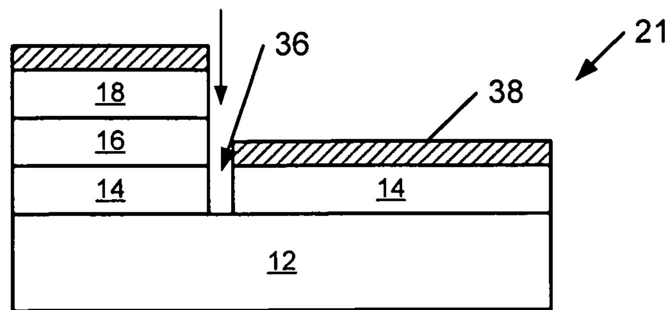

FIG. 2A

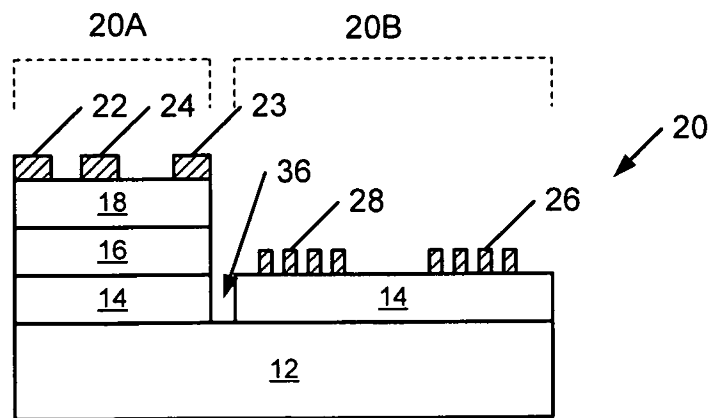

FIG. 2B

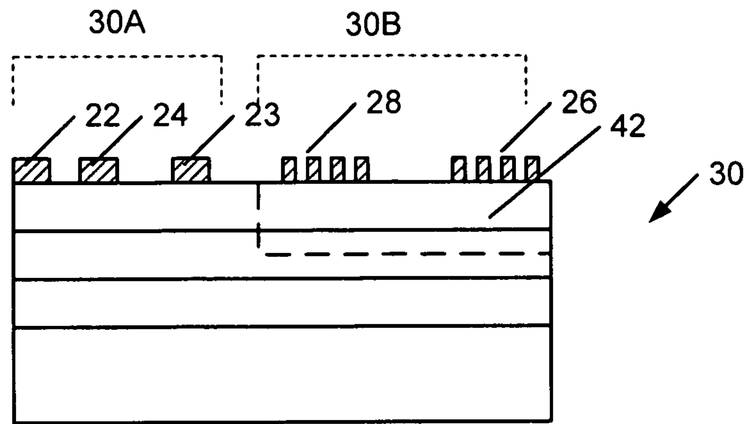

FIG. 3A

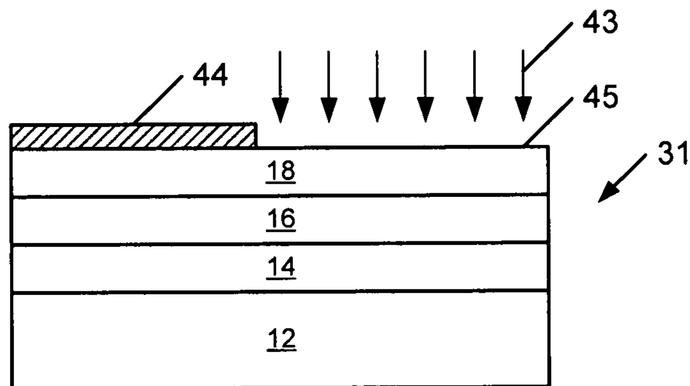

FIG. 3B

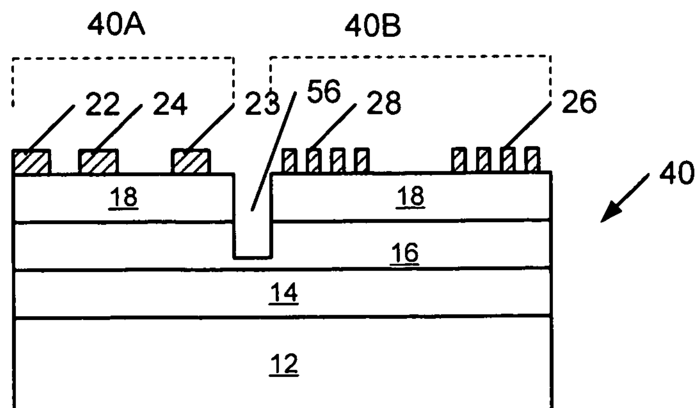

FIG. 4

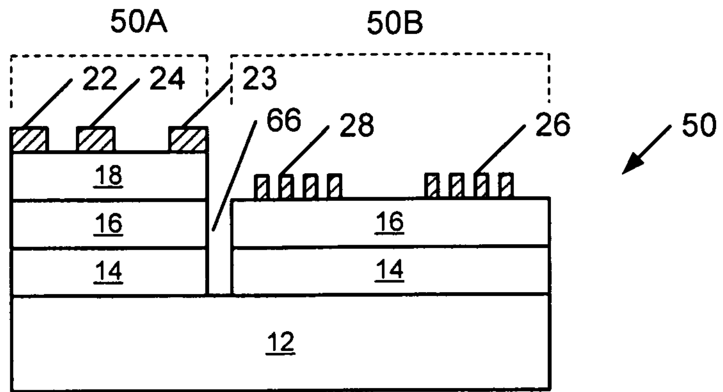

FIG. 5

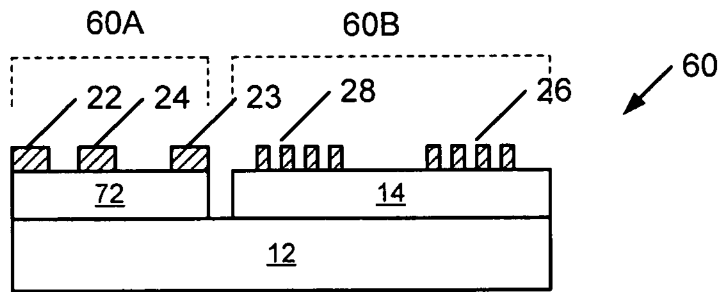

FIG. 6A

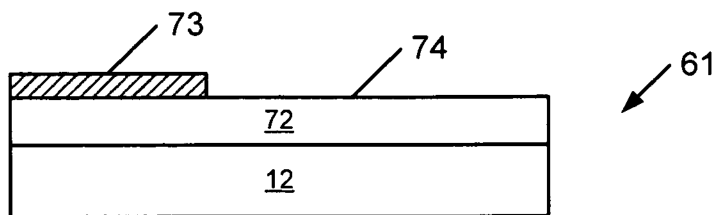

FIG. 6B

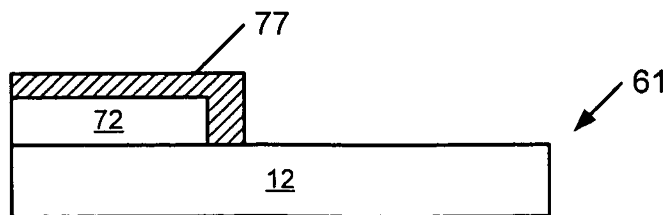

FIG. 6C

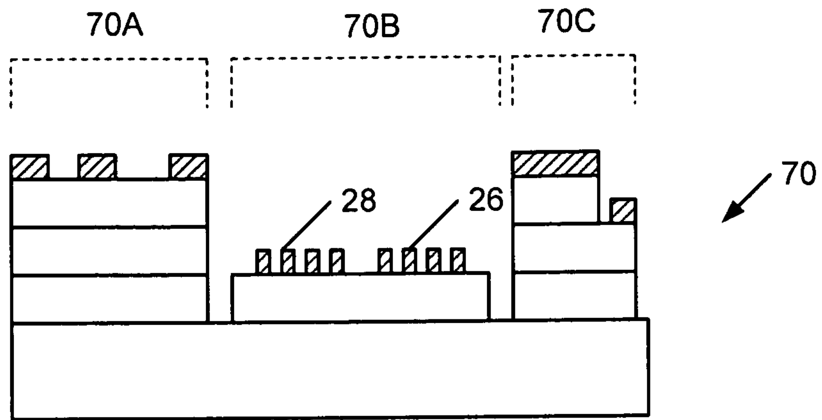

FIG. 7

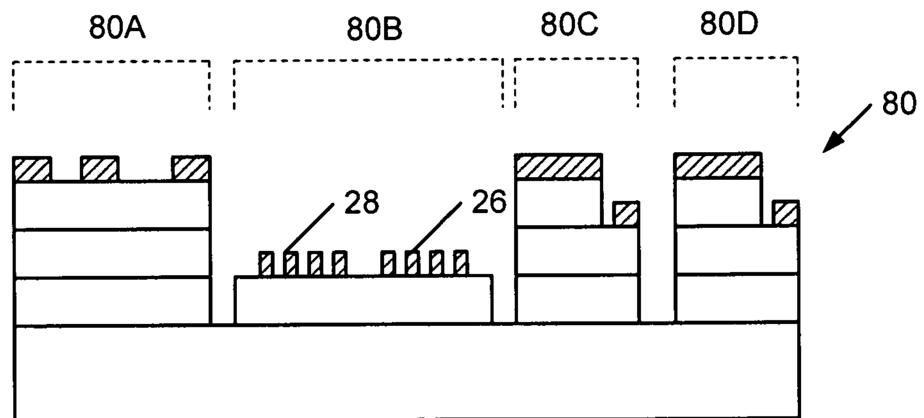

FIG. 8

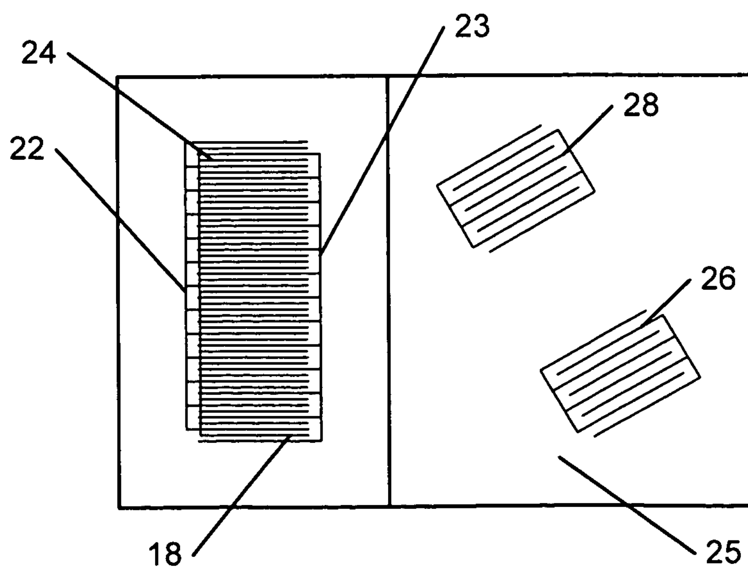

FIG. 9

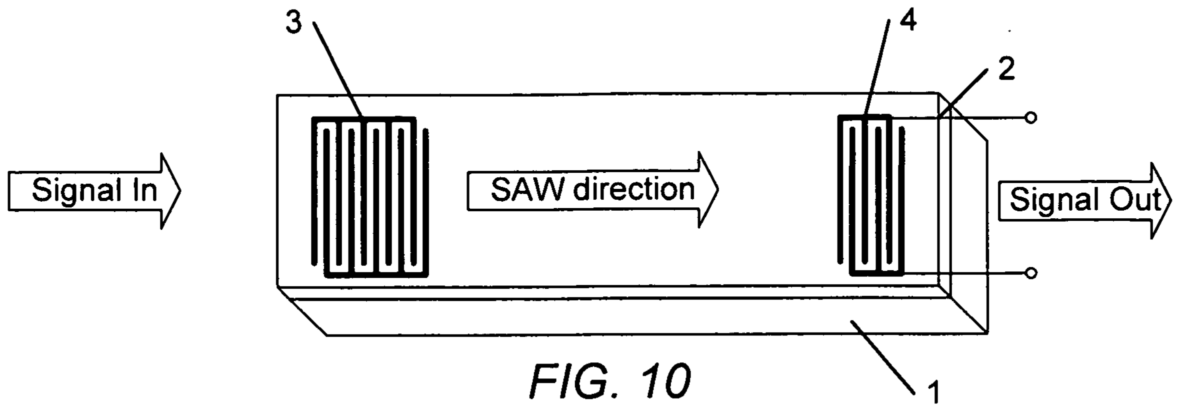

FIG. 10
Prior Art

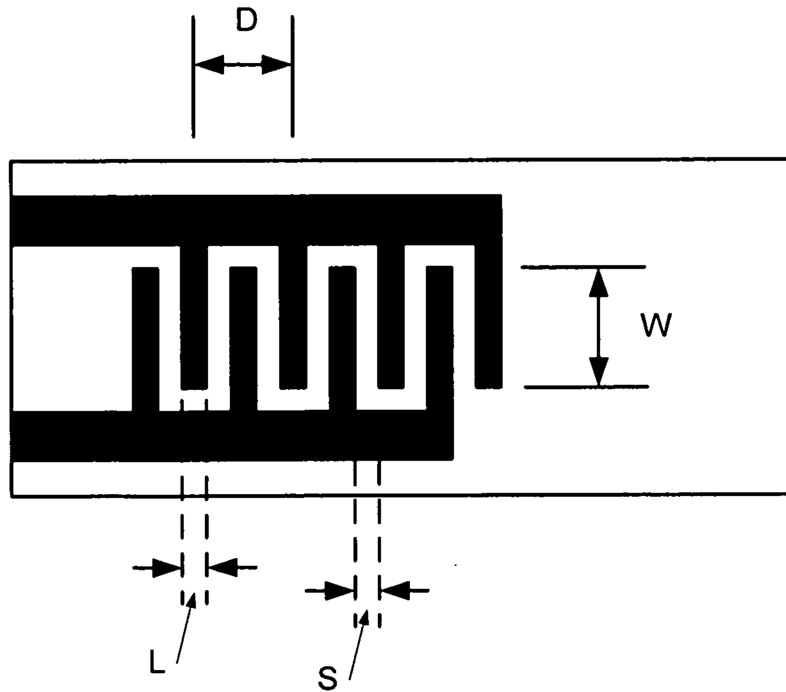

FIG. 11
Prior Art

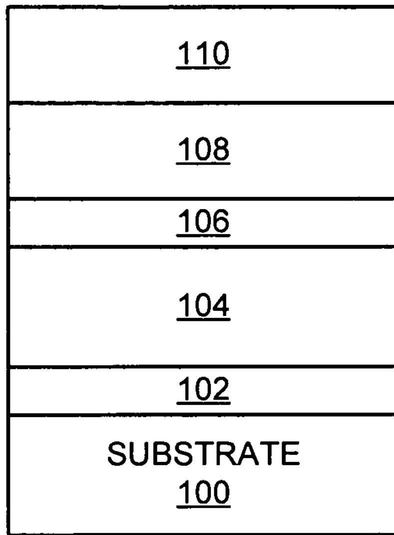

FIGURE 12A

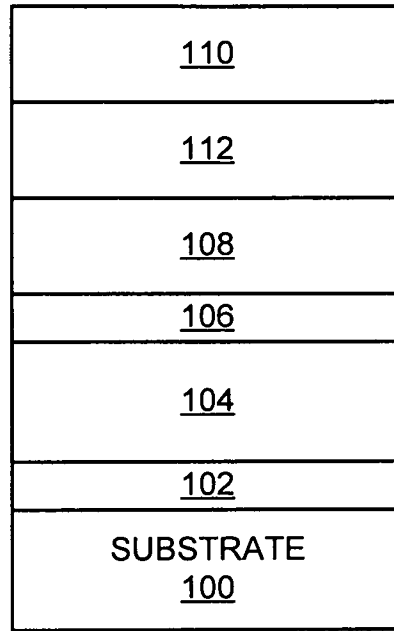

FIGURE 12B

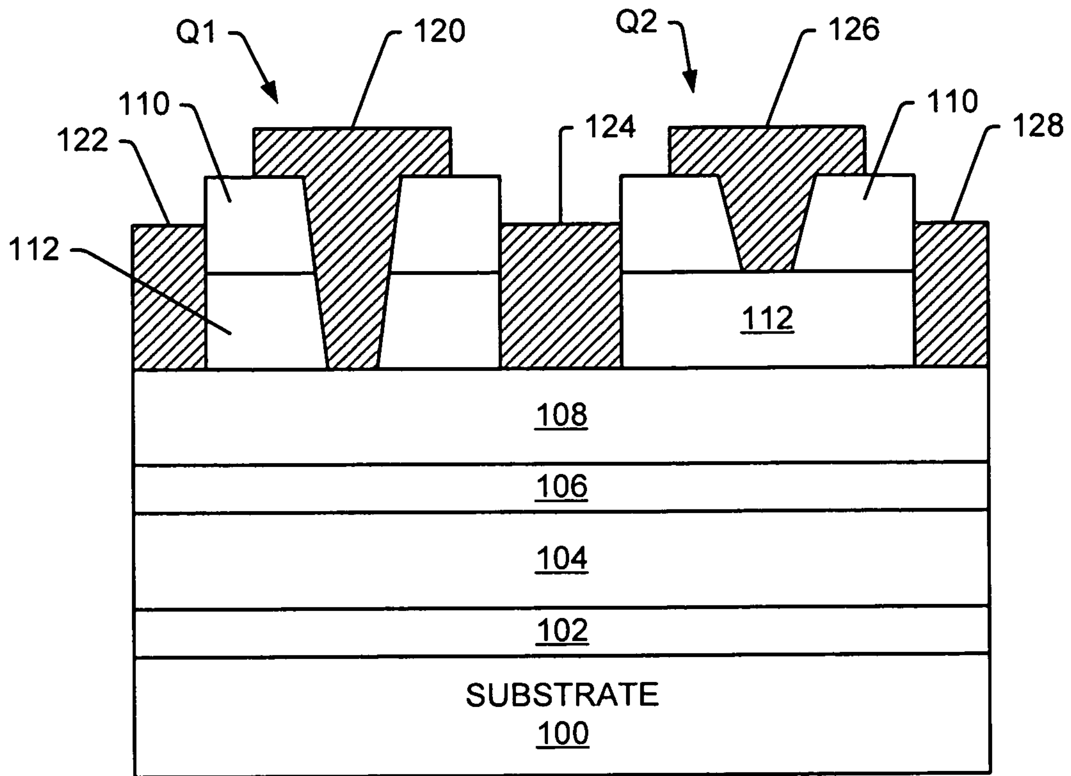

FIGURE 13A

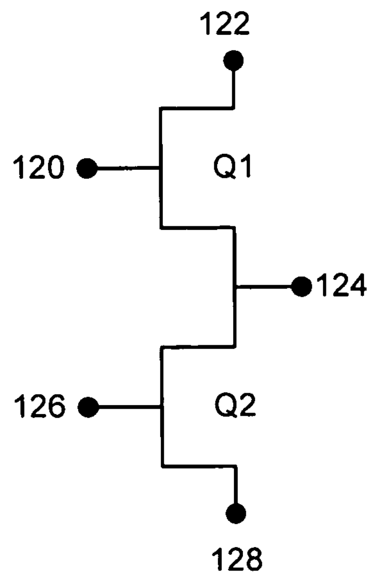

FIGURE 13B

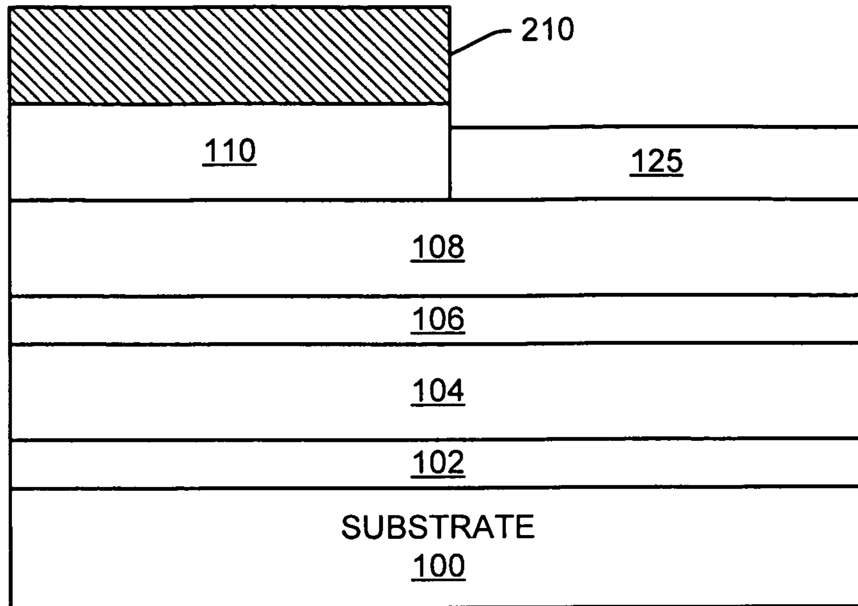

FIGURE 14A

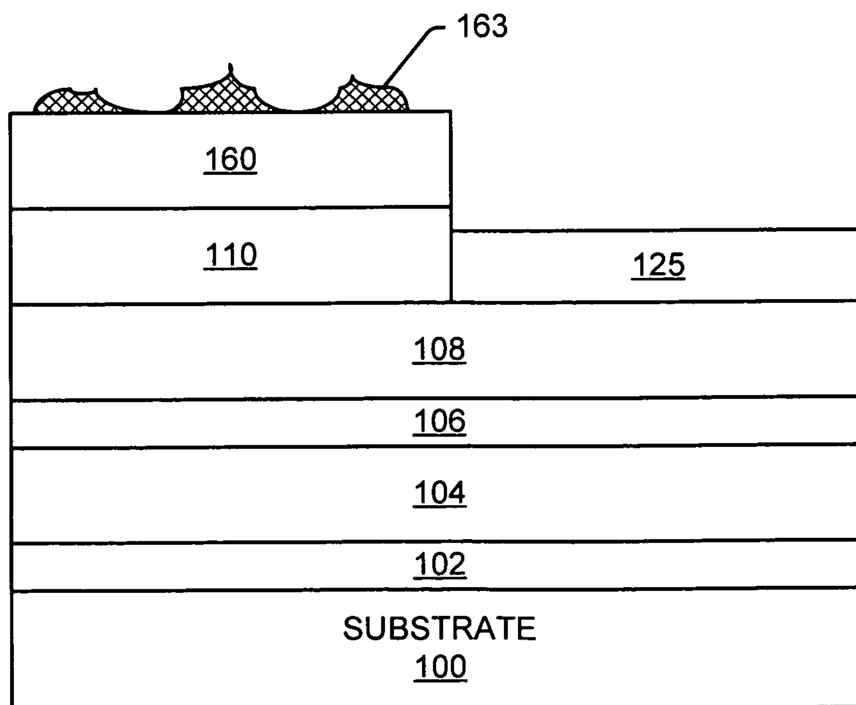

FIGURE 14B

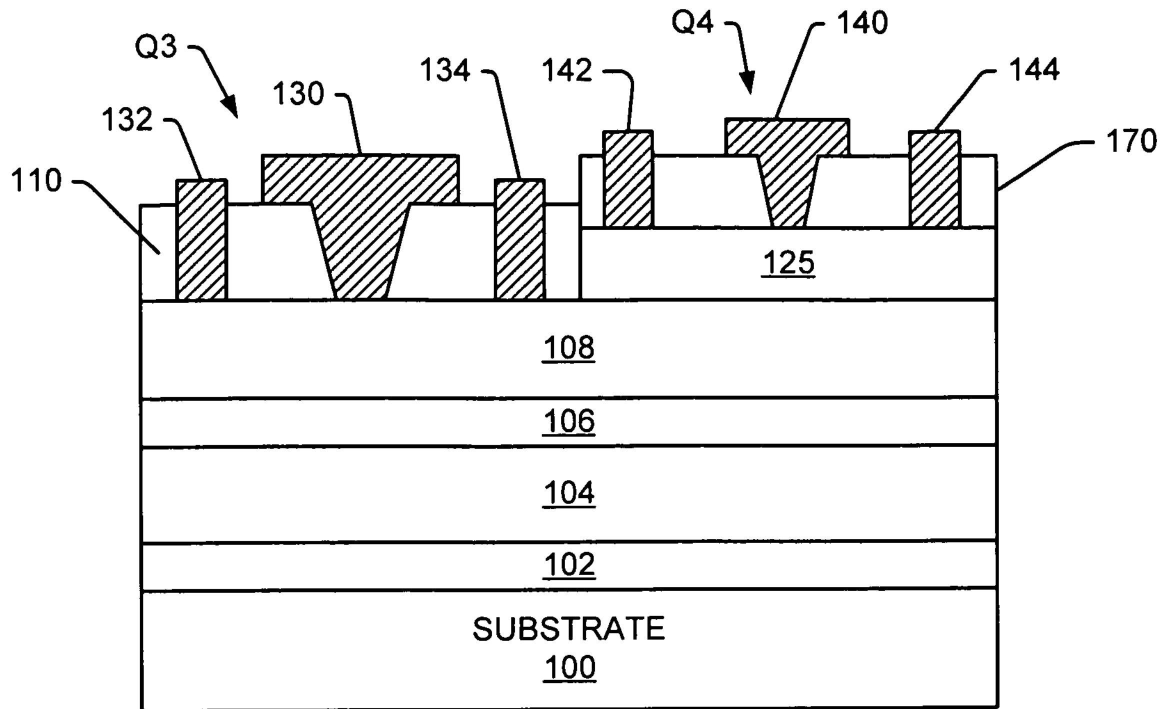

FIGURE 15

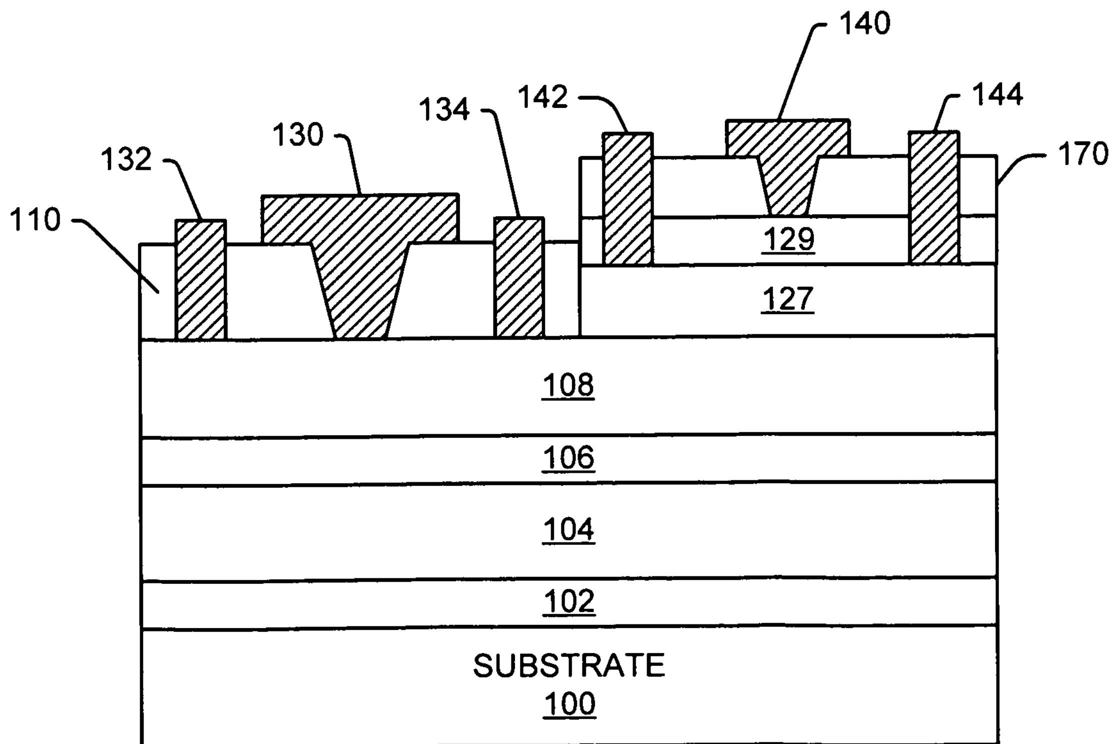

FIGURE 16

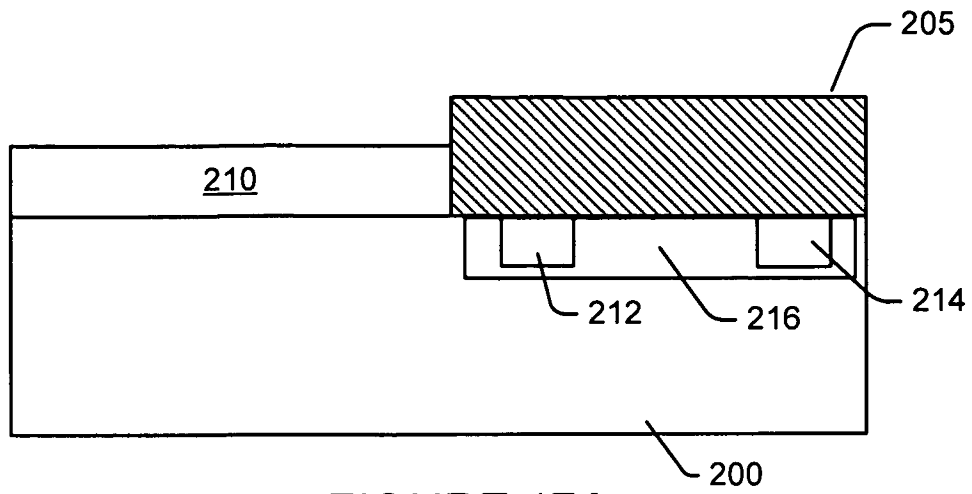

FIGURE 17A

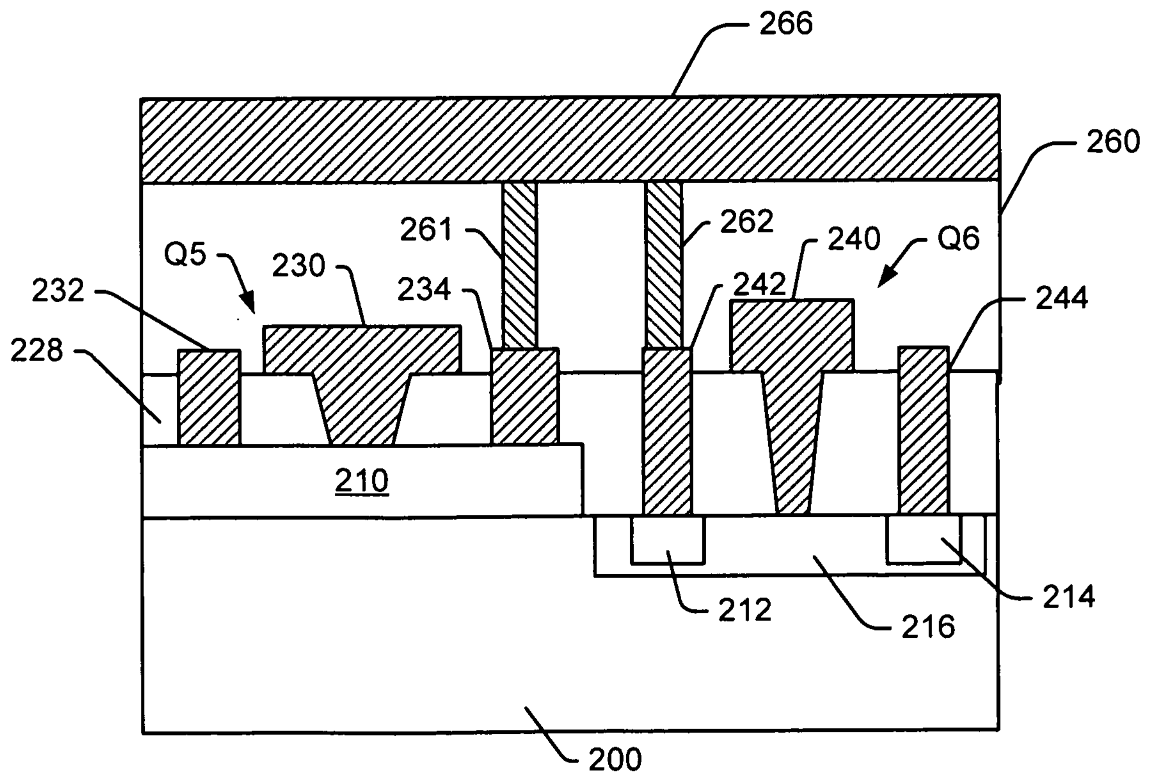

FIGURE 17B

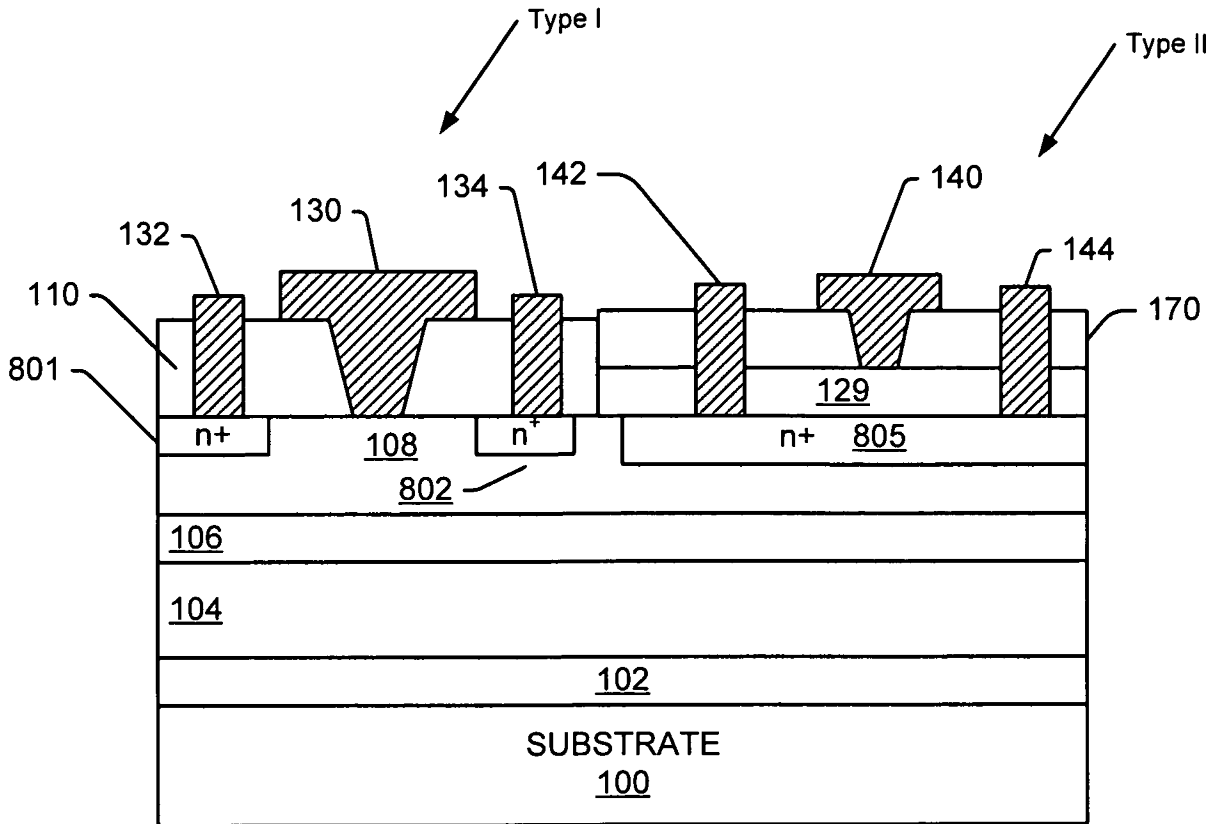

FIGURE 18

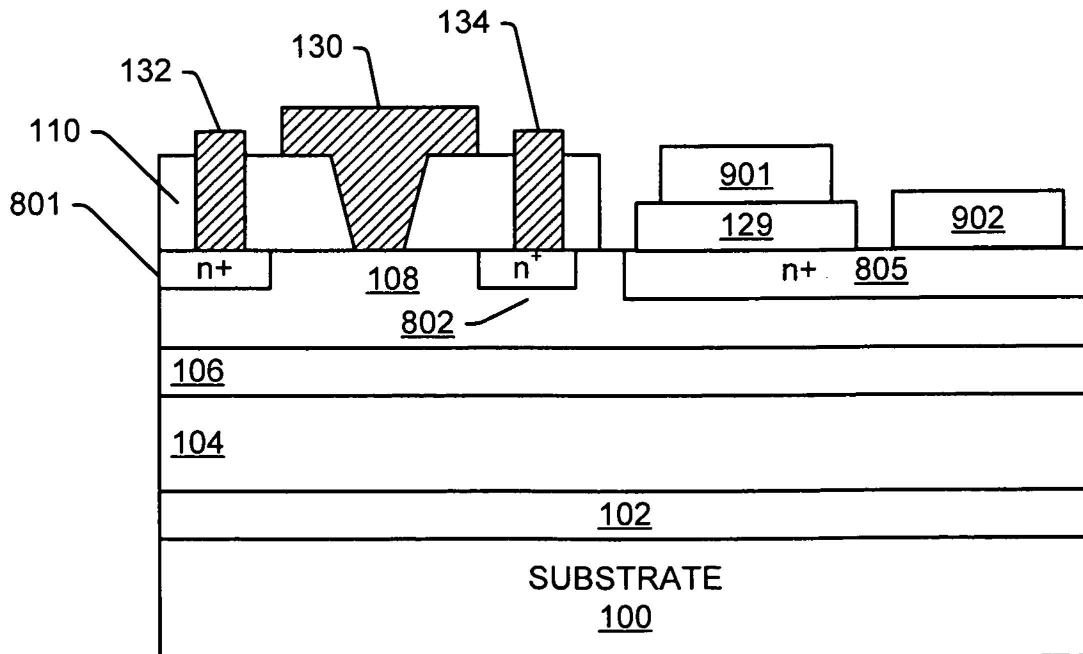

FIGURE 19

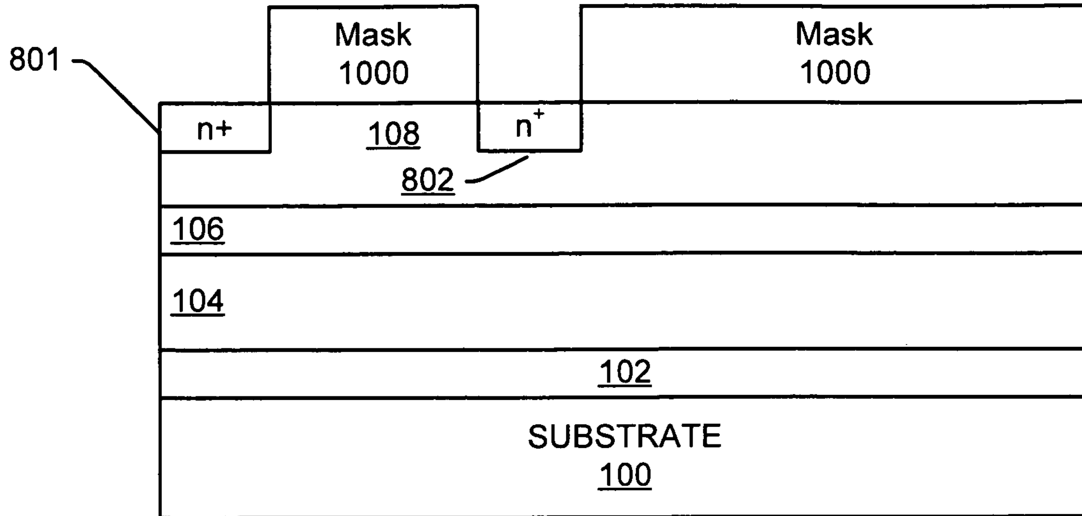

FIGURE 20A

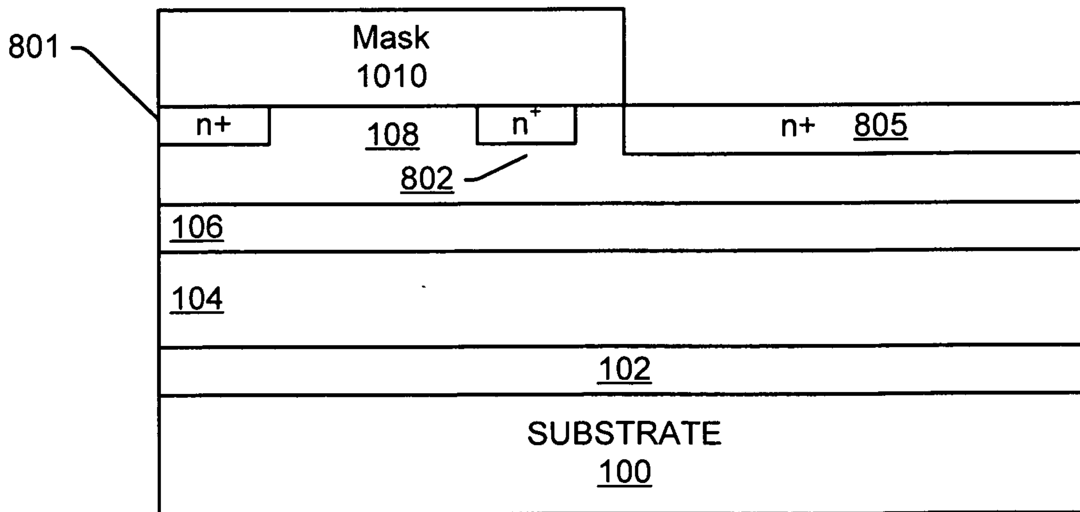

FIGURE 20B

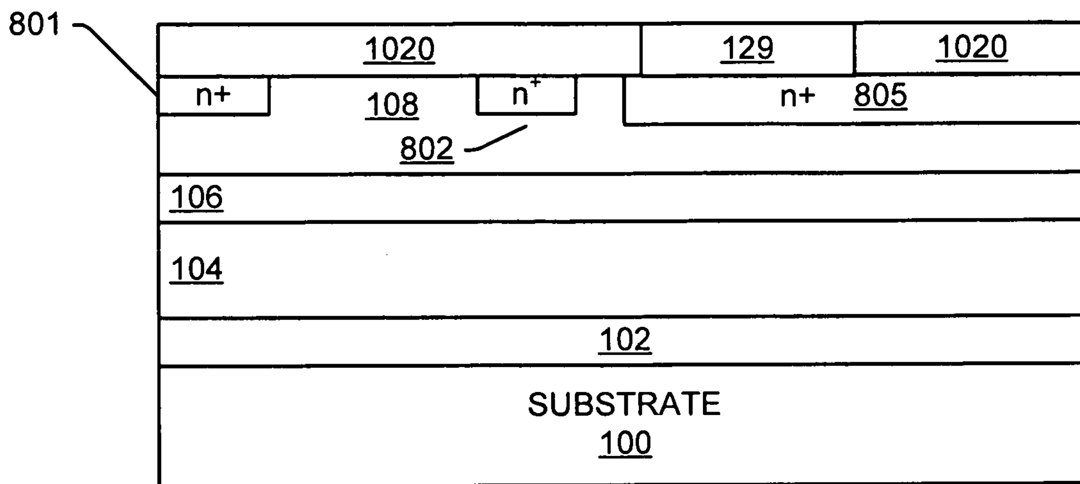

FIGURE 20C

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/000802

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/8252 H01L21/8258 H01L27/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	EP 1 643 561 A (FURUKAWA ELECTRIC CO LTD [JP]) 5 April 2006 (2006-04-05) abstract; claims; figures 2,3 paragraph [0024] - paragraph [0030]	1,2, 9-13,15, 16,19-22
Y	EP 1 798 762 A (CREE INC [US]) 20 June 2007 (2007-06-20) abstract; claims; figures	1,2, 9-13,15, 16,19-22
A	EP 1 734 647 A (MATSUSHITA ELECTRIC IND CO LTD [JP]) 20 December 2006 (2006-12-20) abstract; claims; figures 24-6	1-22
A	US 2006/108660 A1 (UI NORIHIKO [JP]) 25 May 2006 (2006-05-25) abstract; claims; figure 3	1-22

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
26 May 2009	03/06/2009

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Wirner, Christoph

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2009/000802

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WO 2004/079904 A (CREE INC [US]; SAXLER ADAM WILLIAM [US]) 16 September 2004 (2004-09-16) abstract; claims; figures	1-22
A	US 2006/065929 A1 (LEE JAE H [KR] ET AL LEE JAE HOON [KR] ET AL) 30 March 2006 (2006-03-30) abstract; claims; figures	1-22
P,X	US 2008/169474 A1 (SHEPPARD SCOTT T [US]) 17 July 2008 (2008-07-17) abstract; claims; figures	1,14,15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2009/000802

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			US	2007158778	A1	12-07-2007
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