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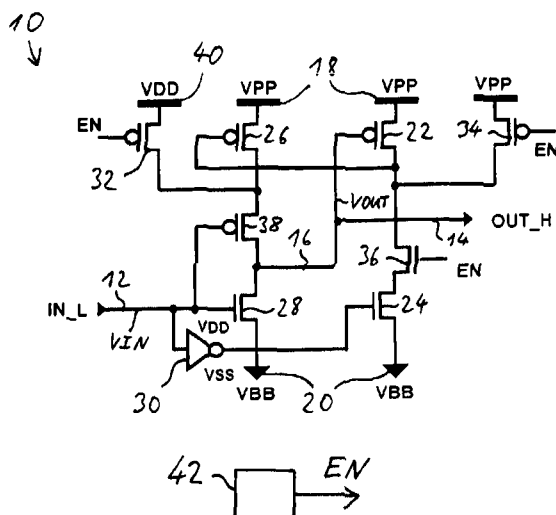
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Fig. 2

(57) Abstract: A voltage level shifter (10) is used to trans-
late a binary input signal (IN_L) representing a binary se-
quence to a binary output signal (OUT_H) representing the
same binary sequence. The input signal is provided by an
input voltage (VIN) varying between a first input voltage
level (VSS) and a second input voltage level (VDD). The
output signal is provided by an output voltage (VOUT)
varying between a first output voltage level (VBB) and a
second output voltage level (VPP). The output signal has a
delay relative to the input signal, and the voltage level
shifter has a leakage current. The voltage level shifter has a
first operating mode and a second operating mode. In the
second operating mode, the delay is shorter while the leak-
age current is higher than in the first operating mode.

Title : Voltage level shifter having a first operating mode and a second operating mode**Description**5 Field of the invention

This invention relates to a voltage level shifter, an apparatus, and a method as described in the accompanying claims.

Background of the invention

10 Voltage level shifters are well-known and described for example in US patents 7,541,837, US 7,501,856 and US 7,567,112. Voltage level shifters serve to translate a binary input signal representing a binary sequence to a binary output signal representing the same binary sequence, with different high/low voltages for the output signal and for the input signal, respectively. The input
15 signal is provided by an input voltage varying between a first input voltage level and a second input voltage level. The output signal is provided by an output voltage varying between a first output voltage level and a second output voltage level, of which at least one is different from the corresponding input voltage level.

Quite generally, the requirement for high frequency and low power of processors, notably for mobile products, often results in complex power management schemes with mixing power
20 domains, supplied by different power supply voltages. A level shifter can be a critical cell, as it participates in timing the critical path. Although in many high performance conditions, voltage levels are usually fairly close and a level shifter may not be required in these conditions, the level shifter is often still included with an impact on the overall delay.

Schematically shown in FIG. 1 is an example of a conventional differential voltage level
25 shifter 10. Level shifter 10 comprises an input port 12 for receiving an input signal IN_L, an output port 14 for delivering a corresponding output signal OUT_H, a node 16, supply voltage providers 18 and 20, PMOS transistors 22 and 26, NMOS transistors 24 and 28, and an inverter 30. PMOS 22 and NMOS 24 form a first pull-up-pull-down-stage 22, 24. PMOS 26 and NMOS 28 form a second pull-up-pull-down-stage 26, 28. Each of the first pull-up-pull-down stage and the second pull-up-pull-down stage has a first state and a second state and is arranged to deliver the first output
30 voltage level VBB when in its first state and the second output voltage level VPP when in its second state. The first pull-up-pull-down stage and the second pull-up-pull-down stage are cross-coupled. Any one of the first pull-up-pull-down stage and the second pull-up-pull-down stage assuming its first state favors the respective other one of the first pull-up-pull-down stage and the second pull-up-pull-down stage to assume its second state. Similarly, any one of the first pull-up-pull-down stage and the second pull-up-pull-down stage assuming its second state favors the
35 respective other one of the first pull-up-pull-down stage and the second pull-up-pull-down stage to assume its first state.

The input signal IN_L is provided by an input voltage VIN which varies between a first input
40 voltage level VSS (low) and a second input voltage level VDD (high). The output signal OUT_H is

provided by an output voltage VOUT which varies between the first output voltage level VBB and the second output voltage level VPP. The binary input signal IN_L represents a binary sequence, and the above mentioned components are coupled to each other in such a manner as to translate the binary input signal IN_L to the binary output signal OUT_H so that both signals represent the same binary sequence, but with the high-low voltage difference being higher (or lower) at the output side than at the input side. The input voltage VIN assuming the first input voltage level VSS causes the first pull-up-pull-down stage 22, 24 to assume its second state and the second pull-up-pull-down stage 26, 28 to assume its first state, whereas the input voltage VIN assuming the second input voltage level (VDD) causes the first pull-up-pull-down stage 22, 24 to assume its first state and the second pull-up-pull-down stage 26, 28 to assume its second state.

More specifically, the level shifter 10 operates as follows. When input voltage VIN is at voltage level VSS (low), NMOS 24 and PMOS 26 are conductive (open) whereas NMOS 28 and PMOS 22 are non-conductive (closed), and the output voltage VOUT which is present at node 16 and at output port 14 is at voltage level VPP (high). In contrast, when the input voltage VIN assumes the voltage level VDD (high), NMOS 28 and PMOS 22 are open while NMOS 24 and PMOS 26 are closed, and the output voltage VOUT assumes the voltage level VBB (low).

The double-stage structure formed of first stage 22, 24 and second stage 26, 28 effectively suppresses leakage currents between the VBB-VPP voltage domain (on the input side) and the VSS-VDD voltage domain (on the output side). On the other hand, it involves a fairly important propagation delay, i.e. a time delay between the output signal OUT_H relative to the input signal IN_L. A leakage current in this context is an electric current that persists when the output voltage VOUT has assumed one of its stationary levels (VBB and VPP). Quite generally, a trade-off often needs to be made between leakage currents and the propagation delay.

Summary of the invention

The present invention provides a voltage level shifter, an apparatus, and a method as described in the accompanying claims.

Specific embodiments of the invention are set forth in the dependent claims.

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

Brief description of the drawings

Further details, aspects and embodiments of the invention will be described, by way of example only, with reference to the drawings. In the drawings, like reference numbers are used to identify like or functionally similar elements. Elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale.

Figure 1 schematically shows an example of an embodiment of a voltage level shifter.

Figure 2 schematically shows an example of another embodiment of a level shifter.

Figure 3 shows a schematic flow chart of an example of an embodiment of a method of operating a voltage level shifter.

Figure 4 schematically represents an experimental input signal and a resulting output signal obtained with a second operating mode.

Figure 5 schematically represents an experimental input signal and a resulting output signal obtained with a first operating mode.

5 Figure 6 schematically represents another experimental input signal and a resulting output signal observed with the second operating mode.

Figure 7 schematically represents another experimental input signal and a resulting output signal obtained with the first operating mode.

10 Figure 8 schematically represents leakage currents observed in the first operating mode and in the second operating mode.

Detailed description of the preferred embodiments

Because the illustrated embodiments of the present invention may, for the most part, be implemented using electronic components and circuits known to those skilled in the art, details will not be explained in any greater extent than that considered necessary, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

Referring to FIG. 2, there is shown a voltage level shifter 10. The level shifter 10 has a first operating mode and a second operating mode. In the second operating mode, the level shifter has a shorter propagation delay, i.e. a shorter delay of the output signal relative to the input signal, but involves a larger leakage current between the two voltage domains, i.e. between the VSS-VDD domain and the VBB-VPP domain. An operating condition can be determined and the first operating mode and the second operating mode can be selected alternatively on the basis of the operating condition.

25 More specifically, the shifter has a first operating mode (low leakage mode) in which the output signal has a first delay relative to the input signal. The level shifter 10 of FIG. 2 differs from the one described above with reference to FIG. 1 at least in that it comprises additional components which interact with the components shown in FIG. 1 to provide a second operating mode (fast mode). In the second operating mode, the output signal has a second delay relative to the input signal, shorter than the first delay. The second operating mode may be selected, for example, when speed (i.e. a short propagation delay) is more desirable than an effective suppression of leakage currents between the two voltage domains connected by the voltage level shifter. In addition to the components discussed above with reference to FIG. 1, the present exemplary level shifter 10 comprises a mode selection unit. In this example, the unit includes switches 32, 34, 36 (in this example three) which are arranged so as to allow selecting between the first operating mode and the second operating mode. Although other configurations may be used, in this example, switches 32, 34, 36 can selectively enable/disable a second input voltage level as alternative to the first voltage level VSS, as explained below in more detail. The level shifter 10 further comprises an additional switch 38 and an additional supply voltage provider 40. Supply voltage provider 40 provides a second input voltage level VDD different from VBB. In the present

example, switches 32, 34, and 38 are PMOS transistors, while switch 36 is an NMOS transistor. PMOS 38 has its source coupled to the drain of PMOS 26 and its drain coupled to the source of NMOS 28, and its gate coupled to the input port 12. PMOS 32 has its source coupled to supply voltage provider 40 and its drain coupled to the drain of PMOS 26. PMOS 34 has its source coupled to supply voltage provider 18 and its drain coupled to the drain of PMOS 22. NMOS 36 has its source coupled to the drain of NMOS 24 and its drain coupled to the drain of PMOS 22.

In the example, switches 32, 34, 36 are responsive to a mode selection voltage (enable voltage) EN. A first level of the mode selection voltage EN sets the voltage level shifter 10 in the first operating mode. A second level of the mode selection voltage EN sets the voltage level shifter 10 in the second operating mode. The gates of transistors 32, 34, and 36 may all be connected to a controller (not shown) for providing alternatively the first level of the mode selection voltage or the second level of the mode selection voltage. In the example, the second and first levels of the mode selection voltage EN are VBB (low) and VPP (high), respectively. In other words, EN=VPP sets the level shifter in the first operating mode, whereas EN=VBB sets the level shifter in the second operating mode.

The voltage level shifter 10 may comprise a detector for determining an operating condition. In such case, the switches 32, 34, 36 select between the first operating mode and the second operating mode on the basis of the operating condition, for example by the controller providing either VBB or VPP depending on the condition. The operating condition may, for example, be one of a bit rate of the input signal, the first input voltage level (VSS), the second input voltage level (VDD), the first output voltage level (VBB), the second output voltage level (VPP), a process corner, a temperature, and any combination thereof, or another suitable operating condition. In the present example, detector 42 determines the operating condition and generates the mode selection voltage EN to provide either VBB or VPP in accordance with the determined operating condition.

The voltage level shifter 10 of this example operates as follows.

When the mode selection voltage EN is set to VPP (high) to select the first operating mode, PMOS transistors 32 and 34 are both closed. NMOS 36 and PMOS 38 may be open or closed, as they are arranged in such a manner that they do not significantly modify the behaviour of the circuit as compared to the one in FIG. 1 (as long as EN=VPP). When the input voltage VIN is VSS (low), transistors 24, 36, 26 and 38 are open, transistors 22 and 28 are closed, and the output voltage VOUT is VPP (high). In contrast, when the input voltage VIN is at VDD (high), transistors 28 and 22 are open, transistors 24 and 26 are closed, and the output voltage VOUT is VBB (low). The state of PMOS 38 is then undefined, which is of no consequence as PMOS 26 and PMOS 32 are both closed. Similarly, the state of NMOS 36 is undefined when VIN=VDD.

The second operating mode is selected by applying the mode selection voltage EN=VBB at the gates of transistors 32, 34, 36. As a consequence, transistors 32 and 34 are open while transistor 36 is closed. Furthermore, PMOS 34 being open, PMOS 26 is closed. The circuit 10 thus reduces to a simple inverter 28, 38 operating at voltage levels VBB (low) and (VDD) high. In the case where VDD is less than VPP, the level shifter 10 thus reduces to a simple inverter 28, 38 which is underdriven with respect to the power supply voltage level VPP. Notably the second pull-

up-pull-down-stage 22, 24 is deactivated. Thus the first pull-up-pull-down stage 22, 24, 38 is not responsive to the second pull-up-pull-down stage 26, 28, and it behaves as an inverter. Compared to the first operating mode, the propagation delay is reduced, while the leakage current between the two voltage domains is increased..

5 The second operating mode may be particularly beneficial when the first input voltage level (VSS) and the first output voltage level (VBB) differ from each other by a value that does not exceed the MOSFET threshold voltage that is characteristic to the specific manufacturing technology. For instance, for the silicon manufacturing technology of 65 nm (bulk), the difference is typically less than 0.2 V, and the second input voltage level (VDD) and the second output voltage
10 level (VPP) might differ from each other by less than 0.2 V, considering the typical power supply voltage at the level of 1.0 V.

Referring now to FIG. 3, there is illustrated in a simplified manner an example of a method of operating a voltage level shifter. Those skilled in the art will recognize that boundaries between the described operations are merely illustrative. The multiple operations may be combined into a single
15 operation, a single operation may be distributed in additional operations and operations may be executed at least partially overlapping in time. Moreover, alternative embodiments may include multiple instances of a particular operation, and the order of operations may be altered in various other embodiments. The voltage level shifter may for example be implemented as a circuit as discussed above with reference to FIG. 2. In the present example, the binary input signal IN_L has
20 a bit rate (measured in bits per seconds) which is detected by a detector. If the detected data rate is found to be a normal data rate (step S1), the first operating mode (low leakage mode) is selected (step S2). When a high data rate is detected (step S3), the second operating mode (fast mode) is selected (step S4). The process may eventually return to step S1.

Referring now to FIG. 4 and 5, there are represented as functions of time t the input voltage
25 VIN (graph 1) which is fed to the input port 12 and a resulting output voltage VOUT (graph 2) obtained at the output port 14 of a specific embodiment of a voltage level shifter 10 of the type described above with reference to FIG. 2. The level shifter 10 was manufactured using 65-nanometer (65nm) silicon manufacturing technology. In both FIGs the input voltage 1 exhibits a falling edge (transition from high to low). The output voltage 2 accordingly exhibits a rising edge
30 (transition from low to high). FIG. 4 relates to the second operating mode (fast mode), whereas FIG. 5 relates to the first operating mode (low leakage mode). I.e., in FIG. 4 the mode selection voltage EN is VBB (low), while in FIG. 5 the mode selection voltage is VPP (high). Comparing FIG. 4 and 5, it is seen that the voltage level shifter has a considerably shorter propagation delay in the fast mode as compared to the low leakage mode.

35 FIGs 6 and 7 are analogous to FIGs 4 and 5, respectively. Graph 1 represents the input voltage while graph 2 represents the resulting output voltage, as functions of time t . Now the input voltage 1 exhibits a rising edge, while the output voltage 2 exhibits a corresponding falling edge. FIG. 6 refers to the second operating mode (fast mode), while FIG. 7 refers to the first operating mode (full contention mode). FIGs 6 and 7 show that in the event of a rising edge in the input
40 signal, the delay of the corresponding falling edge in the output signal is about equal for both

operating modes. This is explained by the fact that in the low leakage mode the level shifter circuit 10 as shown in FIG. 2 has a certain asymmetry due to the fact that the first pull-up-pull-down-stage 22, 24 receives the inverted (by inverter 30) and thus delayed input signal, whereas the second pull-up-pull-down-stage 26, 38 receives the input signal directly.

5 Finally, referring to FIG. 8, there are plotted leakage currents 3, 4, and 5 observed as functions of time during the interval between a falling edge and the subsequent rising edge in the input voltage V_{IN} . Currents 3 and 4 were observed at the high potential provider 18 and at the low potential provider 20, respectively, for the second operating mode (fast mode). Current 5 was observed in the first operating mode. The fast mode clearly involves a substantially higher leakage
10 current as compared to the low leakage mode. In these exemplary experiments based on 65nm silicon manufacturing technology, a propagation delay of 0.59 ns/ 0.65 ns was observed in the fast mode compared to 0.6 ns/1.5 ns in the normal mode. A leakage current of 11.1 μA was observed in the fast mode compared to only 6 nA in the normal mode.

The voltage level shifter 10 as described above with reference to FIG. 2 may also be
15 integrated in an apparatus which comprises

a first logic domain for providing an input voltage (V_{IN}) varying between a first input voltage level (V_{SS}) and a second input voltage level (V_{DD}) to represent a binary sequence,

the voltage level shifter 10, for receiving, as an input signal, the input voltage (V_{IN}) and for generating, as an output signal, an output voltage (V_{OUT}) varying between a first output voltage
20 level (V_{BB}) and a second output voltage level (V_{PP}) to represent the same binary sequence,

a second logic domain for processing the binary sequence on the basis of the output voltage (V_{OUT}).

In the foregoing specification, the invention has been described with reference to specific examples of embodiments of the invention. It will, however, be evident that various modifications
25 and changes may be made therein without departing from the broader spirit and scope of the invention as set forth in the appended claims. For example, a separate inverter could be used to provide the second operating mode.

The switches as discussed herein may be any kind of switch suitable to couple an element of an electronic circuit to another element of the same or different circuit. Although in the
30 embodiments discussed above, the switches are PMOS and NMOS transistors, they may be implemented differently. For instance, a PMOS transistor may be replaced by an NMOS transistor and vice versa. Alternatively, a switch may be implemented as a bipolar transistor, photodiode, cathode ray tube, or any other suitable control element.

The connections as discussed herein may be any type of connection suitable to transfer
35 signals from or to the respective nodes, units or devices, for example via intermediate devices. Accordingly, unless implied or stated otherwise, the connections may for example be direct connections or indirect connections. The connections may be illustrated or described in reference to being a single connection, a plurality of connections, unidirectional connections, or bidirectional connections. However, different embodiments may vary the implementation of the connections.
40 For example, separate unidirectional connections may be used rather than bidirectional

connections and vice versa. Also, a plurality of connections may be replaced with a single connections that transfers multiple signals serially or in a time multiplexed manner. Likewise, single connections carrying multiple signals may be separated out into various different connections carrying subsets of these signals. Therefore, many options exist for transferring signals.

5 Although specific conductivity types or polarity of potentials have been described in the examples, it will appreciated that conductivity types and polarities of potentials may be reversed.

Each signal described herein may be designed as positive or negative logic. In the case of a negative logic signal, the signal is active low where the logically true state corresponds to a logic level zero. In the case of a positive logic signal, the signal is active high where the logically true state corresponds to a logic level one. Note that any of the signals described herein can be designed as either negative or positive logic signals. Therefore, in alternate embodiments, those signals described as positive logic signals may be implemented as negative logic signals, and those signals described as negative logic signals may be implemented as positive logic signals.

10 Furthermore, the terms "assert" or "set" and "negate" (or "deassert" or "clear") are used herein when referring to the rendering of a signal, status bit, or similar apparatus into its logically true or logically false state, respectively. If the logically true state is a logic level one, the logically false state is a logic level zero. And if the logically true state is a logic level zero, the logically false state is a logic level one.

15 Any arrangement of components to achieve the same functionality is effectively "associated" such that the desired functionality is achieved. Hence, any two components herein combined to achieve a particular functionality can be seen as "associated with" each other such that the desired functionality is achieved, irrespective of architectures or intermedial components. Likewise, any two components so associated can also be viewed as being "operably connected," or "operably coupled," to each other to achieve the desired functionality.

20 Also for example, the examples, or portions thereof, may implemented as soft or code representations of physical circuitry or of logical representations convertible into physical circuitry, such as in a hardware description language of any appropriate type.

25 However, other modifications, variations and alternatives are also possible. The specifications and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

30 In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word 'comprising' does not exclude the presence of other elements or steps then those listed in a claim. Furthermore, the terms "a" or "an," as used herein, are defined as one or more than one. Also, the use of introductory phrases such as "at least one" and "one or more" in the claims should not be construed to imply that the introduction of another claim element by the indefinite articles "a" or "an" limits any particular claim containing such introduced claim element to inventions containing only one such element, even when the same claim includes the introductory phrases "one or more" or "at least one" and indefinite articles such as "a" or "an." The same holds true for the use of definite articles. Unless stated otherwise, terms such as "first" and "second" are used to arbitrarily distinguish between the elements such terms describe. Thus, these terms are

not necessarily intended to indicate temporal or other prioritization of such elements. The mere fact that certain measures are recited in mutually different claims does not indicate that a combination of these measures cannot be used to advantage.

Claims

- 5 1. A voltage level shifter (10) for translating a binary input signal (IN_L) representing a binary sequence to a binary output signal (OUT_H) representing the same binary sequence, wherein the voltage level shifter (10) comprises
- an input port (12) for receiving the input signal in the form of an input voltage (VIN) varying between a first input voltage level (VSS) and a second input voltage level (VDD),
- 10 an output port (14) for providing the output signal in the form of an output voltage (VOUT) varying between a first output voltage level (VBB) and a second output voltage level (VPP), and
- a mode selection unit (32, 34, 36) for selecting between a first operating mode and a second operating mode, wherein in the second operating mode a delay of the output signal relative to the input signal is shorter and a leakage current is higher than in the first operating mode.
- 15 2. The voltage level shifter (10) as set forth in claim 1, wherein the mode selection unit comprises one or more switches (32, 34, 36) for selecting alternatively the first operating mode and the second operating mode.
- 20 3. The voltage level shifter (10) as set forth in claim 1 or 2, wherein the mode selection unit (32, 34, 36) is responsive to a mode selection voltage (EN), a first level of the mode selection voltage setting the voltage level shifter in the first operating mode and a second level of the mode selection voltage setting the voltage level shifter in the second operating mode.
- 25 4. The voltage level shifter (10) as set forth in claim 1, 2, or 3, wherein the voltage level shifter (10) further comprises a detector (42) for determining an operating condition and the mode selection unit (32, 34, 36) is arranged to select alternatively the first operating mode and the second operating mode on the basis of the operating condition.
- 30 5. The voltage level shifter (10) as set forth in any one of claims 1 to 4, wherein the operating condition is one or more of the group consisting of: a bit rate of the input signal, the first input voltage level (VSS), the second input voltage level (VDD), the first output voltage level (VBB), the second output voltage level (VPP), a process corner, a temperature, and any combination thereof.
- 35 6. The voltage level shifter (10) as set forth in any one of claims 1 to 5, comprising a first pull-up-pull-down stage (22, 24) and a second pull-up-pull-down stage (26, 28), wherein each of the first pull-up-pull-down stage and the second pull-up-pull-down stage has a first state and a second state and is arranged to deliver the first output voltage level (VBB) when in its first state and the second output voltage level (VPP) when in its second state, and the first pull-up-pull-down stage
- 40 and the second pull-up-pull-down stage are cross-coupled.

7. The voltage level shifter (10) as set forth in claim 6, wherein any one of the first pull-up-pull-down stage and the second pull-up-pull-down stage assuming its first state favors the respective other one of the first pull-up-pull-down stage and the second pull-up-pull-down stage to assume its second state.

8. The voltage level shifter (10) as set forth in claim 7, wherein any one of the first pull-up-pull-down stage and the second pull-up-pull-down stage assuming its second state favors the respective other one of the first pull-up-pull-down stage and the second pull-up-pull-down stage to assume its first state.

9. The voltage level shifter (10) as set forth in any one of claims 6 to 8, wherein in the first operating mode the input voltage (VIN) assuming the first input voltage level (VSS) causes the first pull-up-pull-down stage (22, 24) to assume its second state and the second pull-up-pull-down stage (26, 28) to assume its first state whereas the input voltage (VIN) assuming the second input voltage level (VDD) causes the first pull-up-pull-down stage (22, 24) to assume its first state and the second pull-up-pull-down stage (26, 28) to assume its second state.

10. The voltage level shifter (10) as set forth in any one of claims 6 to 9, wherein in the second operating mode, the first pull-up-pull-down stage (22, 24, 38) is not responsive to the second pull-up-pull-down stage (26, 28) and behaves as an inverter.

11. The voltage level shifter (10) as set forth in any one of the preceding claims, wherein the voltage level shifter (10), when in the second operating mode, behaves as one of an inverter and a conductor.

12. An apparatus comprising

a first logic domain for providing an input voltage (VIN) varying between a first input voltage level (VSS) and a second input voltage level (VDD) to represent a binary sequence,

a voltage level shifter (10) as set forth in any one of claims 1 to 11, for receiving, as an input signal, the input voltage (VIN) and for generating, as an output signal, an output voltage (VOUT) varying between a first output voltage level (VBB) and a second output voltage level (VPP) to represent the same binary sequence, and

a second logic domain for processing the binary sequence on the basis of the output voltage (VOUT).

13. The apparatus as set forth in claim 12, wherein the first input voltage level (VSS) and the first output voltage level (VBB) differ from each other by less than 0.2 V, and the second input voltage level (VDD) and the second output voltage level (VPP) differ from each other by less than 0.2 V.

14. A method of operating a voltage level shifter (10), comprising

operating the voltage level shifter (10) in a first operating mode in which a binary input signal (IN_L) representing a binary sequence is translated to a binary output signal (OUT_H) representing the same binary sequence, the input signal is provided by an input voltage (VIN) varying between a first input voltage level (VSS) and a second input voltage level (VDD), the output signal is provided by an output voltage (VOUT) varying between a first output voltage level (VBB) and a second output voltage level (VPP), the output signal has a delay relative to the input signal, and a leakage current occurs in the voltage level shifter (10); and

operating the voltage level shifter (10) in a second operating mode in which a binary input signal (IN_L) representing a binary sequence is translated to a binary output signal (OUT_H) representing the same binary sequence, the input signal is provided by an input voltage (VIN) varying between the first input voltage level (VSS) and the second input voltage level (VDD), the output signal is provided by an output voltage (VOUT) varying between the first output voltage level (VBB) and the second output voltage level (VPP), the output signal has a delay relative to the input signal shorter than in the first operating mode, and a leakage current which is higher than in the first operating mode occurs in the voltage level shifter (10).

15. The method as set forth in claim 14, further comprising

determining an operating condition and selecting alternatively the first operating mode and the second operating mode on the basis of the operating condition.

Fig. 1

Prior Art

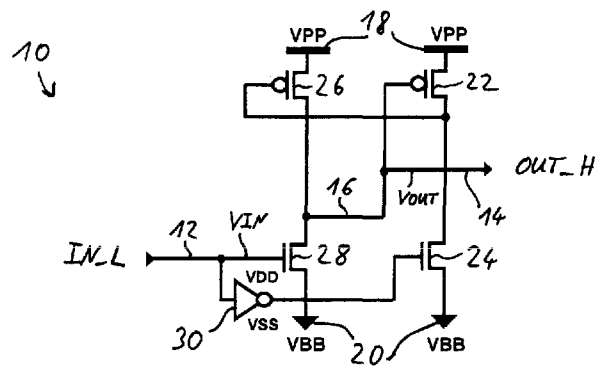


Fig. 2

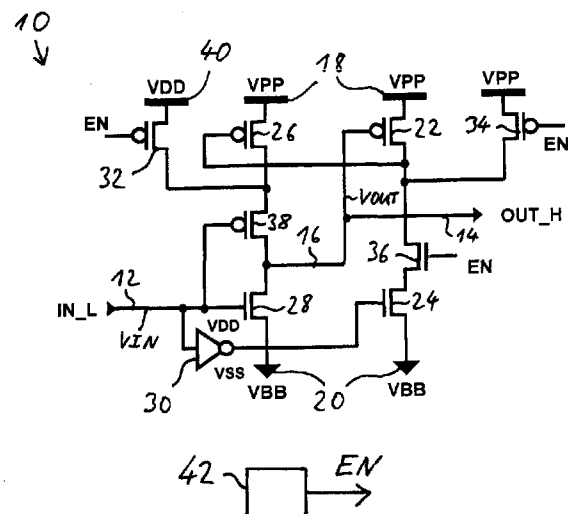


Fig. 3

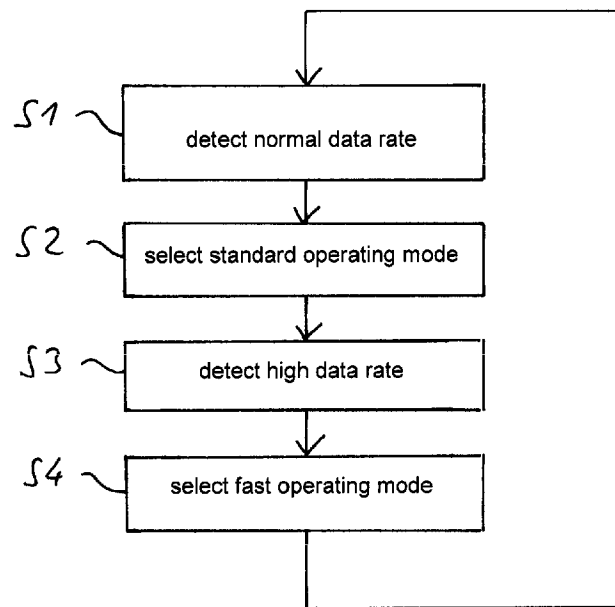


Fig. 4

$EN = 0$

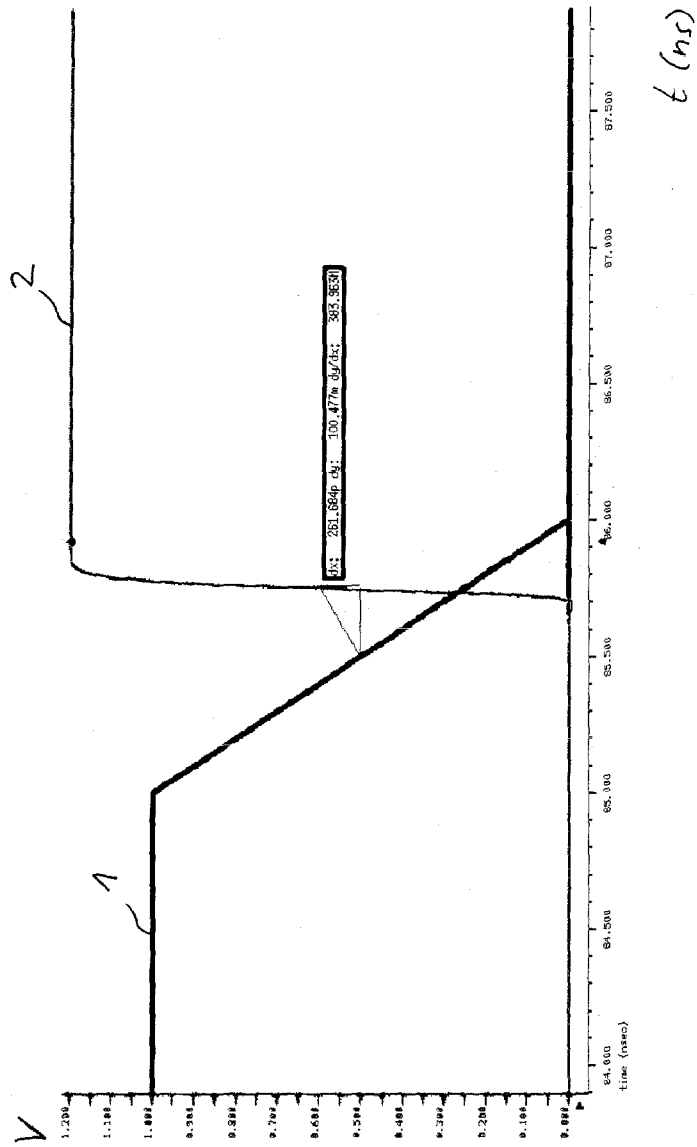


Fig. 5
 $EN = 1$

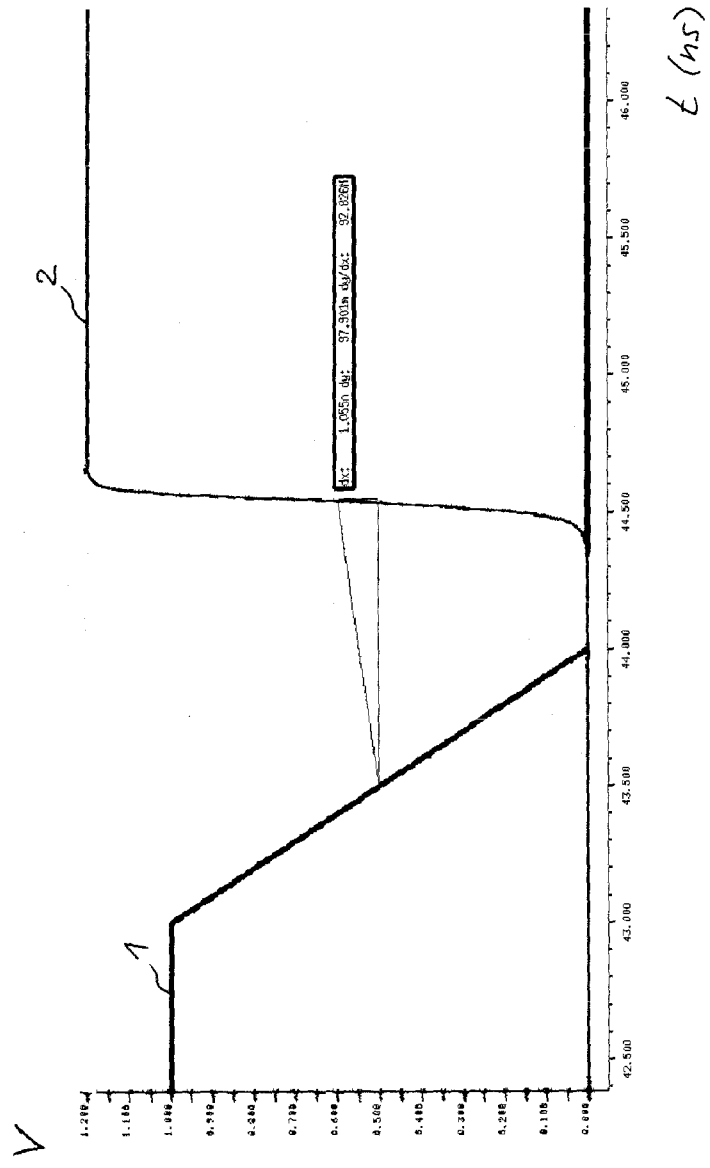


Fig. 6

$EN=0$

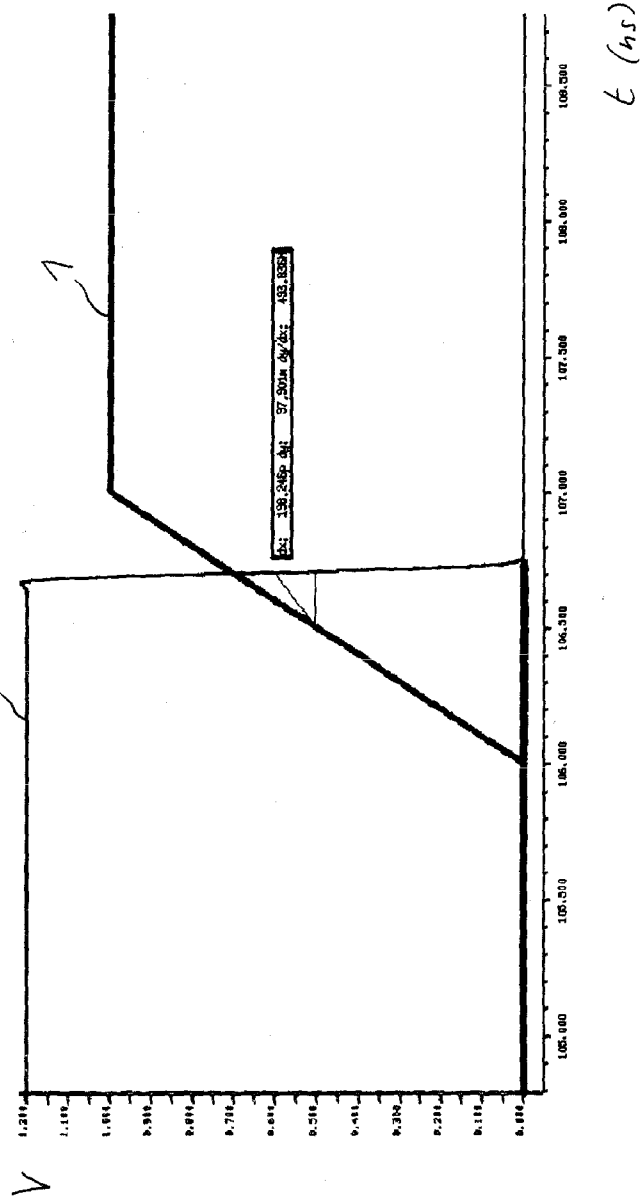


Fig. 7

EN=1

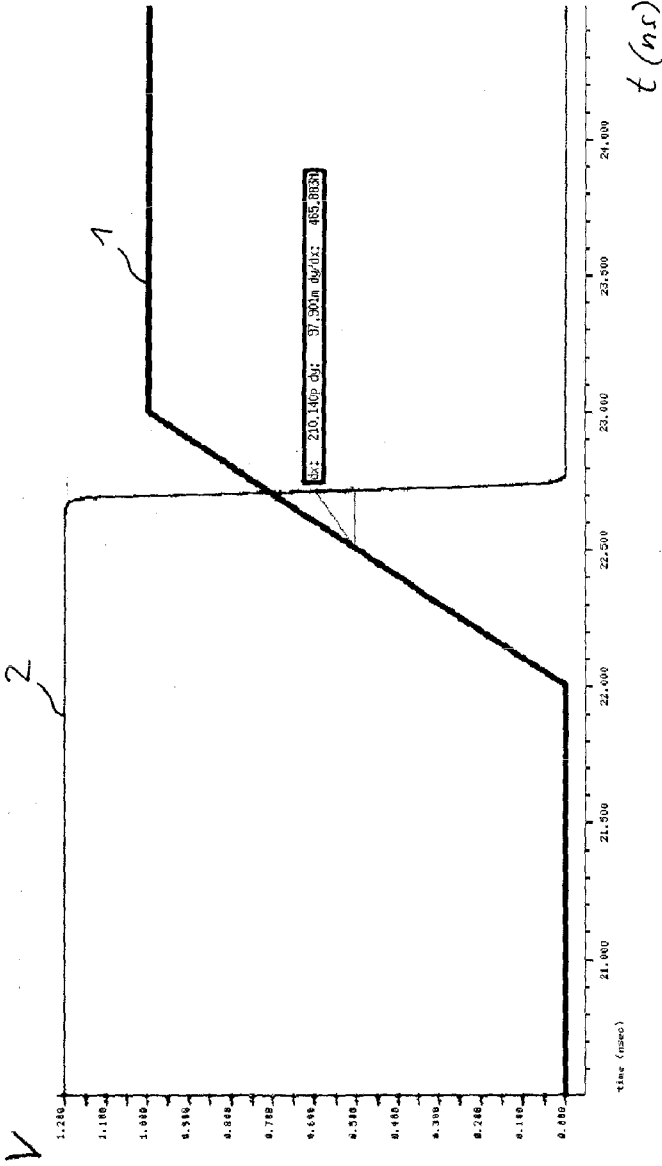
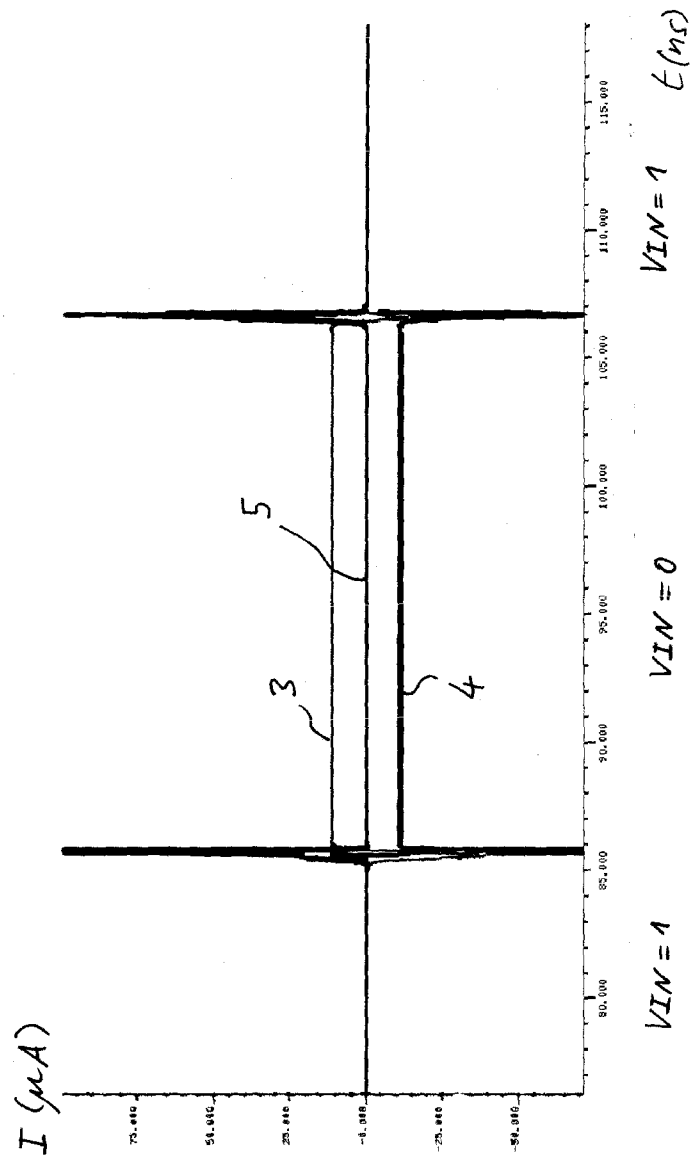


Fig. 8



INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2010/051766**A. CLASSIFICATION OF SUBJECT MATTER*****H03K 19/0185(2006.01)i***

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03K 19/0185; H03K 19/0175; H03K 19/00; H03K 19/0948

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: level shifter, delay, voltage level

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2006-054886 A (SAMSUNG ELECTRONICS CO LTD) 23 February 2006 See abstract; para.24-47; claims 1, 8 and figures 1-2.	1-15
A	JP 2004-222272 A (SAMSUNG ELECTRONICS CO LTD) 05 August 2004 See abstract; claim 1 and figure 2.	1-15
A	KR 10-2005-0015062 A (SAMSUNG ELECTRONICS CO LTD) 21 February 2005 See abstract; claim 1 and figure 2.	1-15
A	KR 10-2006-0134313 A (SAMSUNG ELECTRONICS CO LTD) 28 December 2006 See abstract; claims 1, 3-4 and figure 5.	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search

20 JANUARY 2011 (20.01.2011)

Date of mailing of the international search report

21 JANUARY 2011 (21.01.2011)

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/IB2010/051766

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