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(54) Title: INTEGRATED MASK

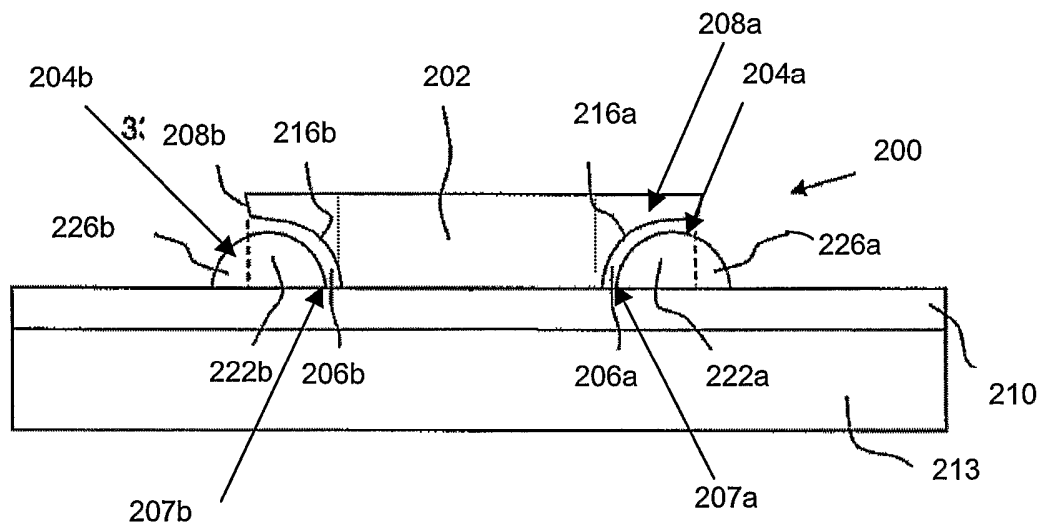


FIG. 2

(57) Abstract: An integrated mask structure (200) for a substrate (213), the structure comprising a pillar structure (202) formed on the substrate, and at least one gap structure (206a,b) extending along the pillar structure, wherein a portion of a wall surface (207a,b) of each gap structure is not in a line of sight from outside of the gap structure, said portion of the wall surface extending along the pillar structure. The gap structure reduces the occurrence of shorting between electrodes deposited using the integrated mask. The mask may be used in the manufacture of OLED devices, flat panel displays, photo-detector arrays and micro-electro-mechanical (MEMS) systems.

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Integrated Mask

FIELD OF INVENTION

5 The present invention relates broadly to an integrated mask structure for a substrate, to a method of fabricating an integrated mask structure for a substrate, and to a multi-layered device structure.

10 BACKGROUND

Deposition processes such as chemical vapour deposition (CVD) and physical vapour deposition (PVD) such as thermal evaporation and sputtering are commonly used in manufacturing industries for fabricating devices that require different layers of materials to be deposited. Typical devices fabricated using these deposition processes
15 include Organic Light Emitting Displays (OLEDs).

OLEDs are electroluminescent (EL) devices that emit light generated by radiative recombination of injected electrons and holes within one or more organic EL layers of the OLEDs. The typical construction of OLED displays comprises first forming anode strips on a substrate and then depositing one or more organic layers on top of
20 the anode strips. The cathode strips are then formed on top of the organic layers.

The anode strips are typically formed by using conventional photolithography and wet etching processes. The organic layers are then deposited on top of the anode strips. However, the cathode strips cannot be patterned using the same methods for the anode strips due to the fact that the developer and etching solutions, used for patterning
25 the anode strips, would cause damage to the underlying organic compounds if used for patterning the cathode strips.

To avoid the damage to the organic compounds, instead of "external" masks, integrated masks may be utilised during fabrication of an OLED. The integrated mask typically allows the organic and electrode layers to be automatically patterned.

30 A simple implementation of an integrated mask utilises a series of parallel walls formed by photolithography prior to deposition of an organic EL layer such that

photolithographic patterning or wet chemistry steps are not required after the organic EL layer has been deposited. To achieve a deposition pattern of cathode strips, the deposition surface is positioned such that each of the parallel walls is disposed between the source of metal to be deposited. Therefore, in such an orientation, metal deposition occurs only on one side of each wall, whereas on the other side of each wall no deposition occurs due to a shadowing effect. One limitation of this technique is that the technique typically requires an extreme, off-axis deposition angle. Off-axis deposition is defined as deposition of a material from an angle not perpendicular to the substrate. Thus, this technique is not viable for mass production where moving conveyor belts or rotators are frequently used.

One variation of the simple implementation of integrated masks using parallel walls, a typical design of an integrated mask 100 utilising a series of pillars, for example 102, with retrograde profiles is illustrated in FIG. 1. The pillar 102 serves as a separator for automatic patterning of cathode layers, 106 and 108. The insulating base layer 110 is required to prevent shorting between the cathode layers, 106 and 108, and anode layer 112 in regions where the organic layers, for example 104, are typically absent (or thin) as a consequence of unavoidable shadowing by the pillar 102 during deposition of the organic layers, for example 104.

The retrograde angle of the pillar 102 must typically ensure that the material of cathode layers, 106 and 108, does not coat the sides 114 of the pillar 102 forming a layer 115 sufficiently thick and continuous to electrically connect across the pillar 102, which would short adjacent rows of fabricated strips of cathode layers, 106 and 108. The required profile of the pillar 102 is typically dependent on the relative orientation of the cathode deposition source to the substrate 116. Therefore, although the retrograde pillar 102 may not require off-axis deposition as mentioned in the previous technique, the pillar 102 is still dependent on the deposition angle of the source since there are still instances where the deposition angle may cause shorts of adjacent strips of cathode layers, 106 and 108. In addition, if the deposition process produces excess scattering and is thus insufficiently unidirectional, the residual layers 115 on the sides 114 of the pillar 102 may become continuous and be electrically connected across the integrated mask 100 via top layer 118. Therefore, an electrical short may occur between cathode layers, 106 and 108, due to deposition processes that are not sufficiently unidirectional. To avoid shorting problems with typical integrated masks, materials and deposition processes are typically limited to those producing relatively

smaller scattering effects. For example, indium tin oxide (ITO) patterning in top-emitting OLEDs is typically hardly performed with such integrated masks as CVD or sputtering is required.

5 SUMMARY

In accordance with a first aspect of the present invention there is provided an integrated mask structure for a substrate, the structure comprising a pillar structure formed on the substrate, and at least one gap structure extending along the pillar structure, wherein a portion of a wall surface of each gap structure is not in a line of sight from outside of the gap structure, said portion of the wall surface extending along the pillar structure.

The pillar structure may comprise one or more pillar elements formed on the substrate, each pillar element having at least one retrograde side surface extending along the first direction; one or more barrier elements formed on the substrate, each barrier element being adjacent one of the retrograde side surfaces of one pillar element, wherein the gap structure is defined between the barrier elements and the respective adjacent retrograde side surfaces.

The gap structure may extend between the barrier elements and the respective adjacent retrograde side surfaces to a surface portion of the substrate.

The barrier elements may have a cross-sectional shape of one of a group consisting of a semi-circle, a partial ellipse, and a rectangle.

The retrograde surfaces may have respective cross-sectional shapes of one of a group consisting of an inverted semi-circle, an inverted partial ellipse, and an inverted rectangle.

The pillar structure may extend on the substrate in a direction perpendicular to one or more contact stripes to be formed on the substrate.

A width of the gap structure may be in a range from about 1 to 8 μ m. The width of the gap structure may be in a range from about 2 to 5 μ m.

In accordance with a second aspect of the present invention there is provided a method of fabricating an integrated mask structure for a substrate, the method comprising forming a pillar structure on the substrate, and forming at least one gap structure extending along the pillar structure, wherein a portion of a wall surface of each gap structure is not in a line of sight from outside of the gap structure, said portion of the wall surface extending along the pillar structure.

The method may comprise forming one or more pillar elements of the pillar structure on the substrate, each pillar member having at least one retrograde side surface; forming one or more barrier elements of the pillar structure on the substrate, each barrier element being adjacent one of the retrograde side surfaces of one pillar element, such that the gap structure is defined between the barrier elements and the respective adjacent retrograde side surfaces.

The gap structure may extend between the barrier elements and the respective adjacent retrograde side surfaces to a surface portion of the substrate.

The barrier elements may have a cross-sectional shape of one of a group consisting of a semi-circle, a partial ellipse, and a rectangle.

The retrograde surfaces may have a cross-sectional shape of one of a group consisting of an inverted semi-circle, an inverted partial ellipse, and an inverted rectangle.

The pillar structure may extend on the substrate in a direction perpendicular to one or more contact stripes to be formed on the substrate.

A width of the gap structure may be in a range from about 1 to 8 μm . The width of the gap structure may be in a range from about 2 to 5 μm .

The pillar structures may be formed utilising photolithography techniques.

The pillar structures may be formed utilising wet etching and lift-off techniques.

In accordance with a third aspect of the present invention there is provided a multi-layered device structure comprising an integrated mask as defined in the first aspect.

- 5 The device may comprise one or more of a group consisting of an electronic, a mechanical, and an electro-mechanical device.

The device may comprise one or more of a group consisting of a flat panel display, a photo-detector array of photodiodes, and a micro electro-mechanical system (MEMS)
10 device.

BRIEF DESCRIPTION OF THE DRAWINGS

- 15 Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

FIG. 1 is a schematic cross-sectional view of a section of a typical
20 integrated mask.

FIG. 2 is a schematic cross-sectional view of a section of an integrated mask in accordance with an example embodiment.

- 25 FIGs. 3(a) to (d) are schematic cross-sectional drawings illustrating a fabrication process for an integrated mask in accordance with an example embodiment.

FIGs. 4(a) to (e) are schematic cross-sectional drawings illustrating a
30 fabrication process for an integrated mask in accordance with an example embodiment.

FIG. 5 is a schematic perspective view of a section of an integrated mask in accordance with an example embodiment.

FIG. 6 is a schematic cross-sectional view of a section of an integrated mask utilised in a fabrication process in accordance with an example embodiment.

5 DETAILED DESCRIPTION

In an example embodiment, with reference to FIG. 2, an integrated mask 200 comprising a pillar 202, and barrier elements in the form of humps 204a, b disposed next to the pillar 202, are provided. The pillar 202 and humps 204a, b define respective gap channels 206a, b. The integrated mask 200 comprises a plurality of similar structures
10 repeated in parallel and disposed perpendicular to bottom electrodes, for example 210. The pillar 202 and humps 204a, b are in the form of strips which may stretch along the length of the area to be deposited in an example embodiment.

In the example embodiment, the gap channels 206a, b formed between the pillar 202 and the humps 204a, b provide "dead corners" 207a, b that effectively separate top
15 electrodes deposited over the pillar 202 into strips so as to avoid electrical shorting. In other words, the "dead corners" 207a, b are not in a line of sight from outside of the gap channels 206a, b. Thus, no deposition takes place in at least the "dead corners" 207a, b in the example embodiment.

Additionally, the humps 204a, b have a function of preventing electrical shorting
20 between the bottom electrode 210 and the top electrodes (not shown). This is because uneven deposition of an insulating layer (not shown) deposited prior to the deposition of the top electrode over the pillar 202 may occur under the overhangs 208a, b, which would provide insufficient insulation between the top electrode and the bottom electrode. In the example embodiment, the humps 204a, b partially
25 extend beyond a vertical line from the corners of the overhangs 208a, b, as indicated as hump portions 226a, b.

In the following, one fabrication process for fabricating an integrated mask in accordance with the example embodiment is described with reference to FIG. 3(a) to (d).

30 With reference to FIG. 3(a), a commercially available positive photoresist AZ4620, is spin coated onto electrode layer 303 on a glass substrate 302 at about 1400 revolutions per minute (rpm) for about 20 seconds. The photoresist layer is baked at about

100 °C for about 5 minutes, and exposed to ultra-violet radiation from a high pressure mercury lamp operated at a power of about 12.5 mW/cm² for about 40 seconds through a photo-mask (not shown) such that only the portions of photoresist that are to be removed after developing are exposed. The photoresist is then developed in a
5 commercially available developer AZ400K to obtain structures, for example 304, for fabricating humps.

After blow drying with nitrogen gas, the substrate 302 with fabricated humps, for example 304, is post-baked at about 120 °C for at least 5 minutes for further strengthening. In the example embodiment, the substrate 302 is then coated with a
10 negative dry film photoresist 308 by a hot lamination process with a lamination machine at a temperature of about 110 °C and a speed of about 20 mm/s, as illustrated in FIG. 3(b). In the example embodiment, each hump, for example 304, has a semi-circle profile with a base width of about 20 µm. The semi-circle profile is believed to be the result of the post-baking and/or hot laminating steps. The dry film photoresist 308 is
15 about 25 µm thick and commercially available. The laminated dry film photoresist 308 is exposed to ultra-violet radiation from a high pressure mercury lamp operated at a power of about 12.5 mW/cm² for at least 10 seconds through a photo-mask such that only the portions, for example 316, of photoresist 308 that are to remain after developing are exposed, as shown in FIG. 3(c).

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The exposed photoresist 308 is then developed in an aqueous solution containing about 1 to 2% sodium carbonate at room temperature to form pillars structures 312. During the developing step, the size of the humps e.g. 304 reduced, thereby "opening" a gap channel e.g. 320 between the pillars e.g. 316 and the humps e.g. 306, as
25 illustrated in FIG. 3(d). This may be caused by an inter diffusion between the positive photoresist material of the humps, e.g. 304, and the negative photoresist layer 308 (compare FIG. 3(b)). As a result, during the developing in the aqueous solution at room temperature to form the pillars structures 312, an outer inter diffusion layer of the humps e.g. 304, is removed to create the gap channels, e.g. 320. The size of the interdiffusion
30 region and the resulting gap structure can be varied depending on the fabrication conditions. After being rinsed and dried, the substrate 302 with dry-film pillars, for example 316, is flood-exposed under the same conditions as the previous exposure for about 60 seconds for further strengthening. The substrate 302 with the resultant

integrated mask or pillar structures 312 is baked in a hot oven for further drying and subsequent use for fabricating an OLED display panel in the example embodiment.

In the following, a second fabrication process for fabricating an integrated mask in accordance with the example embodiment is described with reference to
5 FIG. 4(a) to (e).

A negative dry film photoresist is laminated on to a substrate 400 using a lamination machine at a temperature of about 110 °C and a speed of about 20 mm/s. In the example embodiment, the dry film is about 10 µm thick and commercially available. The laminated dry film is exposed to ultra-violet radiation from a high pressure mercury
10 lamp operated at a power of about 12.5 mW/cm², for at least 20 seconds through a photo-mask. Only the portions of photoresist that are to remain after developing to obtain structures are exposed. A plurality of fine strips of humps, for example 402, are formed on an electrode layer 404 on the substrate 400 after developing the exposed dry film in an aqueous solution containing about 1 to 2% sodium carbonate at room temperature, as
15 shown in FIG. 4(a). The humps, for example 402, are about 10 µm high and about 20 µm wide in rectangular profile, in the example embodiment.

A commercially available positive photoresist 406, AZ2100-45, is spin coated on to the substrate 400 with the pre-formed humps, for example 402, at about 1400 rpm for about 45 seconds as shown in FIG. 4(b). The substrate 400 with the positive
20 photoresist 406 layer is baked at about 105 °C for about 2.5 minutes and then exposed to ultra-violet radiation from a high pressure mercury lamp operated at a power of about 12.5 mW/cm² for about 8 seconds through a photo-mask, such that only the portions of photoresist, for example 608, that are to be removed after developing are exposed. The positive photoresist 406 is then developed in a commercially available
25 developer, AZ732C. The humps, for example 402, are thus completely covered by the remaining positive photoresist layer 410 of about 3 to 4 µm, as shown in FIG 4(c). The substrate 400 is post baked at about 110 °C for at least 2.5 minutes for further strengthening.

In the example embodiment, the substrate 400 is then coated with another
30 negative dry film 412 photoresist by a lamination machine at a temperature of about 110 °C and a speed of about 20 mm/s, as shown in FIG. 4(d). In the example embodiment, the dry film 412 is about 25 µm thick and commercially available. The laminated dry film

412 is then exposed to ultra-violet radiation from a high pressure mercury lamp operated at a power of about 12.5 mW/cm^2 for about 10 seconds through a photo-mask (not shown). Only the portions, for example 414, of the dry film 412 photoresist that are to remain after developing are exposed, as shown in FIG. 4(d). The exposed dry film 412 is developed in an aqueous solution containing about 1 to 2% sodium carbonate at room temperature to form pillars, for example 416, as shown in FIG. 4(e). In the example embodiment, the positive photoresist layer 410 is also removed by the developing process, and gap channels, for example 418, are formed, as shown in FIG. 4(e). After being rinsed and dried, the substrate 400 is flood-exposed under similar conditions for about 60 seconds for further strengthening and is baked in a hot oven for further drying.

In this example embodiment, both the pillars, e.g. 416, and humps e.g. 418, can be made from the same negative (or positive) photoresist material. It will further be appreciated by a person skilled in the art that in different fabrication processes in different embodiments of the present invention, other materials than photoresist materials may be used for the fabrication of the humps, pillars, or both. For example, ceramic materials may be used, and in such embodiments for example wet etching and lift-off techniques may be utilised to create the desired shapes of the ceramic material pillars, humps, or both.

Returning now to FIG. 2, in the example embodiment, the base widths of humps, 204a, b are each less than one-half of the width at the top of pillar 202. A wider base for each of the humps 204a, b increases the depth of overhangs 208a, b, and this may result in weaker support for the overhangs 208a, b. A narrower base for each of the humps 204a, b may influence the functionality of the mask 200. To balance the functionalities of the humps 204a, b, the ratio of the base width of hump portions 226a, b to hump portions 222a, b is about 1:4 to 1:2 in the example embodiment.

In the example embodiment, the width at the top of pillar 202 may vary according to the resolution requirements of the display panel to be fabricated. The height of pillar 202 depends on the material and the fabricating process. In the example embodiment, the height of pillar 202 is less than the width at the top of pillar 202. The width at the base of pillar 202, and the width at the top of pillar 202, are both larger than the height of pillar 202. In the example embodiment, the thickness of the overhangs 208a, b is determined by the height of pillar 202, the height of humps 204a, b and the width of gap channels 206a, b. The thickness of the overhangs 208a, b is more than $1 \mu\text{m}$ in the

example embodiment. The width of the gap channels 206a, b is determined by the selection of materials and processing routes used for fabricating the pillar 202 and humps 204a, b. The width of the gap channels 206a, b can be about 1 to 8 μm and is about 2 to 5 μm in the example embodiment.

5 As previously described, the gap channels, 206a, b each include what is termed herein as "dead corners" 207a, b at locations near to the bottom electrode 210 and substrate 213. These "dead corners" 207a, b are free of deposit materials during subsequent (e.g. vapor) deposition and ensure that adjacent top electrode strips (not shown) are not electrically connected, i.e. shortened. In the example embodiments, the
10 humps 204a, b can be of any geometry in profile, such as semi-circle, partial ellipse or rectangle, as long as "dead corners" 207a, b are formed in the gap channels 206a, b to prevent shortening after subsequent vapour deposition of the top electrode strips (not shown).

 The pillars and humps may be part of one integral pillar structure. In such
15 embodiments, gap channels (compare 206a, b) between hump portions (compare 204a, b) and pillar portions (compare 202) of an integral pillar structure may not extend all the way to the underlying layer (compare 210).

 FIG. 5 shows a schematic diagram of an integrated mask 500 fabricated for a passive-matrix OLED device in the example embodiment. In the example embodiment, the integrated mask 500 is fabricated such that the subsequent deposition of organic EL
20 layers and metallic top electrode layer are automatically patterned. A plurality of mask strips, for example 502, are formed over bottom electrodes, for example 504, and substrate 506 with respect to the bottom electrodes, for example 504, such that an orthogonal spatial relationship is formed. In the example embodiment, the pixel or
25 light-emitting areas are defined by the intersection between patterned bottom electrodes, for example 504, and top electrode strips (not shown). These pixel areas are defined by a span 508. As described previously, each mask strip, for example 502, comprises of a pillar strip 510 with a retrograde profile and two humps, for example 512, defining two gap channels, for example 514.

30 With reference to FIG. 6, a process of fabricating an OLED device 500 incorporating an integrated mask 602 is described.

With reference to FIG. 6, in the example embodiment, bottom electrode 604 is deposited and patterned on a substrate 606 using conventional photolithography and chemical etching processes. In the example embodiment, an integrated mask 602 comprising pillars, for example 608, and humps, for example 610 and 612, is to be fabricated over the bottom electrode 604 and the substrate 606. In the example embodiment, for the fabrication of the integrated mask 602, humps, for example 610 and 612, are fabricated over the bottom electrode 604 and the substrate 606. Pillars, for example 608, are fabricated in between every other two humps, for example 610 and 612, such that gap channels, for example 614, are formed between humps, for example 610 and 612, and sidewalls of the pillars, for example 608.

In the example embodiment, upon fabrication of the integrated mask 602, one or more organic EL layers 616 are deposited onto the substrate 606 with the bottom electrode 604 and the integrated mask 602. The organic EL layers 616 are electrically connected to the bottom electrode 604. After deposition of the organic EL layers 616, a plurality of top electrodes 618 are deposited over organic EL layers 616 with the integrated mask 602 in place. The top electrodes 618 are electrically connected to the organic EL layers 616. In the example embodiment, device 600 emits light when a current is passed between the bottom electrode 604 and the top electrodes 618, through organic EL layers 616.

In the example embodiment, it is noted that the bottom electrode 604 and substrate 606 may comprise conventional materials having conventional dimensions. The substrate 606 can be transparent in the case of bottom- and double-side- emitting devices, such as a glass plate, quartz plate or a plastic plate, and non-transparent in the case of top-emitting devices such as Si wafer. The bottom electrode 604 can be a transparent conductor in the case of bottom-, double-side- as well as top-emitting devices, such as conducting polymers and ITO, and non-transparent in the case of top-emitting devices, such as metals. In the example embodiment, insulating humps, for example 610, are fabricated using conventional techniques, such as photolithography, vapour deposition, wet-coating and combinations of such techniques. Humps, for example 610, may be made of any suitable non-electrically conducting material, such as photoresists, polyimides, oxides and nitrides.

In the example embodiment, organic EL layers 616 may include any conventional OLED organic materials. Organic EL layers 616 may comprise of a single

layer or may comprise multiple layers of conventional OLED structures, such as a single or double heterostructure, or may comprise one or more layers containing a mixture of OLED organic materials. In the example embodiment, top electrodes 618 may comprise a sputter-deposited electrode material such as ITO, Magnesium:Silver (Mg:Ag) and Aluminium (Al). These materials may allow fabrication of thin top electrodes 618 that are transparent, such that light emitted from organic EL layers 616 may pass through top electrodes 618 to a viewer, in which case device 600 would be a top-emitting OLED device. In the example embodiment and with reference to FIG. 6, the OLED device fabricated is intended for use as a regular bottom-emitting OLED display, such that light is emitted through bottom electrode 604 and substrate 606. The fabrication process may similarly be used for fabricating a top-emitting OLED display, such that light is emitted through top electrodes 618.

The integrated mask 602 fabricated in the example embodiment is more suitable to be adopted for mass production than typical masks as the integrated mask 602 is less dependent on the deposition angle of the electrode metal source.

Thus, the integrated mask 602 in the example embodiment can enable the use of processes that are not typically applicable for top electrode deposition, such as chemical vapour deposition (CVD), high pressure chemical vapour deposition (HPCVD) and sputtering with off-axis deposition. Having less dependence on the deposition angle means that mass production of OLED devices utilising the integrated mask 602 in the example embodiment may be relatively easier to achieve than with current typical techniques.

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

For example, it is understood that the integrated mask according to example embodiments may be used to fabricate larger arrays of organic devices than those specifically described. A multi-color display may be fabricated by depositing various down-conversion layers known to the art, or using different organic materials in different devices. For example, a multi-color array may also be fabricated by a number of other

methods and utilising an integrated mask according to an example embodiment, such as using an array of white-emitting OLEDs in combination with color filters or a distributed Bragg reflector. Furthermore, the materials for fabricating the humps and pillars in the integrated mask may be organic, inorganic as well as a hybrid of both. Furthermore, the

5 coating processes used for fabrication of the humps and pillars in the integrated mask in example embodiments may include wet-coating, vapour deposition as well as a combination of both. In addition, the present invention is not limited to OLED applications and may be similarly applied to a wide variety of electronic, mechanical, or electro-mechanical devices including flat panel displays, photo-detectors arrays of

10 photodiodes, and micro electro mechanical system (MEMS) devices.

CLAIMS

1. An integrated mask structure for a substrate, the structure comprising:
a pillar structure formed on the substrate, and
5 at least one gap structure extending along the pillar structure, wherein a portion of a wall surface of each gap structure is not in a line of sight from outside of the gap structure, said portion of the wall surface extending along the pillar structure.
- 10 2. The mask structure as claimed in claim 1, wherein the pillar structure comprises:
one or more pillar elements formed on the substrate, each pillar element having at least one retrograde side surface extending along the first direction;
one or more barrier elements formed on the substrate, each barrier element
15 being adjacent one of the retrograde side surfaces of one pillar element,
wherein the gap structure is defined between the barrier elements and the respective adjacent retrograde side surfaces.
- 20 3. The mask structure as claimed in claim 2, wherein the gap structure extends between the barrier elements and the respective adjacent retrograde side surfaces to a surface portion of the substrate.
- 25 4. The mask structure as claimed in claims 2 or 3, wherein the barrier elements have a cross-sectional shape of one of a group consisting of a semi-circle, a partial ellipse, and a rectangle.
- 30 5. The mask structure as claimed in any one of claims 2 to 4, wherein the retrograde surfaces have respective cross-sectional shapes of one of a group consisting of an inverted semi-circle, an inverted partial ellipse, and an inverted rectangle.
- 35 6. The mask structure as claimed in any one of claims 1 to 5, wherein the pillar structure extends on the substrate in a direction perpendicular to one or more contact stripes to be formed on the substrate.

7. The mask structure as claimed in any one of claims 1 to 6, wherein a width of the gap structure is in a range from about 1 to 8 μ m.

8. The mask structure as claimed in claim 7, wherein the width of the gap structure is in a range from about 2 to 5 μ m.

9. A method of fabricating an integrated mask structure for a substrate, the method comprising:

forming a pillar structure on the substrate, and

10 forming at least one gap structure extending along the pillar structure, wherein a portion of a wall surface of each gap structure is not in a line of sight from outside of the gap structure, said portion of the wall surface extending along the pillar structure.

15 10. The method as claimed in claim 9, comprising:

forming one or more pillar elements of the pillar structure on the substrate, each pillar member having at least one retrograde side surface;

forming one or more barrier elements of the pillar structure on the substrate, each barrier element being adjacent one of the retrograde side surfaces of one pillar element, such that the gap structure is defined between the barrier elements and the respective adjacent retrograde side surfaces.

11. The method as claimed in claim 10, wherein the gap structure extends between the barrier elements and the respective adjacent retrograde side surfaces to a surface portion of the substrate.

12. The method as claimed in claims 10 or 11, wherein the barrier elements have a cross-sectional shape of one of a group consisting of a semi-circle, a partial ellipse, and a rectangle.

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13. The method as claimed in any one of claims 10 to 12, wherein the retrograde surfaces have a cross-sectional shape of one of a group consisting of an inverted semi-circle, an inverted partial ellipse, and an inverted rectangle.

14. The method as claimed in any one of claims 9 to 13, wherein the pillar structure extends on the substrate in a direction perpendicular to one or more contact stripes to be formed on the substrate.
- 5 15. The method as claimed in any one of claims 9 to 14, wherein a width of the gap structure is in a range from about 1 to 8 μ m.
16. The method as claimed in claim 15, wherein the width of the gap structure is in a range from about 2 to 5 μ m.
- 10 17. The method as claimed in any one of claims 9 to 16, wherein the pillar structures are formed utilising photolithography techniques.
18. The method as claimed in any one of claims 9 to 16, wherein the pillar
15 structures are formed utilising wet etching and lift-off techniques.
19. A multi-layered device structure comprising an integrated mask as claimed in any one of claims 1 to 8.
- 20 20. The device as claimed in claim 19, wherein the device comprises one or more of a group consisting of an electronic, a mechanical, and an electro-mechanical device.
- 25 21. The device as claimed in claim 20, wherein the device comprises one or more of a group consisting of a flat panel display, a photo-detector array of photodiodes, and a micro electro-mechanical system (MEMS) device.

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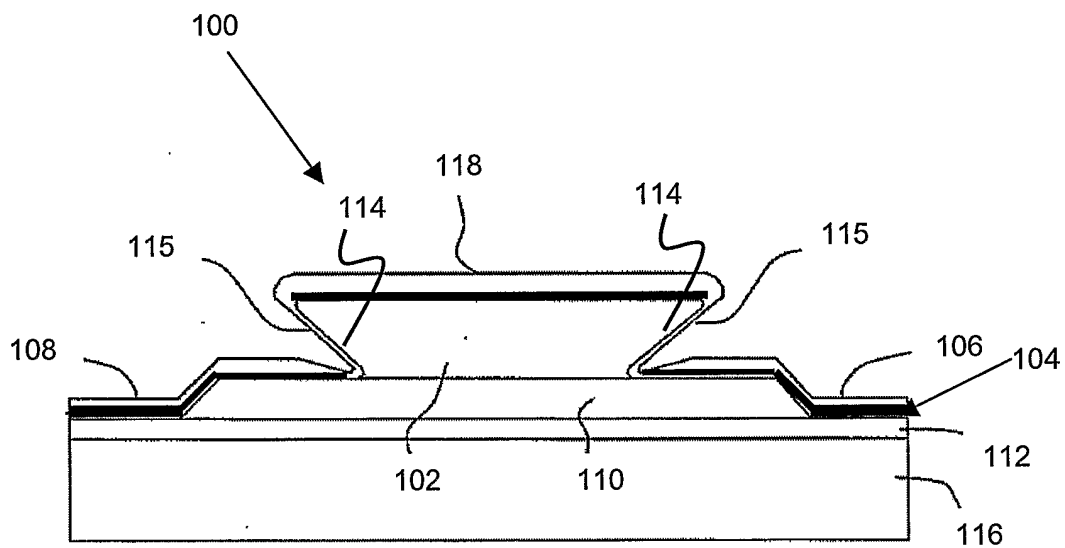


FIG.1

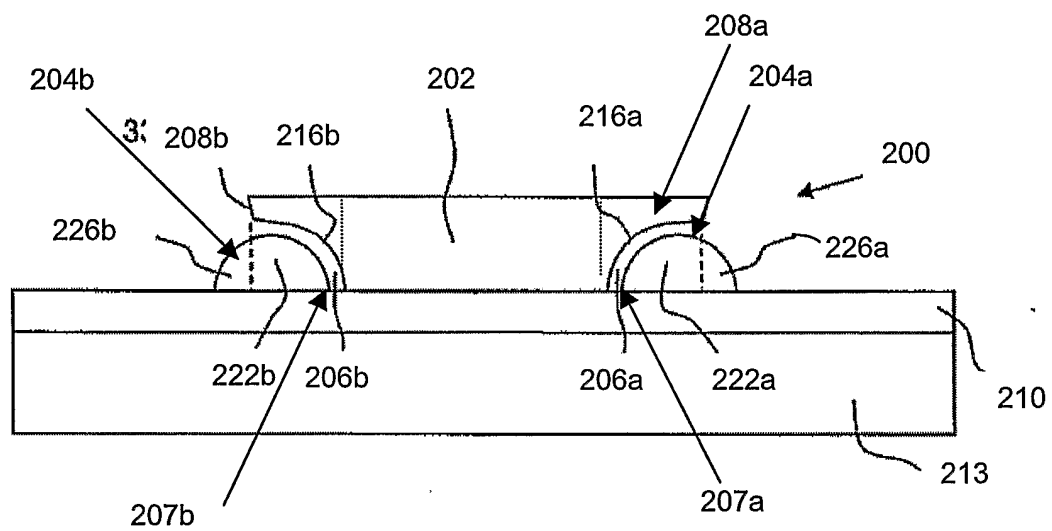


FIG.2

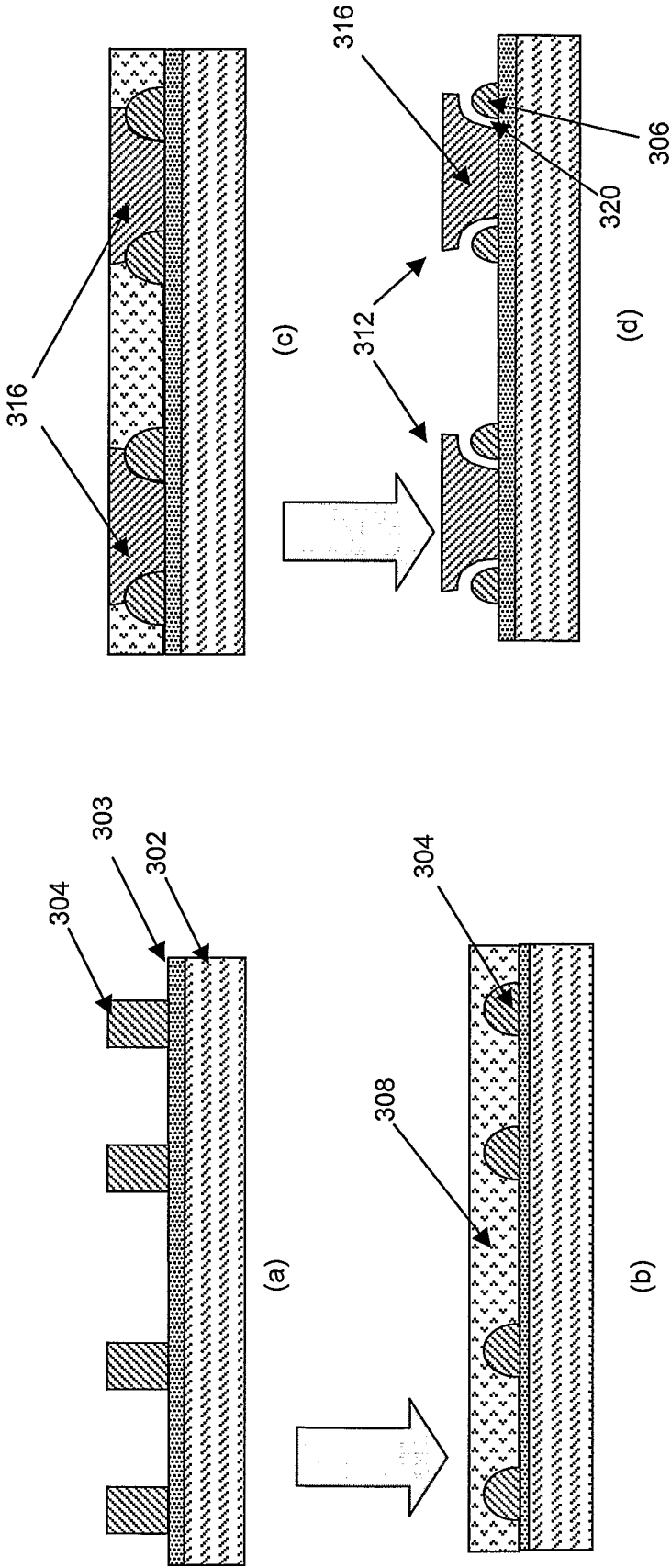


FIG.3

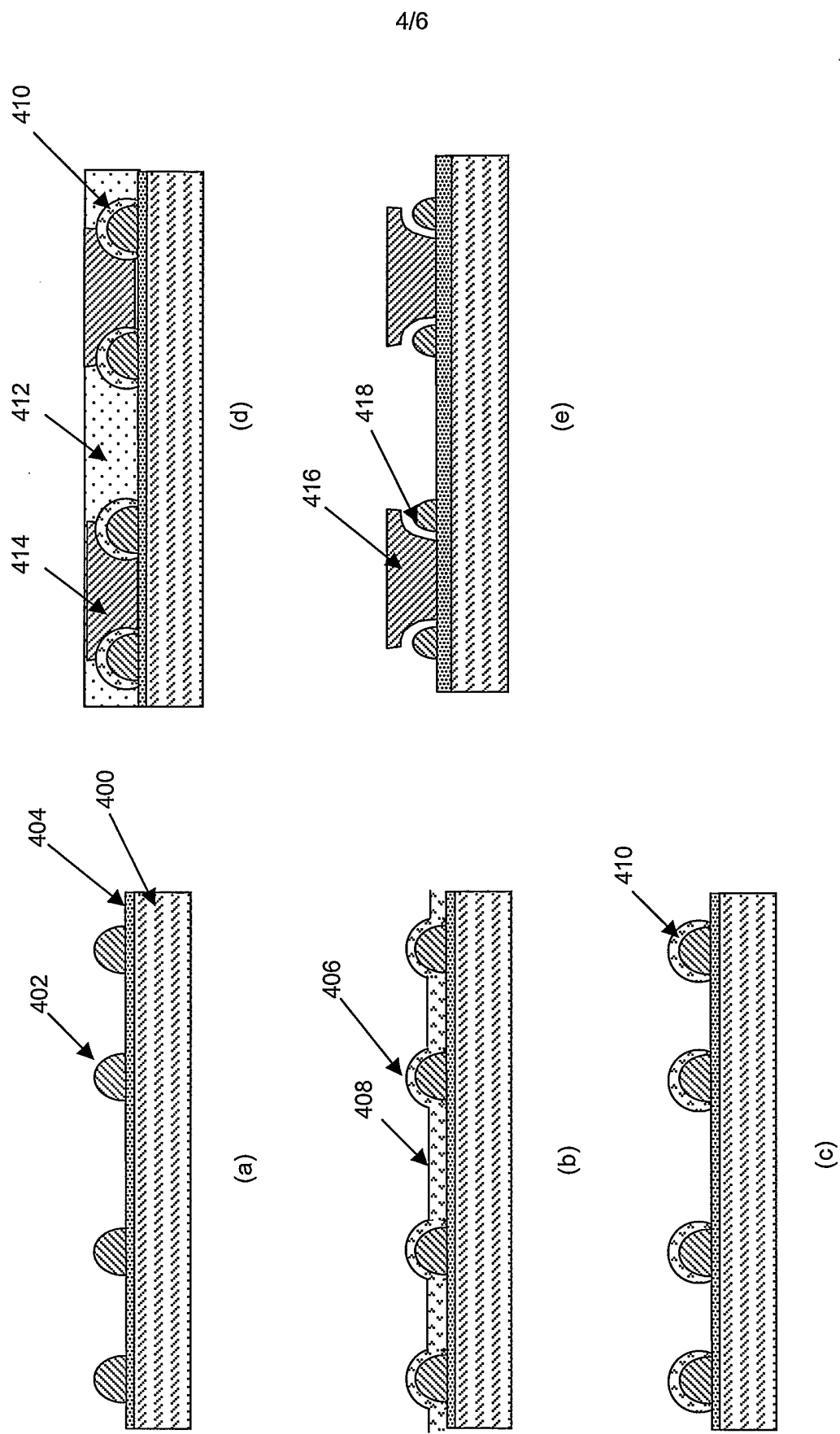


FIG.4

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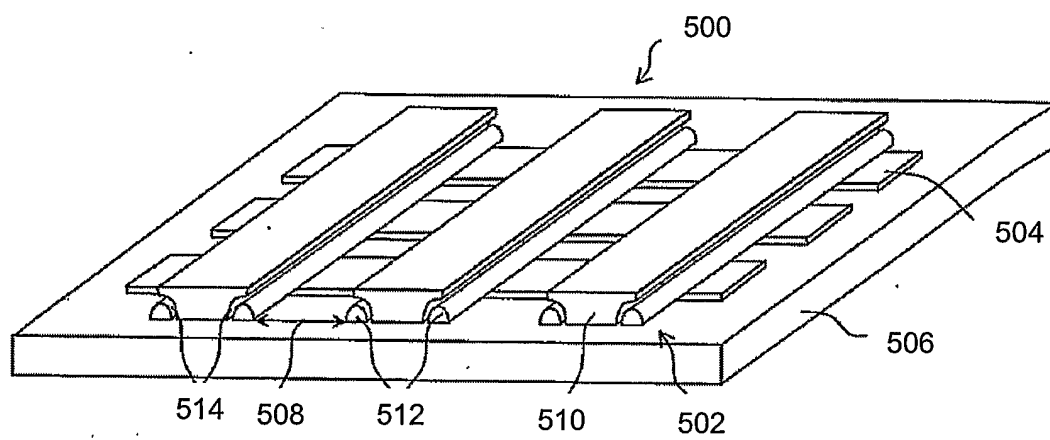


FIG.5

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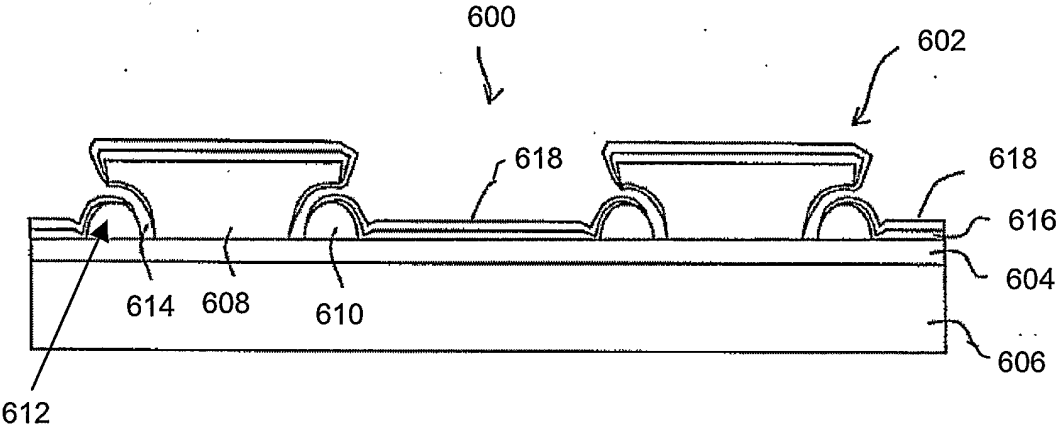
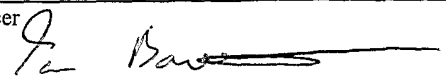


FIG.6

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2006/000051

A. CLASSIFICATION OF SUBJECT MATTER Int. Cl. <i>H01L 51/56</i> (2006.01) <i>B81C 1/00</i> (2006.01) <i>H01L 21/285</i> (2006.01) According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) DWPI, JAPIO; mask+, (overhang+, mushroom, T-shape, retrograd+ etc), (dead, hidden, shad+, line of sight), substrate?, (deposit+, coat+), (gap?, spac+, interval, parallel+, airgap?), (+oled, pled, oeld, mems, H01L-051/IC, H05B-033/IC), (electrode?, anode?, cathode?), (integrated mask), (pillar?, post?, pedestal?, column?), (shortcircuit, shorthing, short circuit, shorts, bridg+), (strip+, line?, bus), (side? or wall?)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6596598 B1 (KRIVOKAPIC et al) 22 July 2003 See the abstract, fig 11,12, col 7 line 43-60, col 8 line 53-65	1-21
P,A	US 2005/0087826 A1 (RODGERS et al) 28 April 2005 See the abstract	
A	US 6407408 B1 (ZHOU et al) 18 June 2002 See the abstract	
☒ Further documents are listed in the continuation of Box C ☒ See patent family annex		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
Date of the actual completion of the international search 12 April 2006	Date of mailing of the international search report 24 APR 2006	
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustalia.gov.au Facsimile No. (02) 6285 3929	Authorized officer  I.A.BARRETT Telephone No : (02) 6283 2189	

INTERNATIONAL SEARCH REPORT

International application No.

PCT/SG2006/000051

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2001/0035393 A1 (LU et al) 1 November 2001 See the abstract	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/SG2006/000051

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member	
US	6596598		
US	2005087826	US 6824278	US 6937131 US 2003174929
		US 2005088765	US 2005101048
US	6407408		
US	2001035393	US 6559604	US 6777256 US 2003157740
Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.			
END OF ANNEX			