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(71) Applicant *(for all designated States except US)*: **TRACIT TECHNOLOGIES** [FR/FR]; Centr'alp, 52, rue du Corporat, F-38430 Moirans (FR).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **ASPAR, Bernard** [FR/FR]; 110 Lotissement le Hameau des Ayes, F-38140 Rives (FR). **LAGAHE-BLANCHARD, Chrystelle** [FR/FR]; Route de la Cascade, F-38134 Saint Joseph de Rivière (FR).

(74) Agents: **POULIN, Gérard** et al.; BREVALEX, 3, rue du Docteur Lancereaux, F-75008 Paris (FR).

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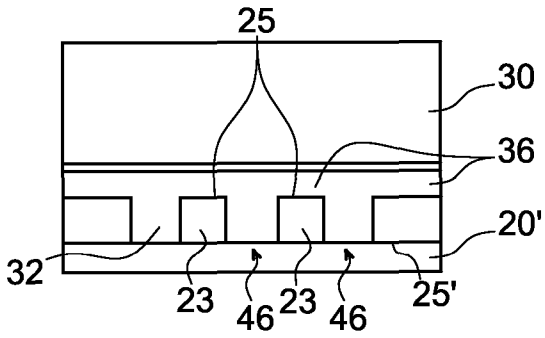
(54) **Title:** METHOD FOR PRODUCING PARTIAL SOI STRUCTURES COMPRISING ZONES CONNECTING A SUPERFICIAL LAYER AND A SUBSTRATE



(57) **Abstract:** The invention relates to a method for producing a semiconductor structure comprising a superficial layer (20'), at least one embedded layer (36, 46), and a support (30), which method comprises: a step of forming, on a first support, patterns (23) in a first material, a step of forming a semiconductor layer, between and on said patterns, a step of assembling said semiconductor layer with a second support (30).

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METHOD FOR PRODUCING PARTIAL SOI STRUCTURES COMPRISING ZONES CONNECTING A SUPERFICIAL LAYER AND A SUBSTRATE

TECHNICAL FIELD AND PRIOR ART

The invention relates to the production of new structures of semiconductor components or MEMS-type devices, and in particular SOI or SOI-type devices.

Numerous microsystems or MEMS (Micro Electro Mechanical Systems) are produced using SOI (Silicon On Insulator) materials, which make it possible in particular to obtain monocrystalline silicon membranes suspended above a cavity.

In various applications in the field of power electronics and microsystems, it can be advantageous to have a structure combining the functions of a "bulk" silicon substrate and an SOI substrate: i.e. comprising local zones 2 of embedded oxide (for example SiO_2) under an active layer 4, as shown in figure 1.

To obtain this type of structure, a number of methods have already been described, for example in document FR 0216646.

In this type of method, one problem is that of having to condition a heterogeneous surface.

The problem of producing a structure comprising SOI zones and Si zones, as shown in figure 1, is posed.

More specifically, the goal is to find a technique simpler than those already known, in particular overcoming the problem associated with the

presence of heterogeneous surfaces, which require specific methods to be used.

DESCRIPTION OF THE INVENTION

The invention first relates to a method for producing a semiconductor structure, comprising a superficial layer, at least one buried or embedded layer, and a support, which method comprises:

- a step of forming, on a first support or substrate, patterns in a first material,
- a step of forming a layer made of a second, semiconductor material between and on said patterns,
- a step of heat-treating the semiconductor layer so as to totally or partially modify the crystallinity thereof,
- a step of assembling said semiconductor layer with a second support or substrate.

The semiconductor layer can be made of monocrystalline and/or polycrystalline and/or amorphous silicon.

It can also comprise zones of a first type of crystallinity and zones of a second type of crystallinity, different from the first. For example it comprises zones of amorphous material and zones of polycrystalline material. According to another example it comprises crystalline zones and zones of amorphous or polycrystalline material.

The invention also relates to a method for producing a semiconductor structure, comprising a superficial layer, at least one buried or embedded layer, and a support or substrate, which method comprises:

- a step of forming, on a first support or substrate, patterns in a first material,
- a step of forming a second layer, made of amorphous silicon or monocrystalline silicon, between and on said patterns,
- a step of assembling this second layer with a second support or substrate.

A step of heat-treating the semiconductor layer can be performed so as to totally or partially modify the crystallinity thereof.

The semiconductor layer can comprise zones of a first type of crystallinity and zones of a second type of crystallinity, different from the first one. For example it comprises zones of amorphous material and zones of polycrystalline material. According to another example it comprises crystalline zones and zones of amorphous or polycrystalline material.

The invention also relates to another method for producing a semiconductor structure comprising a superficial layer, at least one buried or embedded layer, and a support or substrate, which method comprises:

- a step of forming, on a first support or substrate, patterns in a first material,
- a step of forming a semiconductor layer, between and on said patterns, which semiconductor layer comprises zones of a first type of crystallinity and zones of a second type of crystallinity, different from the first one,
- a step of assembling this second layer with a second support or substrate.

The semiconductor layer can be, for example, made of monocrystalline and/or polycrystalline and/or amorphous silicon.

The patterns can be formed, for example, from a layer, which can be an insulating layer, for example an oxide or nitride layer. It is, for example, produced by thermal oxidation, or by oxide deposition using the LPCVD technique, or by oxide deposition using the PECVD technique. The patterns can be formed by any other conventional means used in microelectronics.

In general, this layer, from which the patterns can be formed, can be a layer consisting of different materials and/or multilayers.

In general, the semiconductor layer can also be formed by epitaxy or deposition; in the case of epitaxy, it can be formed at a speed dependent on the surface on which the epitaxy is performed, which enables a relatively planar surface to be obtained after growth.

A step of planarisation of the semiconductor layer can be performed, before assembly with the second substrate.

A step of hydrophilic or hydrophobic preparation of the surface of the semiconductor layer can be performed before assembly of this layer with the second support or substrate.

An annealing step can be performed after assembly of the semiconductor layer with the second support or substrate.

A step of thinning, and optionally a routing stage or a step of edge grinding of the

substrate to be thinned, before or after thinning, can also be performed.

The invention also relates to a semiconductor device comprising a superficial layer, at least one embedded layer, and a support or substrate, the embedded layer comprising a first sublayer of amorphous or monocrystalline silicon, and a second sublayer comprising an alternation of patterns of a first material and zones of amorphous or monocrystalline silicon.

The invention also relates to a semiconductor device comprising a superficial layer, at least one buried or embedded layer, and a support or substrate, the buried or embedded layer comprising a first sublayer comprising an alternation of patterns of a first material and zones of a second, semiconductor material, and a second sublayer made of a semiconductor material comprising zones of a first type of crystallinity and zones of a second type of crystallinity.

The second sublayer can be made of monocrystalline and/or polycrystalline and/or amorphous silicon.

By one of the methods according to the invention, it is possible to obtain a structure comprising an active superficial layer of variable thickness, of which certain zones are insulated from the substrate, for example by an embedded or a buried oxide layer, and of which other zones act as a semiconductor (for example: Si) bulk (or massive);

there is then vertical thermal and/or electrical conduction with the substrate.

By one of the methods according to the invention, it is possible to obtain a structure comprising an active superficial layer of variable thickness, of which certain zones are insulated from the substrate, for example by an embedded or a buried oxide layer, and of which other zones act as a semiconductor (for example: Si) bulk (or massive); there is then vertical thermal and/or electrical conduction with the substrate.

With respect to the techniques already known, the invention avoids the planarisation of the heterogeneous surface (for example having an alternation of SiO_2/Si). The surface to be planarised is homogeneous (it is, for example, a deposit of Si or silicon obtained by epitaxial growth), in which case the implementation of specific and complex planarisation methods can be avoided so as to solve the problems of differential attack speeds ("dishing").

The invention can be applied to other semiconductors, such as Ga, SiC, AsGa, InP or SiGe.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figure 1 shows a mixed BSOI-type structure,
- figures 2A to 2G show various steps of a production method according to the invention,
- figure 3 shows a structure according to the invention from a top view,
- figure 4 shows an alternative of a device according to the invention,

- figure 5 shows the case of epitaxial growth on different surfaces.

DETAILED DESCRIPTION OF SPECIFIC EMBODIMENTS

A method according to the invention, for developing a structure such as that shown in figure 1, will be described in reference to figures 2A to 2G, starting with a semiconductor material, for example Si 20 (figure 2A).

A layer 22 is first produced, which is intended to be a buried layer or an embedded layer or an embedded or a buried layer structured by patterns, for example a dielectric layer, in particular of oxide, such as a silicon oxide, of which the thickness will correspond to the desired thickness of the patterns 23 buried or embedded in the final structure (figure 2B). This layer 22 can be made in different ways: by thermal oxidation, or LPCVD oxide deposition, or PECVD oxide deposition, and so on. This embedded layer 22 can also be made up of different materials (for example: a nitride such as Si_xN_y and/or an oxide such as Al_2O_3 and/or a doped silicon oxide (PSG- or BPSG-type, etc.)), and/or multilayers (again, with a nitride such as Si_xN_y and/or an oxide such as Al_2O_3 and/or a doped silicon oxide such as PSG or BPSG), according to the functionalities desired for the application.

Then, the distribution of patterns 23 is defined in this layer 22. The zones 24 between these patterns are, for example, etched to the level of the underlying substrate 20, for example, by lithography and etching of the layer 22 (figure 2C). Thus, at the surface of the substrate, an alternation of patterns 23

and zones 24 between the patterns is obtained. The distribution of patterns 23 can be obtained by any other technique, not only by etching. This distribution is arranged according to the needs of the application. In addition, the patterns can have different shapes (from the top view: circular shape, and/or square, and/or other, etc.) and variable sizes (submicronic to millimetric). The zones 24 between the patterns 23 can reach the surface 21 of the substrate 20, which makes it possible to alternate, on this surface 21, patterns of material 23 (oxide in the example given) and, between these patterns, zones 24 without material and directly reaching the substrate 20. The patterns are thus formed directly on semiconductor substrate 20.

The patterns can be obtained by other combinations of microelectronic methods such as oxidation, oxide deposition, etching, photolithography, and so on.

A deposition or epitaxial production of semiconductor material 26 is performed on the substrate thus prepared (figure 2D). In general, the layer of thickness e above the patterns 23 substantially matches the shape and distribution of the patterns 23.

A layer of semiconductor material 26 is therefore made directly on and between the patterns. Between said patterns, the semiconductor layer is in contact with semiconductor substrate 20.

Figure 3 shows an example, from a top view, of a substrate on which etched zones 24, filled with material 26, are produced between patterns 23.

Configurations other than that of figure 3 can be produced.

The semiconductor material 26 is, for example, silicon (amorphous, polycrystalline or crystalline), with the type of silicon being selected according to the needs of the application and/or according to the possibilities of each technique, in particular according to the thicknesses that must be deposited. Other semiconductor materials can be chosen, for example SiC, or GaN or materials of type III to V. For these materials, there is also the possibility of having various types of crystallinity (for example, polycrystalline or monocrystalline SiC).

It can be advantageous to choose the semiconductor 26 of the same type (material, doping, etc.) as the material of the future superficial layer 20', 30' (see figures 2F and 2G). However, in some cases, it can be advantageous for the type of semiconductor layer 26 to be different from that of the superficial layer 20', 30'.

This material 26 is alternatively in contact with the surface 21 of the substrate 20 and with the insulating patterns 23.

The thickness e of the deposited material is chosen so as to then allow for a reduction in the topology by planarisation, so as to obtain a thickness e' (figure 2D) with $0 < e' < e$, without leading to the apex 25 of the oxide patterns 23 or without leaving said apex with no deposited material on it.

According to the type of technique used to produce this semiconductor material layer 26, various

crystallinities can be obtained: for example, in the case of Si, it is possible to produce an epitaxial layer of monocrystalline Si, or a deposit of polycrystalline or amorphous Si using different techniques (LPCVD, PECVD, etc.).

The production of an amorphous Si deposit on alternating zones of Si (surface 21 of the substrate 20) and SiO_2 (patterns 23) can result in a layer alternating between polycrystalline material (on the surface 21) and amorphous material (on the patterns 23), while the epitaxial production of Si on alternating zones of Si (surface 21) and SiO_2 (patterns 23) generally results in a layer alternating between crystalline material (on the surface 21) and amorphous or polycrystalline material (on the patterns 23).

It can thus be advantageous, for certain applications, to alternate between different crystallinities of the layer 26 according to the requirements in terms of electrical and/or thermal conduction and/or in terms of gettering and/or mechanical features. Therefore, it is possible to form, as shown in figure 4, on a single sublayer comprising an alternation between patterns 23 and semiconductor material 26, an alternation of zones of semiconductor material 26a having a first type of crystallinity, and semiconductor material 26b having a second type of crystallinity, different from the first. Examples of various combinations are shown below.

Moreover, it is possible to choose the physical properties, for example electrical (conductor, insulating, etc), and/or thermal (conductibility)

and/or mechanical, of this deposited layer 26 according to the needs of the application. For this, it is possible to vary the composition (with greater or less doping) and/or the conditions under which this layer 26 is formed.

A heat treatment of the deposited layer 26 can be performed so as to modify the crystallinity of the layer. For example, a layer 26 of amorphous and/or polycrystalline Si can be deposited, then annealed at 1100 °C.

This heat treatment of layer 26 is performed before assembly and adhesion with substrate 30 (see figure 2E) and can therefore physically modify said layer 26 (by modifying its crystallinity).

The layer 26 can then be conditioned so as to obtain a smooth surface 27 (figure 2D) enabling a surface state compatible with the subsequent bonding phase to be obtained.

This conditioning of the layer 26 can be performed by planarisation, for example by chemical-mechanical polishing, mechanical thinning or chemical thinning (dry plasma attack or RIE: reactive ion etching capable of reducing the surface topology) or by a combination of these different techniques.

This planarisation can be substantially reduced and/or avoided if, for example, the speed of epitaxy of the layer 26 is controlled according to the surfaces on which the growth is being carried out: for example (figure 5), the speed of growth on the surfaces 240 of semiconductor material can be greater than the speed of growth at the level of the oxide zones 25; the

control of these relative speeds can make it possible to obtain a relatively planar surface after growth of this layer.

The substrate 20 thus prepared is then bound by molecular adhesion to a substrate 30, for example made of silicon (figure 2E). The various types of surface preparation and binding that can be performed are indicated below.

A hydrophilic- or hydrophobic-type surface preparation can be performed before this assembly of the substrates. If the patterns 23 are electrically insulating (for example, made of oxide), the desired final structure comprises zones 36 isolated from the substrate 20' (SOI) and conductive zones 46 between these zones 36 (figure 2F).

In the case of hydrophilic bonding, a native oxide layer 34 is present at the bonding interface, and can compromise the ohmic contact between the substrates 20 and 30. In this case, if an ohmic contact is desired for a particular application, it is possible to treat the structure at high temperature (> 1100 °C) so as to cause the dissolution of this oxide at the level of the bonding interface and thus produce an ohmic contact at the level of the conductive zones 46.

For some applications, the heat treatment can be performed at a lower temperature.

In the case of hydrophobic bonding, the surfaces placed in contact are free of native oxide 34 and an ohmic contact is obtained directly.

Preferably, after bonding, the structure is annealed at high temperature, on the one hand so as to allow for consolidation of the bonding interface (reinforcement of the bonding strength) and, on the other hand, as shown above in the case of hydrophilic bonding, so as to generate the dissolution of the interface oxide and an ohmic contact.

The heat treatment is performed at a temperature compatible with the structure and/or with the subsequent steps to be performed to produce the final structure.

Preferably, a heat treatment step will be performed after deposition of the layer 26, at a temperature preferably higher than or equal to the subsequent temperature for consolidation of the bonding interface. In some cases, it may be lower than the consolidation temperature.

For example, in the case of silicon, the heat treatment can take place at a temperature within the range of 700 to 1300 °C.

The substrate 20 and/or the substrate 30 can be thinned by its rear surface so as to obtain the future active semiconductor layer 20' (figure 2F) in which the components will be developed. In figure 2F, it is substrate 20 that is thinned. When substrate 30 is thinned, a structure like that of figure 2G is obtained, in which the apex 25 of the pads 23 is turned toward substrate 30' (substrate 30 after thinning), but separated from 30' by the layer 36. In figure 2F, it is the other apex 25' of the pads 23 that is turned toward

the substrate or the thinned layer 20', which apex is even in contact with layer 20' in the example shown.

This thinning can be performed by mechanical grinding and/or chemical-mechanical polishing and/or mechanical polishing and/or chemical etching (wet or dry) techniques.

Preferably, it is substrate 20 that will be thinned (figure 2F). The thinning can also be performed by using a "Smart-Cut®"-type technique, or by substrate fracture. The "Smart-Cut®"-type technique is disclosed for example in the article by A.J. Auberton-Hervé et al. « Why can Smart-Cut change the future of microelectronics ? » International Journal of High Speed Electronics and Systems, Vol. 10, N°.1 (2000), p. 131-146.

Examples of embodiments according to the invention will now be provided.

Example 1:

In this example, the following steps are performed:

a_1) thermal oxidation of a silicon substrate 20, for example by generating 2 μm of oxide;

b_1) lithography of the patterns 24 to define future SOI and Si zones;

c_1) etching of the oxide 22 at the level of the future Si zones defined and removal of the etching mask;

d_1) cleaning of the surface and deposition of a polycrystalline silicon (p-Si) layer 26 by LPCVD (at around 650 °C), for example, deposition of a layer having a thickness of around 4 μm;

e_1) heat treatment at 1100 °C;

f_1) planarisation of the p-Si surface 26 so as to remove the topology between the SOI and Si zones by chemical-mechanical polishing; however, one remains on a homogenous poly-Si surface, and never move onto a heterogeneous SiO_2/Si surface;

g_1) hydrophilic-type cleaning and placement in contact for direct bonding by molecular adhesion of the substrate 20 - pattern 23 - layer 26 assembly and a silicon-free substrate 30;

h_1) heat treatment for consolidation of the bonding interface at 1100 °C;

i_1) thinning of the rear surface of the substrate 20 by mechanical grinding, then by chemical-mechanical polishing, for example until a thickness of 10 µm is obtained (this final thickness may vary according to the needs of the application between 2 µm and several hundred microns, for example 500 µm). A structure as shown in figure 2F is thus obtained.

Example 2:

In this example, the following steps are performed:

- steps a_2 to c_2: same as steps a_1 to c_1.

d_2) cleaning of the surface and deposition of an amorphous silicon (a-Si) layer 26 by PECVD, for example, deposition of a layer having a thickness of around 5 µm;

e_2) heat treatment at 1100 °C;

f_2) planarisation of the a-Si surface 26 so as to remove the topology between the SOI and Si zones by chemical-mechanical polishing;

g_2) hydrophobic-type cleaning and placement in contact for direct bonding by molecular adhesion of the substrate 20 and a silicon-free substrate 30;

h_2) same as h_1;

i_2) thinning of the rear surface of the substrate 30 by mechanical grinding, then by chemical-mechanical polishing, for example until a thickness of 20 μm is obtained. A structure as shown in figure 2G is thus obtained.

Example 3:

In this example, the following steps are performed:

a_3) thermal oxidation of a silicon substrate 20, for example by generating 3 μm of oxide;

b_3) to c_3): same as b_1) to c_1);

d_3) cleaning of the surface and deposition of a polycrystalline silicon (p-Si) layer 26 by LPCVD (at around 650 °C), for example, deposition of a layer having a thickness of around 7 μm;

e_3) same as e_1);

f_3) planarisation of the p-Si surface 26 so as to remove the topology between the SOI and Si zones by dry polishing, then surface finishing by chemical-mechanical polishing;

g_3) to h_3): same as g_1) to h_1);

i_3) thinning of the rear surface of the substrate 20 by mechanical grinding, then by chemical-mechanical

polishing, for example until a thickness of 20 μm is obtained. A structure as shown in figure 2F is thus obtained.

Example 4:

In this example, the following steps are performed:

a_4) to e_4): same as a_3) to e_3);

f_4) planarisation of the p-Si surface 26 so as to remove the topology between the SOI and Si zones by mechanical grinding with a fine wheel (for example #8000), then chemical-mechanical polishing for surface finishing;

g_4) to i_4): same as g_3) to i_3).

Example 5:

In this example, the following steps are performed:

a_5) to c_5): same as a_3) to c_3);

d_5) cleaning of the surface and epitaxy of a silicon layer 26 (at around 750 °C), for example, growth of a layer having a thickness of around 10 μm;

e_5) heat treatment at 1100 °C;

f_5) planarisation of the Si surface so as to remove the topology between the SOI and Si zones by chemical-mechanical polishing;

g_5) same as g_2);

h_5) heat treatment for consolidation of the bonding interface at 1150 °C;

i_5) thinning of the rear surface of the substrate 30 by mechanical grinding, then by chemical-mechanical

polishing, for example until a thickness of 10 μm is obtained.

Example 6:

In this example, the following steps are performed:

a_6) to c_6): same as a_2) to c_2);

d_6) cleaning of the surface and epitaxy of a silicon layer 26 (at around 850 °C), for example, by growth of a layer having a thickness of around 10 μm;

e_6) to f_6): same as e_5) to f_5);

g_6) hydrophobic-type cleaning and placement in contact for direct bonding by molecular adhesion of the substrate 20 and a silicon-free substrate 30;

h_6) heat treatment for consolidation of the bonding interface at 850 °C;

i_6) same as h_5).

The fields of application concerned by the invention are power electronics applications and the production of MEMS.

It is also possible to produce an insulating structure with contact pads providing vertical electrical conduction.

It is also possible to produce mixed components (on Si and on SOI), as well as components requiring heat evacuation (vertical heat conductibility). In the second case, the conduction can be essentially thermal and not electrical. Typically, it is possible to deposit a semiconductor layer, for example of amorphous silicon, with electrically insulating characteristics, while having good vertical

heat conductivity (corresponding to components requiring greater heat evacuation, for example).

Materials other than those indicated above can be used for one of the substrates, or the bonding layer (epitaxy, deposition, etc.), so as to satisfy various needs in terms of electrical and/or heat conduction, and/or other needs: SiC (good heat conductivity properties), or GaN, or materials III to V, and so on.

CLAIMS

1. Method for producing a semiconductor structure comprising a superficial layer (20', 30'), at least one buried layer (23, 26, 36), and a substrate (30), which method is characterised in that it comprises:

- a step of forming, on a first substrate (20), patterns (23) in a first material,
- a step of forming a layer (26) made of a second, semiconductor material between and on said patterns,
- a step of heat-treating the layer (26) made of a second material, so as to totally or partially modify the crystallinity thereof,
- a step of assembling the layer (26) made of a second material with a second substrate (30).

2. Method according to claim 1, said layer made of a second material being made of monocrystalline and/or polycrystalline and/or amorphous silicon.

3. Method according to claim 1 or 2, said layer made of the second material comprising zones of a first type of crystallinity (26a) and zones of a second type of crystallinity (26b), different from the first.

4. Method for producing a semiconductor structure comprising a superficial layer (20', 30'), at least one buried layer (23, 26, 36), and a substrate (30), which method comprises:

- a step of forming, on a first support (20), patterns (23) in a first material,
- a step of forming a layer (26), made of a second material, made of amorphous silicon or monocrystalline silicon, between and on said patterns,
- a step of assembling this layer (26) of a second material with a second substrate (30).

5. Method according to claim 4, also comprising a step of heat treating the amorphous silicon or monocrystalline silicon layer, so as to modify the crystallinity thereof.

6. Method according to claim 4 or 5, said amorphous silicon or monocrystalline silicon layer comprising zones of a first type of crystallinity (26a) and zones of a second type of crystallinity (26b), different from the first.

7. Method for producing a semiconductor structure comprising a superficial layer (20'), at least one buried layer (23, 26, 36), and a substrate (30), which method comprises:
- a step of forming, on a first substrate (20), patterns (23) in a first material,
- a step of forming a layer (26) made of a second, semiconductor material, between and on said patterns, which semiconductor layer comprises zones (26a) of a first type of crystallinity and zones (26b) of a second type of crystallinity, different from the first,

- a step of assembling this layer made of a second material with a second substrate (30).

8. Method according to claim 7, the layer made of a second material being made of monocrystalline and/or polycrystalline and/or amorphous silicon.

9. Method according to any of claims 1 to 8, said patterns (23) being produced from a first layer (22) made of a dielectric material.

10. Method according to claim 9, said dielectric material being an oxide or a nitride.

11. Method according to claim 10, said dielectric material being an oxide, produced by thermal oxidation, or by oxide deposition using the LPCVD technique, or by oxide deposition using the PECVD technique.

12. Method according to any of claims 1 to 11, said patterns (23) being produced from a first layer (22) made up of different materials and/or multilayers.

13. Method according to any of claims 1 to 12, said layer (26) made of a second material being formed by epitaxy or deposition.

14. Method according to claim 13, said layer (26) made of a second material being formed by

epitaxy, at a speed dependent on the surface on which the epitaxy is performed.

15. Method according to any of claims 1 to 14, comprising a step of planarisation of the layer (26) made of a second material before assembly with the second substrate (30).

16. Method according to any of claims 1 to 15, a hydrophilic or hydrophobic step of preparation of the surface of the layer (26) made of a second material being performed before assembly with the second substrate (30).

17. Method according to any of claims 1 to 16, an annealing step being performed after assembly of the layer (26) made of a second material with the second substrate (30).

18. Method according to any of claims 1 to 17, further comprising a step of thinning at least one of the two substrates (20, 30).

19. Method according to any of claims 1 to 18, said patterns (23) being produced by etching.

20. Semiconductor device comprising a superficial layer (20'), at least one buried or embedded layer (23, 26, 36), and a substrate (30), characterised in that the buried or embedded layer comprises a first sublayer (36, 26a, 26b) made of

amorphous or monocrystalline silicon, and a second sublayer comprises an alternation of patterns (23) of a first material and zones of amorphous or monocrystalline silicon.

21. Semiconductor device comprising a superficial layer (20'), at least one buried or embedded layer (22, 26), and a substrate (30), characterised in that the buried or embedded layer comprises a first sublayer comprising an alternation of patterns (23) made of a first material and zones made of a second, semiconductor material, and a second sublayer comprising zones (26a) of a first type of crystallinity and zones (26b) of a second type of crystallinity.

22. Device according to claim 21, said second sublayer being made of monocrystalline and/or polycrystalline and/or amorphous silicon.

23. Device according to any of claims 20 to 22, said first material being a dielectric material.

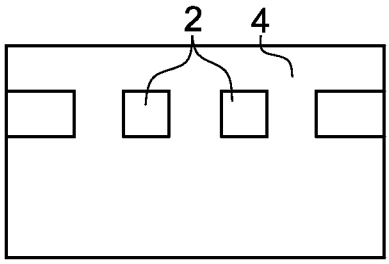

FIG. 1

FIG. 2A

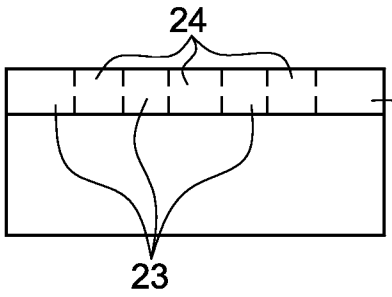

FIG. 2B

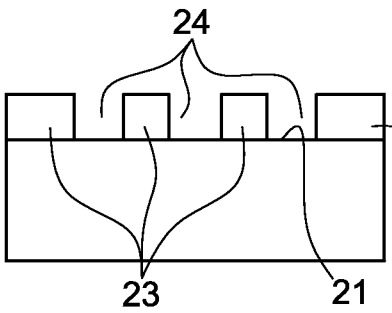

FIG. 2C

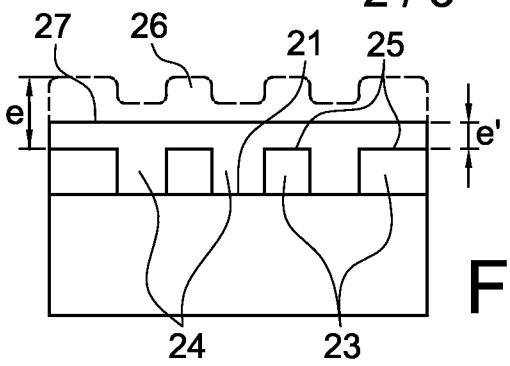

FIG. 2D

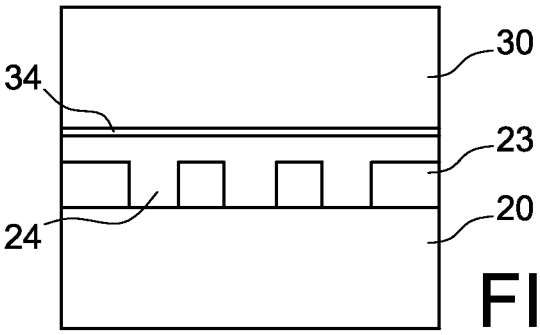

FIG. 2E

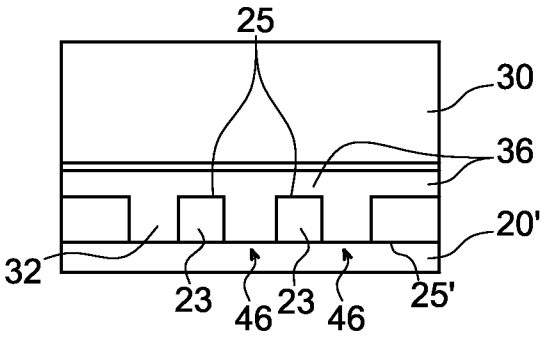

FIG. 2F

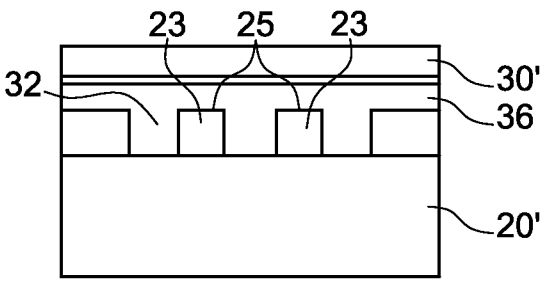

FIG. 2G

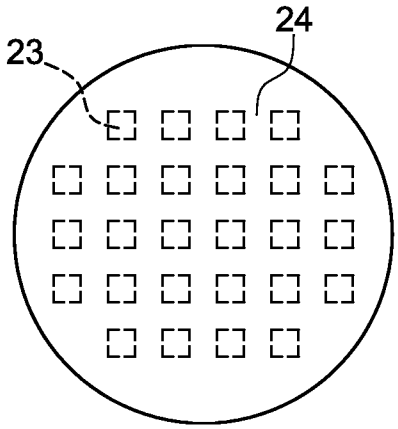

FIG. 3

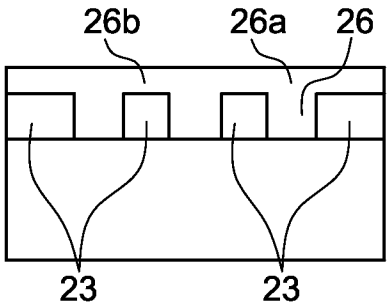

FIG. 4

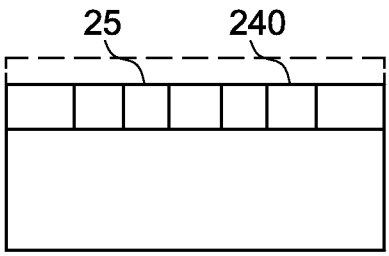

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2007/051783

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/762

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, INSPEC, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 191 007 B1 (MATSUI MASAKI [JP] ET AL) 20 February 2001 (2001-02-20)	1,2,4,5, 8-13, 15-23
A	page 11, line 65 - page 16, line 61; figures 1a-7d	3,6,7,14
A	EP 1 398 829 A2 (CANON KK [JP]) 17 March 2004 (2004-03-17) column 4, paragraph 24 - column 6, paragraph 37; figures 1a-1i	1-23
P,X	FR 2 876 220 A (COMMISSARIAT ENERGIE ATOMIQUE [FR]) 7 April 2006 (2006-04-07) page 17, line 18 - page 37, line 31; figures 1a-9e	1-23

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search	Date of mailing of the international search report
3 April 2007	11/04/2007

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Hedouin, Mathias

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2007/051783

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6191007 B1	20-02-2001	NONE	
EP 1398829 A2	17-03-2004	JP 2004103855 A	02-04-2004
		US 2004048454 A1	11-03-2004
FR 2876220 A	07-04-2006	WO 2006072871 A2	13-07-2006