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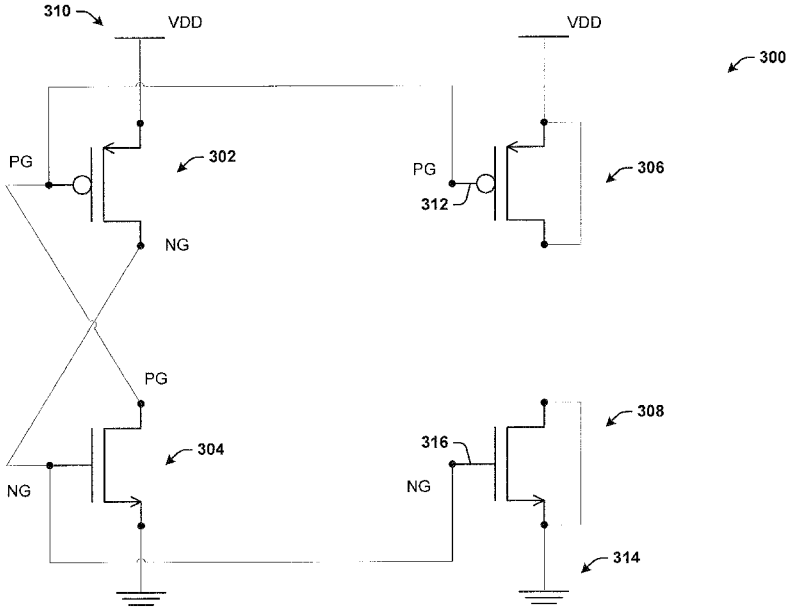
(54) Title: HIGH EFFICIENCY HALF-CROSS-COUPLED DECOUPLING CAPACITOR

FIG. 3



(57) Abstract: A decoupling capacitor circuit design facilitates high operational frequency without sacrificing area efficiency. In order to disassociate the sometimes opposing design criteria of high operational frequency and area efficiency, a p-channel field effect transistor (PFET) and an n-channel field effect transistor are connected in a half-cross-coupled (HCC) fashion. The HCC circuit is then supplemented by at least one area efficient capacitance (AEC) device. The half-cross-coupled transistors address the high frequency design requirement, while the AEC device(s) address the high area efficiency requirement. The design eliminates the undesirable trade-off between operating frequency and area efficiency inherent in some conventional DCAP designs.

WO 2016/200411 A1

HIGH EFFICIENCY HALF-CROSS-COUPLED DECOUPLING CAPACITOR

TECHNICAL FIELD

[0001] This disclosure relates generally to a decoupling capacitor circuit design for suppressing supply noise that provides high operational frequency and high area efficiency.

BACKGROUND

[0002] Decoupling capacitors (DCAPs) are an important component of power distribution networks (PDNs) for very-large-scale-integration (VLSI) designs. These decoupling capacitors shunt the supply noise caused by active circuit elements through the capacitor, thereby suppressing the supply noise observed by other elements of the circuit that are about to become active.

[0003] Several considerations are important to DCAP design, including high area efficiency, robust electrical properties, and properly targeted operational frequency. However, some DCAP designs are susceptible to damage from electro-static discharge (ESD) events, particularly as the transistor designs enter into ultra-deep sub-micron and finFET process nodes. Moreover, designs intended to render the DCAP more resistant to ESD damage are often hindered by an inherent trade-off between high area efficiency and high frequency operation.

SUMMARY

[0004] In an embodiment, a decoupling capacitor (DCAP) circuit is provided that yields high operational frequency without sacrificing area efficiency. In order to decouple the sometimes opposing design requirements of high operational frequency and area efficiency, a p-channel field effect transistor (PFET) and an n-channel field effect transistor are connected in a half-cross-coupled (HCC) fashion, and the resulting HCC circuit is supplemented by at least one area efficient capacitance (AEC) device. The half-cross-coupled FETs address the high frequency design requirement, while the AEC device(s) address the high area efficiency requirement. As a result, the size of the HCC FETs can set the operating frequency of the circuit independently of the area efficiency, while the size of the AEC device(s) can set the area efficiency

independently of the operating frequency. Thus, the DCAP design described herein eliminates the undesirable trade-off between operating frequency and area efficiency inherent in some conventional DCAP designs.

[0005] An embodiment provides a decoupling capacitor circuit comprising a first p-channel field effect transistor (PFET); a first n-channel field effect transistor (NFET); and at least one capacitive device, wherein a first PFET source and a first PFET body of the first PFET are connected to a voltage supply, a first NFET source and a first NFET body of the first NFET are connected to ground, the at least one capacitive device is connected to at least one of a first PFET gate of the first PFET or a first NFET gate of the first NFET, and inclusion of the at least one capacitive device increases an area efficiency of the decoupling capacitor circuit without changing a frequency response of the decoupling capacitor circuit.

[0006] A method for suppressing power supply noise is provided, comprising connecting a first source and a first body of a first p-channel field effect transistor (PFET) to a voltage supply; connecting a second source and a second body of an n-channel field effect transistor (NFET) to ground; connecting a first drain of the first PFET to a first gate of the NFET; connecting a second drain of the NFET to a second gate of the first PFET; connecting a third drain, a third source, and a third body of a second PFET to the voltage supply; and connecting a third gate of the second PFET to the second gate of the first PFET.

[0007] An embodiment provides a system for suppressing power supply noise, comprising a first p-channel field effect transistor (PFET), wherein a first PFET source and a first PFET body of the first PFET are connected to a voltage supply; a first n-channel field effect transistor (NFET), wherein a first NFET source and a first NFET body of the first NFET are connected to ground; and a second NFET, wherein a first PFET drain of the first PFET is connected to a first NFET gate of the first NFET, a first NFET drain of the first NFET is connected to a first PFET gate of the PFET, a second NFET drain, a second NFET source, and a second NFET body of the second NFET is connected to ground, and a second NFET gate of the second NFET is connected to the first NFET gate of the first NFET.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] **FIG. 1** is a circuit diagram illustrating an example approach to DCAP design.

[0009] **FIG. 2** is a circuit diagram illustrating an example half-cross-coupled DCAP design approach.

[0010] **FIG. 3** is a circuit diagram of an example DCAP design that provides high area efficiency and high frequency operation.

[0011] **FIG. 4** is a circuit diagram of an example DCAP design that uses a single PFET AEC device.

[0012] **FIG. 5** is a circuit diagram of an example DCAP design that uses a single NFET AEC device.

[0013] **FIG. 6** is a graph illustrating the frequency response for the DCAP circuit of FIG. 3 for various sizes of AEC devices.

[0014] **FIG. 7** is a circuit diagram of an example DCAP design that includes an AEC device comprising a PFET having a gate tied to the NG node, a source and drain tied to ground, and a body tied to VDD.

[0015] **FIG. 8** is a circuit diagram of an example DCAP design that includes an AEC device comprising an NFET having a gate tied to node PG, a drain and source tied to VDD, and body tied to ground.

[0016] **FIG. 9** is a circuit diagram of an example DCAP design that includes a PFET AEC device of FIG. 7 and an NFET AEC device of FIG. 8.

[0017] **FIG. 10** is a circuit diagram of an example DCAP design that includes a first PFET AEC device of FIG. 4 and a second PFET AEC device of FIG. 7.

[0018] **FIG. 11** is a circuit diagram of an example DCAP design that includes a first NFET AEC device of FIG. 5 and a second NFET AEC device of FIG. 8.

[0019] **FIG. 12** is a circuit diagram of an example DCAP design that includes a PFET AEC device of FIG. 4 and an NFET AEC device of FIG. 8.

[0020] **FIG. 13** is a circuit diagram of an example DCAP design that includes an NFET AEC device of FIG. 5 and a PFET AEC device of FIG. 7.

[0021] **FIG. 14** illustrates a flow diagram of an embodiment for manufacturing a decoupling capacitor (DCAP) circuit.

DETAILED DESCRIPTION

[0022] DCAPs are often used in power distribution networks of VLSI systems to suppress voltage supply noise or ripples induced by active circuit elements, thereby shielding other elements of the circuit from power supply voltage fluctuations that may damage the elements or impede their functions. Robust DCAP designs are characterized by high area efficiency, robust electrical properties, and properly targeted operational frequency. In the case of on-die DCAP design, the targeted operational frequency ranges from the operating frequency to the switching slew of the gates in the design, thus constituting the high operational frequency of the DCAP used in the power distribution network.

[0023] FIG. 1 is a circuit diagram illustrating one approach to DCAP design. According to this design approach, the drain, source, and body of the p-channel field effect transistor (PFET) 102 is directly tied to the supply voltage 106, and the drain, source, and body of the n-channel field effect transistor (NFET) 104 is tied to ground. The gate 110 of the PFET 102 is tied to ground, and the gate 112 of the NFET 104 is tied to the supply voltage 106. This design can decouple supply noise to high operating frequencies while being area efficient. However, as the transistor designs enter into ultra-deep sub-micron and finFET process nodes, the gate oxides become exceedingly thin. Consequently, the design in FIG. 1 can become vulnerable to electro-static discharge (ESD) events that may cause damage to the gate oxide and short out the supply and ground nodes. Since the gates 110 and 112 are directly connected to the supply and ground nodes, the design in FIG. 1 may not be able to tolerate extreme ESD events even in the presence of ESD clamps. Designs that use metal gate material rather than poly-silicon are particularly susceptible to this problem.

[0024] FIG. 2 is a circuit diagram illustrating another DCAP design approach that attempts to address this issue by tying the source and body of the PFET 202 to the supply voltage 208 and the source and body of the NFET 204 to ground 206, while connecting the drain and gate nodes of the PFET and NFET in a half-cross-coupled (HCC) fashion. That is, the drain 210 of PFET 202 is connected to the gate 212 of NFET 204, while the drain 214 of NFET 204 is connected to the gate 216 of PFET 202. This design provides a resistive path

from the supply voltage and ground nodes to the gate through device channels, thereby protecting the gate oxide during an ESD event until the ESD clamp can shunt the excess charge.

[0025] However, using the design in FIG.2, it is difficult to achieve both high area efficiency and high frequency operation. This is because the HCC connectivity places these two design targets in direct conflict. For example, to achieve high area efficiency the PFET 202 and NFET 204 would require large channels to maximize the gate area. However, these large channels would add resistance to the decoupling path, thereby limiting the type of high frequency decoupling the capacitor circuit may achieve. If the channel lengths were reduced in the PFET 202 and NFET 204 to address this concern, the area efficiency would be penalized.

[0026] Moreover, a large channel for the design depicted in FIG. 2 will result in a high start-up time. This high start-up time is due to a "dead" zone in which the HCC nodes are brought up in states opposite to the values they require for the DCAP to function, and the design depends on the device leakage of the two FETS 202 and 204 to set the correct state values. A large channel will reduce this device leakage, resulting in a large increase in start-up time before the DCAP will be useful.

[0027] To address these and other issues, one or more embodiments described herein provide a DCAP circuit design that maintains the high frequency operation offered by the HCC DCAP's electrical properties, while also achieving high area efficiency. FIG. 3 is a circuit diagram of an example DCAP circuit 300 that provides high area efficiency and high frequency operation. This design includes a PFET 302 and an NFET 304 connected in an HCC configuration, and area efficient capacitance (AEC) devices 306 and 308 that serve as an area efficiency decoupling capacitor. The AEC devices 306 and 308 can comprise, for example, a second PFET and a second NFET, respectively. With AEC devices 306 and 308 in place, the HCC devices can be optimized to provide a high frequency response without being limited by the conflicting design requirements of high area efficiency.

[0028] According to this design, the drain, source, and body of PFET AEC device 306 are connected to the supply voltage 310, while the gate 312 is connected to the PG node produced by the HCC connections. The drain,

source, and body of NFET AEC device 308 is connected to ground 314, while the gate 316 is connected to the NG node produced by the HCC connections.

[0029] The circuit 300 depicted in FIG. 3 allows the device channel length of the HCC devices (PFET 302 and NFET 304) – and thus the corresponding resistance of the decoupling path through the PFET and NFET – to be kept low, thereby providing high frequency supply noise decoupling. Keeping the device channel length low also increases leakage in the HCC devices, thereby keeping start-up times low for scenarios in which the HCC connectivity is initialized to the incorrect states.

[0030] Whereas the HCC devices 302 and 304 achieve high frequency operation, the AEC devices 306 and 308 can be optimized to provide high area efficiency. In this regard, the AEC devices 306 and 308 can be sized to provide high area efficiency without changing the channel length (and resistance) of the decoupling path through the PFET 302 and NFET 304, and thus without changing the operating frequency of the circuit 300. In some cases, optimizing the AEC devices 306 and 308 for high area efficiency corresponds to having a large length (L). By satisfying the high frequency operation requirement using the HCC devices 302 and 304, and the high area efficiency requirement using the AEC devices 306 and 308, the design depicted in FIG. 3 effectively unlocks the high frequency component from the area efficiency component, allowing the design to be optimized to address high frequency applications without sacrificing area efficiency.

[0031] Although circuit 300 includes two AEC devices 306 and 308 corresponding to the PFET 302 and NFET 304, respectively, some embodiments may include only one AEC device. FIG. 4 illustrates an embodiment in which only the PFET AEC device 306 is connected to the HCC circuit (omitting the NFET AEC device 308), while FIG. 5 illustrates an embodiment in which only the NFET AEC device 308 is connected (omitting the PFET AEC device 306).

[0032] FIG. 6 is a graph 602 illustrating the frequency response for circuit 300 for various sizes of AEC devices 306 and 308. Each plot of graph 602 represents the frequency response for a given size of AEC devices 306 and 308, with the sizes of the HCC devices 302 and 304 kept constant for each plot. For each scenario, the roll-off frequency ω – that is, the frequency at which

the capacitance of circuit 300 loses its effectiveness – is characterized by 1/(RC), where R is the resistance of the decoupling path determined by the size of the HCC devices 302 and 304, and C is the capacitance determined by the size of the AEC devices 306 and 308. As the capacitance of the AEC devices 306 and 308 increases, the roll-off frequency ω decreases. As a general design consideration, as the sizes of the AEC devices 306 and 308 increase, the HCC devices 302 and 304 can also be increased in order keep up with the increased capacitance of the AEC devices and thereby maintain high frequency supply noise decoupling. In general, the ratio between the sizes of the HCC devices 302 and 304 to the capacitance on the AEC devices 306 and 308 determines the degree of high frequency operation.

[0033] In addition to AEC devices 306 and 308, other types of AEC devices are also within the scope of one or more embodiments of this disclosure. For example, FIG. 7 is a circuit diagram of an example DCAP circuit 700 that includes an AEC device 702 comprising a PFET having gate 704 tied to the NG node, source and drain tied to ground 314, and body tied to VDD 310. FIG. 8 is a circuit diagram of an example DCAP circuit 800 that includes an AEC device 802 comprising an NFET having gate 804 tied to node PG, drain and source tied to VDD 310, and body tied to ground 314. FIG. 9 is a circuit diagram of an example DCAP circuit 900 that includes both AEC devices 702 and 802.

[0034] AEC devices 306, 308, 702, and 802 can be combined in any permutation to yield a DCAP circuit. For example, FIG. 10 is a circuit diagram of an example DCAP circuit 1000 that includes AEC device 702 and AEC device 306, while FIG. 11 is a circuit diagram of an example DCAP circuit 1100 that includes AEC device 802 and AEC device 308.

[0035] FIG. 12 is a circuit diagram of another example DCAP circuit 1200 that includes AEC devices 306 and 802. In this example, the gates of both AEC devices are connected to the PG node. FIG. 13 is a circuit diagram of yet another example DECAP circuit 1300 that includes AEC devices 308 and 702. In this example, the gates of both AEC devices are connected to the NG node.

[0036] The decoupling capacitor circuits described above and illustrated in FIGs. 3-5 and FIGS. 7-13 can be embodied using any suitable FET

implementation. For example, any of circuits 300, 400, 500, 700, 800, 900, 1000, 1100, 1200, and/or 1300 can be embodied as an integrated circuit that can be used to provide supply noise suppression for a power distribution network of a VLSI system. Any of circuits 300, 400, 500, 700, 800, 900, 1000, 1100, 1200, or 1300 can be implemented as an on-chip component of such VLSI systems, or as an off-chip component embodied on a dedicated integrated circuit that provides supply voltage suppression for a VLSI system residing on a separate chip. In other embodiments, any of circuits, 400, 500, 700, 800, 900, 1000, 1100, 1200, or 1300 may be constructed using solid state components.

[0002] FIG. 14 illustrates a methodology in accordance with one or more embodiments. While the methodology shown herein is shown as a series of acts, the subject innovation is not limited by the order of acts, as some acts may, in accordance therewith, occur in a different order and/or concurrently with other acts from that shown and described herein. For example, those skilled in the art will understand and appreciate that a methodology could alternatively be represented as a series of interrelated states or events, such as in a state diagram. Moreover, not all illustrated acts may be required to implement a methodology in accordance with the innovation. Furthermore, interaction diagram(s) may represent methodologies, or methods, in accordance with the subject disclosure when disparate entities enact disparate portions of the methodologies. Further yet, two or more of the disclosed example methods can be implemented in combination with each other, to accomplish one or more features or advantages described herein.

[0037] FIG. 14 is a flow diagram of an embodiment for assembling a decoupling capacitor (DCAP) circuit. The DCAP circuit can be used, for example as a component of power distribution networks (PDNs). Method 1400 can begin at block 1402, where the source and body of a first p-channel field effect transistor (PFET) is connected to a supply voltage (e.g., a supply voltage of a power distribution network or other system requiring supply noise suppression). At block 1404, the source and body of a first n-channel field effect transistor (NFET) is connected to ground. At block 1406, the drain of the first PFET is connected to the gate of the first NFET. At block 1408, the drain of the first NFET is connected to the gate of the first PFET.

[0038] At block 1410 the drain, source, and body of a second PFET is connected to the supply voltage. At block 1412, the gate of the second PFET is connected to the gate of the first PFET. At block 1414, the drain, source, and body of a second NFET is connected to ground. At block 1416, the gate of the second NFET is connected to the gate of the first NFET. The circuit yielded by blocks 1402-1416 can be used to suppress power supply noise, and can achieve high area efficiency as well as high frequency operation.

[0039] In some embodiments, either of the second PFET or the second NFET can be omitted from the circuit (see, e.g., FIGS. 4 and 5). That is, in some embodiments, blocks 1410 and 1412 can be omitted, while in other embodiments blocks 1414 and 1416 can be omitted.

[0040] The disclosed subject matter can be implemented as a method, apparatus, or article of manufacture using typical manufacturing, programming or engineering techniques to produce hardware, firmware, software, or any suitable combination thereof to control an electronic device to implement the disclosed subject matter. Computer-readable media can include hardware media, software media, non-transitory media, or transport media.

CLAIMS

What is claimed is:

1. A decoupling capacitor circuit, comprising:

a first p-channel field effect transistor (PFET);

a first n-channel field effect transistor (NFET); and

at least one capacitive device,

wherein

a first PFET source and a first PFET body of the first PFET are connected to a voltage supply,

a first NFET source and a first NFET body of the first NFET are connected to ground,

the at least one capacitive device is connected to at least one of a first PFET gate of the first PFET or a first NFET gate of the first NFET, and

inclusion of the at least one capacitive device increases an area efficiency of the decoupling capacitor circuit without changing a frequency response of the decoupling capacitor circuit.

2. The decoupling capacitor circuit of claim 1, wherein

a first PFET drain of the first PFET is connected to the first NFET gate of the first NFET, and

a first NFET drain of the first NFET is connected to the first PFET gate of the first PFET.

3. The decoupling capacitor circuit of claim 2, wherein

the at least one capacitive device comprises a second PFET,

a second PFET drain, a second PFET source, and a second PFET body of the second PFET are connected to the voltage supply, and

a second PFET gate of the second PFET is connected to the first PFET gate of the first PFET.

4. The decoupling capacitor circuit of claim 2, wherein

the at least one capacitive device comprises a second NFET,

a second NFET drain, a second NFET source, and a second NFET body of the second NFET are connected to ground, and

a second NFET gate of the second NFET is connected to the first NFET gate of the first NFET.

5. A method for suppressing power supply noise, comprising:

connecting a first source and a first body of a first p-channel field effect transistor (PFET) to a voltage supply;

connecting a second source and a second body of an n-channel field effect transistor (NFET) to ground;

connecting a first drain of the first PFET to a first gate of the NFET;

connecting a second drain of the NFET to a second gate of the first PFET;

connecting a third drain, a third source, and a third body of a second PFET to the voltage supply; and

connecting a third gate of the second PFET to the second gate of the first PFET.

6. The method of claim 5, wherein the NFET comprises a first NFET, and the method further comprises:

connecting a fourth drain, a fourth source, and a fourth body of a second NFET to ground; and

connecting a fourth gate of the second NFET to the first gate of the first NFET.

7. The method of claim 5, wherein the connecting the first source and the first body of the first PFET to the voltage supply comprises connecting to a voltage supply of a power distribution network.

8. A system for suppressing power supply noise, comprising:

a first p-channel field effect transistor (PFET), wherein a first PFET source and a first PFET body of the first PFET are connected to a voltage supply;

a first n-channel field effect transistor (NFET), wherein a first NFET source and a first NFET body of the first NFET are connected to ground; and

a second NFET,

wherein

a first PFET drain of the first PFET is connected to a first NFET gate of the first NFET,

a first NFET drain of the first NFET is connected to a first PFET gate of the PFET,

a second NFET drain, a second NFET source, and a second NFET body of the second NFET is connected to ground, and

a second NFET gate of the second NFET is connected to the first NFET gate of the first NFET.

9. The system of claim 8, further comprising a second PFET, wherein

a second PFET drain, a second PFET source, and a second PFET body of the second PFET are connected to the voltage supply, and

a second PFET gate of the second PFET is connected to the first PFET gate of the first PFET.

10. The system of claim 8, wherein

inclusion of the second NFET increases an area efficiency of the system without increasing a channel length of the first PFET and the first NFET, and

the voltage supply is a voltage supply of a power distribution network of a very-large-scale-integration (VLSI) system.

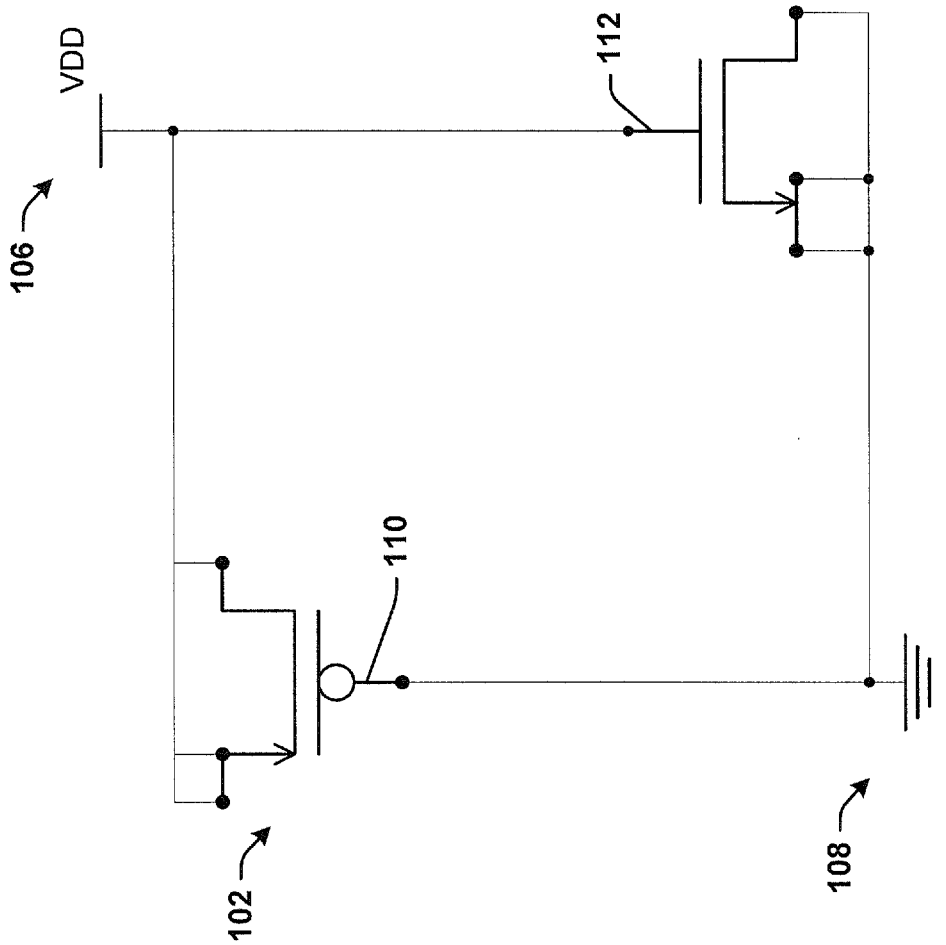
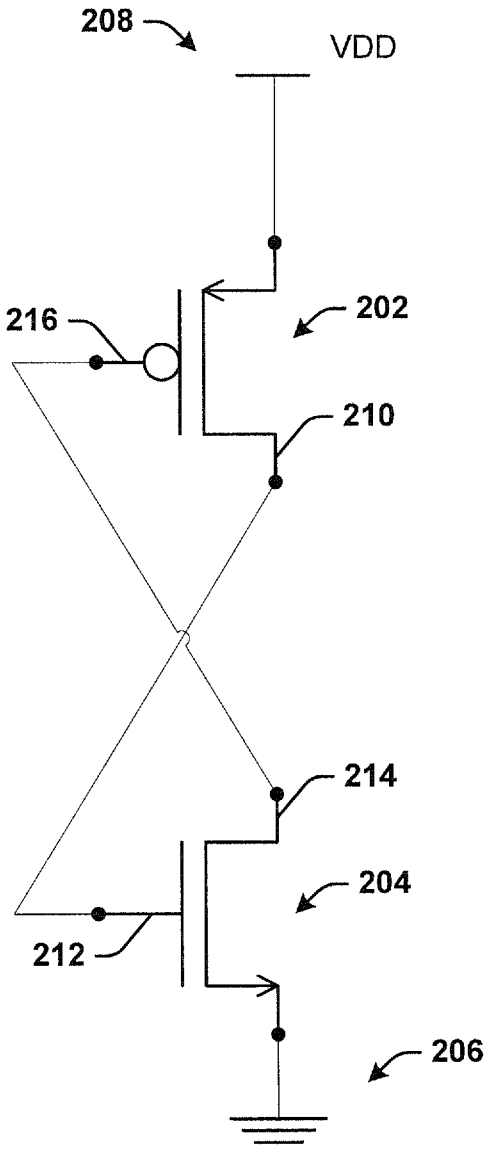


FIG. 1
PRIOR ART



PRIOR ART

FIG. 2

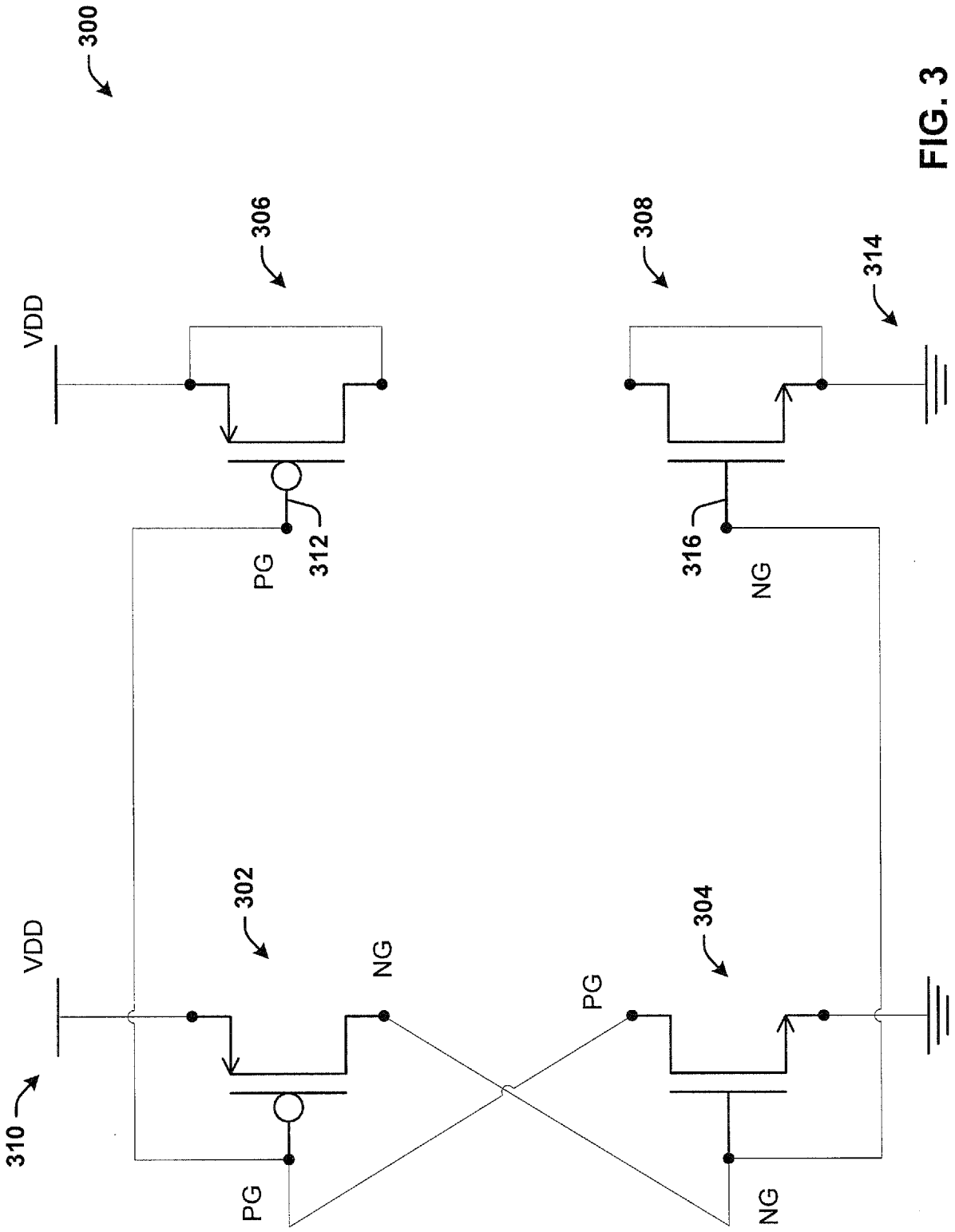


FIG. 3

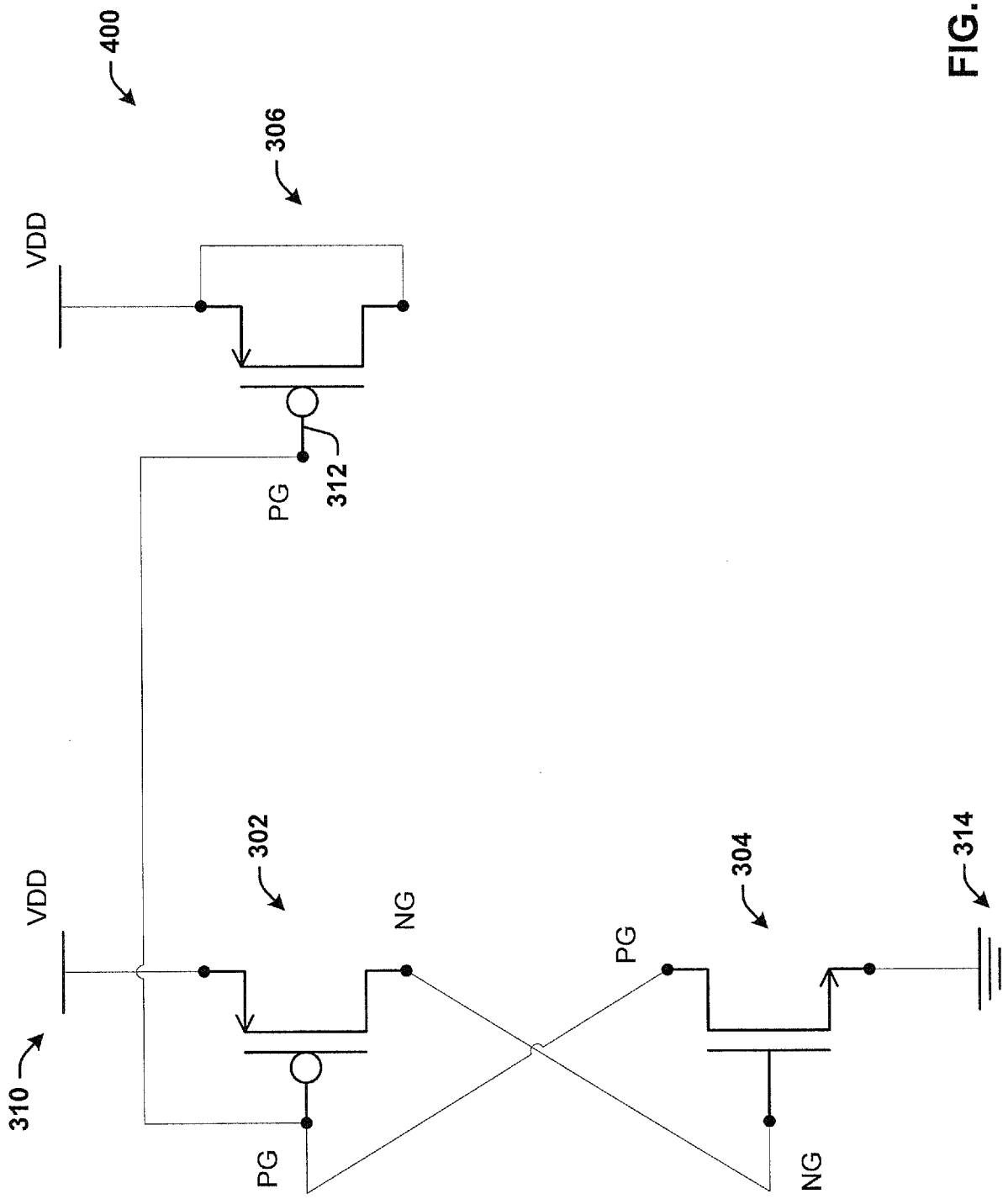


FIG. 4

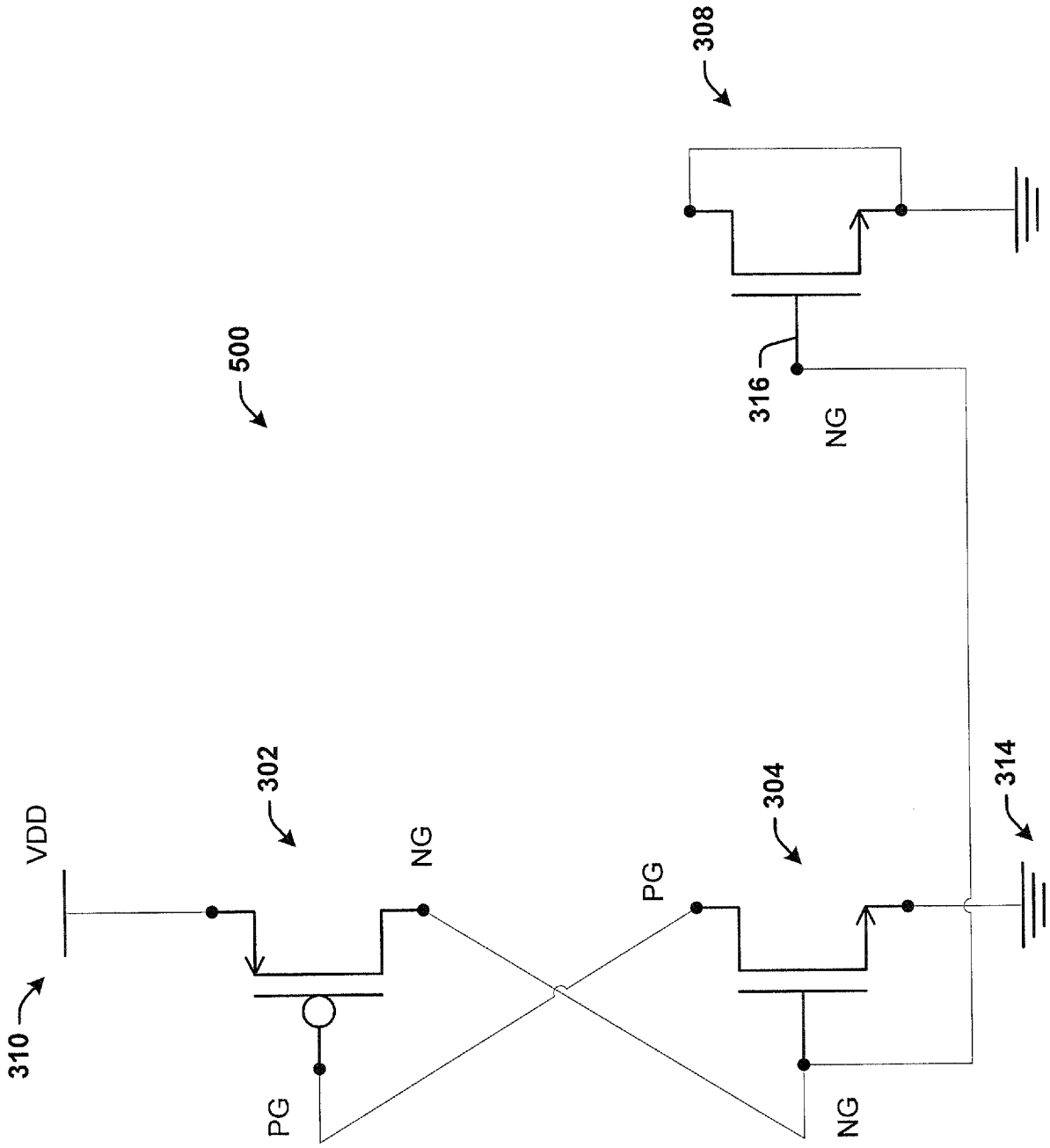


FIG. 5

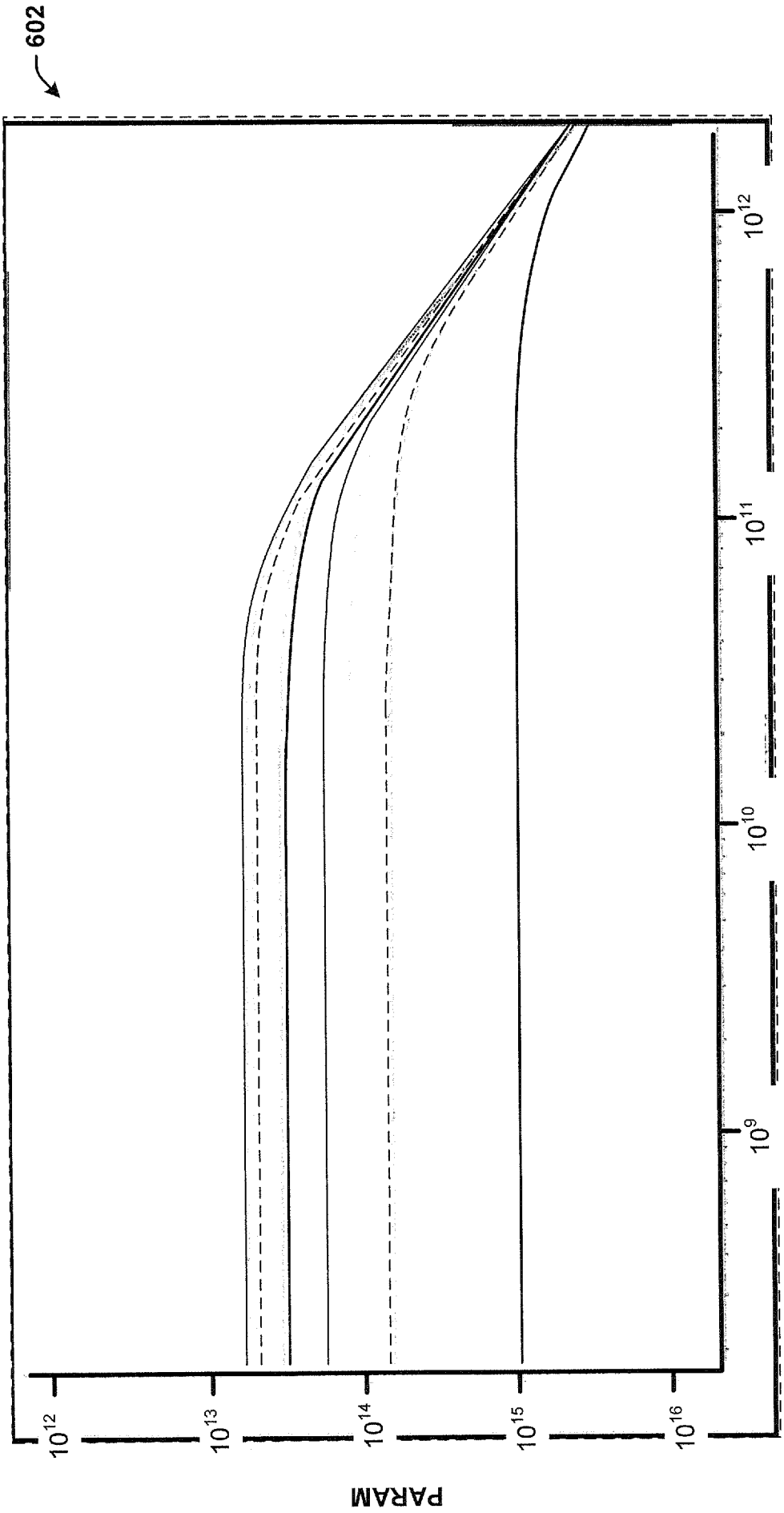

602
PARAM
10^{12}
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FIG. 6

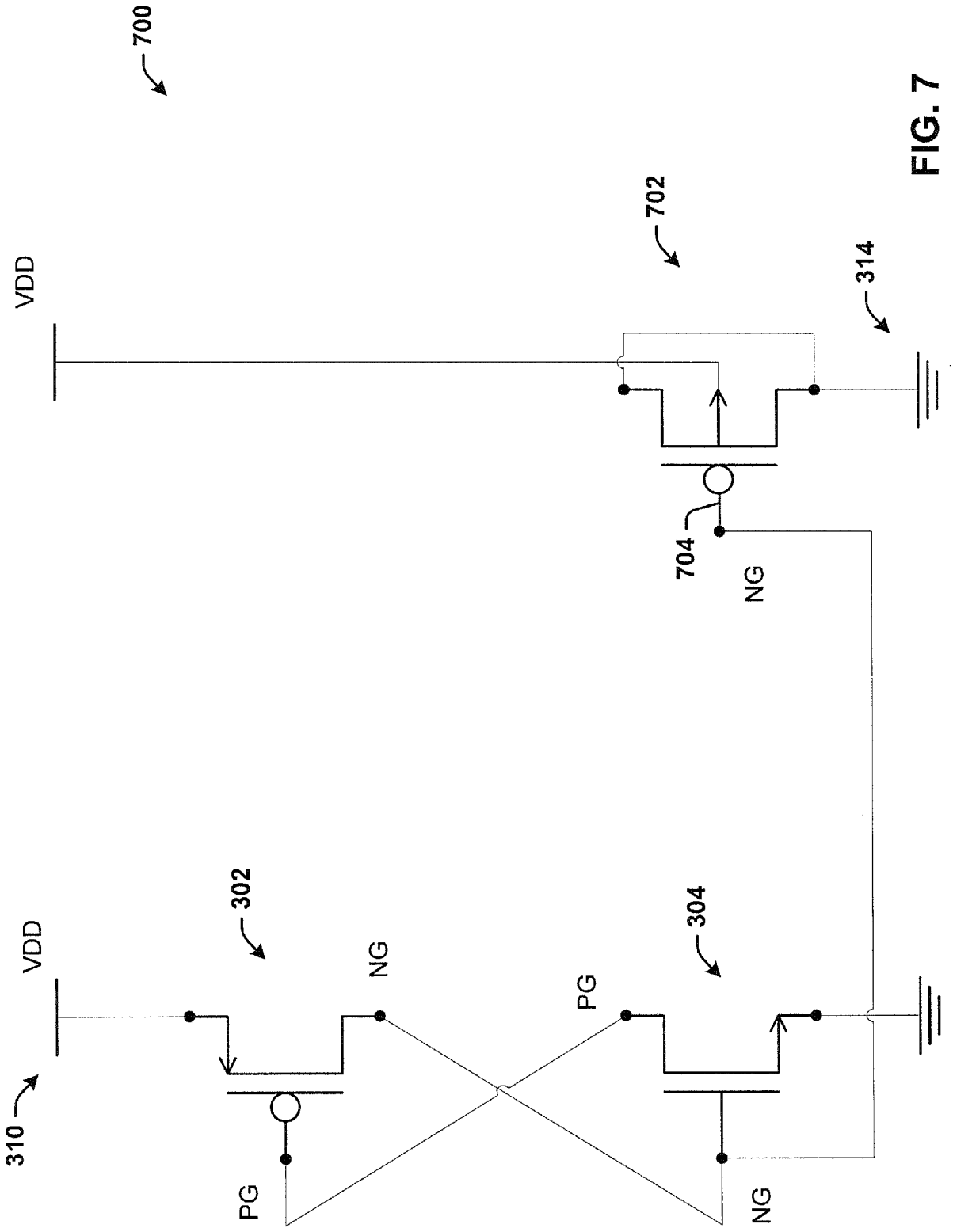

FIG. 7

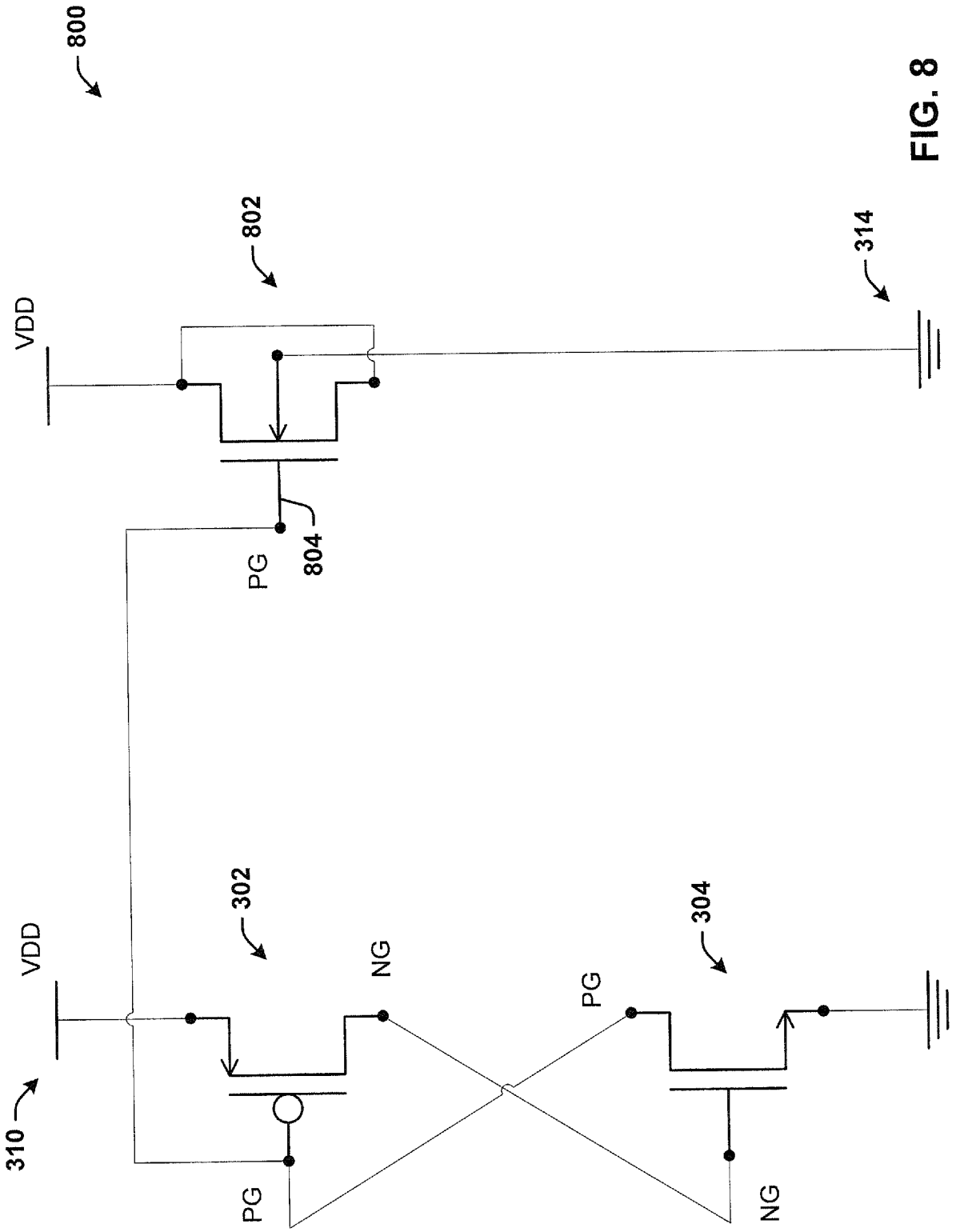

FIG. 8

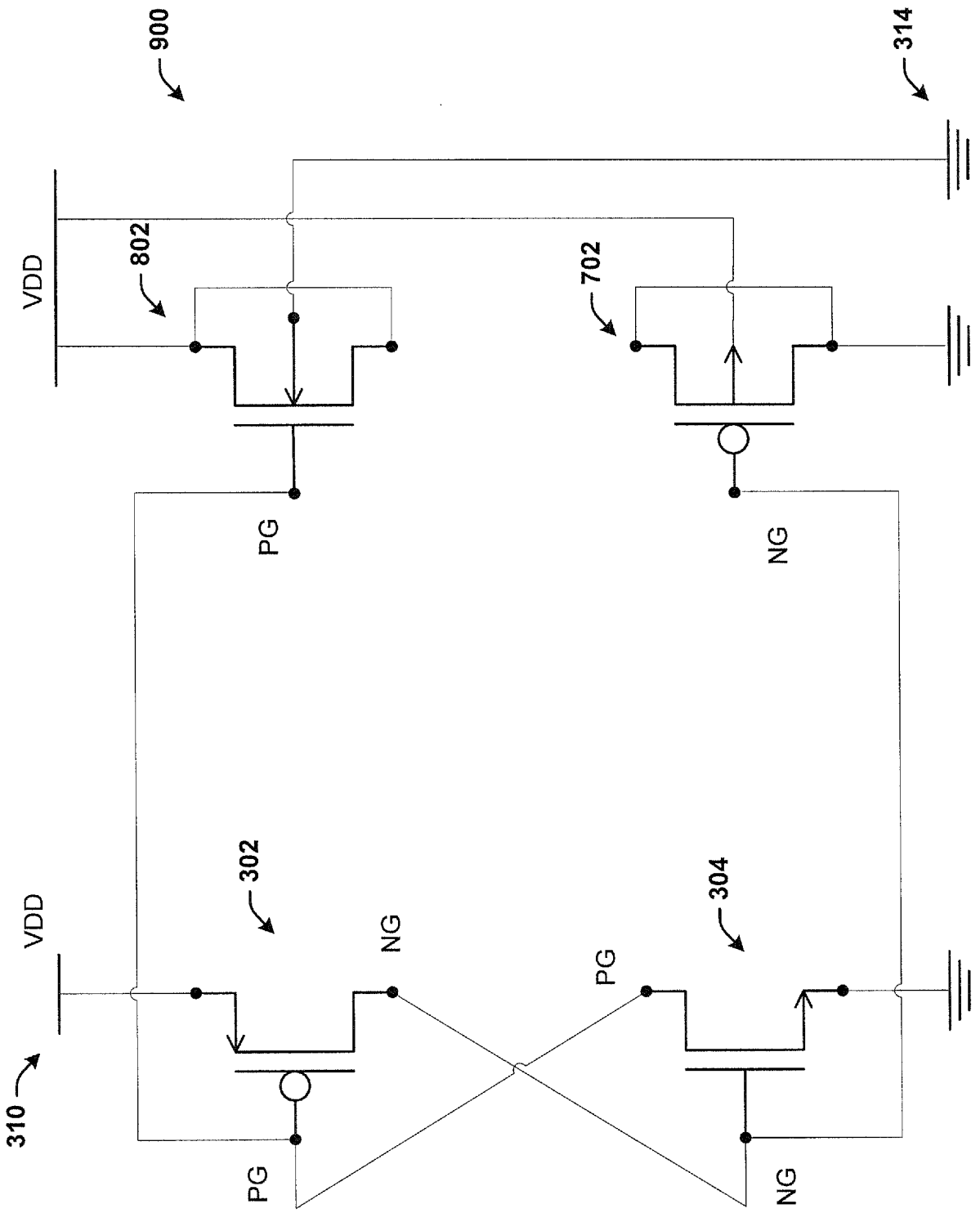

FIG. 9

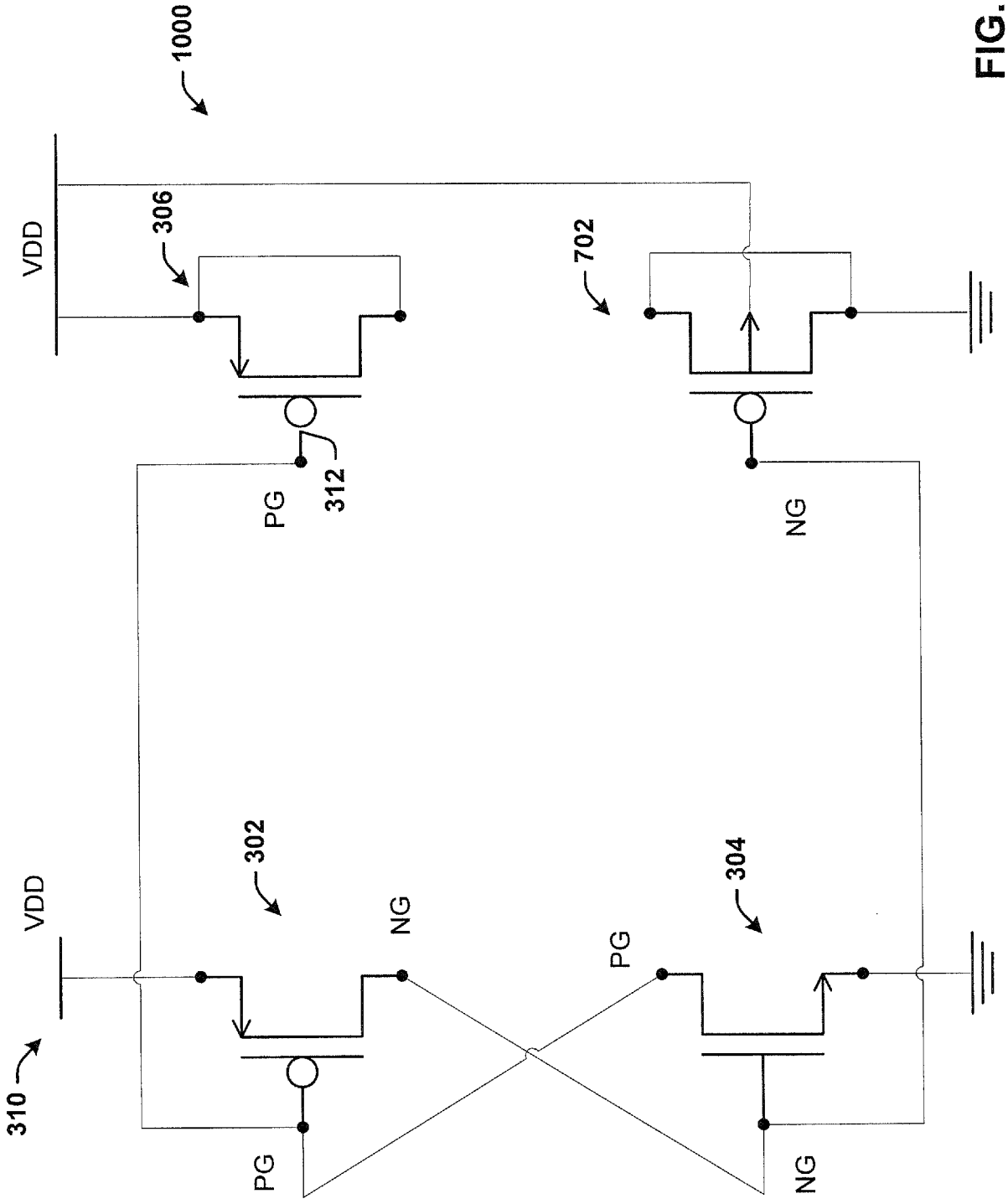

FIG. 10

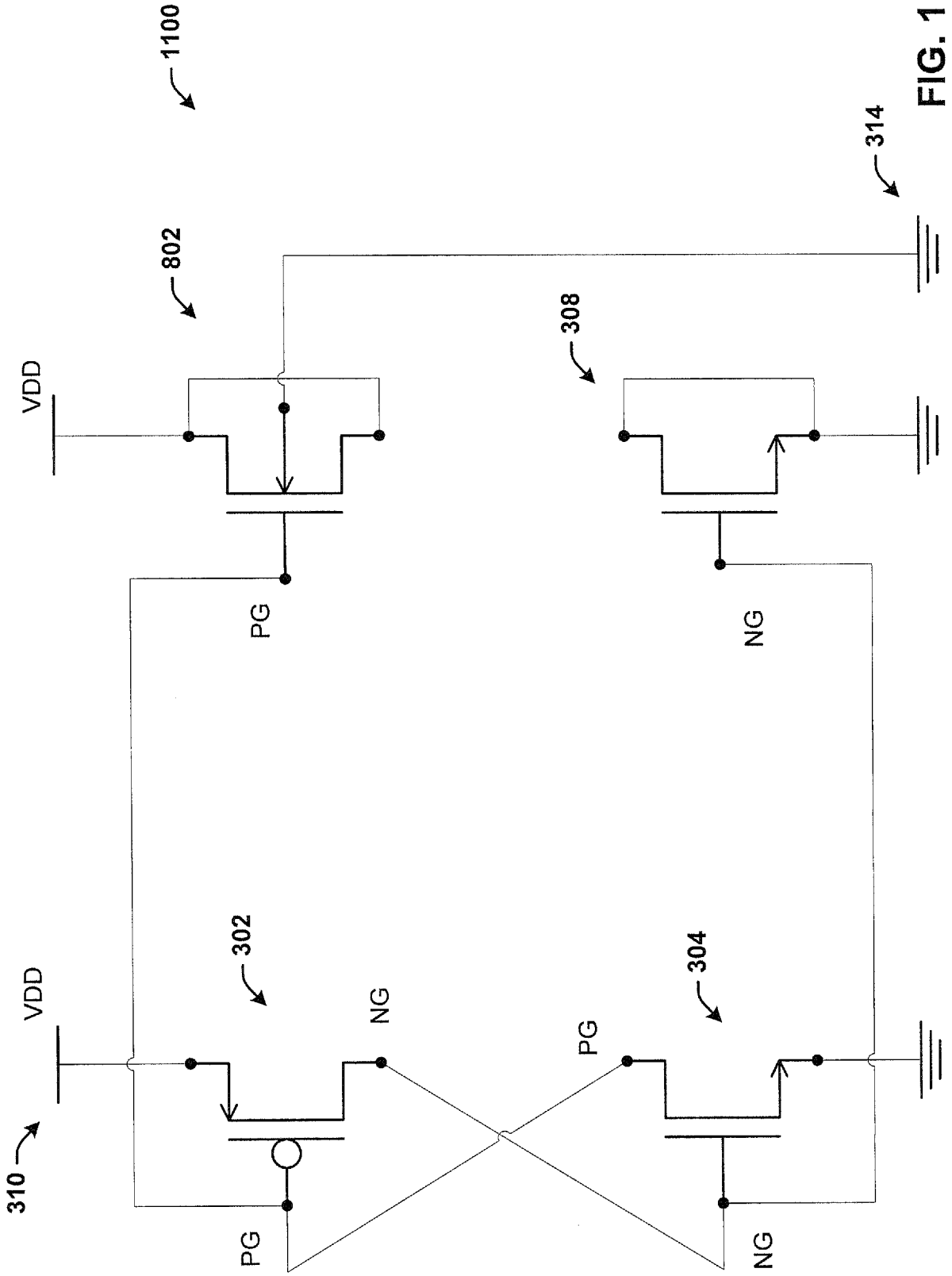

FIG. 11

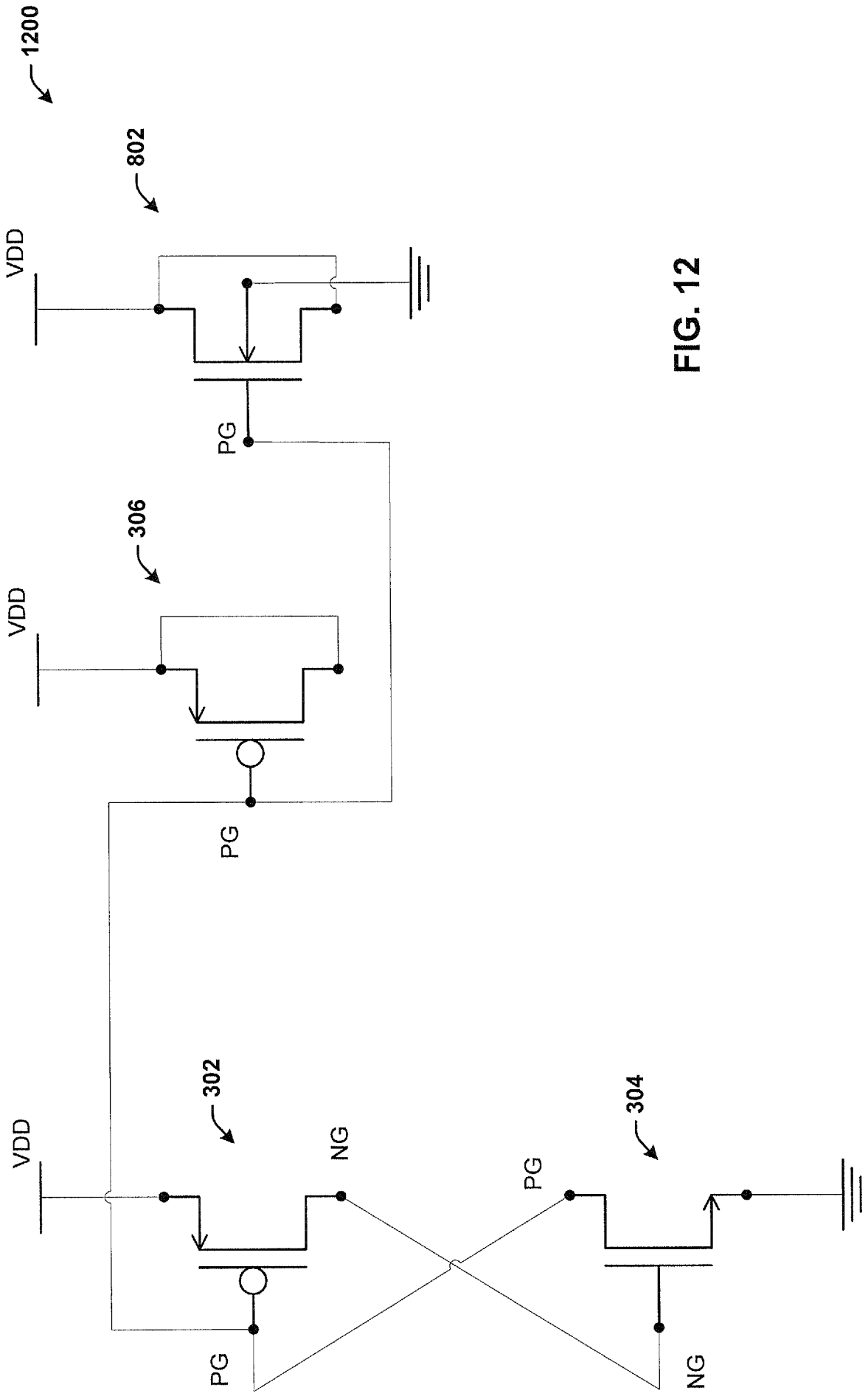

FIG. 12

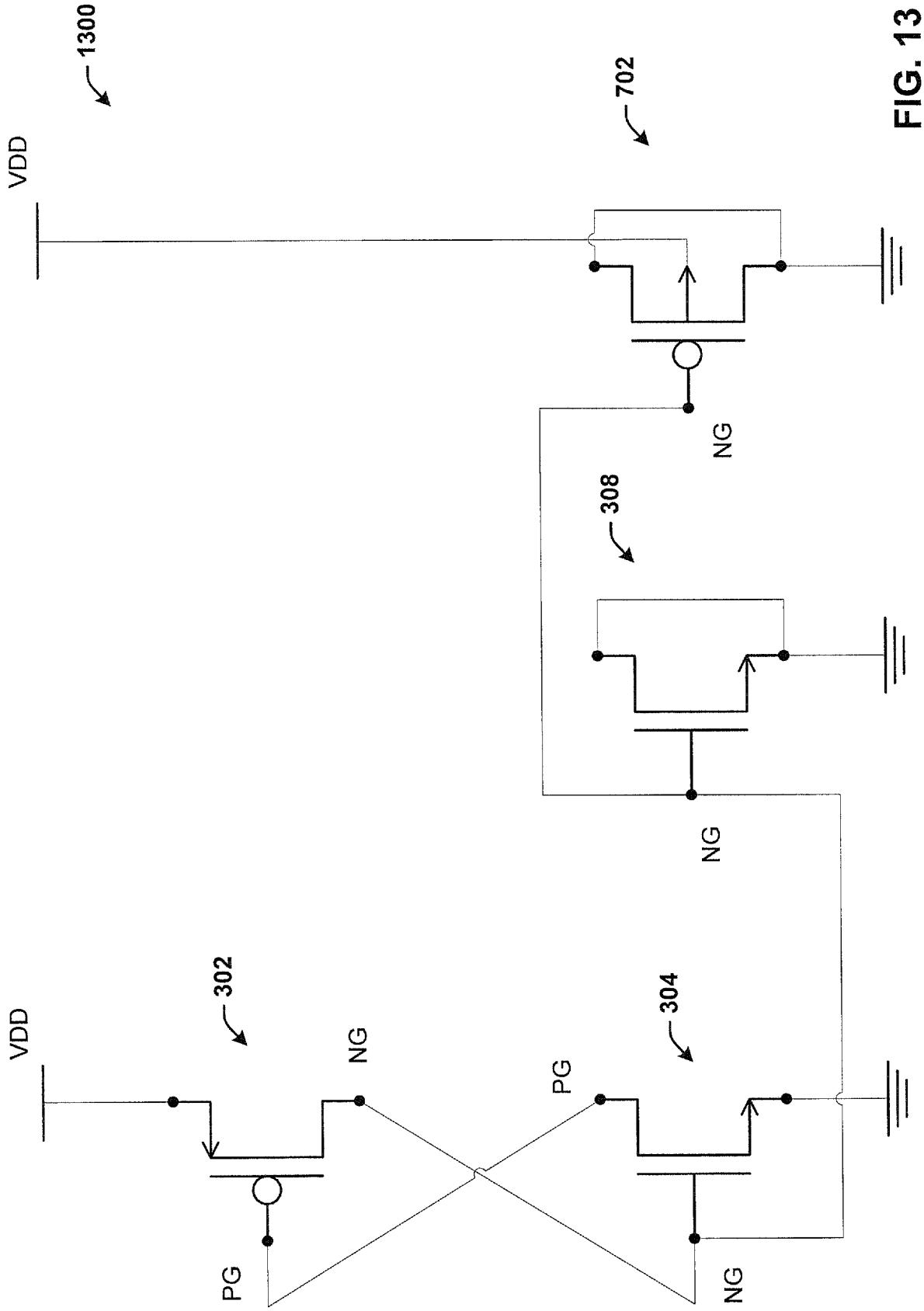

FIG. 13

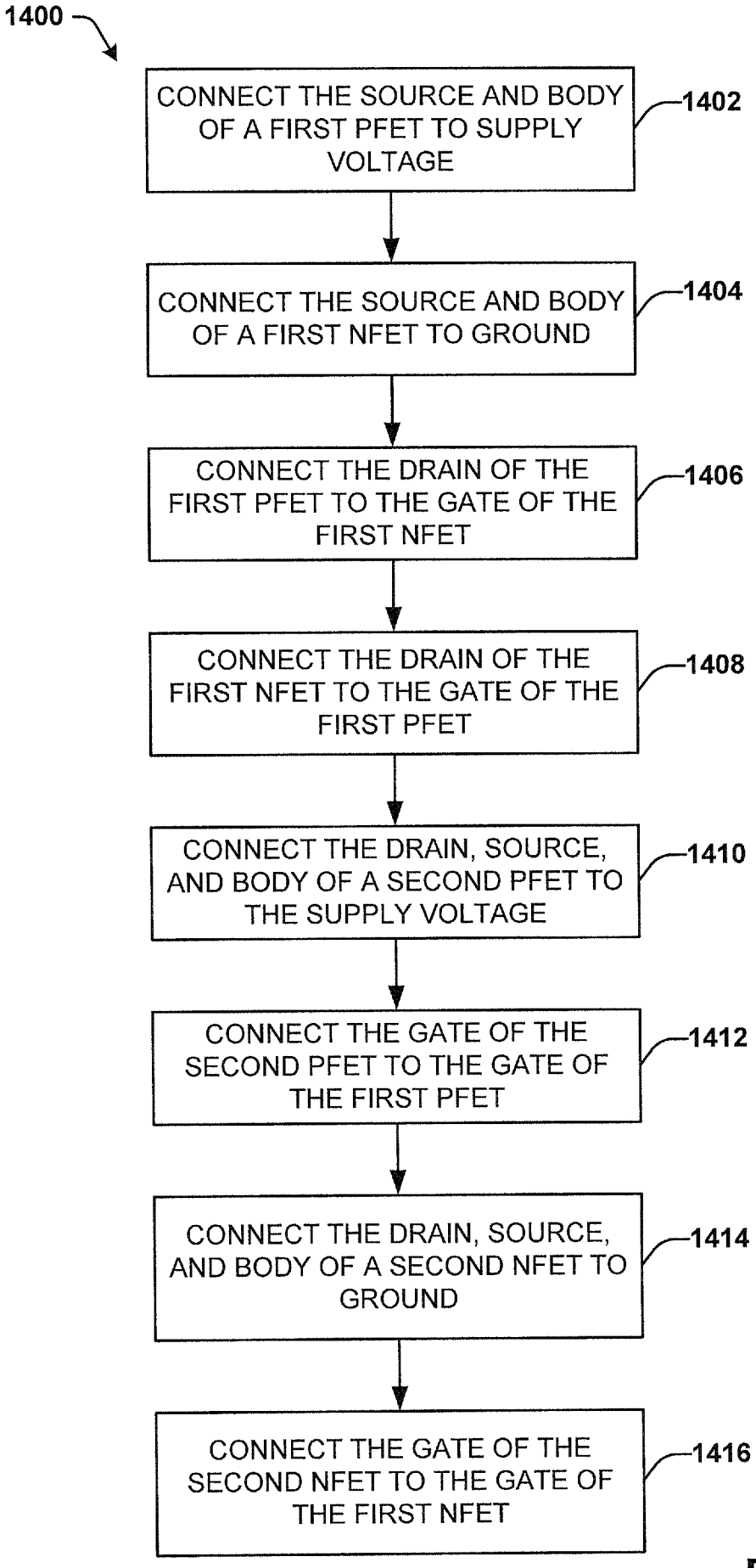
1400
CONNECT THE SOURCE AND BODY OF A FIRST PFET TO SUPPLY VOLTAGE
1402
CONNECT THE SOURCE AND BODY OF A FIRST NFET TO GROUND
1404
CONNECT THE DRAIN OF THE FIRST PFET TO THE GATE OF THE FIRST NFET
1406
CONNECT THE DRAIN OF THE FIRST NFET TO THE GATE OF THE FIRST PFET
1408
CONNECT THE DRAIN, SOURCE, AND BODY OF A SECOND PFET TO THE SUPPLY VOLTAGE
1410
CONNECT THE GATE OF THE SECOND PFET TO THE GATE OF THE FIRST PFET
1412
CONNECT THE DRAIN, SOURCE, AND BODY OF A SECOND NFET TO GROUND
1414
CONNECT THE GATE OF THE SECOND NFET TO THE GATE OF THE FIRST NFET
1416

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2015/042798

A. CLASSIFICATION OF SUBJECT MATTER

H03K 19/094(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K 19/094; H03K 19/0175; H03K 5/12; H03K 17/16; H03K 17/687; H03K 19/003; G11C 11/409

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: decoupling capacitor, p-channel field effect transistor (PFET), n-channel field effect transistor (NFET), capacitive device, area efficiency

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 08-307229 A (FUJI ELECTRIC CO., LTD.) 22 November 1996 See abstract, paragraphs [0011]-[0015], claim 1 and figure 1.	1-10
A	JP 11-191729 A (KAWASAKI STEEL CORP.) 13 July 1999 See paragraphs [0036]-[0070], claim 1 and figure 1.	1-10
A	JP 08-102652 A (SEIKO EPSON CORP.) 16 April 1996 See paragraphs [0017]-[0028], claim 1 and figure 1.	1-10
A	JP 09-093111 A (TOSHIBA MICROELECTRON CORP. et al.) 04 April 1997 See paragraphs [0023]-[0049], claim 1 and figure 1.	1-10
A	JP 09-148909 A (HITACHI LTD.) 06 June 1997 See paragraphs [0014]-[0030], claim 1 and figure 1.	1-10

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
06 April 2016 (06.04.2016)	**08 April 2016 (08.04.2016)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2015/042798

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 08-307229 A	22/11/1996	None	
JP 11-191729 A	13/07/1999	JP 3838769 B2	25/10/2006
JP 08-102652 A	16/04/1996	None	
JP 09-093111 A	04/04/1997	None	
JP 09-148909 A	06/06/1997	None	