

(51) International Patent Classification:
H01L 21/336 (2006.01)(21) International Application Number:
PCT/US2014/011934(22) International Filing Date:
16 January 2014 (16.01.2014)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
13/839,533 15 March 2013 (15.03.2013) US(71) Applicant: **SILICON STORAGE TECHNOLOGY, INC.** [US/US]; 450 Holger Way, San Jose, CA 95134 (US).(72) Inventors: **SU, Chien-sheng**; 20300 Kirkmont Drive, Saratoga, CA 95070 (US). **YANG, Jeng-wei**; No. 48 Zhuangjing 3rd Rd., Zhubei, 302 (TW). **TADAYONI, Mandana**; 21900 Dolores Avenue, Cupertino, CA 95014 (US). **CHEN, Yueh-hsin**; 6264 Camino Del Lago, Pleasanton, CA 94566 (US).(74) Agent: **LIMBACH, Alan, A.**; DLA Piper LLP US, 2000 University Avenue, East Palo Alto, CA 94303 (US).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JP, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: METHOD OF MAKING HIGH-VOLTAGE MOS TRANSISTORS WITH THIN POLY GATE

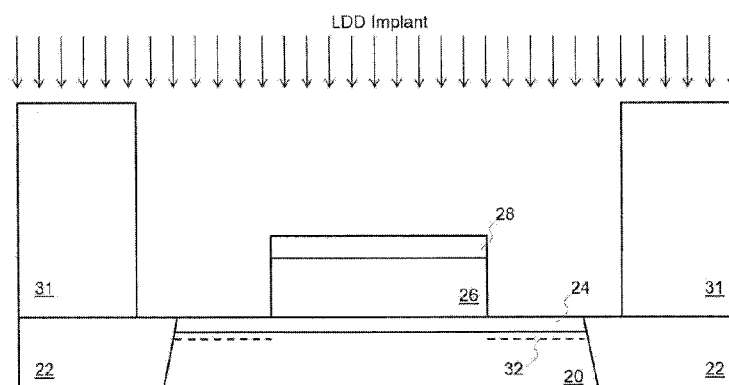


FIG. 2E

(57) Abstract: A method of forming an MOS transistor by forming a poly gate over and insulated from a substrate, forming a layer of protective insulation material on the poly gate, and then performing a first implant of dopant material into portions of the substrate adjacent the poly gate, wherein the layer of protective insulation material and the poly gate block most or all of the first implant from reaching a portion of the substrate underneath the poly gate. One or more spacers are then formed adjacent the poly gate, followed by a second implant of dopant material into portions of the substrate adjacent to the one or more spacers.

METHOD OF MAKING HIGH-VOLTAGE MOS TRANSISTORS WITH THIN POLY GATE

5 FIELD OF THE INVENTION

[0001] The present invention relates to semiconductor devices, and more particularly to the fabrication of high-voltage MOS Transistors.

BACKGROUND OF THE INVENTION

10 [0002] Figure 1 illustrates a partially fabricated conventional MOS transistor, which includes an insulation layer 12 (e.g. oxide) formed over a substrate 10, a polysilicon layer 14 formed over the insulation layer 12, and photo-resist 16 over the polysilicon layer 14. The photo-resist has been patterned, which was followed by a polysilicon etch to result in the structure of Figure 1 (i.e. a poly gate 14 disposed over and insulated from the substrate 10).

15 [0003] In order to create MOS transistors capable of high voltage operation, it is known to perform a high voltage LDD (lightly doped drain) implant step to the structure of Fig. 1, to lightly dope the source/drain. It is preferred to perform the LDD implant after the formation of the poly gate 14, so that the LDD implant is self-aligned to the poly gate 14. The LDD implant is performed with relative high energy, so the lightly doped region of the LDD region
20 (or junction) extends deep enough into the substrate 10 to achieve a high gated-diode breakdown voltage BVDSS.

[0004] As device geometries shrink, including the thickness of poly gate 14 (e.g. less than 1000Å), the LDD implant can penetrate through the thin poly gate 14, and into the channel region underneath poly gate 14. The implant impurities in that portion of the channel region
25 have the undesirable effect of reducing the maximum operating voltage of the transistor. Lowering the implant energy to avoid LDD implant penetration through the poly gate 14 is also undesirable because that would reduce the gated-diode breakdown voltage.

BRIEF SUMMARY OF THE INVENTION

30 [0005] The aforementioned problems and needs are addressed by a method of forming an MOS transistor that includes forming a first insulation layer on a substrate, forming a poly layer on the first insulation layer, forming a second insulation layer on the poly layer,

-2-

selectively removing portions of the second insulation layer and the poly layer to create a poly gate from the poly layer and a layer of protective insulation on the poly gate from the second insulation layer, performing a first implant of dopant material into portions of the substrate adjacent the poly gate, wherein the protective insulation and poly gate block most or all of the first implant from reaching a portion of the substrate underneath the poly gate, forming one or more spacers adjacent the poly gate, and performing a second implant of dopant material into portions of the substrate adjacent to the one or more spacers.

[0006] Another aspect of the present invention is a method of forming an MOS transistor that includes providing a substrate, forming a poly gate over and insulated from the substrate, forming a layer of protective insulation material on the poly gate, performing a first implant of dopant material, after the forming of the poly gate and layer of insulation material, into portions of the substrate adjacent the poly gate, wherein the layer of protective insulation material and the poly gate block most or all of the first implant from reaching a portion of the substrate underneath the poly gate, forming one or more spacers adjacent the poly gate, and performing a second implant of dopant material into portions of the substrate adjacent to the one or more spacers.

[0007] Other objects and features of the present invention will become apparent by a review of the specification, claims and appended figures.

20

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Fig. 1 is a side cross-sectional view of a partially formed conventional MOS transistor.

[0009] Fig. 2A-2J are cross sectional views showing in sequence process steps in the formation of a high voltage MOS transistor.

25

DETAILED DESCRIPTION OF THE INVENTION

[0010] The present invention is a method of manufacturing an MOS transistor that has a thin poly gate yet can be operated at high voltages. The method continues to employ a high voltage LDD implant, and achieves the same high voltage operation characteristics as those transistors with thicker poly gates.

30

[0011] Figures 2A-2J show the cross sections of the structure as the processing steps are performed in the manufacture of the high voltage transistor. As illustrated in Fig. 2A, a semiconductor substrate 20 (or a semiconductor well) is provided, which is preferably of P type and is well known in the art. The substrate 20 includes STI insulation regions 22 formed by the well-known process of STI isolation region formation. Alternately, isolation regions 22 could be formed by the well-known LOCOS isolation method. See for example U.S. Patent 6,891,220, which is incorporated herein by reference for all purposes.

[0012] A first layer of insulation material 24, such as silicon dioxide (oxide), is deposited or formed on the surface of the substrate between adjacent STI insulation regions 22, as shown in FIG. 2B. The first insulation layer 24 can be formed on the substrate 10 by well-known techniques such as oxidation or deposition (e.g. chemical vapor deposition or CVD), and has a thickness of 100 to 500 Å. A thin layer of polysilicon 26 (hereinafter "poly") is deposited on top of the first layer of insulation material 24 (e.g. 300 to 1000 Å thick). The deposition and formation of the polysilicon layer 26 on the first insulation layer 24 can be made by a well-known process such as Low Pressure CVD or LPCVD. A sacrificial (second) layer of insulation material 28 (e.g. oxide having a thickness of 200 to 2000 Å) is deposited over the polysilicon layer 26. A photo-resist (masking) material 30 is then deposited over sacrificial oxide layer 28. The resulting structure is shown in Fig. 2C.

[0013] A photolithographic step is performed which selectively removes portions of photo-resist 30. Oxide and poly anisotropic etches are performed to remove the exposed portions of sacrificial oxide 28 and poly 26 (i.e. those portions not underneath the remaining portions of photo-resist 30). The photo-resist 30 is then removed, resulting in the structure shown in Fig. 2D.

[0014] A second photo-resist 31 is applied, and selectively removed by a photolithography process, leaving the space between adjacent STI regions 22 unobstructed. A high voltage LDD implant process is performed to create lightly doped areas 32 in the substrate between poly gate 26 and STI regions 22, as illustrated in Fig. 2E. As a non-limiting example, the LDD implant is phosphorus with 30 KeV energy for high voltage NMOS transistor. The relatively thick oxide 28 and poly gate 26 minimizes any implantation of dopant from the LDD implant into that portion of the substrate underneath poly gate 26 (i.e. most if not all of

the LDD implant is blocked by oxide 28 alone or together with poly gate 26 from reaching the substrate under poly gate 26).

[0015] An oxide etch is next performed that removes oxide 28 over poly 26, and removes exposed portions of oxide 24 and STI 22, resulting in the structure of Fig. 2F. The oxide etch
5 can be a wet etch or a dry etch, however a dry etch is preferred to avoid any undesirable undercut issues. The second photo-resist 31 is then removed. Spacers 34 of insulation material (e.g. oxide or nitride) are then formed along the sidewalls of poly gate 26. Formation of spacers is well known in the art, and involves the deposition of a material over the contour of a structure, followed by an anisotropic etch process, whereby the material is
10 removed from horizontal surfaces of the structure, while the material remains largely intact on vertically oriented surfaces of the structure (with a rounded upper surface). The resulting structure is shown in Fig. 2G.

[0016] A third photo-resist 35 is applied, and selectively removed by a photolithography process, leaving the space between adjacent STI regions 22 unobstructed. A source/drain
15 implant process is next performed to form source/drain regions 36/38 in the exposed portions of substrate 20 between spacers 34 and STI regions 22, as shown in Fig. 2H. As a non-limiting example, the source/drain implant is a combination of phosphorus 25KeV, $3E13/cm^2$, arsenic 30KeV, $2E15$, and phosphorus 10KeV, $1.5E14/cm^2$. The above described method results in graded source/drain regions through the combination of the source/drain
20 implant and the LDD implant which partially overlap each other (i.e. the lightly doped areas 32 created by the LDD implant partially overlaps with the source/drain regions 36/38 created by the source/drain implant, with the non-overlapping portion of the lightly doped areas 32 created by the LDD implant being disposed under spacers 34). The third photo-resist 35 is then removed. A thermal anneal is next performed to activate and drive the high-voltage
25 LDD implant as well as source/drain implant in substrate 22. The resulting LDD junction 32 and source/drain junction 36/38 are shown in Fig. 2I. Since high-voltage LDD implant region 32 and source/drain region 36/38 have the same type of dopant material (N type for NMOS or P type for PMOS), the high-voltage LDD junction and source/drain junction are superimposed as shown in Fig. 2J. After the thermal anneal, the LDD extends its lightly-
30 doped region 32 underneath the poly gate 26. The LDD implant is performed with relative

high energy, the lightly doped region of the LDD implant 32 extends deep enough into the substrate 10 to achieve a high gated diode breakdown voltage BVDSS.

[0017] It is to be understood that the present invention is not limited to the embodiment(s) described above and illustrated herein, but encompasses any and all variations falling within
5 the scope of the appended claims. For example, references to the present invention herein are not intended to limit the scope of any claim or claim term, but instead merely make reference to one or more features that may be covered by one or more of the claims. Materials, processes and numerical examples described above are exemplary only, and should not be deemed to limit the claims. Further, as is apparent from the claims and specification, not all
10 method steps need be performed in the exact order illustrated or claimed, but rather in any order that allows the proper formation of the MOS transistor of the present invention. Lastly, single layers of material could be formed as multiple layers of such or similar materials, and vice versa.

[0018] It should be noted that, as used herein, the terms “over” and “on” both inclusively
15 include “directly on” (no intermediate materials, elements or space disposed therebetween) and “indirectly on” (intermediate materials, elements or space disposed therebetween). Likewise, the term “adjacent” includes “directly adjacent” (no intermediate materials, elements or space disposed therebetween) and “indirectly adjacent” (intermediate materials, elements or space disposed there between). For example, forming an element “over a
20 substrate” can include forming the element directly on the substrate with no intermediate materials/elements therebetween, as well as forming the element indirectly on the substrate with one or more intermediate materials/elements therebetween.

-6-

What is claimed is:

1. A method of forming an MOS transistor, comprising:
forming a first insulation layer on a substrate;
forming a poly layer on the first insulation layer;
5 forming a second insulation layer on the poly layer;
selectively removing portions of the second insulation layer and the poly layer to
create a poly gate from the poly layer and a layer of protective insulation on the poly gate
from the second insulation layer;
performing a first implant of dopant material into portions of the substrate adjacent
10 the poly gate, wherein the protective insulation and poly gate block most or all of the first
implant from reaching a portion of the substrate underneath the poly gate;
forming one or more spacers adjacent the poly gate; and
performing a second implant of dopant material into portions of the substrate adjacent
to the one or more spacers.
15
2. The method of claim 1, wherein the first and second implants partially overlap
each other in the substrate.
3. The method of claim 2, wherein:
20 the second implant creates source and drain regions in the substrate; and
the first implant creates doped areas in the substrate each extending underneath one of
the spacers and into one of the source and drain regions.
4. The method of claim 1, further comprising:
25 removing the layer of protective insulation before the forming of the one or more
spacers.
5. The method of claim 1, wherein the selective removing portions of the second
insulation layer and the poly layer comprises:
30 forming photo-resist on the poly layer;

-7-

performing a photolithography process to selectively remove some but not all of the photo-resist in a manner leaving some but not all portions of the second insulation layer exposed;

- 5 performing an etch process to remove the exposed portions of the second insulation layer leaving some but not all portions of the poly layer exposed; and
performing an etch process to remove the exposed portions of the poly layer.

6. The method of claim 5, further comprising:
removing all of the photo-resist before the performing of the first implant.

10

7. A method of forming an MOS transistor, comprising:
providing a substrate;
forming a poly gate over and insulated from the substrate;
forming a layer of protective insulation material on the poly gate;
15 performing a first implant of dopant material, after the forming of the poly gate and layer of insulation material, into portions of the substrate adjacent the poly gate, wherein the layer of protective insulation material and the poly gate block most or all of the first implant from reaching a portion of the substrate underneath the poly gate;
forming one or more spacers adjacent the poly gate; and
20 performing a second implant of dopant material into portions of the substrate adjacent to the one or more spacers.

8. The method of claim 7, wherein the first and second implants partially overlap each other in the substrate.

25

9. The method of claim 8, wherein:
the second implant creates source and drain regions in the substrate; and
the first implant creates doped areas in the substrate each extending underneath one of the spacers and into one of the source and drain regions.

30

10. The method of claim 7, further comprising:

-8-

removing the layer of protective insulation before the forming of the one or more spacers.

11. The method of claim 7, wherein the forming of the poly gate and the layer of insulation material comprises:
- 5 forming a layer of polysilicon;
forming a layer of insulation on the layer of polysilicon;
forming a layer of photo-resist on the layer of insulation;
performing a photolithography process to selectively remove some but not all of the photo-resist in a manner leaving some but not all portions of the insulation layer exposed;
- 10 performing an etch process to remove the exposed portions of the insulation layer leaving some but not all portions of the layer of polysilicon exposed; and
performing an etch process to remove the exposed portions of the layer of polysilicon.
12. The method of claim 11, further comprising:
removing all of the photo-resist before the performing of the first implant.

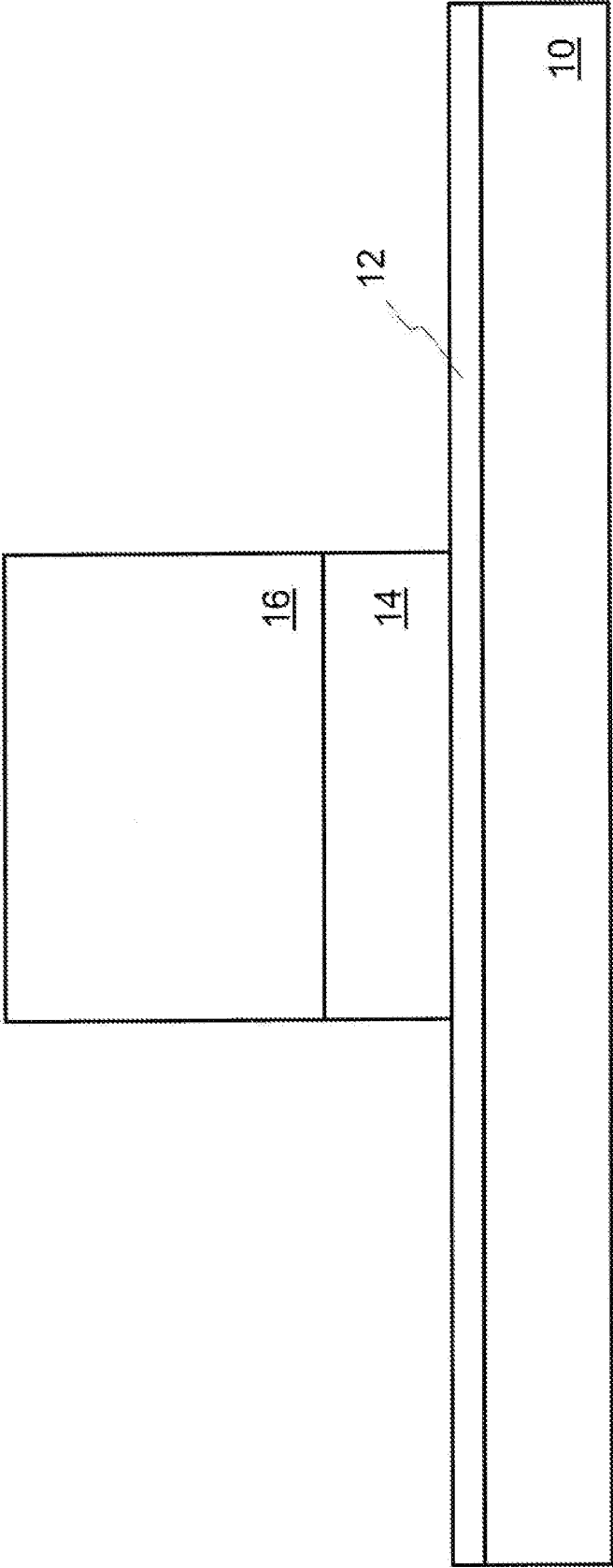


FIG. 1
(Prior Art)

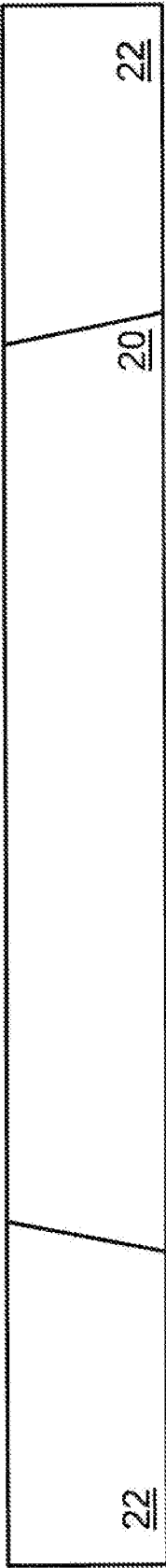


FIG. 2A

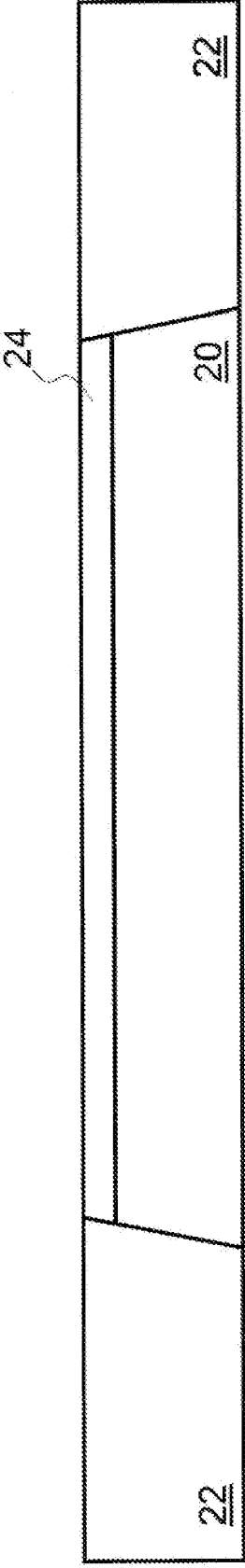


FIG. 2B

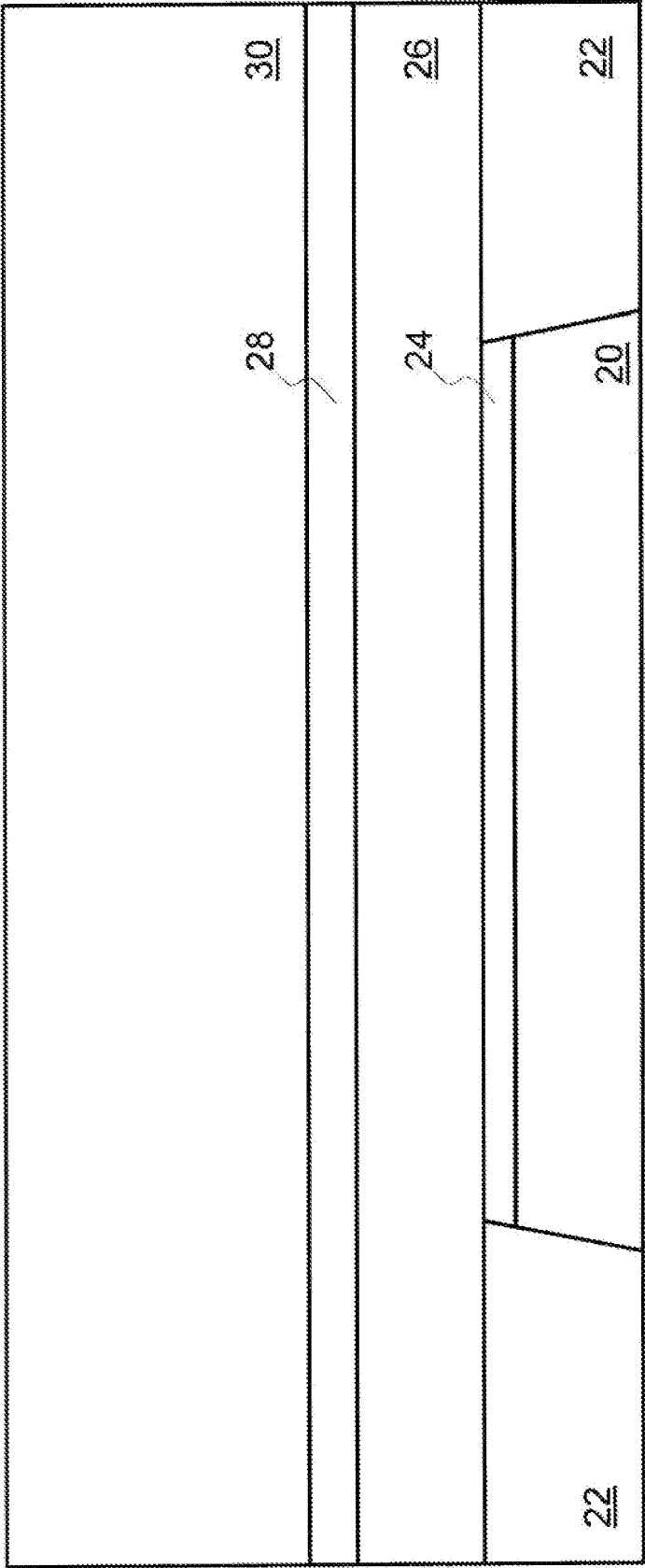


FIG. 2C

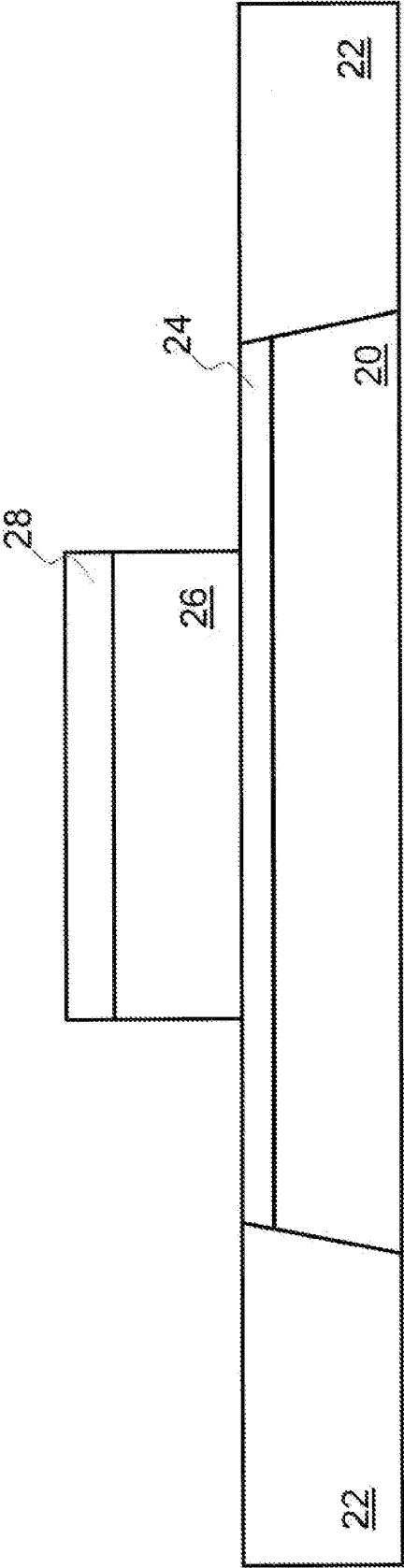


FIG. 2D

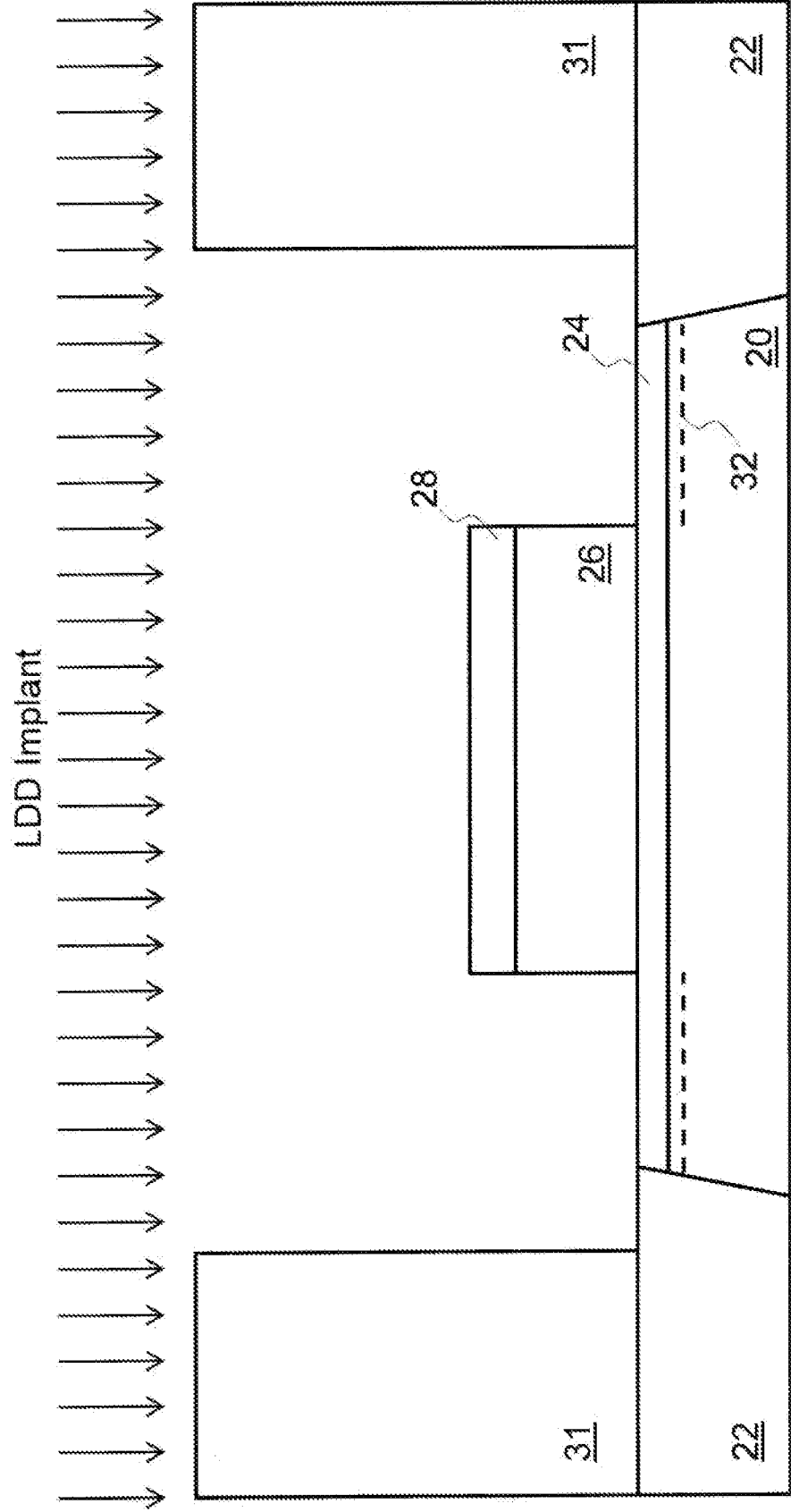


FIG. 2E

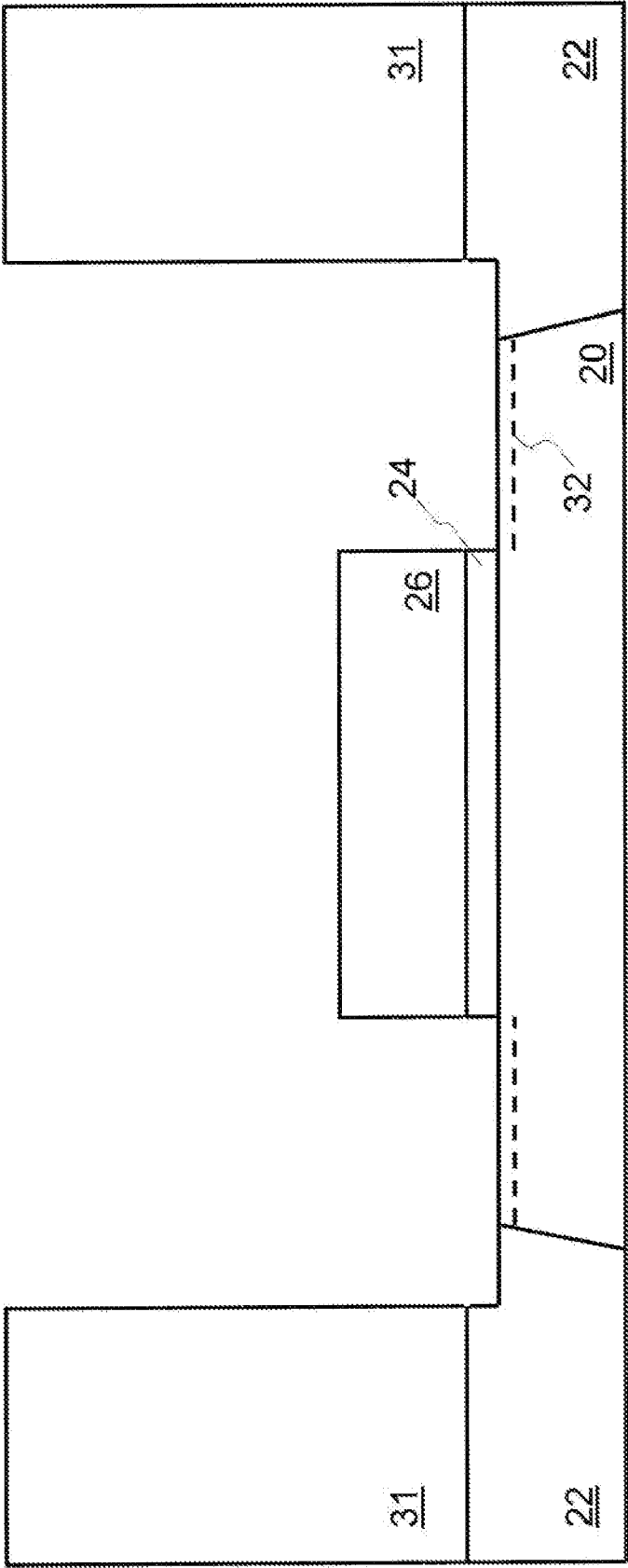


FIG. 2F

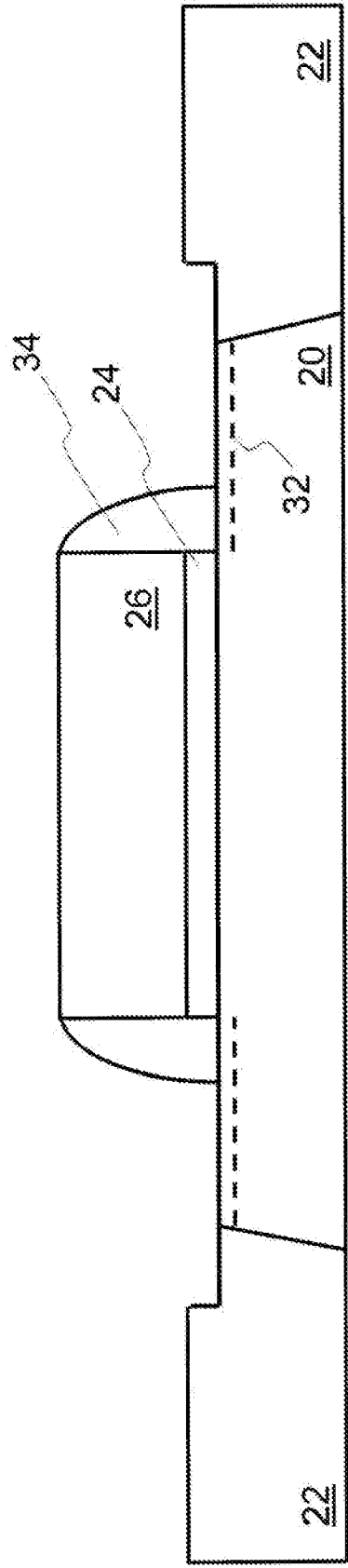


FIG. 2G

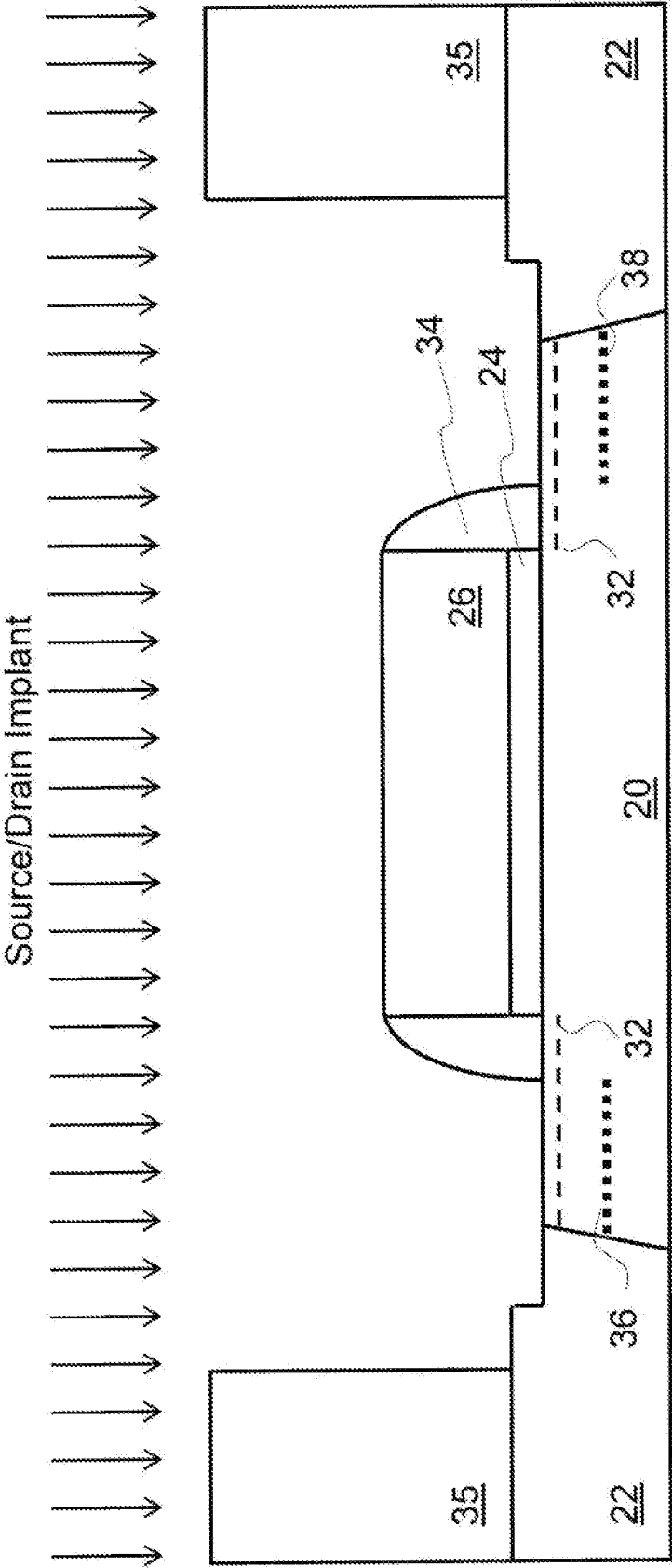


FIG. 2H

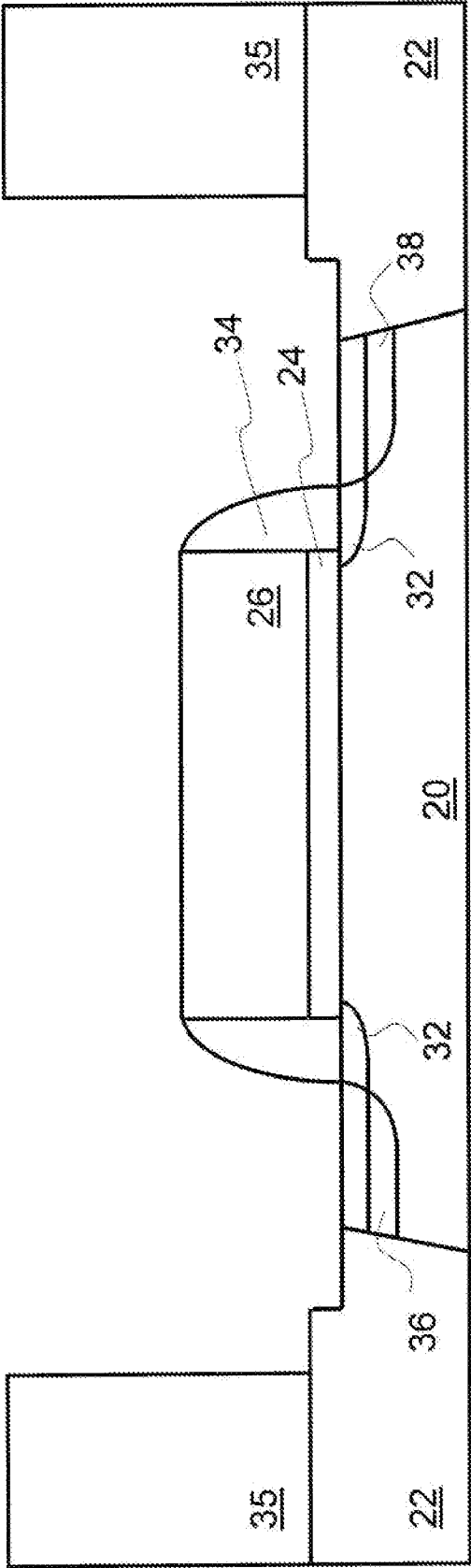


FIG. 2I

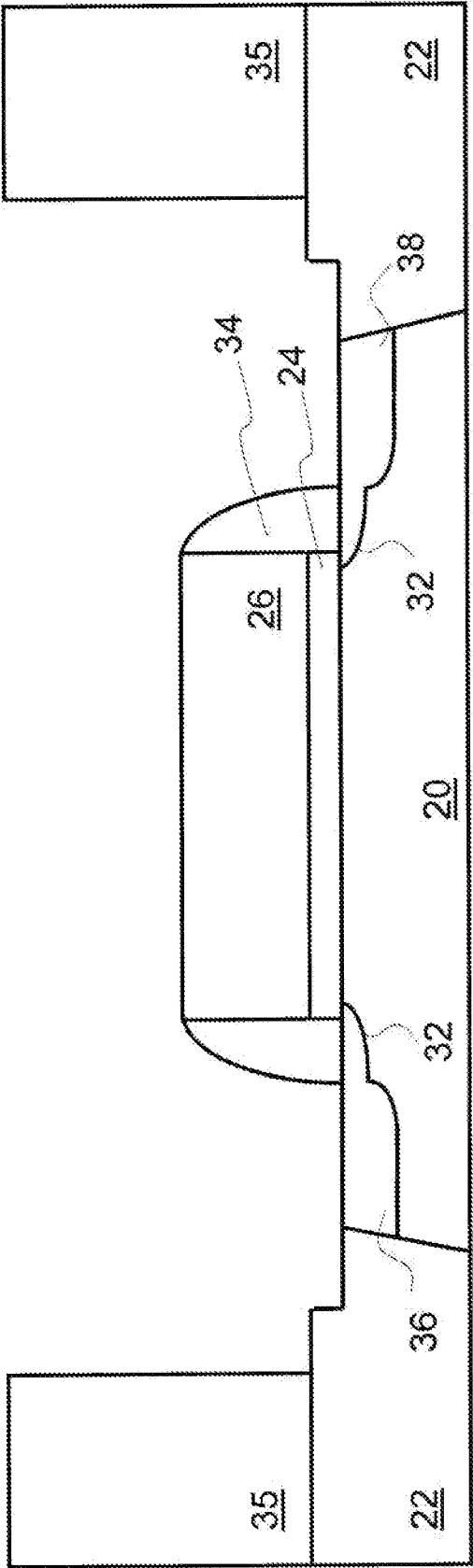


FIG. 2J

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/011934

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/336
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007/161249 A1 (KO CHOUL J [KR] KO CHOUL JOO [KR]) 12 July 2007 (2007-07-12) the whole document -----	1-12
X	CHANG S-J ET AL: "A NOVEL SACRIFICIAL GATE STACK PROCESS FOR SUPPRESSION OF BORON PENETRATION IN P-MOSFET WITH SHALLOW BF2-IMPLANTED SOURCE/DRAIN EXTENSION", IEEE ELECTRON DEVICE LETTERS, IEEE SERVICE CENTER, NEW YORK, NY, US, vol. 21, no. 8, 1 August 2000 (2000-08-01), pages 381-383, XP000935744, ISSN: 0741-3106, DOI: 10.1109/55.852957 page 381, right-hand column -----	1-3,5-9, 11,12
X	US 5 719 424 A (AHMAD AFTAB [US] ET AL) 17 February 1998 (1998-02-17) figures 7-14 ----- -/-	1-3,5-9, 11,12

☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

23 April 2014

Date of mailing of the international search report

08/05/2014

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Gélébart, Jacques

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2014/011934

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 024 960 A (HAKEN ROGER A [US]) 18 June 1991 (1991-06-18) column 4, line 14 - column 5, line 8; figures 1-6	1-3,5-9, 11,12
A	----- US 5 021 851 A (HAKEN ROGER A [US] ET AL) 4 June 1991 (1991-06-04) column 1, line 62 - column 2, line 26 -----	1,3,7,9

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2014/011934

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2007161249 A1	12-07-2007	NONE	

US 5719424 A	17-02-1998	US 5719424 A	17-02-1998
		US 6046472 A	04-04-2000
		US 6159813 A	12-12-2000
		US 6448141 B1	10-09-2002
		US 6495885 B1	17-12-2002
		US 2002182813 A1	05-12-2002
		US 2002190315 A1	19-12-2002

US 5024960 A	18-06-1991	NONE	

US 5021851 A	04-06-1991	NONE	
