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Collomosse et al.

[11] **3,790,704**

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[54] **PATTERN CONTROL SYSTEM FOR CONTROLLING TEXTILE MACHINERY**

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[21] Appl. No.: **315,287**

[30] **Foreign Application Priority Data**

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[51] **Int. Cl.** **H04n 7/18,** H04n 9/02

[58] **Field of Search** 178/6.8, DIG. 22, 5.2 R, 5.4 R, 178/5.4 CD; 340/324 AD

[56] **References Cited**

UNITED STATES PATENTS

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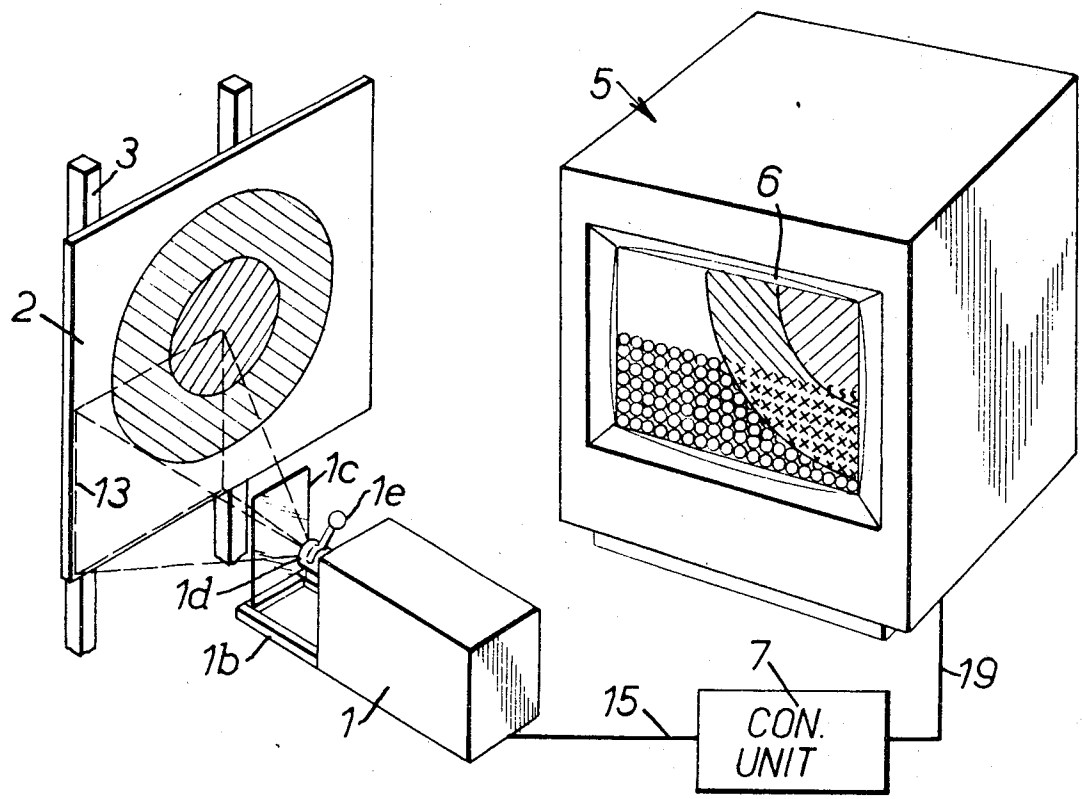
Primary Examiner—Howard W. Britton

Attorney, Agent, or Firm—Lawrence E. Laubscher

[57] **ABSTRACT**

A television camera views a representation of a pattern to be knitted by a knitting machine. A television picture tube displays a monochrome image of the pattern and coloured picture elements, each representing stitch information stored at an individual address in a memory, are superimposed upon the pattern image so that the correspondence between the stored information and the original pattern may be determined. A keyboard enables pattern information to be progressively entered in a memory, each stitch so entered appearing immediately as a coloured element in a display. Any portion of the pattern information stored in the memory may be displayed at will. A pulsating marker element shows the position in the displayed pattern at which information will be entered upon actuation of a key. Automatic return and pattern line advance and "tabulator" return to preselected positions in the pattern may be effected.

28 Claims, 10 Drawing Figures



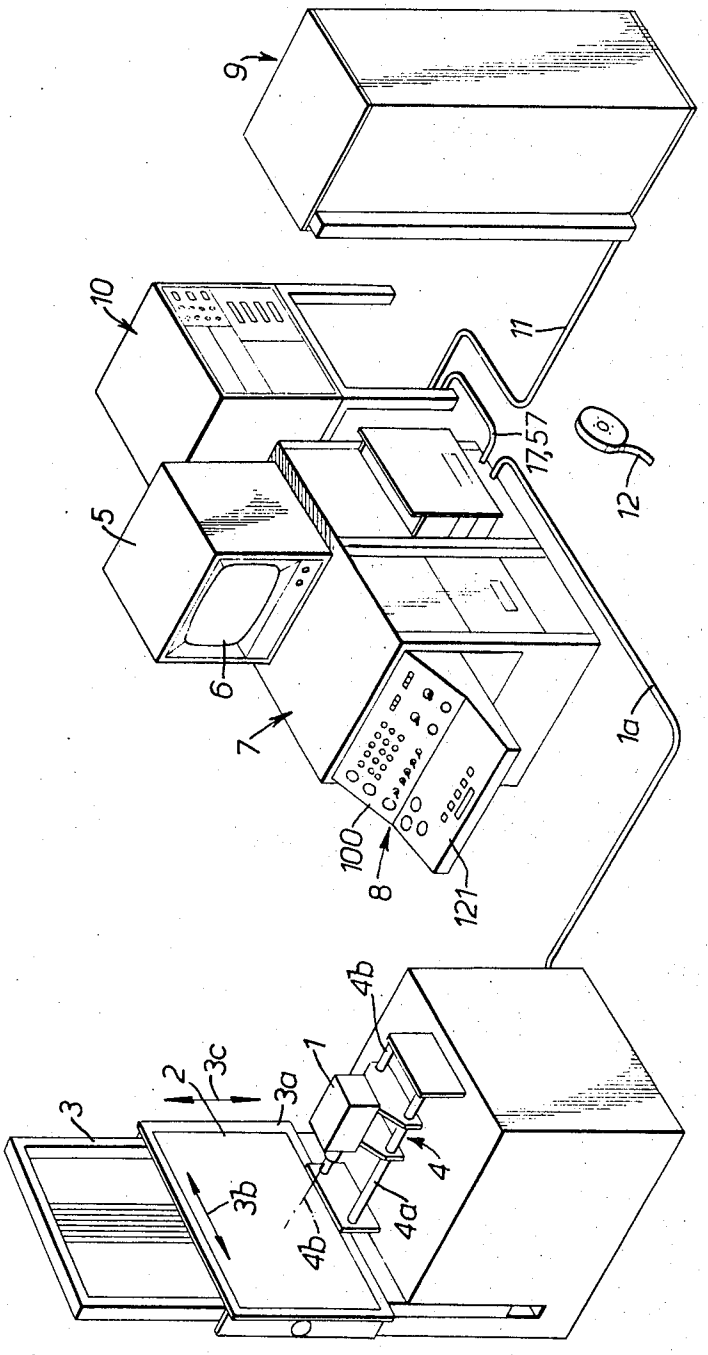


FIG. 1.

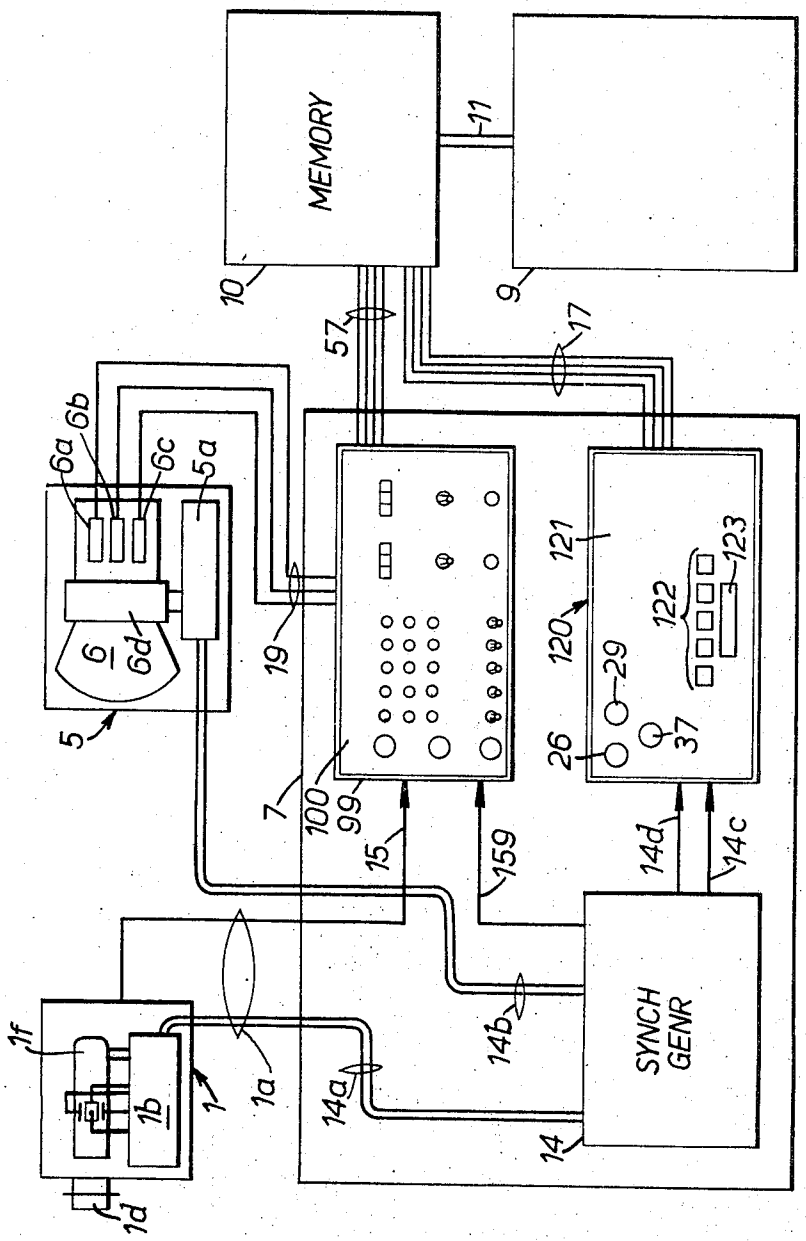

MEMORY
11
10
9
57
17
6a
6b
6c
5a
6
6d
5
19
7
100
99
15
159
121
120
122
123
29
26
37
14d
14c
14b
14a
14
SYNCH GENR
1f
1b
1
1a
1d

FIG. 2.

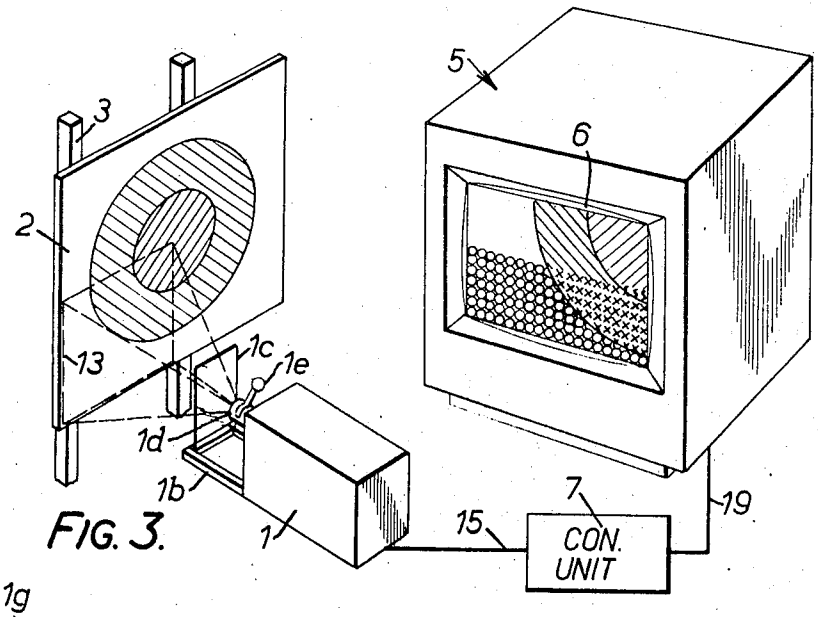

5
6
3
2
13
1c
1e
1d
1b
1
7
CON.
UNIT
15
19

FIG. 3.

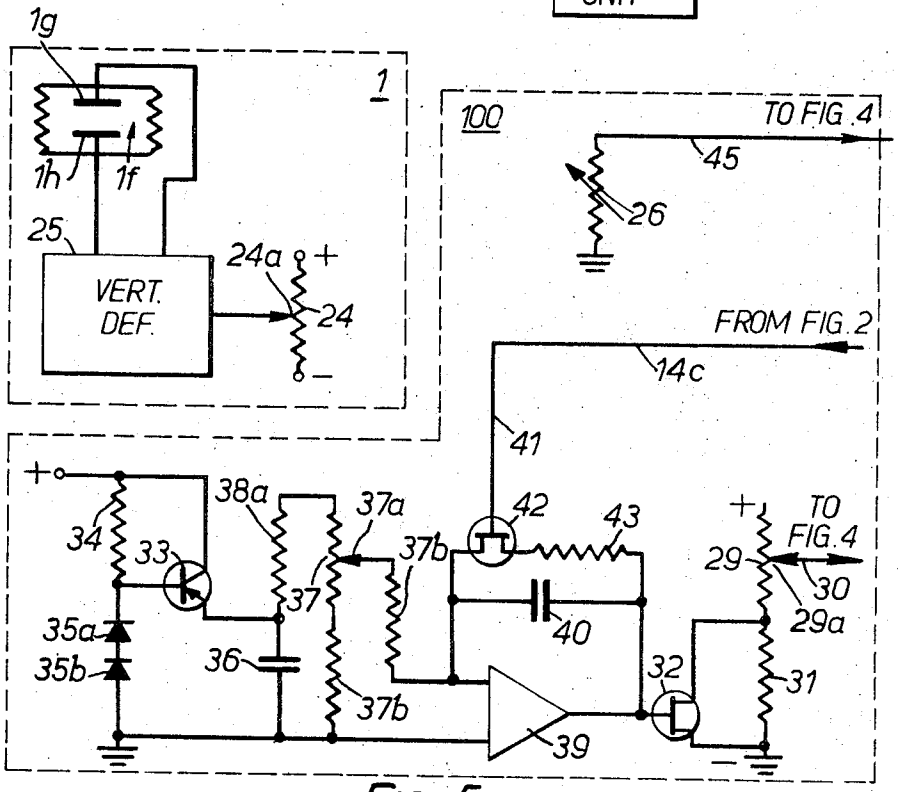

1g
1
1h
1f
25
VERT.
DEF.
24a
24
100
TO FIG. 4
45
26
FROM FIG. 2
14c
41
38a
37a
42
43
37b
34
33
37
40
35a
35b
36
37b
39
32
29
30
29a
31
TO
FIG. 4

FIG. 5.

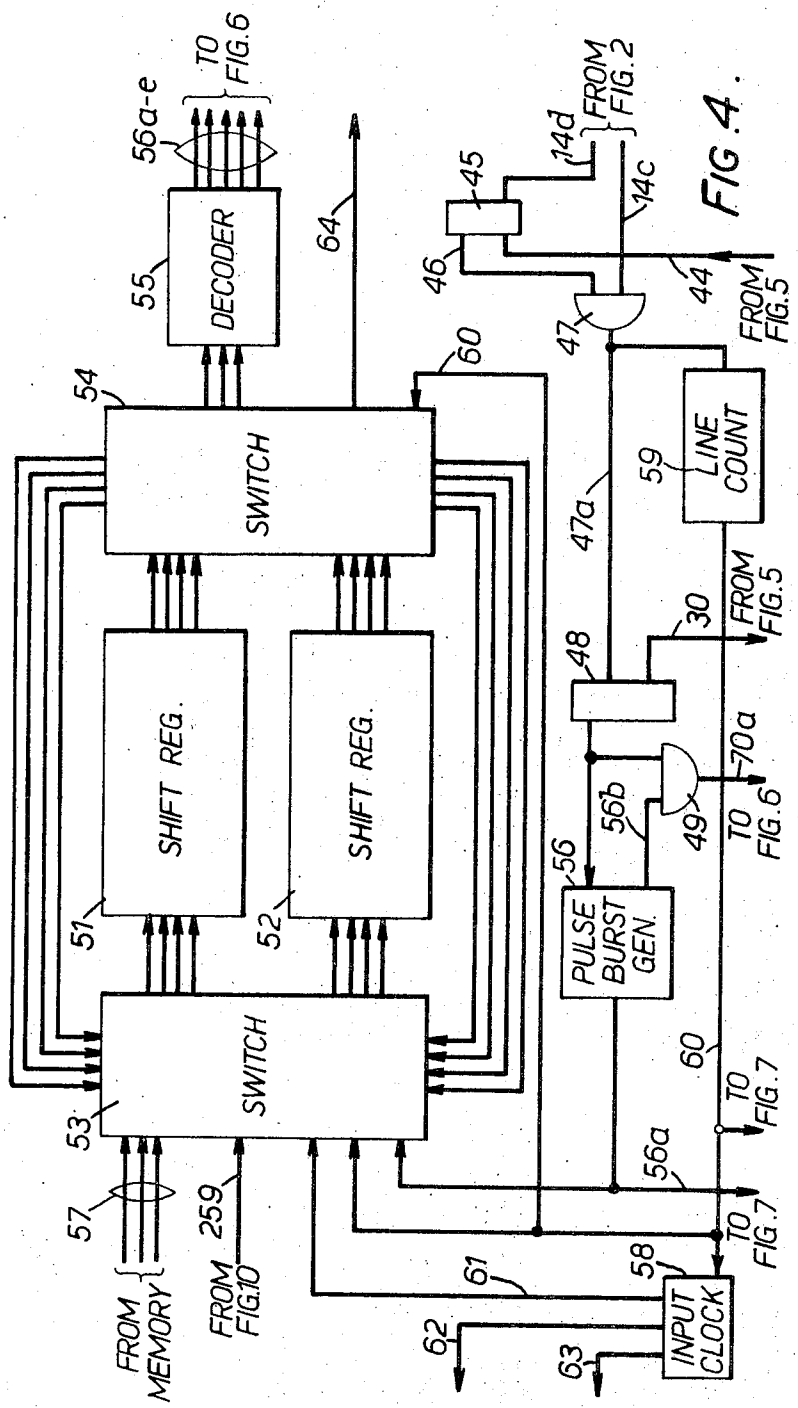

56a-e
TO FIG.6
55
DECODER
64
45
14d
FROM FIG.2
14c
46
44
FROM FIG.5
47
60
54
SWITCH
59
LINE COUNT
47a
30
FROM FIG.5
48
70a
TO FIG.6
49
56b
56
PULSE BURST GEN.
SHIFT REG.
SHIFT REG.
51
52
SWITCH
53
60
TO FIG.7
56a
TO FIG.7
57
259
FROM MEMORY
FROM FIG.10
61
58
INPUT CLOCK
62
63

FIG. 4.

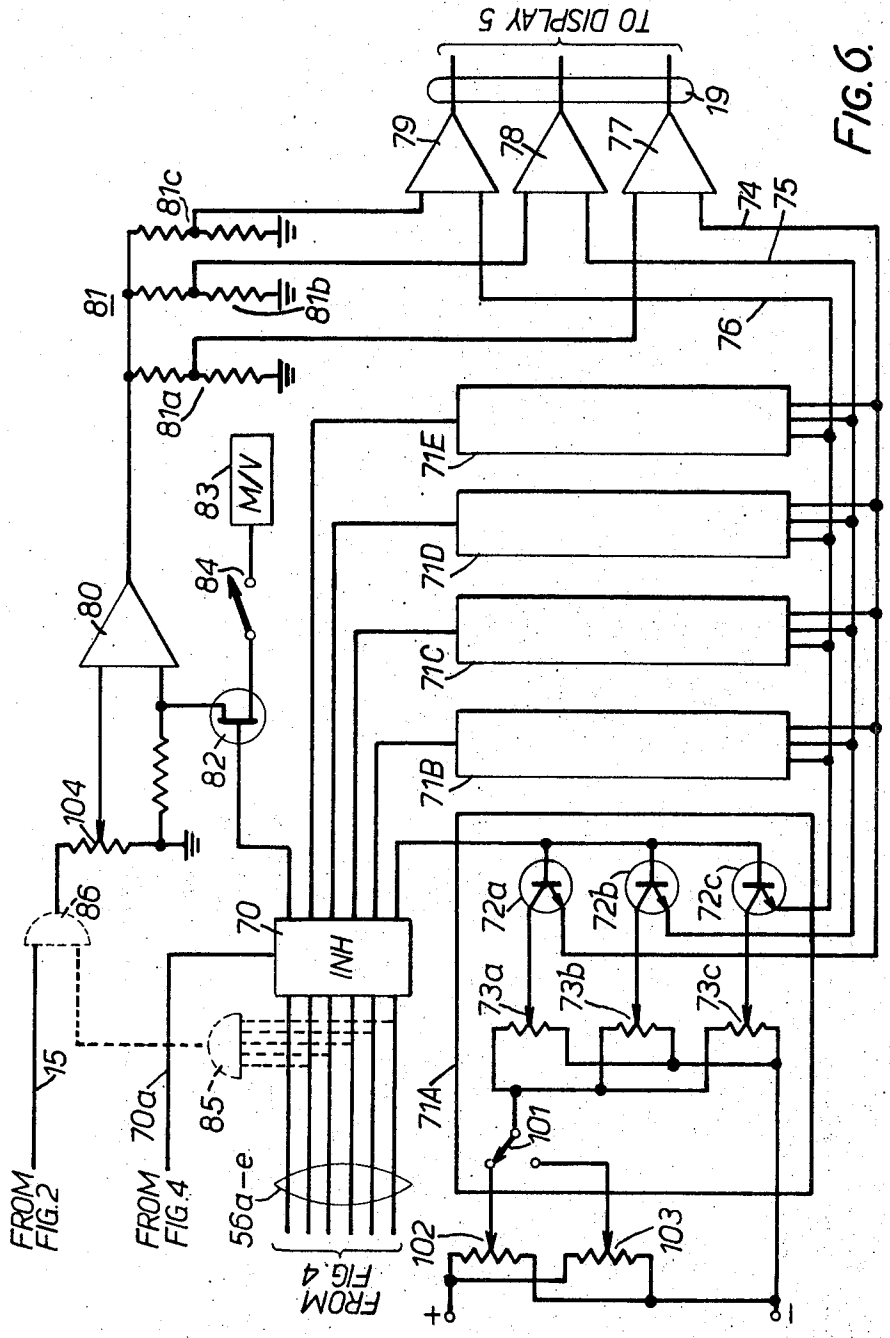

TO DISPLAY 5
19
79
78
77
74
75
76
81c
81
81b
81a
83
M/V
84
80
82
104
86
70
INH
71E
71D
71C
71B
72a
72b
72c
73a
73b
73c
71A
101
102
103
+
−
15
70a
85
56a-e
FROM FIG.2
FROM FIG.4
FROM FIG. 4

FIG. 6.

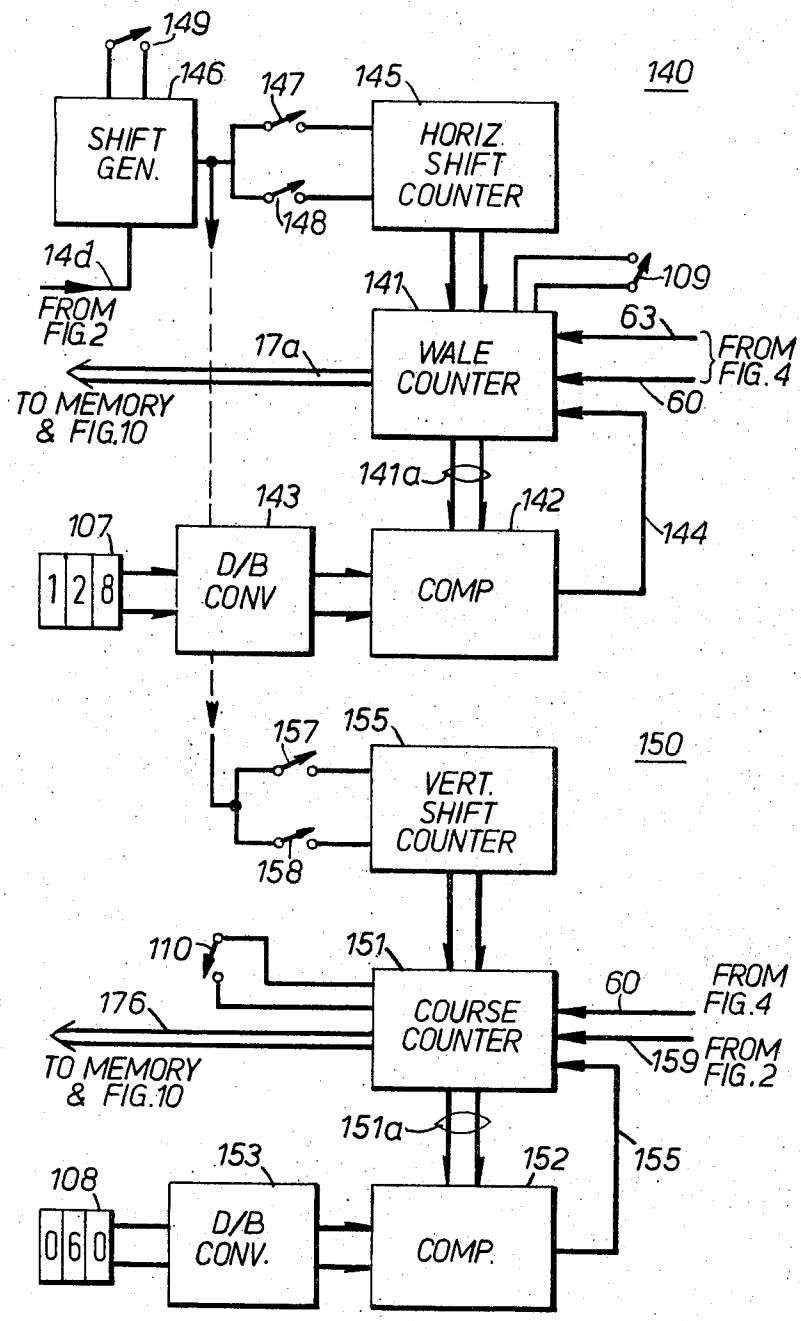

149
146
147
145
140
SHIFT GEN.
HORIZ. SHIFT COUNTER
148
14d
FROM FIG.2
141
109
63
FROM FIG.4
17a
WALE COUNTER
60
TO MEMORY & FIG.10
141a
143
142
144
107
1 2 8
D/B CONV
COMP
157
155
150
VERT. SHIFT COUNTER
158
110
151
60
FROM FIG.4
176
COURSE COUNTER
159
FROM FIG.2
TO MEMORY & FIG.10
151a
153
152
155
108
0 6 0
D/B CONV.
COMP.

FIG. 7.

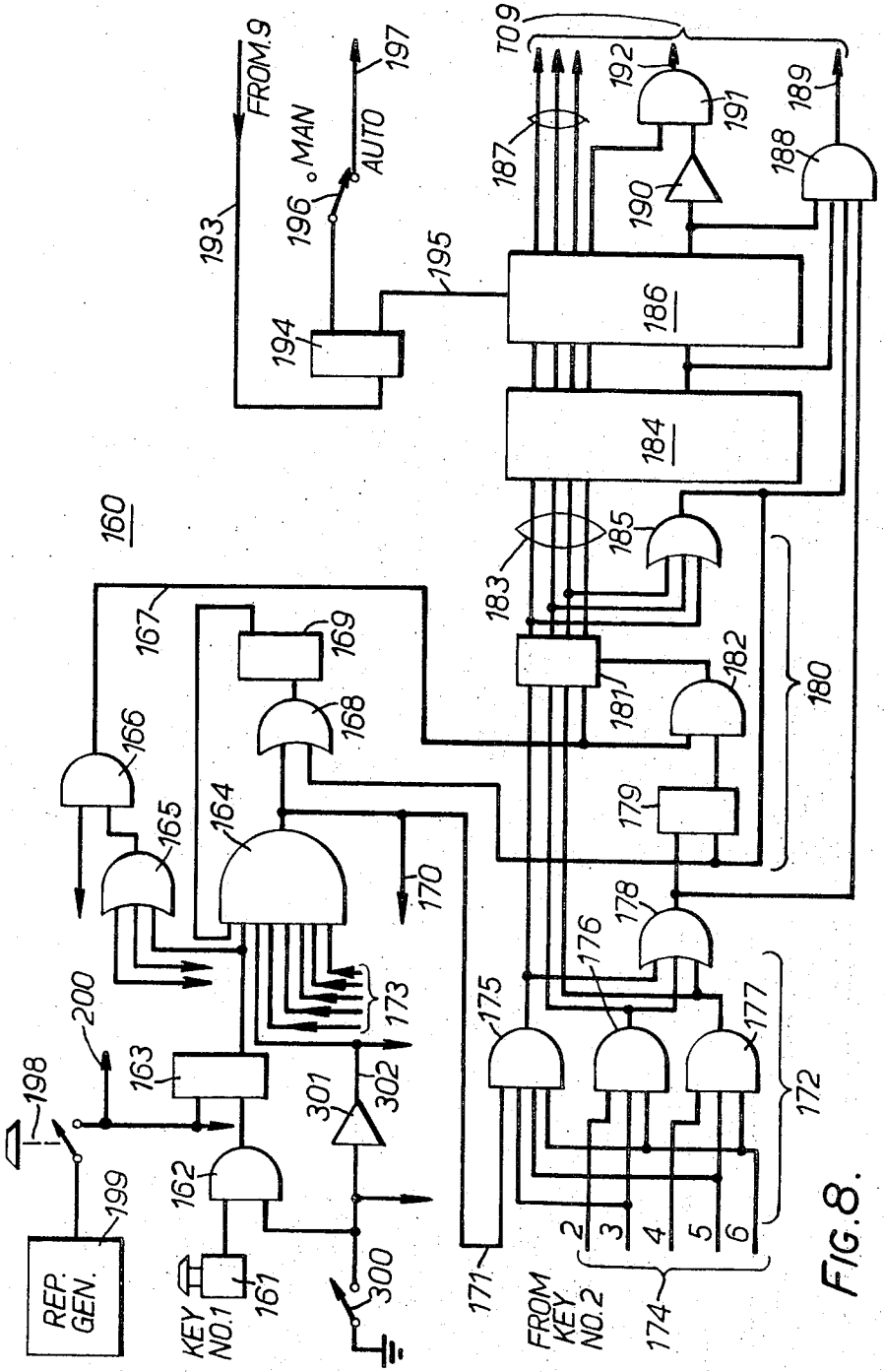

FROM 9
193
196
MAN
AUTO
197
194
195
709
187
192
191
189
188
190
186
184
185
183
181
182
180
179
178
176
175
177
172
160
167
169
168
166
165
164
170
200
163
173
198
199
301
302
162
161
300
171
REP. GEN.
KEY NO.1
FROM KEY NO.2
174
2
3
4
5
6

FIG. 8.

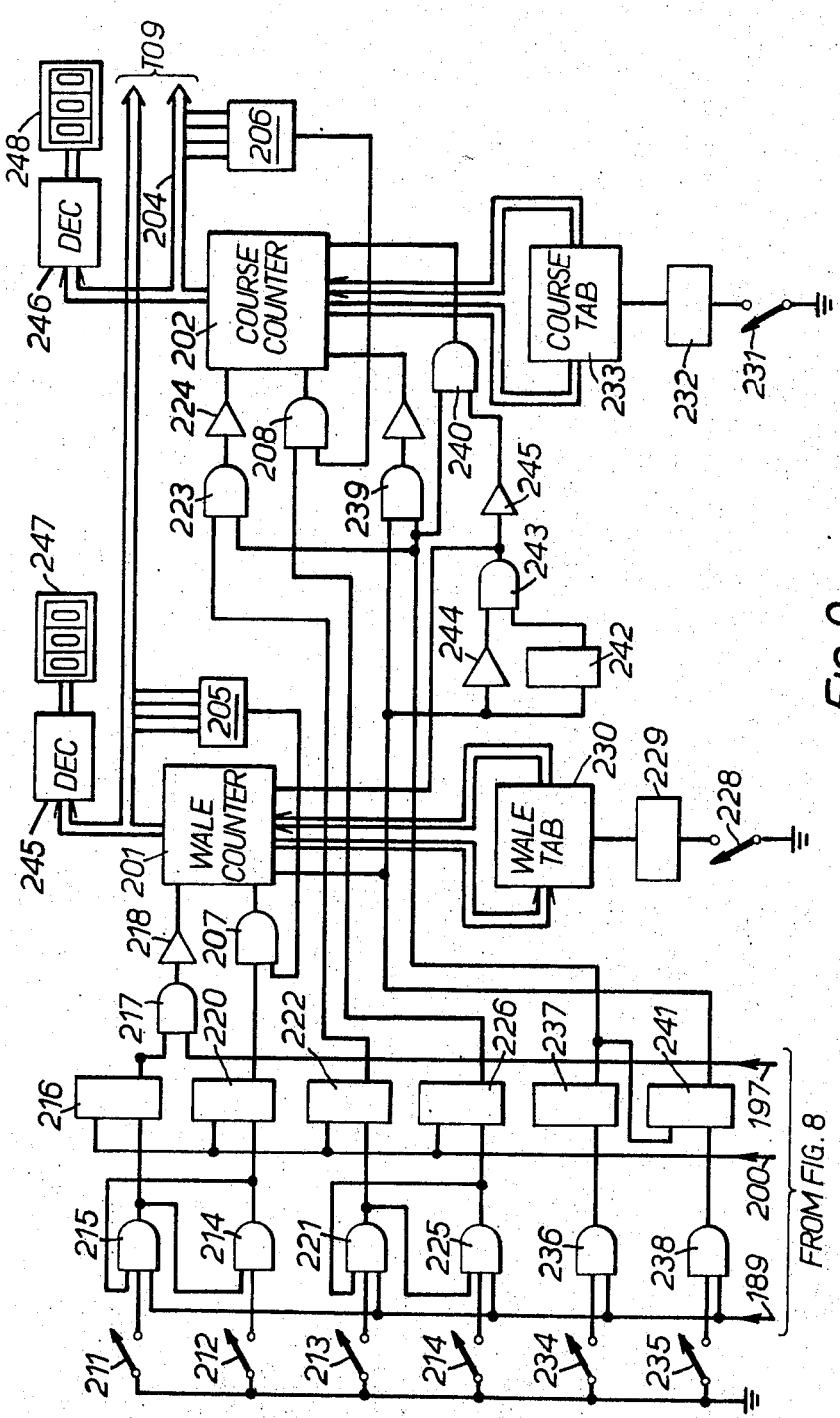

DEC
DEC
COURSE COUNTER
COURSE TAB
WALE COUNTER
WALE TAB
FROM FIG. 8

FIG. 9

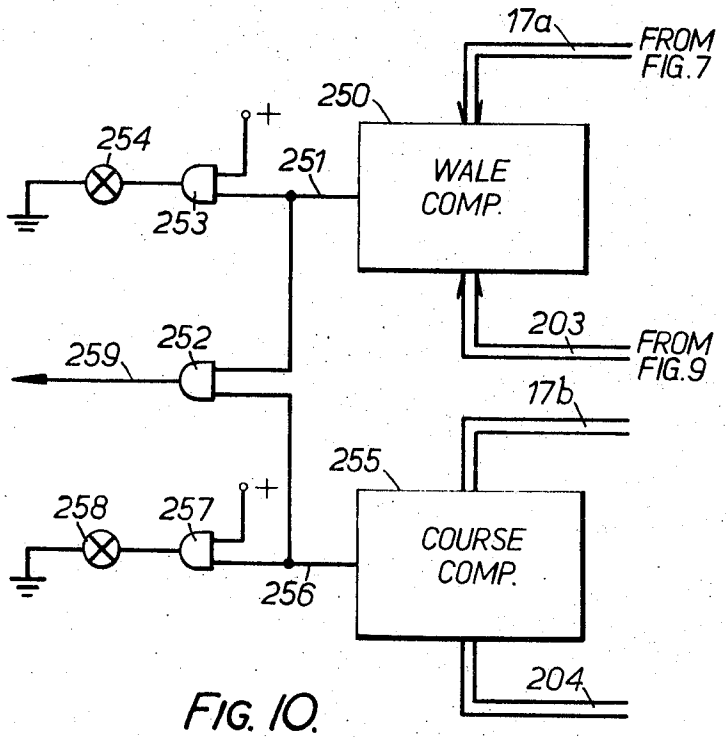

17a
FROM FIG. 7
250
254
251
WALE COMP.
253
203
FROM FIG. 9
259
252
17b
255
258
257
COURSE COMP.
256
204

FIG. 10.

PATTERN CONTROL SYSTEM FOR CONTROLLING TEXTILE MACHINERY

BACKGROUND OF THE INVENTION

This invention relates to a pattern control system for controlling a textile machine producing patterned textile material in response to pattern information stored in a memory device. The invention has particular, though not exclusive, application in the control of knitting machines and will be particularly described as applied to that purpose. It will be apparent to those skilled in the art, however, that the invention may also be applied to controlling other machines for producing patterned fabrics, in which a plurality of successively or simultaneously performed operations are required to be varied in order to produce the required pattern.

It is known from United Kingdom Patent Specification No. 1,199,291 to provide opto-electronic picture storage apparatus including a cathode ray tube display of an image by means including a respective feedback loop for each picture element, so that a picture to be stored may be introduced point by point into the storage system.

It is also known from French Patent Specification No. 2,032,334 to provide a pattern control system for a knitting machine which includes a store for a limited number of pattern elements in the form of coded information, in which information is entered into a temporary store by the actuation of keys while a display of the stored information is exhibited to the operator. The original design is then directly compared with the display and the corrected information is then transferred piecemeal into a computer.

SUMMARY OF THE INVENTION

It is an object of the invention to provide pattern control means wherein correspondence between an original pattern and pattern information stored in a memory device may be determined immediately upon entry of the information into the memory.

It is a further object of the invention to provide pattern control means whereby pattern information entered into a memory device containing all the pattern information necessary for the production of a textile article at the same time as a display representing the relevant portion of the pattern information is provided to the operator.

One embodiment of the invention comprises a pattern control system including a television camera having a pickup tube viewing an original pattern representation to develop a video signal representative thereof and scan generators for said pickup tube, together with memory means containing stored information representative of the pattern. The system further comprises display means including a television picture tube having a viewing screen and scan generators for the pickup tube, a synchronizing signal generator producing line and field synchronizing signals which are applied to the camera and to the display means to control the scanning thereof. The system also comprises access means sequentially withdrawing pattern information from the memory means and applying the information to the display means to produce a display representative of the stored information. The system additionally comprises means applying the camera video signal to the cathode ray picture tube to produce a monochrome image of the original pattern representation.

Another embodiment of the invention comprises a pattern control system for entering pattern element information into a memory device, said system comprising display means including a scanned television picture tube, a memory means operable to store said pattern information; access means sequentially withdrawing information from said memory means to develop individual control signals representative of display elements corresponding to the information; means applying said control signals to said picture tube to produce an information display representative of the stored pattern information; keyboard encoder means responsive to selective actuation of a plurality of data keys to develop coded signals representative of different pattern information, keyboard address means developing numerical address signals denotive of a location within said memory means; and means applying said coded signals and said address signals to said memory means so as to insert pattern representative signals in the memory means at the location represented by the address.

An embodiment of a system in accordance with the invention will be described by way of example with reference to the accompanying drawings, of which:

FIG. **1** is a pictorial diagram showing the appearance of illustrative components of one embodiment of a pattern control system in accordance with the invention;

FIG. **2** is a block schematic diagram illustrating the interconnections of the components of the pattern control system of FIG. **1**;

FIG. **3** is a pictorial diagram showing that the system according to the invention produces a display denotive of an original pattern representation and of pattern information entered into a memory;

FIG. **4** is a block circuit diagram of display shift register circuitry used in the embodiment;

FIG. **5** is a block schematic diagram illustrating the arrangement of certain display controls in the embodiment;

FIG. **6** is a circuit diagram, partly in block form, of display switching and mixing circuits used in the embodiment;

FIG. **7** is a simplified logic diagram of display address circuitry used in the embodiment;

FIG. **8** is a simplified logic diagram of keyboard encoder circuitry used in the embodiment;

FIG. **9** is a logic diagram of keyboard address circuitry used in the embodiment; and

FIG. **10** is a simplified logic diagram of marker signal generating circuitry used in the embodiment.

FIG. **1** shows the apparatus forming an embodiment of a pattern control system in accordance with the invention. A television camera **1** is arranged to view an artist's design or other original pattern representation **2**, which is supported upon an easel **3**. The work support **3***a* of the easel is supported so that it can be moved in two perpendicular directions in its own plane, as indicated by arrows **3***b* and **3***c*. Camera **1** is advantageously supported, as shown, by a camera stand **4** movably mounted on rails **4***a* to permit the camera to be moved along an axis **4***b* perpendicular to the plane of movement of easel **3**. Alternative arrangements apparent to those skilled in the art may be used to permit appropriate relative movement of camera **1** and pattern representation **2**. Camera **1** is connected by a cable **1***a*

to a control unit 7 upon which and electrically connected thereto is a display unit 5 including a television display tube 6. Alternative positions for display unit 5 may be adopted if preferred.

It is very desirable in the present system that the television camera 1 shall provide a video signal capable of providing a display of high geometrical accuracy. It is found advantageous for this purpose to employ an electrostatically scanned pickup tube, for this choice enables the required scanning accuracy to be obtained more conveniently than when a magnetically scanned pickup tube is employed.

Control unit 7 is provided with a keyboard portion 8 having a control panel 100 and a keyboard 121, the purposes of which are described later in relation to FIG. 2. If desired, the keyboard portion 8 may be placed remotely from the control unit proper and connected thereto over suitable wiring. Control unit 7 is also connected to a memory unit 10, in which pattern information is stored. The stored information is used to provide a display on display unit 5 representative of the stored information and may additionally or alternatively be fed out by way of a cable 11 to the control unit 9 of a circular knitting machine (not further shown) of known, electrically controllable kind.

The memory unit 10 may conveniently include a known memory device using a matrix of magnetic core stores to receive, retain and reproduce coded pattern information as desired. Other known forms of memory device 9 may however be used as convenient. Many such memory devices and appropriate means for reading-in and reading-out the stored information have long been known in the data processing art and are not considered to require further description.

The pattern information stored in memory unit 10 may be additionally be used, if so desired, to control a tape punch system housed in the control unit 7 and arranged to produce a punched tape 12 carrying pattern-representative information corresponding with that stored in the memory, this information being arranged in any required code or sequence, but typically providing a tape which may be used in turn to control the punching of control discs for disc-controlled knitting machines of known type, or a tape which may itself be used to control a knitting machine.

FIG. 2 shows a block schematic diagram of one embodiment of a system in accordance with FIG. 1. Control unit 7 contains a synchronizing signal generator 14 of known type which provides conventional television line and field synchronizing signals over leads 14*a* to control a line and field scan generator unit 1*k* in camera 1, over leads 14*b* to control a line and field scan generator unit 5*a* in display unit 5 and which provides line and field synchronizing signals over respective lines 14*c*, 14*d* to control unit 7. The television camera 1 includes a pickup tube 1*f* to which line and field deflection signals are applied from the respective line and field scan generators included in scan generator unit 1*k*. Display unit 5 includes a colour picture tube 6 having deflection means 6*d* to which line and field deflection signals are applied from respective line and field scan generators contained in scan generator unit 5*a*. Video signals representative of the original pattern representation are fed from camera 1 over a lead 15 to a switching and mixing circuit 99 controlled by a control panel 100. Information signals withdrawn from memory 10 are passed to the switching and mixing circuit 99 by way of leads 57, while signals representing pattern information are fed into the memory 10 from a keyboard unit 120, controlled by a keyboard 121, over leads 17.

Display controlling signals are applied from switching and mixing circuit 99 to display unit 5 by way of leads 19, where they are applied to control the intensity of the electron beams produced by the red, blue and green guns 6*a*, 6*b* and 6*c* of colour television picture tube 6. Finally, signals withdrawn from memory 9 by way of memory control unit 10 may be applied over a control cable 11 to control the operation of a knitting machine.

The camera 1 views the original pattern representation 2 and the video signal which is thus developed is used to produce on the screen of cathode ray tube 6 of display unit 5 a corresponding half-tone image. Existing cathode ray picture tubes of the most convenient size cannot be used to display a pattern containing more than some 152×96 pattern information units, stitches in the present embodiment. With a pattern containing more than this number of pattern elements, therefore, the camera is positioned by means of the traveling camera stand 4, and the pattern representation is positioned in its own plane by adjustment of easel 3, so that the camera views only a portion of the pattern, as shown in FIG. 3, where it will be observed that the field of view of the camera, denoted by broken line 13, encompasses only some one-quarter of the whole pattern, so that this portion only of the design is displayed as a half-tone image upon cathode ray tube 6.

In a system according to the invention there is superimposed upon the half-tone image of the pattern which is produced on the screen of display cathode ray tube 6 a display indicative of the individual elements of pattern information which have been entered in memory unit 9 for use in the direct or indirect control of a knitting machine. If display cathode ray tube 6 is a monochrome display tube the different kinds of information entered in the memory may be displayed by symbols of different geometric form appropriately positioned on the screen of the display tube.

It is, however, preferred that display tube 6 shall be a colour television display tube and that the different kinds of pattern information shall be displayed by respectively differently coloured elements in the display. It is not necessary that the displayed elements shall be of the same colours as the pattern elements produced in a knitted particle in response to the stored pattern information, though it is usually most convenient that this shall be so.

The display produced by the pattern information stored in the memory unit is illustrated in the lower part of the display shown in FIG. 2 by the symbols X, O and S, representing the symbols or distinct colour displays produced by different information codes in the memory, superimposed upon the shaded display areas representing the monochrome image of the pattern representation, the different portions of which are denoted by different shadings. It should be noted that for the sake of clarity in illustration a few symbols only are shown and that these are much larger than they would be in practice, in relation to the size of the display.

Although the original pattern representation 2 will usually be coloured, it is most economical to arrange that the displayed pattern portion appears in monochrome, the colours of the original appearing as vary-

ing half-tones between black and white. It will sometimes be desirable to dispose a colour filter between the original pattern representation **2** and the camera **1**, in order that all the pattern colours shall be represented in the monochrome image by readily distinguishable half-tone values. FIG. **3** shows how the camera **1** may be provided with a support means **1***b* arranged to accept interchangeable colour filter members, such as filter **1***c*.

However, it may in some cases be found desirable to provide a coloured display of the original pattern representation, and it is then necessary to provide a colour television camera and appropriate known associated circuitry to form television camera **1**.

It is assumed in the following description that television camera **1** and display unit **5** employ a standard scanning raster as used in commercial broadcast apparatus, as this choice permits many commercially available parts to be used, especially the display unit. Other scanning standards may be used if preferred without departing from the scope of the invention as defined by the claims.

The area of the original pattern representation appearing upon the display screen may be adjusted by varying the distance between the camera and the design, by movement of the camera stand **4** upon the rails **4***a* (FIG. 1). Alternatively or in addition the camera may include a variable magnification lens with constant focal distances, that is a zoom lens **1***d*, of which the magnification may be adjusted by means of a manual control **1***e*. The usual requirement is to adjust the camera or lens so that a specific area of the original design representation corresponds with a predetermined number of courses and wales of a display which is produced on the tube screen as later described under the control of the information stored in the memory unit. If the aspect ratio of the original pattern representation differs from that of the information display this will obviously be impossible, and a means for adjusting the aspect ratio of the pattern image is therefore provided. When setting-up the system prior to entering pattern information into the memory, the distance of the camera from the original pattern representation is first adjusted until the width of the reproduced monochrome image of the pattern representation is the same as the width of the information display derived from the information stored in the memory. An image height control, usually most conveniently provided on the camera itself, is then adjusted to vary the amplitude of the camera scan as is described below in relation to FIG. **5**.

It is in practice inconvenient to provide a memory from which information may be withdrawn at the rate at which it must be made available to control a cathode ray tube display using a standard television raster. Information withdrawn from the memory and representing one pattern line is therefore entered into one of two circulating registers and meanwhile information representing the adjacent pattern line, which has previously been entered into the other circulating register, is repeatedly withdrawn from that other register to control the display.

A block diagram illustrating this part of the system is shown in FIG. **4**. For simplicity, the system is described only as set up for **6** raster lines per pattern row and for a display width of 128 pattern elements. Because display unit **5** uses standard interlaced scanning, only three raster lines are consecutively provided with the same information during each field scanned.

Each of two shift registers **51** and **52** is arranged to provide four storage channels, which are used to store sequences of 3-bit codes which are withdrawn from the memory and the fourth channel is used to receive a "marker" bit, the purpose of which is described later. Each channel has a maximum capacity of 160 bits; these may be switchable to provide different effective storage capacities, as may be convenient. In the following description a total storage of 128 bits per channel is assumed. By means of switching units **53** and **54** the shift registers are used alternately, one being filled with information from the memory, whilst the other is recirculating and presenting its stored information to the display by way of a decoder **55**, which causes the pattern information contained in the 3-bit code groups to energise a selected one of five different display-control lines, or none of them.

When one of the shifting registers **51, 52** is operating in the recirculating mode it is clocked by the output of a pulse burst generator **56**, which conveniently takes the form of a gated multivibrator. The line synch. pulses from the synch. generator **14** (FIG. **2**) are applied over a line **14***c* to the pulse burst generator **56**, this latter produces a burst of pulses equal in number to the number of bits stored in each channel of the register, in the present instance, 128 pulses, which produces a complete recirculation of the information stored in the register. The timing of the generated pulse burst in relation to the initiating pulse on line **14***c* is determined by a potential received over a line **30** from the circuits described later with reference to FIG. **5**. The 128 pulses must occur within a time not greater than that taken for the electron beam of the display cathode ray tube **6** to scan one raster line on the screen. This requires a fast clock frequency appropriate to the number of lines in the raster.

That one of the shift registers **51** and **52** which is at any time receiving data from memory **9** over lines **16** is clocked by the output of a Data Input Clock generator **58**. This generator also produces a burst of 128 pulses, but at a slow clock speed which is compatible with the maximum output speed of the memory. In order to ensure that the information in the register feeding the display is recirculated the correct number of times a Line Counter circuit **59** is provided, to which the line synch. signals received over line **14***c* are provided and which provides an output pulse on a line **60** only when the appropriate number of line pulses (three in the present case) has been received. The input clock generator **58** provides a slow clock signal over a line **61** to the shift register **51** or **52** which is receiving information, over a line **62** to the memory, where they constitute read/restore cycle initiating pulses controlling read-out of stored information from the memory in known manner and over a line **63** to the Display Address circuit described below with reference to FIG. **7**.

Pulses provided by line counter **59** on line **60** are also applied to switching units **53** and **54** to control the change-over from one to the other of shifting registers **51** and **52**, these being alternately connected to receive and to supply information, as has been said. As the information-supplying register is circulated the successive code groups are applied to decoder **55**, with the result that for each code an output is applied to one of the five output lines **55***a* – **55***e* of the decoder, or to none

of them if the code represents a 'space'; additionally if a marker bit is present in the line being circulated it is fed out over a line **64** to the control panel circuitry for display.

In the system as described above the elements of the display corresponding to the information in the memory are superimposed upon the image of the original pattern representation, both being simultaneously visible on the screen. It may be preferred that the display elements representing the stored information shall replace the pattern image. This effect may be produced by providing an OR gate **85** (FIG. **6**) responding to any output signal from decoder **55** received over lines **55***a*–**55***e* to develop an inhibiting signal which is applied to a gate **86** introduced into the line **15** which carries the video signal from the camera **1** to the display unit by way of the video amplifier **80.** The presence of any display signal thus suppresses the video signal appropriate to the corresponding position on the display screen.

The necessity for providing an adjustment of the raster height used in the camera has already been explained. This height adjustment may be effected by means of a potentiometer **24** (FIG. **5**) which may most conveniently be placed on the camera **1,** though it can if required be placed elsewhere. Potentiometer **24** is connected across a direct-voltage source represented only by terminals + and − and the potential selected by the setting of its slider **24***a* is applied in known manner to control the amplitude of the deflection voltage produced by a scan generator **25** supplying sawtooth voltages to the vertical deflection plates **1***g*, **1***h* of the camera pickup tube **1***f*.

It is advantageous to provide means for fine adjustment of the position of the information display in relation to the monochrome pattern image, and for adjustment of the orthogonality of the information display, as will now be described in relation to FIG. **5.** Fine adjustment of the vertical position of the information display is effected by means of an UP/DOWN control **26** on the keyboard **121** (FIGS. **2** and **5**). Control **26** adjusts the value of a variable resistor which is connected over a line **44** to form the timing resistor of a variable-delay flip-flop **45** (FIG. **4**). Flip-flop **45** is fired by field synchronizing impulses received over line **14***d* from synchronizing signal generator **14** (FIG. **2**) and yields on a line **46** variably delayed inhibiting signals which are applied to a gate **47** by way of which line synchronizing pulses received over a line **14***c* from the synchronizing signal generator **14** (FIG. **2**) are fed to control the operation of the burst pulse generator **56,** as later described. Gate **47** thus prevents line synchronizing pulses from triggering burst pulse generator **46** until a time after the commencement of the field period of the display raster which is determined by the setting of control **26.**

The gated line synchronizing pulses provided on line **47***a* by gate **47** are applied to fire a further variable-delay flip-flop **48** providing drive signals to the Brust Pulse Generator **56** of which the operation has already been described. The delay of flip-flop **48** is controlled by circuit arrangements shown in FIG. **5,** to which flip-flop **48** is connected by way of a lead **30.** As shown in FIG. **5,** line **30** is connected to the slider **29***a* of a variable resistor **29,** which is connected to ground by way of the parallel combination of a resistor **31** and the controlled path of a transistor **32.** The effective value of the timing resistance for flip-flop **48** thus depends upon the setting of variable resistor **29** and upon the potential applied to the gate of transistor **32.** This gate potential is variable throughout the field scan period, as will now be described.

Direct voltage from a source represented only by a − terminal and an earth symbol is applied to a voltage stabilizer circuit formed by an NPN transistor **33,** the base of which is held at a fixed potential above ground by being returned to the tapping of the series combination of a resistor **34** and a pair of Zener diodes **35***a*, **35***b*, the series combination being connected across the supply. The transistor collector is returned to the positive supply terminal and its emitter provides a stabilized direct voltage to the parallel combination of a capacitor **36** and a voltage divider chain including a potentiometer **37** and range-limiting resistors **38***a*, **38***b*. The potential appearing at the slider **37***b* of potentiometer **37** is fed over a resistor **38***b* to one input of an amplifier **39,** the other input of which is grounded. Amplifier **39** is provided with a feedback capacitor **40** and thus acts as an integrator, developing an output voltage increasing proportionally with time. At each field scan a pulse is received over a line **14***c* which turns on a transistor **42** to discharge capacitor **40** through a resistor **43** to return the amplifier output voltage to zero. The amplifier output voltage is applied to the gate of transistor **32,** which thus offers a linearly decreasing resistance during the field scan period. The amount of change is determined by the setting of potentiometer **37,** which thus forms an ORTHOGONALITY CONTROL determining the difference in timing between successively displayed lines of information derived from the memory.

In FIG. **6** it will be seen that the five output lines **55***a*–**55***e* of decoder **55** and the marker signal line **64** all pass through an Inhibit circuit **70** controlled by a signal which is formed by combining the delayed line synch. pulse from flip-flop **48** (FIG. **4**) which is used to trigger the burst pulse generator **56** with a signal provided over a line **56***b* by burst pulse generator **56** when this is quiescent. These two signals are combined in an OR gate **49** whence they are fed over a line **70***a* to the Inhibit circuit **70,** thus allowing the outputs of decoder **56** on lines **56***a* – **56***e* to become effective only when the shift register **51** or **52** is actually recirculating. When the inhibit circuit permits the signal on each decoder output line **55***a–e* controls a respective switching unit **71**A – **71**E. The internal arrangements of switching units **71**A – **71**E are identical, so that unit **71**A only is shown in detail. Each unit contains three semiconductor switches of any suitable type. For the sake of convenience these are illustrated as being n-p-n transistors **72***a*, **72***b*, **72***c*, the bases of all three of which are supplied from the decoder output line **55***a* with a potential making the transistor operative when that output line is selected. When operative, transistors **72***a–c* connect the potentials selected by three potentiometers **73***a*, **73***b*, **73***c* to respective common lines **74, 75, 76.** Potentiometers **73***a* – **73***c* are led to a Blister switch **101** by which they normally receive the potential selected by an Intensity potentiometer **102** connected across a direct voltage supply represented only by terminals + and −. If the switch **101** is actuated, when the three potentiometers of the group receive the potential selected by a Blister Intensity potentiometer **103** connected across the same supply. The three potentiometers **72***a–c* and the corresponding groups of potentiometers in the other units, are used to control the respective RED,

BLUE and GREEN components of the display element produced then the respective decoder output line is energized. The lines **74–76** conduct the elected potentials to first inputs of respective video amplifiers **77, 78, 79,** of which the outputs are taken to control the intensity of the electron beam of a respective gun in the cathode ray display tube **6.** To the second input of each of video amplifiers **77–79** is applied an appropriate proportion of the output of a video amplifier **80,** to the input of which the video signal developed by camera **1** is applied at a level determined by a Monochrome Intensity control potentiometer **104.** The signal proportions applied to the second input of each of video amplifiers **77–79** are fixed by a resistance network **81** including individual voltage dividers **81***a*, **81***b* and **81***c*. The signal proportions are conveniently so fixed that for full intensity a white spot is traced on the screen of cathode ray tube **6.**

To a seocnd input of video amplifier **80** is applied a marker signal which is received over a line **64** from the circulating register and is applied to the gate of a transistor **82** having its controlled path connected between the second input of amplifier **80** and a pulsed voltage supply obtained from a multivibrator **83,** to which the transistor is connected by way of a switch **84** allowing the marker display to be discontinued when desired.

In order to display indications representing information stored in the memory, it is necessary to withdraw this information from the memory. For this purpose it is required that the address of each memory position containing information relating to the pattern field which is to be displayed shall be generated in turn and applied to the memory. This operation is effected by the course and wale address generators represented schematically in FIG. **7,** the two numbers generated by which are combined to form a single location address which is fed to the memory.

Each 3 bit word is addressed using an 8 bit binary number equal to actual wale number and an 8 bit binary number equal to actual course number these numbers being combined to form the total **16** bit address. The stitches may therefore be said to be stored in "visual" order. The information thus withdrawn from the memory is fed over lines **57** to the shifting registers in the control unit which have already been described in relation to FIG. **5.**

The addresses to be applied to the memory are developed by the identically operating wale and course address generators **140** and **150** shown in FIG. **7.** The wale address generator **140** includes a wale counter **141** which is an up/down counter with facilities for parallel insertion. The **8** bit binary output of this counter is connected to the memory **9** by way of lines **17***a* and forms one half of the address. The counter receives batches of **128** pulses over line **63** from the data input clock **58** (FIG. **5**) whenever information is to be read out from the memory. Counter **141** will normally count upwards so that its binary output increases sequentially, thus withdrawing from the memory in turn all of the **128** information codes corresponding to one line of the pattern to be displayed. This information is fed out from the output register of the memory over lines **57** to the shift register **51** or **52** in the control unit, whence it is withdrawn as already described to control the display. The output of wale counter **141** is also applied to a comparator **142,** in which it is compared with a number representing the required width of display, this second number being developed by a decimal-binary converter which receives as its input the decimal nubmer set up by a three-digit SET WIDTH switch **107.** When the two compared numbers coincide, the main counter is reset to zero over a line **144.** This causes the stitch sequence displayed across the screen to repeat at the set pattern-width intervals.

If a wale Mirror Repeat has been selected by actuating a Mirror switch **109,** when the counter **141** reaches a predetermined number it recounts that number once and then counts sequentially downwards until it reaches zero, thus again withdrawing the same information from the memory, but this time in the reverse order. After repeating the zero count once, the counter then counts sequentially upwards again to extract either the next line of information, or the same information once again if a multiple repeat is required by the set width of pattern.

The Wale Counter is cleared and restarted by a signal over line **60** from the line pulse counter **59** (FIG. **4**). This pulse occurs at the end of each displayed line of stitches. It is usually convenient to arrange that the return to its initial state of count of the wale counter **141,** when the set pattern width has been reached, shall be accompanied by a corresponding change in the course number, so that further information will be entered in the adjacent pattern line. The line return signal which appears on line **144** may therefore be applied over a switch **111** to deduct one from the course number in counter **151,** causing subsequent data key operation to introduce codes into the next higher line in the display.

In order that the displayed information may be taken from any desired portion of the memory, the wale address circuitry includes a horizontal shift counter **145,** which also is an up/down counter and is driven by trains of pulses repeated at a rate of some 8 Hz, which are typically generated by a shift generator **146** which counts field synch. pulses and delivers a shift drive pulse for every three field pulses and are applied either to the up or to the down input of shift counter **145** by actuation of a respective Right-Shift key **147** or a Left-Shift key **148.** A further Fast key **149,** when actuated, increases the repetition rate of shift generator **146** to 25 Hz. The shift generator **146** may be a multivibrator of which a coupling time-constant is changed by actuation of Fast key **149.**

Before each count of **128** on Wale Counter **141** commences, the output of shift counter **145** is introduced into the Wale Counter. This initial count determines the position in the memory at which the sequential addressing of memory locations by the output of the wale counter will commence, that is, the position of the left-hand edge of the pattern portion which will be displayed on the screen. Thus the pattern display starts from a position determined by the actuation of the pattern shift controls and appears to move to the left or to the right on the screen when one of these is actuated.

The Course address circuit **150** is almost identical with the Wale address circuit, but normally operates at a lower speed. Moreover, the signal applied to course counter **151** reduces the number in the counter, because successive courses in the display are required to appear upwards from the bottom of the screen.

The elements of this circuit which have functions exactly corresponding with elements of circuits **140** are denoted by reference numerals ten higher than those of the like elements in circuit **140.** The number in the

Course counter **151**, however, is changed only at the end of each line of stitches and to this end is driven by pulses received over line **60** from the line counter **59** of FIG. **4**, while it is cleared and re-started by field synchronizing signals received over a line **14***c* from the synch. generator **14** of FIG. **2**. A separate shift generator is not needed, the signals from generator **146** are applied by way of switches **157** or **158** to the up or down inputs of counter **155** to produce upward or downward vertical displacement of the displayed pattern portions.

The system as so far described operates to display on the display unit **5** a monochrome image of an original pattern representation, upon which is superimposed a preferably coloured display representing pattern information stored in the memory unit. If upon commencing operations there is no pattern information contained in the memory unit, then the pattern image will appear in monochrome without any superimposed display. If pattern information is now progressively entered into the memory, it will immediately appear on the display screen, and the correspondence between the pattern image and the stored information may be discerned.

In accordance with a preferred feature of the invention, therefore, means are provided for inserting pattern information into the memory unit at a position which may be selected at will and which is preferably denoted by an indication on the display. In the system described in relation to the accompanying drawings an operator viewing the monochrome pattern image produced on the screen of display cathode ray tube **6** may proceed to enter corresponding pattern information in an empty memory unit by actuating corresponding ones of a plurality of data keys **122** provided on a keyboard **120** of control unit **7**. When actuated, each of the keys **122** causes a respective unique 3-bit code to be entered into the accessible keyboard address in the memory **9**, which code may represent a particular colour or type of switch and will consequently give rise to an appropriately coloured element in the display. Actuation of a key **122** normally also produces a change of keyboard address by one element. Conveniently, the first pattern element entered in the memory appears at one end of a line and, because the bottom of a pattern is usually the first portion to be knitted, it will be convenient to arrange that the first pattern indication appears at the bottom, left-hand corner of the display.

In the present embodiment information is withdrawn from the memory during the scanning period of each display and inserted into the memory during the fly-back periods of the scan. Other time division methods may be used if preferred.

Because information is required to be withdrawn from the memory during the whole of each field scanning period, though not during the fly-back periods, the information to be inserted in the memory, denoted by the actuation of the data keys, must be stored until the end of a field scan and then fed into the memory in the appropriate locations. These operations are effected by the Keyboard Encoder and Address circuits described below in relation to FIGS. **8** and **9**.

FIG. **8** shows the keyboard encoder circuit **160**; in this Figure, those circuit elements which are identically repeated are shown in full only once. The keying circuit, which is repeated for each of the five data keys and for the space bar (here referred to as Keys Nos. **1** – **6**) is first described. The No. **1** key when actuated applies an enabling signal by way of a Schmidt NAND gate **162** to a flip-flop **163**, which generates an output pulse of **400** nS duration. This pulse is applied to one input of an **8**-input NAND gate **164**. The output signal of flip-flop **163** is also applied by way of a NOR gate **165** and NAND gate **166** to develop a signal on a line **167**. Signals are similarly developed on line **167** when any other one of keys Nos. **1** – **6** is actuated. The signal on line **167** thus denotes that a key has been actuated and is employed to prevent other circuits responding to spurious signals which may arise when a key has not been actuated, and also as a preparatory signal to enable a buffer store which is described later.

The output signal of NAND gate **164** is applied by way of a NOR gate **168** to a further flip-flop **169** which generates a **476** nS pulse. This pulse is returned to an input of gate **164** as a lock-out pulse to prevent the circuit responding a second time if the key should still be held actuated at the end of the first pulse from flip-flop **163**. The output of the eight-input gate **164** is also fed over a line **170** to each of the eight-input gates in the other five keying circuits, to act as a lock-out signal, and is additionally directed over a line **171** to the coding circuit **172** described below. Gate **164** itself receives a lock-out signal over one of the lines **173** from the output of the eight-input gate in each of the other keying circuits, whenever the respective key is actuated.

The keying signals provided on line **171** and on corresponding lines **174** from the other keying circuits are each applied to a different combination of three NAND gates **175, 176, 177** in the coding circuit **172**, so that output signals appear at a unique combination of the three gates in response to actuation of each of the six keys. In the present embodiment the codes produced by actuation of the keys are as shown below, but these may be altered as desired by reconnection of the key outputs to the gates.

	Gate		
Key	175	176	177
1	x	—	—
2	—	x	—
3	x	x	—
4	—	—	x
5	x	—	x
6	x	x	x

Whenever a signal appears at the output of any one of gates **175** – **177** a NOR gate **178** connected to all of the outputs itself provides an output signal to a flip-flop **179** in a first buffer store stage **180**. Stage **180** includes a Quad D-type flip-flop **181** into which are fed the outputs of gates **175** – **177** and also the preparatory signal on line **167**. This latter signal is also applied to a NAND gate **182** which ensures that the output signal of flip-flop **179** can pass to clock store flip-flop **181** only when a preparatory signal is present on line **167**. When buffer flip-flop **181** is clocked by the output from flip-flop **179** the signals applied to its four inputs appear on corresponding output lines **183** and are applied to a succeeding buffer store stage **184**. The code output signals are also applied to a NOR gate **185** yielding a drive signal to buffer stage **184** whenever a signal appears on any output line of stage **180**. The arrangement of stage **184** and of a third succeeding buffer store stage **186** are identical with those of stage **180**. The signals appearing on the output lines **187** of third buffer store stage **186** are fed to the memory **9** to be entered in the currently accessible address. Output signals from NOR gate **178**,

from NOR gate **185** in the first buffer store stage **180** and from the corresponding NOR gates in second and third buffer store stages **184** and **186** are applied to a NAND stage yielding a NO DATA IN STORE signal on a line **189** to the address circuit (FIG. **9**) when all the store stages are empty and the on coder output is zero. A signal which is developed by the NOR gate of third buffer store stage **186** when any output signal is present is inverted in an inverter **190** and applied to a NAND gate **191** which also receives the preparatory output signal from stage **186** and which yields a NEW DATA AVAILABLE signal to the memory on a line **192.**

If the same or other keys are pressed twice more, then corresponding codes will be entered into the second and the first buffer store stages **184, 180.** When the information on output lines **187** has been entered into the memory in known manner which does not require description a DATA TRANSFER COMPLETE signal is provided by the memory on a line **193** and applied to a flip-flop **194** yielding a **105** nS pulse over a line **195** to clear the third buffer stage **186.** When all lines of the stage carry logical 0's the output signal from the NOR gate fires the flip-flop which clocks the code from the output of the second stage **184** to the output of the third stage **186.** This operation causes firing of the drive flip-flop of stage **180** also, in a similar manner, so that a code at the output of the first buffer store stage **180** is transferred to the second stage **184.** Thus as soon as a code is read by the memory it is cleared from the buffer store and the next code is automatically clocked into its place.

When flip-flop **194** is fired by the DATA TRANSFER COMPLETE signal on line **193** it will if an AUTO/MANUAL switch **196** is set to AUTO, pass a STEP ADDRESS ON ONE signal on to a line **197** to control the keyboard address circuit described below in relation to FIG. **9.**

A Repeat key **198** may be pressed simultaneously with any one of the Data keys. When actuated, this key allows pulse signals from a Repeat Generator **199** to recycle the respective keying circuit flip-flop as long as both the Repeat and Data keys are actuated. The repeat signal is also fed out over a line **200** to the address circuits described below in relation to FIG. **9** where they are used as there described to produce repetitive movement of the Marker display.

An Inhibit key **300** applies a signal to NAND gate **162** and another signal, inverted by an inverter **301,** by way of a line **302** to an input of the eight-input NAND gate of the keying circuits, to prevent inadvertent actuation of the keys producing a change in the data in the memory during periods in which operation of the system is interrupted.

The keyboard addressing circuitry is shown in FIG. **9.** It comprises a Wale Counter **201** and a Course counter **202,** the outputs of which are fed over cables **203, 204** to the wale and course address circuits of the memory **9.** Each counter provides an eight-bit address to the memory. The outputs from each counter are monitored by a respective logic circuit **205, 206** which detects the presence of an all 0's output from the respective counter and when this is present applies an inhibiting signal to a respective gate **207, 208** which locks out the "Down" input to that counter and thus prevents it being made to count down through zero to provide a fixed datum position for the display.

The addressing circuits are chiefly controlled by four Marker keys **211, 212, 213** and **214** which produce movement of the keyboard address and therefore of the displayed marker, in the four directions RIGHT, LEFT, UP and DOWN, respectively. When key **211** is actuated it applies a logic signal by way of a NAND gate **215** to initiate a flip-flop **216,** which in turn applies a signal by way of a NAND gate **217** and an inverter **218** to the UP input of wale counter **201,** thus producing a shift of the marker to the right in the display. The output signal from gate **215** is also applied to lock out a gate **214** through which the logic signal from the LEFT key **212** is applied to initiate a flip-flop **220** from which a signal is applied by way of lockout gate **207** to the DOWN input of the wale counter **201.** The output signal of gate **214** is applied to lock-out gate **215,** so that inadvertent actuation of both keys simultaneously does not produce incorrect operation of the system.

UP key **213** when actuated provides a logic signal to a gate **221,** the output signal of which initiates a flip-flop **222,** the signal from which is applied by way of a gate **223** and an inverter **224** to the UP input of Course Counter **202.** The DOWN key **214** supplies a logic signal to a gate **225,** of which the output initiates a flip-flop **226,** of which the output is applied by way of lock-out gate **208** to the Down input of the Course Counter **202.** The outputs of each of gates **221, 225** lock-out the other gate to prevent operating errors. The keys thus far described permit the addresses generated in the counters **201, 202** to be increased or reduced and so would suffice to obtain access to any address in the memory. To expedite operation of the system, facilitates for obtaining immediate return to a predetermined setting of one or both counters, as desired, may be provided. To this end, a set of D-type flip-flops is provided to store the number appearing on the output lines of each counter when a respective Wale Tab key or Course Tab key is actuated. Actuation of the Wale Tab key **228** applies an initiating signal to a flip-flop **229,** the output of which clocks the WALE TAB set of flip-flops shown as a single unit **230.** These flip-flops receive the counter output signals at their inputs and, when clocked, apply the signals on their inputs to reset the respective counter stages to that number. To establish a position to which the counter may be returned from any other position, therefore, the counter is set by actuation of the marker controls to the appropriate position and the respective TAB key is actuated. This enters into the D-type flip-flops the number to which the counter is then set, and clocking of the counter load line at any layer time will reset the counter to that number. A similar operation occurs on actuation of the Course TAB key **231,** which actuates a flip-flop **232** to clock the load lines of the COURSE counter **202.**

Return of the marker to a predetermined position may be effected in either of two ways; by depressing the Line Return key **234** or the Block Return key **235.** Actuation of the Line Return key **234** passes a logic signal through a gate **236** to actuate a flip-flop **237.** The output signal of gate **236** is applied to inhibit a gate **238** in the Block Return circuit next to be described. The output signal of flip-flop **237** applies an inhibiting signal to gates **239, 240** inhibiting the Load and Clear lines of the Course Counter **202.** Finally, the output signal from flip-flop **237** is applied by way of gate **223** to the Up input of the Course Counter **202,** thus adding one to the number present in the counter, and also fires a fur-

ther flip-flop **241**, the output signal of which clears the Wale Counter **201** and also fires a third flip-flop **242** yielding an output which, is applied to a NAND gate **243** together with the output of flip-flop **241** after inversion in an inverter **244**, so that the output of NAND gate **243** is inhibited. When flip-flop **241** returns to normal the output of gate **243** is applied to load the Wale counter **201** with the number then present in the output of the Wale Tab flip-flops. This number then appears on the address output lines.

Actuation of the Block Return key **235** produces an action generally similar to that of the Line Return key, but in this case flip-flop **237** is not fired, so that the Course Count remains unchanged and the clear and load lines of the course counter are not inhibited. Thus both counters are cleared and then loaded with the predetermined numbers set into the respective TAB stores, as described above.

The NO DATA IN STORE signal developed in the Keyboard encoder described with reference to FIG. **8** is received on line **189** and is applied to inhibit all the keys controlling the address until all information from the keyboard has been entered into the store. The STEP ADDRESS signal from the keyboard is received on line **197** and is applied to gate **217** to add one to the Wale count.

When it is desired to change the address, i.e., to move the marker, by more than one stitch or course, then the appropriate Marker Key, **211–214** is actuated together with the Repeat key **198** adjacent the Data keys. A pulsed signal is then received over line **200** and causes repeated firing of the respective flip-flop to produce rapid movement of the marker in the desired direction.

The number representing actual address to which access is at any time available is shown to the operator numerically. Decoders **245, 246** connected to the output lines **203, 204** of counters **201** and **202** respectively control 3-digit displays **247** and **248** which show the present Wale and Course numbers.

To generate the marker signal which gives rise to the appearance of a pulsating white element in the display, the keyboard wale and course addresses are continuously compared with the display wale and course addresses and a marker bit is inserted in the circulating register when both addresses coincide. The circuit arrangement is shown in FIG. **10.** The Wale Display and Keyboard addresses appearing on line **17***a* of FIG. **7** and on lines **203,** of FIG. **9** are applied to a comparator circuit **250** of known kind which yields an output signal on a line **251** only when the corresponding digits of the two addresses are identical in each case. This signal is applied to a Marker gate **252** and to a gate **253** which controls the lighting of a Wale Marker lamp **254.** The lamp is lit whenever the marker address set by the keyboard is within the display in the Wale direction. The Course addresses for the display and the keyboard which appear on lines **17***b* of FIG. **7** and on line **204** of FIG. **9** are applied to a Course Comparator **255** yielding an output on a line **256** only when the compared address numbers are identical. The signal on line **256** controls a gate **257** to light a Course Marker lamp indicating that the marker address set by the keyboard is within the display in the Course Direction. When signals on lines **251** and **256** are applied simultaneously to marker gate **252** a signal will appear on line **259** to be inserted in the display as described with reference to FIGS. **5** and **6.** The purpose of the two Marker lamps is to indicate when the marker address is or is not present in the displayed area of the pattern information.

It will be understood that although an advantageous complete system has been described, the described means for superimposing a pattern information display representative of pattern information stored in a memory device upon an image of an original pattern representation may be used without providing the means for entering pattern information into the memory. Similarly, means for displaying pattern information contained in a memory and for entering pattern information into the memory may be employed without the provision of means for combining an image of an original pattern information with the display.

It will be seen that the pattern control system described above enables pattern information corresponding with an image of an original pattern representation to be very rapidly introduced into a memory while providing an immediate visual display of the information so entered for comparison with the image of the original pattern.

We claim:

1. A pattern control system comprising a television camera including a pickup tube viewing an original pattern representation to develop a video signal representative thereof and scan generators for said pickup tube;

memory means containing pattern information storage locations represented by address numbers, whereby application of signals representative of said numbers to said memory means obtains access to said locations;

display means including a television picture tube having a viewing screen and scan generators for said picture tube;

synchronizing signal generator means producing line and field synchronizing signals;

circuit means applying said synchronizing signals to said scan generators of said television camera and of said display means to produce corresponding scans thereon;

means applying said video signals to said picture tube to develop an image of said pattern on said viewing screen;

access means operable to develop said address numbers thereby to withdraw said pattern information from said memory means as memory output signals;

display control means fed with said memory output signals to develop individual control signals representative of display elements corresponding to said information;

and combining means applying said control signals to said picture tube together with said video signals to produce thereon a display representative of said image and of said stored pattern information.

2. The system claimed in claim **1** and further including support means supporting said pattern representation in a plane and camera mounting means, said support means and mounting means together providing relative movement of said representation and said camera in two directions in said plane and along an axis perpendicular thereto.

3. The system claimed in claim **1** and further including adjustable support means supporting said pattern representation for movement in two directions in a plane, said camera having a variable magnification lens of constant focal distances.

4. The system claimed in claim 1 and further including variable amplification means whereby vertical deflection signals produced by said scan generator means are applied to said pickup tube and means controlling said variable amplification whereby to change the aspect ratio of said pattern image.

5. The system claimed in claim 1 wherein said pickup tube is an electrostatically deflected pickup tube.

6. The system claimed in claim 1 wherein said pickup tube is an electrostatically deflected pickup tube.

7. The system claimed in claim 1 wherein said television picture tube is a colour television picture tube, said system further including individual potentiometer means operable to adjust individually the colour of the said display element produced in response to the application of each of said control signals to said picture tube.

8. The system claimed in claim 7 wherein said television camera is a colour television camera developing colour television video signals and including circuit means whereby said colour television video signals are applied to said colour television picture tube to produce a coloured image of said pattern representation.

9. The system claimed in claim 7 and further including common potentiometer means connected in circuit with all said respective potentiometer means, whereby the intensity of all said display elements may be adjusted simultaneously.

10. The system claimed in claim 9 and further including individual switch means whereby any one of said respective potentiometer means may be disconnected from said common potentiometer means and connected to an additional potentiometer means permitting individual control of the intensity of the respective pattern indication.

11. The system claimed in claim 1 wherein said access means includes:

two shifting registers;

switching means operable to connect said shifting registers in alternation to receive information signals from said memory means and to supply information signals to control said display;

first pulse generator means responsive to said line synchronizing signals to develop first pulse trains each including a predetermined number of pulses, said pulse train having a first repetition rate;

pulse counter means responsive to said line synchronizing pulses to develop a counter output pulse in response to each predetermined plurality of said synchronizing pulses;

second pulse generator means responsive to said counter pulses to develop second pulse trains each including said predetermined number of pulses, said second pulse train having a repetition rate equal to said first repetition rate divided by the number of said predetermined plurality;

first display address counter means holding a number denotive of part of the address of an information storage location in said memory means;

means applying said second pulse train to change the number in said first display address counter and to shift said shifting register connected to receive information signals from said memory means;

means applying said display address number to said memory means to cause the development of information signals sequentially representative of information stored in said predetermined number of adjacent locations;

means applying information signals developed by said memory to said shifting register connected to receive information signals;

means applying said plurality of first pulse trains to said shifting register connected to supply information signals to cause the repeated development of information signals stored therein;

and means applying said repeatedly developed information signals to control said display means to develop said information display.

12. The system claimed in claim 11 and including adjustable signal delay means having a signal delay adjustable by an applied voltage, means including said signal delay means for applying said line synchronizing pulses to said first pulse generator, voltage divider means developing an adjustable voltage and circuit means applying said adjustable voltage to said signal delay means whereby to provide lateral adjustment of the position of said display.

13. The system claimed in claim 12 and further including adjustable further signal delay means adjustable by an applied voltage, gate means controlling the application of said line synchronizing signals to said first pulse generator means, means including said further signal delay means for applying said field synchronizing signals to said gate means, and potentiometer means providing a further adjustable voltage to control said further delay means whereby to provide vertical adjustment of the position of said display.

14. The system claimed in claim 12 wherein said voltage divider means voltage-variable resistance means, and further including ramp voltage generator means actuated by said field synchronizing pulses to develop a ramp voltage of adjustable amplitude repetitive at field frequency, and circuit means applying said ramp voltage to control the resistance of said variable resistance means whereby to provide adjustment for the orthogonality of said display.

15. The system claimed in claim 11 and including a second address counter holding a second address number denotive of the remainder of the address of said location;

presettable switch means adjustable to establish a further predetermined number:

comparator means responsive to said first address number and to said further predetermined number to develop a return signal when said numbers are identical;

means applying said return signal to restore said first address counter to a predetermined state of count;

means applying said return signal also to said second address counter to change said second address number; and

means applying said second address number to said memory means to control the development of said information signals.

16. The system claimed in claim 15 and further including:

number signal storage means;

transfer means operable to apply signals representative of the number in a said address counter to said storage means to be stored therein;

resetting means operable to reset said address counter with signals from said storage means to said stored number.

17. The system claimed in claim 15 wherein said address counter means contains means operable by said return signal to reverse the direction of count of said counter and means operating in response to said counter reaching a zero state of count to again reverse its direction of counting.

18. The system claimed in claim 15 and further including:

signal generator means generating repetitive signals;

first shift key means operable to apply said repetitive signals to said first display address counter means to change the number therein in a first sense;

second key means operable to apply said repetitive signals to said first address counter means to change the number therein in the sense opposite to said first sense;

third key means operable to apply said repetitive signals to said second address counter means to change the number therein in said first sense; and

fourth key means operable to apply said repetitive signals to said second address counter means to change the number therein in said opposite sense.

19. The system claimed in claim 18 and including also a further key means operable to change the repetition rate of said repetitive signals.

20. The system claimed in claim 1 and further including keyboard means operable to introduce any one of a plurality of predetermined pattern-representative coded signals into any selected location in said memory means, said keyboard means comprising:

keyboard encoder means responsive to the actuation of any one of a plurality of data keys to develop a respective said coded signal;

keyboard address means including keyboard address counter means holding a number representative of a said location in said memory means;

pulse generator means responsive to actuation of any one of said data keys to apply a pulse to said address counter means to change the number therein; and

means applying said coded signal and said address number to said memory means whereby to enter said signal in said location.

21. The system claimed in claim 20 and further including coded signal storage means receiving said coded signals developed by actuation of said data keys and signal transfer means operable to transfer said stored signals sequentially to said memory means.

22. The system claimed in claim 20 and further including a repeat pulse generator developing periodically repeated pulses and a repeat key operable to apply said repeated pulses to said keyboard encoder means to produce repeated generation of a said coded signal selected by actuation of a said data key and to said keyboard address means to produce repeated change of said address number.

23. The system claimed in claim 20 wherein said keyboard address counter means includes first and second counters, a tabulator key, number storage means, transfer means operable in response to actuation of said tabulator key to transfer the number in a said counter into said number storage means, a return key and loading circuit means responsive to the actuation of said return key to set said counter to the number stored in said number storage means.

24. The system claimed in claim 23 and including a line return key, means coupling said line return key to said transfer means, a pulse generator, means initiating said pulse generator in response to actuation of said line return key and means applying pulses generated by said pulse generator to the other of said keyboard address counters, whereby actuation of said line return key returns one said counter to a predetermined state of count and changes by one the count in the other said counter.

25. The system claimed in claim 20 and further including first pulse generator means operable by a first marker key to apply a signal to said keyboard address counter means to change a first component of said address number in a first sense, second pulse gnerator means operable by a second marker key to apply a signal to said keyboard counter means to change said first component of said address number in the sense opposite to said first sense, third pulse generator means operable by a third marker key to change a second component of said address number in a first sense and fourth pulse generator means operable by a fourth marker key to change said second component in the sense opposite to said first sense.

26. The system claimed in claim 25 and further including a repeat pulse generator developing periodically repeated pulses and a repeat key operable when a said data key is actuated to apply said repeated pulses to said keyboard encoder means to produce repeated generation of the said coded signal selected by actuation of said data key and to said keyboard address means to produce repeat change of said address number, and said repeat key being operable when a said marker key is actuated to apply said repeated pulses to said keyboard address counter means to produce repeated change of the selected address number component in the selected sense.

27. The system claimed in claim 25 wherein said access means includes display address counter means holding a display address number, said system further including comparator means responsive to said display address number and to said keyboard address number to develop a marker signal when said numbers are identical and marker display means applying said marker signal to produce an individual component of said display.

28. The system claimed in claim 27 and further including shifting register means operable alternately to receive signals and to supply signals to control said display, said shifting register means including a plurality of channels receiving signals from said memory means and a further channel, said marker display means operating to apply said marker signal to said further shifting register channel.

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