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11/013,573 15 December 2004 (15.12.2004) US(71) Applicant (for all designated States except US): **HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.** [US/US]; HEWLETT-PACKARD COMPANY, INTELLECTUAL PROPERTY ADMINISTRATION, 20555 S.H. 249, Houston, Texas 77070 (US).

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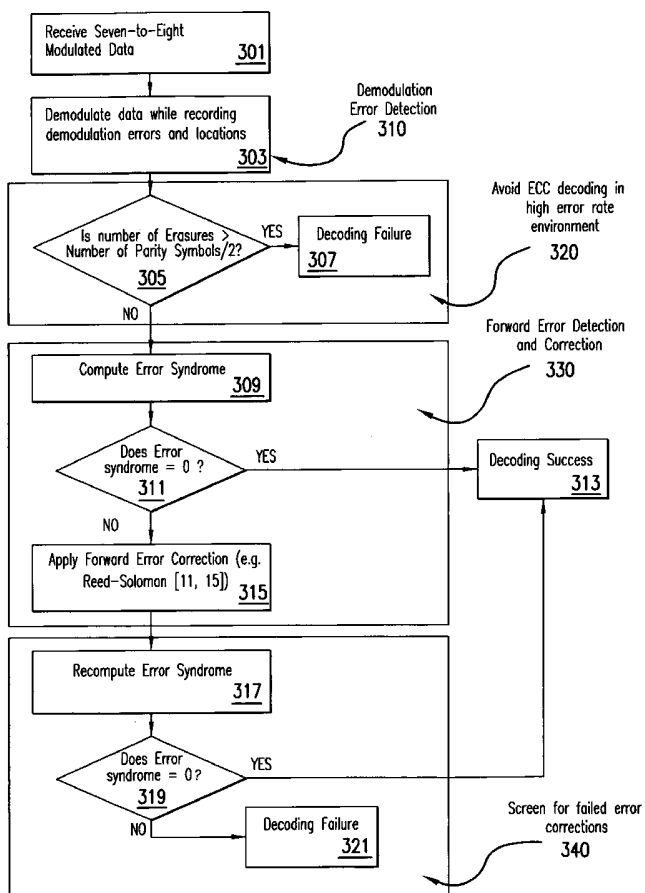
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(54) Title: ERROR DETECTION AND CORRECTION



(57) Abstract: A method for error detection and correction comprising performing a first modulation error scan (310) of said modulation symbol, marking (305) data that fails to comply with a predetermined criteria, demodulating (303) said modulation symbols, computing a first error syndrome (309) using said demodulated symbols, and correcting (315) errors using said error syndrome computation.

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ERROR DETECTION AND CORRECTION

Related Application

The present invention claims priority to a provisional application, serial number unknown, by the same inventors and entitled "Error Correction Technique" (attorney docket 200404329-1) filed on December 12, 2004.

Background

[0001] Numerous applications utilize digital data storage and transmission for data communication, such as sending information via internet web sites or storing information on compact discs. Digital transmission systems or digital data storage systems typically use a sequence of binary information, either delivered to a receiver across a transmission channel or stored to a medium (e.g., CDROM). However, the binary information may become corrupted during storage or transmission, which could impair the accuracy of the information.

[0002] As a result, error control coding is often applied to the transmitted or stored data. Techniques known as forward error correction schemes have been developed to improve the reliability of the data communicated in digital applications. Forward error

correction schemes are error control techniques that can detect and correct corrupt data without requiring the transmitter to re-send the information. An example of such a scheme is the Reed-Solomon code.

[0003] Many forward error correction schemes, such as the Reed-Solomon code, typically encode a group of data symbols into blocks of a predetermined size. For each block, an additional number of “parity” symbols are computed and added. The resulting augmented block is typically referred to as a “codeword.” Following transmission, or following reading of the stored data, a decoding technique is applied to the codeword to correct for errors that occurred during storage or transmission to thus restore the original data.

[0004] While such techniques have improved the reliability of transmitted digital data, further improvement is desirable. Despite the use of current error correction techniques, undetected errors may still occur, or errors may be detected but not properly corrected. This results in data that is less reliable than desired.

Brief Description of the Drawings

[0010] For the purpose of illustrating the invention, there is shown in the drawings one exemplary implementation; however, it is understood that this invention is not limited to the precise arrangements and instrumentalities shown.

[0011] Figure 1A is a flow chart illustrating an exemplary implementation of the encoding process of present invention.

[0012] Figure 1B is a flow chart illustrating an exemplary implementation of the decoding process of the present invention.

[0013] Figure 2 is a table illustrating the codebook of an exemplary modulation scheme used in an exemplary implementation the present invention.

[0014] Figure 3 is a flow chart illustrating a second exemplary implementation of the present invention.

Detailed Description

Overview

[0015] Various types of systems utilize digital data storage or transfer to communicate information. One exemplary system that employs digital data transfer is the LightScribe® Media Identification System (hereinafter “the LightScribe system”) produced by Hewlett-Packard (Palo Alto, CA). The exemplary embodiment of the invention described herein shall be described with reference to its use in conjunction with the LightScribe system; however, it is understood that the invention could be used on other systems that uses digital data storage or transfer.

[0016] In an encoding process, a sequence of information in binary form is initially partitioned into error control coding (ECC) symbols. In the exemplary implementation, each ECC symbol comprises seven data bits. Eleven ECC symbols containing message data are combined with four ECC parity symbols to form a fifteen-symbol codeword. Each individual seven-bit ECC symbol within the codeword is then modulated using a seven-to-eight bit modulation scheme to create a modulation symbol that is 8 bits in length. A fifteen-symbol modulation codeword is thus created from the fifteen-symbol ECC codeword. The details of one useable modulation scheme employed in the LightScribe system is further described in a U.S. Patent Application entitled “Data Modulation” filed on December 14, 2004 and is fully incorporated herein by reference.

[0017] Typically, existing error correction techniques have been used to perform forward error correction on received codewords to correct for bit errors which may occur in transmission or storage. However, existing techniques fail to adequately address certain conditions. First, existing error correction techniques may fail to detect

a particular error pattern. This type of failure is referred to as a “missed detection” event. Second, an error correction scheme may detect the existence of an error, and thus apply a correction, but fail to accurately correct the data to reflect the original data. This type of failure is referred to as a “false correction” event.

[0018] Missed detection events and false correction events reduce the overall reliability of the forward error correction process. The occurrence of these events is significantly reduced by the error correction scheme in accordance with an exemplary implementation of the present invention.

Error Correction Technique

[0019] Figure 1A is a flow chart illustrating one embodiment of the steps involved in performing the encoding in accordance with the present invention. Alternatively, the flow chart of Figure 1A may be viewed as describing the operation of a system configured to practice an embodiment of the present invention. The original raw digital data comprises a series of binary digits, or bits. In the exemplary implementation of the encoding process, these bits are divided into groups of seven, forming seven-bit ECC symbols. A sequence of seven-bit ECC symbols representing the original data constitutes the message data (step 101).

[0020] In the forward error control encoding process, additional ECC parity symbols are computed and added to the message data to form the ECC codeword data (step 103). These additional ECC parity symbols provide redundancy that is used by a corresponding error detection and correction process performed on received data to detect and correct for errors that occur during storage or transmission of the data.

[0021] In the modulation process, the seven-bit ECC symbols of the ECC codeword are modulated to create eight-bit modulation symbols using a seven-to-eight modulation technique (step 105). The modulation technique employed in the exemplary embodiment results in each valid modulation symbol containing no fewer than three “1” bits and three “0” bits. The seven-to-eight modulation technique used in the exemplary embodiment is a codebook modulation technique. Each seven-bit ECC symbol is assigned to a valid modulation symbol obtained from the codebook for the seven-to-eight bit modulation.

[0022] Referring to Figure 2, a table illustrating an exemplary seven-to-eight bit modulation codebook is shown. Column 1 (“Data”) lists the possible unmodulated seven-bit ECC symbols. Column 2 (“Symbol”) lists the corresponding modulation symbols assigned to each possible seven-bit ECC symbol. Modulation symbols that contain fewer than three binary “1” bits of the eight possible bits are deemed to be invalid, and thus are not used as a valid modulation symbol for a seven-bit ECC symbol. Modulation symbols that contain fewer than three binary “0” bits of the eight possible bits are deemed to be invalid, and thus are also not used as a modulation symbol for a seven-bit ECC symbol. Using such a codebook, the resulting modulation symbols have a “3-to-5” bit condition, meaning that each valid modulation symbol contains between three and five “1” bits and between three and five “0” bits.

[0023] In the exemplary embodiment, each seven-bit ECC symbol is assigned in numerical order to a valid modulation symbol (i.e., an eight-bit modulation symbol that meets the 3-to-5 condition) to perform the modulation process. For example, referring to Figure 2, the first ECC symbol comprising “0000000” is assigned to the first valid modulation symbol, which is “00000111.” The first seven eight-bit modulation symbols

(00000000, 00000001, 00000010, 00000011, 00000100, 00000101, and 00000110) are skipped, as these modulation symbols are deemed to be invalid for failing to meet the “3-to-5” condition. The next three eight-bit modulation symbols are also skipped (00001000, 00001001, 00001010) for the same reason, with the next seven-bit ECC symbol (0000001) being assigned to the next valid eight-bit modulation symbol (00001011). This process is repeated until all possible seven-bit ECC symbols have been assigned to a corresponding eight-bit modulation symbol.

[0024] After all possible seven-bit ECC symbols have been assigned, there are several valid eight-bit modulation symbols remaining that have not been matched with a seven-bit block. These remaining modulation symbols may be used for various purposes (e.g., as control words, etc.), but they are not required to implement the exemplary embodiment of the error correction technique, and thus shall not be addressed herein.

[0025] The sequence of eight-bit modulation symbols forms a signal that may be stored or transmitted (step 109). Upon receipt of the stored or transmitted signal, the encoding process is reversed in a decoding process, as shown in Figure 1B and discussed below.

[0026] Referring to Figure 1B, in the decoding process each modulation symbol contained in the fifteen symbol codeword is subjected to a demodulation process (step 151). Typically, this demodulation process is performed upon the modulation symbols following reading from a storage medium or transmission over a transmission channel. However, the storage or transmission of the modulated symbols is not pertinent to the error correction technique of the present invention, and thus shall not be discussed in detail herein.

[0027] The demodulation process reverses the modulation process described above. Each modulation symbol is mapped to an ECC symbol. During the demodulation process, a check is conducted to determine if any modulation symbol contains fewer than three or more than five of either a binary "1" bit or a binary "0" bit (step 153). Because the parameters of the seven-to-eight bit modulation requires the 3-5 condition as described above, any modulation symbols that fail to conform to the 3-5 condition are marked as containing symbol erasures (i.e., bit errors in the modulation symbol) at this point (step 155). This marking of symbol erasures consists of recording the location of the symbol erasure in the codeword and, since we do not have an ECC symbol associated with the modulation symbol erasure, the assignment of the ECC symbol "0" (all seven bits zero) at that codeword location. The number and locations of symbol erasures are thereby noted to indicate errors in the modulation symbols.

[0028] The demodulation process is conducted for each modulated symbol contained in a codeword. That is, after demodulating a symbol and marking any erasures, a check is performed to determine if there are remaining symbols in the codeword (step 157), and if so, the next symbol is selected to be demodulated (step 159).

[0029] Some storage or transmission errors may cause bit errors in a modulation symbol that do not result in the modulation symbol being flagged as an erasure. Therefore, the erasure check does not reliably detect all storage or transmission errors. Consequently, performing forward error correction using erasure ECC symbols may still result in a false correction event, which would decrease the reliability of the data. If performing the error correction process on data that is more likely to result in false

correction events can be avoided, the occurrence of false correction events will be reduced and thus the data reliability will be improved.

[0030] The exemplary embodiment of the error correction method determines the location and magnitude of symbol errors through a search procedure. If the location of a symbol error is known *a priori*, as is the case with a detected modulation error, the error correction method utilizes less information in computing the symbol correction at that location than would have been used to both detect the symbol error location and to compute the symbol error correction at that location. Since not all symbol errors may be detected in the demodulation process, by recording the location of those symbol errors that are detected in the demodulation process and providing those locations to the error correction method, increased performance of the error correction method is obtained.

[0031] The demodulation process results in retrieving an ECC codeword comprising seven-bit ECC symbols. The number of modulation errors detected in the demodulation process serves as an estimate of the total error rate in the stored or transmitted data, including errors not detected in the demodulation process. Once all symbols in a codeword have been demodulated, a determination is made to decide if error correction is to be applied. If the demodulation process detects a number of modulation errors that exceeds a specified threshold (step 161), the decoding process is terminated (step 163). By avoiding applying the forward error correction method when the number of modulation errors exceeds a threshold, the risk of false corrections that exists in the presence of a high error rate is reduced. In the exemplary embodiment, this threshold is the number of errors the forward error correction scheme could correct without any other error detection process. The exemplary embodiment uses a Reed-Solomon code. Reed-Solomon codes typically can correct for errors when the number of errors is fewer

than the number of parity symbols divided by two. For the exemplary Reed-Solomon (15,11) code, the modulation threshold is two (i.e., four parity symbols divided by two equals two). Therefore, if the number of modulation errors exceeds two, the decoding process is terminated and a decoding failure is noted.

[0032] A forward error correction scheme is applied using the demodulated ECC codeword and the number and location of detected modulation errors (step 165). In the exemplary embodiment, a Reed-Solomon (15,11) forward error correction scheme using seven-bit symbols is applied. However, other error correction techniques could also be used such other Bose, Chaudhuri, and Hocquenghem (BCH) codes or other cyclic linear block codes (e.g., Hamming codes). The operation of such codes are well known in the art.

[0033] Following the application of the Reed-Solomon (15,11) code, further reduction of possible false correction events is achieved by performing a second screening process on the data. To further filter out false correction events, the error syndrome is recomputed (step 167). The error correction process is not considered to be successful if the recomputed error syndrome after data correction is non-zero, which would indicate the presence of additional errors (step 169). By adding an error correction syndrome recomputation process following the application of the error correction syndrome, additional instances of false correction events are identified. If such a recomputed error syndrome is nonzero, the decoding process is terminated (step 163). If the recomputed error syndrome is zero, the correction is deemed successful (step 171).

[0034] Figure 3 is a flow chart illustrating the decoding process of the exemplary embodiment of the present invention. Alternatively, the flow chart of Figure 3 may be

viewed as describing the operation of a system configured to practice an embodiment of the present invention. Initially, the ECC symbols are modulated to obtain seven-to-eight modulated symbols, which may be transmitted to a receiver (301). Using the Reed-Solomon error correction scheme described above, four parity symbols are used in a fifteen symbol ECC codeword.

[0035] During demodulation of the data, the first error detection process is performed (step 303). A comparison is made to determine if the number of modulation errors exceeds a predetermined threshold equal, for example, to the number of parity symbols divided by two (step 305). In the exemplary embodiment, a Reed-Solomon (15,11) code is used. This code uses four parity bits, so the number of parity bits divided by two is equal to two. If, during demodulation, more than two errors or erasures are found, the symbol is deemed uncorrectable (step 307).

[0036] If the number of modulation errors does not exceed the predetermined threshold, then an error syndrome is computed (step 309). A determination is made to see if the computed error syndrome is equal to zero (step 311). If it is, the data is determined to be successfully decoded (step 313). However, if the computed error syndrome is non-zero, errors likely exist in the data. Error correction is applied to the data (step 315). After correction, the error syndrome is recomputed (step 317). If the syndrome now returns a zero result, the data is determined to be successfully decoded (step 313). If the syndrome yields a non-zero result, the data is deemed uncorrectable (step 321).

[0037] Figure 3 illustrates that the error detection and correction scheme in accordance with the present invention reduces the occurrence of false error corrections by combining a demodulation error detection process with a forward error detection and

correction process, while avoiding attempts to correct data when the error rates are high. The invention combines a demodulation process 310 (comprising steps 301 and 303) with a first determination of whether the error environment is higher than desired for reliable error correction 320 (comprising steps 305 and 307). A forward error detection and correction stage is then performed 330 (comprising steps 309, 311, and 315). Following error correction, an additional screening process further identifies false error corrections 340 (comprising steps 317, 319, and 321). By combining these processes, the amount of false correction events is significantly reduced.

[0038] A variety of modifications to the embodiments described will be apparent to those skilled in the art from the disclosure provided herein. Thus, the present invention may be embodied in other specific forms without departing from the spirit or essential attributes thereof and, accordingly, reference should be made to the appended claims, rather than to the foregoing specification, as indicating the scope of the invention.

What is claimed is:

1. A method for detection and correcting within a data codeword in which a plurality of data bits are grouped into an error control coding (ECC) symbol and then modulated into a modulation symbol, the codeword including a plurality of the modulation symbols and at least one parity symbol, the method comprising:
 - performing a first modulation error scan (310) of each of said modulation symbols in said codeword;
 - marking (305) said modulation symbols that fail to comply with a first predetermined criteria;
 - demodulating (303) each of said modulation symbol in said codeword;
 - computing a first error syndrome (309) using each of said demodulated symbols;
 - and,
 - correcting errors (315) using said error syndrome computation.
2. The method as set forth in claim 1, further comprising:
 - computing a second error syndrome (317) following said correcting step; and
 - marking as uncorrectable (321) data where said second error syndrome is non-zero.
3. The method as set forth in claim 1, further comprising terminating the error detection and correction process (307) if the number of marked modulation symbols exceeds a second predetermined threshold.

4. The method as set forth in claim 1, wherein the modulated symbol is modulated using a seven-to-eight bit modulation (105).
5. The method as set forth in claim 1, wherein said first predetermined criteria requires said modulation symbol to have no fewer than three binary "1" bits and no fewer than three binary "0" bits (153).
6. The method as set forth in claim 1, wherein said first predetermined criteria requires said modulation symbol to have no more than five binary "1" bits and no more than five binary "0" bits (153).
7. The method as set forth in claim 1, wherein the plurality of ECC symbols in said codeword is equal to eleven and the at least one parity symbol is four parity symbols.
8. The method as set forth in claim 1, wherein said first predetermined criteria requires the number of marked modulated symbols to be less than the number of parity symbols divided by two (305) in order for the correcting to be performed.
9. The method as set forth in claim 1, wherein said first error syndrome is computed using a forward error code (315).
10. The method as set forth in claim 2, wherein said second error syndrome is computed using a forward error code (317).

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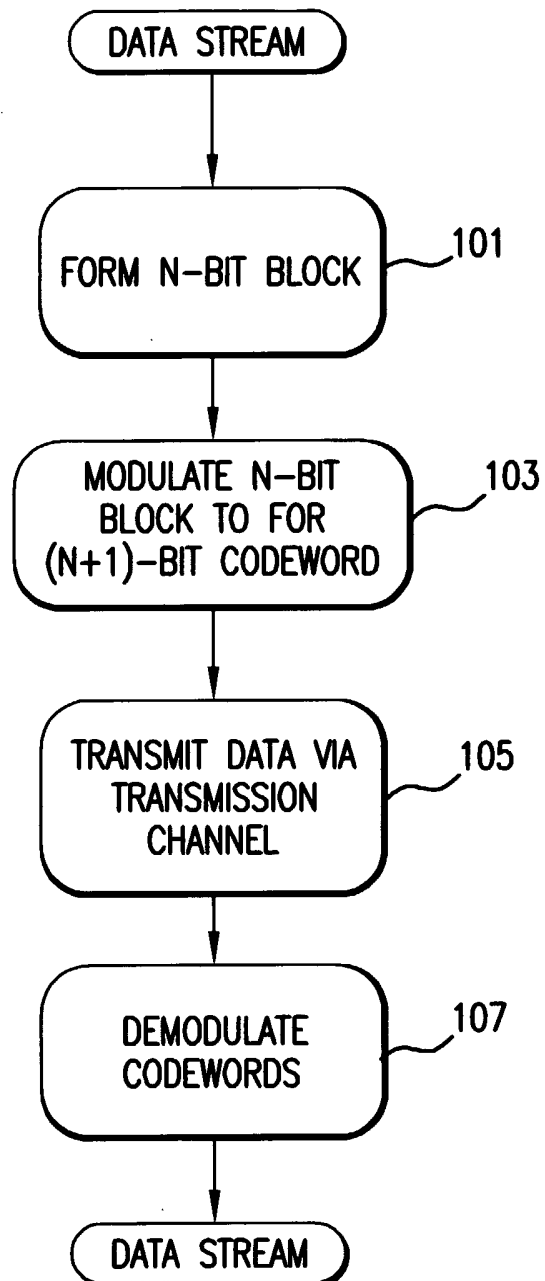


FIG.1A

2/5

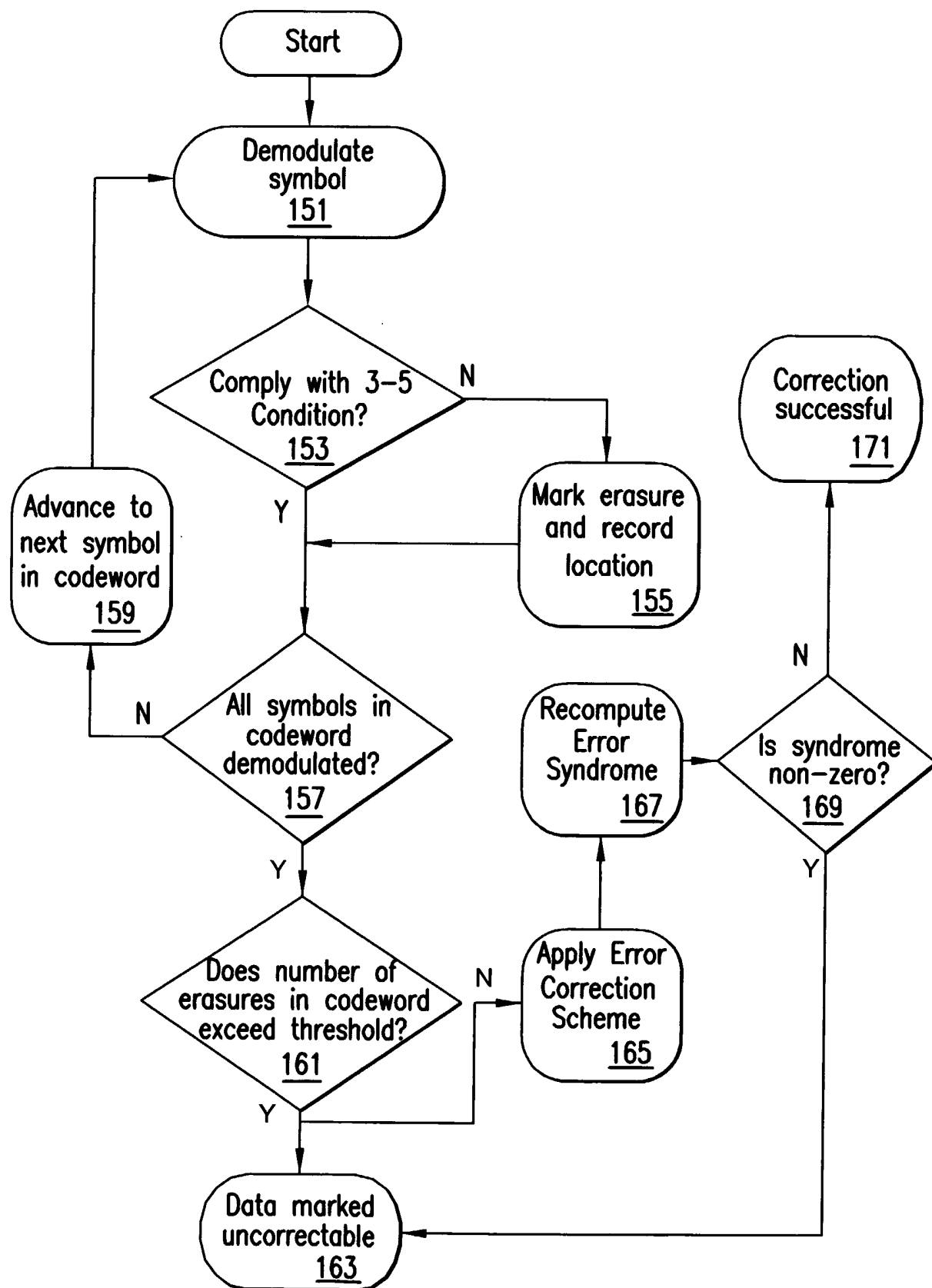


FIG.1B

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7 to 8 bit modulation code

x' denotes Legal symbol

Cxx' denotes reserved control code (to be defined)

7-bit Data	8-bit Symbol	Data	Symbol	Data	Symbol	Data	Symbol	Data	Symbol
Index	0000000	x	0010000	x	0100000	x	0110000	x	1000000
x	0000001	x	0010001	x	0100001	1000010	0110001	x	1000001
x	0000010	x	0010010	x	0100010	1000011	0110010	x	1000010
x	0000011	0010000	00100011	0101001	0100011	1000100	0110011	1011011	1000011
x	0000100	x	00100100	x	01000100	1000101	01100100	x	10000100
x	0000101	0010001	00100101	0101010	01000101	1000110	01100101	1011100	10000101
x	0000110	0010010	00100110	0101011	01000110	1000111	01100110	1011101	10000110
0000000	00000111	0010011	00100111	0101100	01000111	1001000	01100111	1011110	10000111
x	00001000	x	00101000	x	01001000	1001001	01101000	x	10001000
x	00001001	0010100	00101001	0101101	01001001	1001010	01101001	1011111	10001001
x	00001010	0010101	00101010	0101110	01001010	1001011	01101010	1100000	10001010
0000001	00001011	0010110	00101011	0101111	01001011	1001100	01101011	1100001	10001011
x	00001100	0010111	00101100	0110000	01001100	1001101	01101100	1100010	10001100
0000010	00001101	0011000	00101101	0110001	01001101	1001110	01101101	1100011	10001101
0000011	00001110	0011001	00101110	0110010	01001110	1001111	01101110	1100100	10001110
0000100	00001111	0011010	00101111	0110011	01001111	x	01101111	1100101	10001111
x	00010000	x	00110000	x	01010000	1010000	01110000	x	10010000
x	00010001	0011011	00110001	0110100	01010001	1010001	01110001	1100110	10010001
x	00010010	0011100	00110010	0110101	01010010	1010010	01110010	1100111	10010010
0000101	00010011	0011101	00110011	0110110	01010011	1010011	01110011	1101000	10010011
x	00010100	0011110	00110100	0110111	01010100	1010100	01110100	1101001	10010100
0000110	00010101	0011111	00110101	0111000	01010101	1010101	01110101	1101010	10010101
0000111	00010110	0100000	00110110	0111001	01010110	1010110	01110110	1101011	10010110
0001000	00010111	0100001	00110111	0111010	01010111	x	01110111	1101100	10010111
x	00011000	0100010	00111000	0111011	01011000	1010111	01111000	1101101	10011000
0001001	00011001	0100011	00111001	0111100	01011001	1011000	01111001	1101110	10011001
0001010	00011010	0100100	00111010	0111101	01011010	1011001	01111010	1101111	10011010
0001011	00011011	0100101	00111011	0111110	01011011	x	01111011	1110000	10011011
0001100	00011100	0100110	00111100	0111111	01011100	1011010	01111100	1100001	10011100
0001101	00011101	0100111	00111101	1000000	01011101	x	01111101	1110010	10011101
0001110	00011110	0101000	00111110	1000001	01011110	x	01111110	1110011	10011110
0001111	00011111	x	00111111	x	01011111	x	01111111	x	10011111

TO
FIG.2
CONT.

FIG.2

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FROM
FIG.2

Data	Symbol	Data	Symbol	Data	Symbol
x	10100000	x	11000000	C41	11100000
1110100	10100001	C14	11000001	C42	11100001
1110101	10100010	C15	11000010	C43	11100010
1110110	10100011	C16	11000011	C44	11100011
1110111	10100100	C17	11000100	C45	11100100
1111000	10100101	C18	11000101	C46	11100101
1111001	10100110	C19	11000110	C47	11100110
1111010	10100111	C20	11000111	x	11100111
1111011	10101000	C21	11001000	C48	11101000
1111100	10101001	C22	11001001	C49	11101001
1111101	10101010	C23	11001010	C50	11101010
1111110	10101011	C24	11001011	x	11101011
1111111	10101100	C25	11001100	C51	11101100
C1	10101101	C26	11001101	x	11101101
C2	10101110	C27	11001110	x	11101110
x	10101111	x	11001111	x	11101111
C3	10110000	C28	11010000	C52	11110000
C4	10110001	C29	11010001	C53	11110001
C5	10110010	C30	11010010	C54	11110010
C6	10110011	C31	11010011	x	11110011
C7	10110100	C32	11010100	C55	11110100
C8	10110101	C33	11010101	x	11110101
C9	10110110	C34	11010110	x	11110110
x	10110111	x	11010111	x	11110111
C10	10111000	C35	11011000	C56	11111000
C11	10111001	C36	11011001	x	11111001
C12	10111010	C37	11011010	x	11111010
x	10111011	x	11011011	x	11111011
C13	10111100	C38	11011100	x	11111100
x	10111101	x	11011101	x	11111101
x	10111110	x	11011110	x	11111110
x	10111111	x	11011111	Index-bar	11111111

FIG.2 Cont.

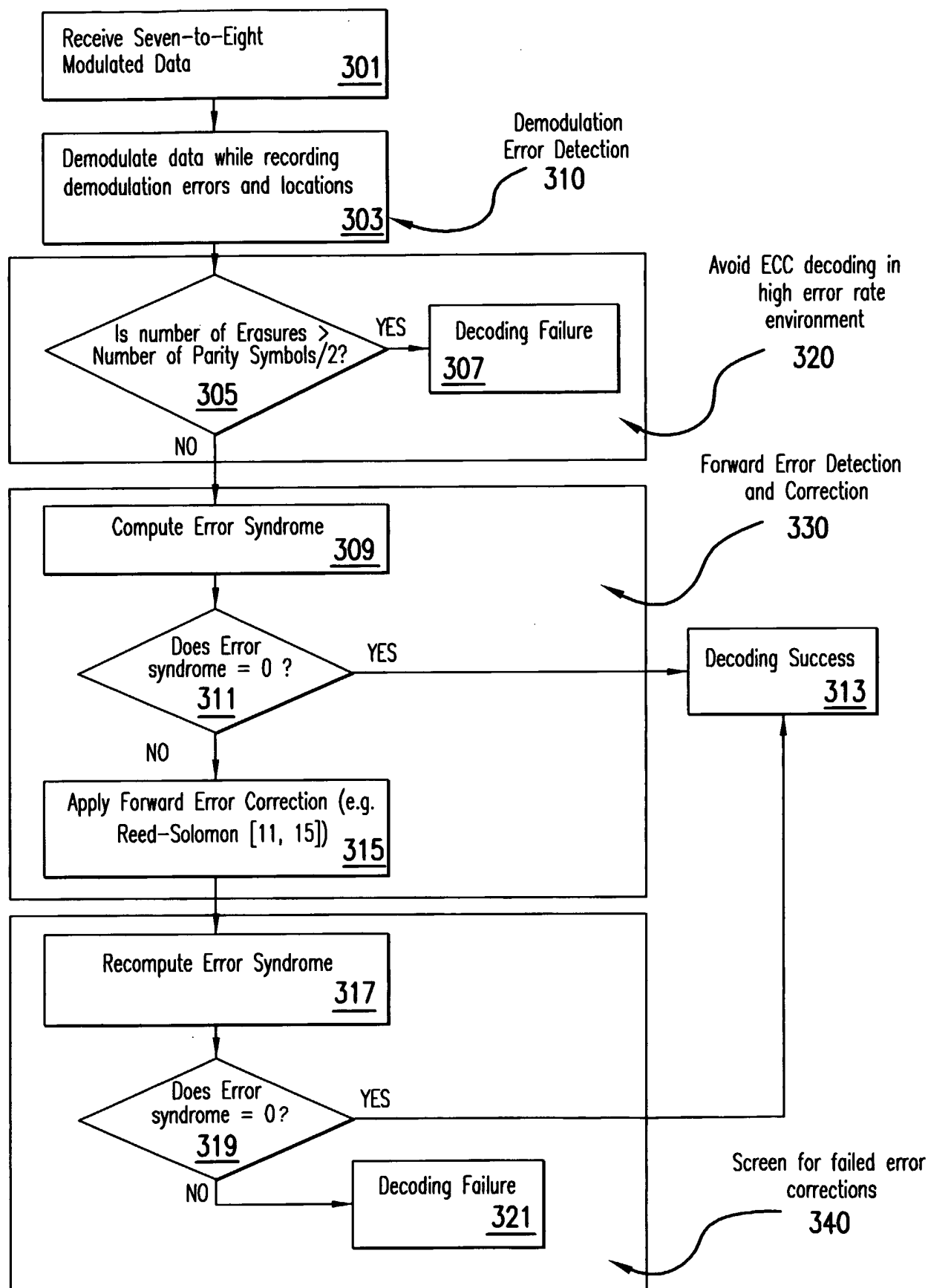


FIG.3

INTERNATIONAL SEARCH REPORT

national application No
PCT/US2005/038610

A. CLASSIFICATION OF SUBJECT MATTER

G11B20/18 H03M13/13 H03M5/14

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G11B H03M H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 592 229 A (SAMSUNG ELECTRONICS CO., LTD; SAMSUNG ELECTRONICS CO LTD) 13 April 1994 (1994-04-13)	1-3,8-10
Y	page 4, line 15 - page 7, line 2	4,7
X	US 2001/023495 A1 (CHANG WEN-JENG ET AL) 20 September 2001 (2001-09-20) paragraphs [0022] - [0043]	1,9
X	US 2002/010888 A1 (KWON HYUNG-JOON) 24 January 2002 (2002-01-24) paragraphs [0004] - [0010] paragraphs [0046], [0051], [0058]	1,9
X	US 6 029 266 A (LEE ET AL) 22 February 2000 (2000-02-22) column 2, line 55 - column 3, line 26 column 6, line 16 - column 7, line 12	1,9
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☒ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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Date of the actual completion of the international search

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INTERNATIONAL SEARCH REPORT

International application No
PCT/US2005/038610

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 772 384 B1 (NOGUCHI NOBUAKI) 3 August 2004 (2004-08-03) column 1, lines 24-62 column 5, lines 6-52 -----	1,9
X	CHIEN-CHAN LIANG: "IMPROVEMENT OF PERFORMANCE IN DIGITAL RECORDING WITH DISTANCED MODULATION CODE" IEEE TRANS. CONSUMER ELECTRONICS, vol. 39, no. 4, 1 November 1993 (1993-11-01), pages 740-744, XP000423059 the whole document -----	1,9
Y	GB 1 540 617 A (POST OFFICE) 14 February 1979 (1979-02-14)	4
A	page 2, line 80 - page 11, line 29 -----	5,6
Y	MCGREGOR M S, WATSON J C: "Implementing the Reed-Solomon Code: A Case Study" IEE COLLOQUIUM ON SIGNAL PROCESSING APPLICATIONS OF FINITE FIELD MATHEMATICS, 1 June 1989 (1989-06-01), pages 7/1-7/7, XP006525428 the whole document -----	7

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2005/038610

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
EP 0592229	A	13-04-1994	DE 69332556 D1	23-01-2003
			DE 69332556 T2	20-11-2003
			JP 6208767 A	26-07-1994
			KR 9502304 B1	16-03-1995
			US 5450421 A	12-09-1995
US 2001023495	A1	20-09-2001	TW 509900 B	11-11-2002
			US 2006015794 A1	19-01-2006
US 2002010888	A1	24-01-2002	CN 1328326 A	26-12-2001
			JP 2002008326 A	11-01-2002
			NL 1017381 C2	12-12-2001
			TW 501098 B	01-09-2002
US 6029266	A	22-02-2000	CN 1173668 A	18-02-1998
			DE 19733738 A1	10-06-1998
			GB 2316584 A	25-02-1998
			JP 10093446 A	10-04-1998
			KR 229015 B1	01-11-1999
US 6772384	B1	03-08-2004	CN 1264962 A	30-08-2000
			JP 3502559 B2	02-03-2004
			JP 2000228634 A	15-08-2000
GB 1540617	A	14-02-1979	NONE	