

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
9 March 2006 (09.03.2006)

PCT

(10) International Publication Number
WO 2006/025025 A1

(51) International Patent Classification:
H03K 19/0185 (2006.01)

(21) International Application Number:
PCT/IB2005/052843

(22) International Filing Date: 31 August 2005 (31.08.2005)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2004-257675 3 September 2004 (03.09.2004) JP

(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL];
Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(72) Inventor; and

(75) Inventor/Applicant (for US only): **HASHIMOTO, Kazuyuki** [JP/JP]; c/o Philips Electronics Japan, Ltd., Philips Bldg., 2-13-37, Kohnan, Minato-ku, Tokyo 108-8507 (JP).

(74) Agents: **TSUGARU, Susumu** et al.; c/o Philips Electronics Japan, Ltd., Philips Bldg., 2-13-37, Kohnan, Minato-ku, Tokyo 108-8507 (JP).

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

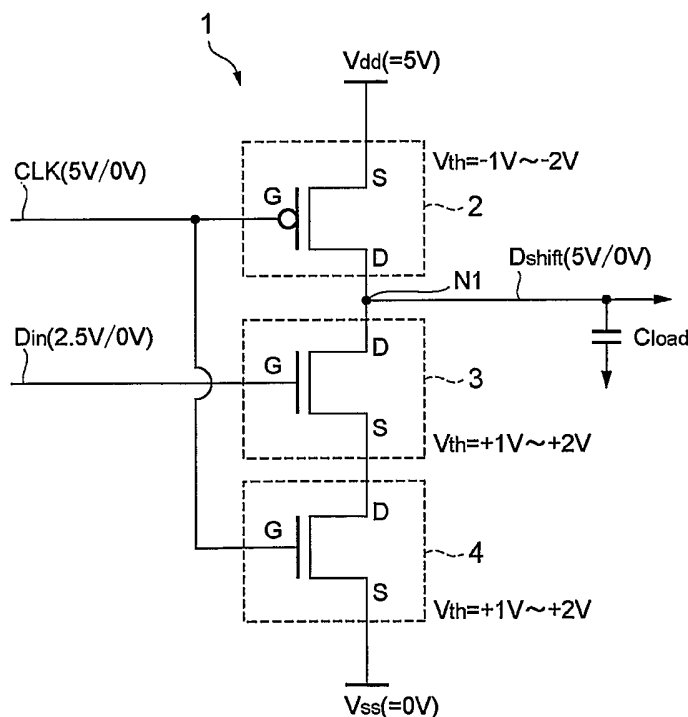
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- with international search report
- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: LEVEL SHIFTER AND VOLTAGE CONVERTING DEVICE



(57) Abstract: A level shifter voltage contributing to a simplified interface and realizing a reduced power consumption and a voltage supplying device using such a level shifter are provided. A level shifter (1) receives an input data (Din) having a voltage of 0V (zero) and a clock signal (CLK) to shift said voltage of 0V to 5V. The level shifter (1) comprises a first means for supplying a voltage of Vdd(=5V) to a node (N1) and a second means for supplying a voltage of Vss(=0V) to the node (N1). The second means operates so as to block a supply of the voltage of Vss to the node (N1) when the first means supplies the voltage of Vdd to the node (N1).

Description

LEVEL SHIFTER AND VOLTAGE CONVERTING DEVICE

Technical Field

- [1] The invention relates to a level shifter for shifting a first voltage to a second voltage, and a voltage converting device using the level shifter.

Background Art

- [2] A display device such as a mobile phone comprises, for example, an IC chip for outputting image data and transistors (e.g. TFT), each of the transistors being formed on glass substrate at respective one of pixels. Each pixel is supplied through respective one of the transistors with a voltage on the basis of the image data outputted from the IC chip. The power supply voltage required for the IC chip is usually different from the power supply voltage required on the glass substrate, so that a level shifter is provided in the IC chip or on the glass substrate.
- [3] Fig. 1 is one example of a voltage converting device 100 using the known level shifter.
- [4] The voltage converting device 100 comprises a level shifter 101 and a latch 102. The level shifter 101 shifts a voltage level of an input data D_{in} . In order to shift the voltage level of the input data D_{in} , the level shifter requires not only the input data D_{in} but also an inverted input data D_{in_inv} having voltage levels inverted with respect to the voltage levels of the input data D_{in} . Therefore, for example, if the input data D_{in} and the inverted input data D_{in_inv} are supplied from an IC chip to the level shifter 101, the IC chip requires not only an output terminal for the input data D_{in} but also an output terminal for the inverted input data D_{in_inv} . If a display device requires only one level shifter 101, the IC chip requires one pair of the output terminals for the input data D_{in} and the inverted input data D_{in_inv} . However, if the display device processes e.g. multiple bits of data in parallel, a plurality of level shifters 101 are required, so that the IC chip requires a plurality of pairs of an output terminal of the input data D_{in} and an output terminal of the inverted input data D_{in_inv} . Therefore, an interface for connecting the IC chip to the level shifters is complicated.
- [5] In addition to the level shifter shown in Fig. 1, level shifters described in e.g. US2002/0118040A1 and US6650167B1 are known.
- [6] Unlike the level shifter 101 shown in Fig. 1, the level shifter described in US2002/0118040A1 and US6650167B1 can shift an input voltage level without the inverted input data and thus have an advantage that no inverted input data line is required. However, in the case of these level shifters, a DC current flows from a supply portion of a voltage V_{dd} to a supply portion of a voltage V_{ss} while these level shifters shift the voltage level, so that a problem of increased power consumption arises.

Disclosure of Invention

Technical Problem

- [7] It is an object of the invention to provide a level shifter contributing to a simplified interface and realizing reduced power consumption, and provide a voltage supplying device using such level shifter.

Technical Solution

- [8] A level shifter according to the present invention for achieving the object described above receives a first clock signal and data having a first voltage to shift said first voltage to a second voltage, said level shifter comprises a first voltage supplying means for supplying said second voltage to a predetermined position and a second voltage supplying means for supplying a third voltage to said predetermined position, and said second voltage supplying means operates so as to block supply of said third voltage to said predetermined position when said first voltage supplying means supplies said second voltage to said predetermined position.
- [9] In the level shifter according to the present invention, said second voltage supplying means operates so as to block supply of said third voltage to said predetermined position when said first voltage supplying means supplies said second voltage to said predetermined position. Therefore, it can be prevented that current flows between the first and second voltage supplying means when the first voltage supplying means supplies the second voltage to the predetermined position, so that the lower power consumption can be achieved.
- [10] The level shifter according to the present invention shifts the first voltage to the second voltage using the first clock signal. If a plurality of level shifters each of which is the level shifter according to the invention are required, the first clock signal can be commonly used for the plurality of level shifters. Therefore, complication of an interface can be reduced, as compared with the prior art in which a plurality of inverted data for a plurality of prior art level shifters are required.
- [11] The level shifter according to the invention may be structured in such a way that, during a first period, said first voltage supplying means supplies said second voltage to said predetermined position and said second voltage supplying means blocks supply of said third voltage to said predetermined position, and that, during a second period succeeding to said first period, said first voltage supplying means blocks supply of said second voltage to said predetermined position and said second voltage supplying means continues to block supply of said third voltage to said predetermined position. In this case, such voltage supply and such block of voltage supply may be carried out by a response of the first voltage supplying means to the first clock signal and a response of the second voltage supplying means to the first clock signal and the data.

- [12] With such structure, the second voltage supplied to the predetermined position during the first period can be held during the second period. This makes it possible that a level of the first voltage of data is shifted to the second voltage during the second period.
- [13] The level shifter according to the invention may be structured in such a way that, during a first period, said first voltage supplying means blocks supply of said second voltage to said predetermined position and said second voltage supplying means supplies said third voltage to said predetermined position, and that during a second period succeeding to said first period, said first voltage supplying means supplies said second voltage to said predetermined position and said second voltage supplying means blocks supply of said third voltage to said predetermined position. In this case, such voltage supply and such block of voltage supply may be carried out by a response of the first voltage supplying means to the first clock signal and a response of the second voltage supplying means to the first clock signal and the data.
- [14] With such structure, after the third voltage is supplied to the predetermined position during the first period, the second voltage instead of the third voltage is supplied to the predetermined position during the second period. This makes it possible that a level of the first voltage of data is shifted to the second voltage during the second period.
- [15] The level shifter according to the invention may be structured in such a way that said first voltage supplying means comprises a first switch means, said first switch means becoming on-state and off-state in response to said first clock signal, that said second voltage supplying means comprises a second switch means, said second switch means becoming on-state and off-state in response to said first clock signal, and that said second switch means is off-state when said first switch means is on-state and said second switch means is on-state when said first switch means is off-state.
- [16] If said second switch means is off-state when said first switch means is on-state and said second switch means is on-state when said first switch means is off-state, it is prevented that current flows between the first and the second voltage supplying means, so that low power consumption is achieved.
- [17] The level shifter according to the invention may be structured in such a way that said level shifter comprises a third switch means between said predetermined position and said second switch means, and that said third switch means becoming on-state and off-state in response to said data.
- [18] By providing such third switch means, the voltage on the predetermined position during the second period can be made the second voltage, so that a level of the first voltage of the data can be shifted to the second voltage during the second period.
- [19] The level shifter according to the invention may be structured in such a way that

said first voltage supplying means comprises a fourth switch means, said fourth switch means becoming on-state and off-state in response to said first clock signal, that said second voltage supplying means comprises a data processing means for processing said data and a fifth switch means, said fifth switch means becoming on-state and off-state in response to said processed data, and that said fifth switch means is in off-state when said fourth switch means is in on-state and said fifth switch means is in on-state when said fourth switch means is in off-state. In this case, the level shifter according to the invention may be structured in such a way that the data has a data valid period and a data invalid period and that said data processing means changes a voltage of said data of said data in valid period to a voltage used for making said fifth switch means on-state or off-state.

- [20] The data processing means may be structured so as to change a voltage of said data of said data in valid period to a voltage used for making said fifth switch means on-state or off-state by using second clock signal which has voltage levels in versed with respect to voltage levels of said first clock signal. If a plurality of level shifters each of which is the level shifter according to the present invention are required, the second clock signal can be commonly used for the plurality of level shifters. Therefore, complication of an interface can be reduced, as compared with the prior art in which a plurality of inverted data for a plurality of prior art level shifters are required.

Description of Drawings

- [21] Fig. 1 is one example of the voltage converting device 10 in which the known level shifter is used.
- [22] Fig. 2 shows a level shifter 1 of first embodiment according to the present invention.
- [23] Fig. 3 is a timing chart of the level shifter 1 shown in Fig. 2.
- [24] Fig. 4 shows a level shifter 11 of the second embodiment according to the present invention.
- [25] Fig. 5 is a timing chart of the level shifter 11 shown in Fig. 4.
- [26] Fig. 6 shows a level shifter 10 of the third embodiment according to the present invention.
- [27] Fig. 7 is a timing chart of the level shifter 10 shown in Fig. 6.
- [28] Fig. 8 is a schematic diagram showing a voltage converting device 50 in which the level shifter 1 shown in Fig. 2 is used.
- [29] Fig. 9 shows a timing chart of the voltage converting device 50.
- [30] Fig. 10 is schematic diagram showing a voltage converting device 60 of a different example from the voltage converting device 50 shown in Fig. 8.
- [31] Fig. 11 is a timing chart of the voltage converting device 60.
- [32] Fig. 12 shows an example in which the voltage converting device 50 shown in Fig.

8 is applied to a mobile phone 200.

[33] Fig. 13 shows an example in which a mobile phone 201 comprises a plurality of voltage converting devices 50 and each of the voltage converting devices 50 is the voltage converting device 50 shown in Fig. 8.

[34] Fig. 14 shows an example in which the level shifter 10 shown in Fig. 6 is applied to a mobile phone 300.

[35] Fig. 15 shows an example in which a mobile phone 301 comprises a plurality of voltage converting devices and each of the voltage converting devices is the voltage converting device 82 shown in Fig. 14.

Best Mode

[36] Fig. 2 shows a level shifter 1 of first embodiment according to the present invention.

[37] The level shifter 1 receives a digital signal of 1 bit as an input data D_{in} , and the digital signal is represented by voltage levels of e.g. 0V and 2.5V. The level shifter 1 shifts the voltage level 0V of the input data D_{in} to 5V and shifts the voltage level 2.5V of the input data D_{in} to 0V, and outputs the shifted input data D_{in} as a level shift data D_{shift} . In order to shift the voltage level as described above, the level shifter 1 comprises one p-type transistor 2 and two n-type transistors 3 and 4. The p-type transistor 2 has a threshold voltage V_{th} of -1V to -2V and the n-type transistors 3 and 4 have threshold voltages V_{th} of +1V to +2V. The transistors 2, 3, and 4 are connected in series. A source S of the transistor 2 is connected to a power supply V_{dd} and a source S of the transistor 4 is connected to a power supply V_{ss} . The power supplies V_{dd} and V_{ss} supply 5V and 0V, respectively, but may supply different voltages as needed. A node N1 between the transistors 2 and 3 is connected to load capacitance C_{load} . The load capacitance C_{load} hypothetically represents input capacitance of a circuit (not shown) receiving the level shift data D_{shift} . It is noted that, in the level shifter 1 structured as described above, ON/OFF of the transistor 3 is controlled using the input data D_{in} , but ON/OFF of the further transistors 2 and 4 is controlled using a clock signal CLK instead of the input data D_{in} .

[38] The level shifter 1 mainly has two features.

[39] A first feature is that the clock signal CLK is used in order to carry out a level shift. A second feature is that the transistor 2 is the p-type but the transistor 4 is the n-type, and the transistors 2 and 4 are controlled by the clock signal CLK, so that if one of the transistors 2 and 4 is on-state, the other is off-state.

[40] In the following, operation of the level shifter 1 will be described, and next, advantages obtained by providing the level shifter 1 with the features described above will be described.

[41] Fig. 3 is a timing chart of the level shifter 1 shown in Fig. 2.

[42] The input data D_{in} received by the level shifter 1 comprises data valid periods $Pv1$, $Pv2$, $Pv3$,... and data invalid periods $Pi1$, $Pi2$, $Pi3$,.... The data valid period and the data invalid period alternate. The data valid period is a period during which a voltage to be shifted is present, so that the voltage of the data valid period is an object to be shifted. On the other hand, the data invalid period is a period during which a voltage level of a data valid period is changed to a voltage level of the next data valid period, and the voltage of the data invalid period is not an object to be shifted. The clock signal CLK received by the level shifter 1 has a high level voltage (5V) during the data valid periods $Pv1$, $Pv2$, $Pv3$,... and has a low level voltage (0V) during the data invalid periods $Pi1$, $Pi2$, $Pi3$,.... In Fig. 3, the clock signal CLK has a duty ratio of 50:50, so that a ratio of a length of the data valid period to a length of the data invalid period is defined as 50:50 accordingly, but these ratios are not limited to 50:50. If the clock signal CLK has not the duty ratio of 50:50 but has the duty ratio of e.g. 60:40, the ratio of the length of the data valid period to the length of the data invalid period is defined as 60:40.

[43] Basic operation of the level shifter 1 is as follows. That is, the level shifter 1 operates during the data invalid period so as to pre-charge the node $N1$ to the voltage V_{dd} (= 5V), and then operates during the next data valid period so as to hold the voltage V_{dd} on the pre-charged node $N1$ or so as to discharge the node $N1$ from the voltage V_{dd} (= 5V) to the V_{ss} (= 0V) on the basis of the voltage level of the input data D_{in} . For example, as shown in Fig. 3, the level shifter 1 pre-charges the node $N1$ to the voltage V_{dd} (= 5V) during the data invalid period $Pi1$ and then discharges the node $N1$ from the voltage V_{dd} (= 5V) to the V_{ss} (= 0V) during the next data valid period $Pv1$. And, the level shifter 1 pre-charges the node $N1$ to the voltage V_{dd} (= 5V) during the data invalid period $Pi2$ and then holds the voltage V_{dd} (= 5V) on the node $N1$ during the next data valid period $Pv2$. In such a manner, the level shifter 1 shifts the voltage 0V of the input data D_{in} to 5V and shifts the voltage 5V of the input data D_{in} to 0V and then outputs the level shift data D_{shift} .

[44] Operation when the level shifter 1 outputs the level shift data D_{shift} will be in detail described below with respect to Figs. 2 and 3.

[45] During a period from an instant $t1$ to an instant $t2$, the clock signal CLK has the low level voltage (= 0V), so that the voltage of 0V is applied to the gates G of the p-type and n-type transistors 2 and 4. Therefore, with regard to p-type transistor 2, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[46]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate } G) - V_S (= \text{a voltage on the source } S) \\ &= 0V - V_{dd} \\ &= -5V \end{aligned}$$

[47] In this case, since the voltage V_{GS} (= -5V) is smaller than the threshold voltage V_{th} (= -1V to -2V) of the p-type transistor 2, the p-type transistor 2 becomes on-state.

[48] On the other hand, with regard to the n-type transistor 4, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[49]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 0V - V_{SS} \\ &= 0V \end{aligned}$$

[50] In this case, since the voltage V_{GS} (= 0V) is smaller than the threshold voltage V_{th} (+1V to +2V) of the n-type transistor 4, the n-type transistor 4 becomes off-state.

[51] Therefore, the transistors 2 and 4 are in the on-state and the off-state, respectively, during the period from the instant t1 to the instant t2 (data invalid period Pi1). The node N1 is connected to the power supply Vdd (= 5V) since the transistor 2 is ON, but is not connected to the power supply Vss (= 0V) irrespective of whether the transistor 3 is ON or OFF since the transistor 4 is OFF. Therefore, the node N1 is pre-charged to the voltage Vdd (= 5V) during the period from the instant t1 to the instant t2 (the data invalid period Pi1), so that the voltage of the level shift data Dshift is set to 5V.

[52] The node N1 is pre-charged to 5V during the data invalid period Pi1 in this way, and then a transition is made to a data valid period Pv1 (the instant t2 to the instant t3).

[53] Since the clock signal CLK has the high level voltage (= 5V) during the period from the instant t2 to the instant t3, the voltage of 5V is applied to the gates G of the p-type and n-type transistors 2 and 4. Therefore, with regard to p-type transistor 2, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[54]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 5V - V_{dd} \\ &= 0V \end{aligned}$$

[55] In this case, since the voltage V_{GS} (= 0V) is larger than the threshold voltage V_{th} (= -1V to -2V) of the p-type transistor 2, the p-type transistor 2 becomes off-state.

[56] On the other hand, with regard to n-type transistor 4, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[57]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 5V - V_{ss} \\ &= 5V \end{aligned}$$

[58] In this case, since the voltage V_{GS} (= 5V) is larger than the threshold voltage V_{th} (= +1V to +2V) of the n-type transistor 4, the n-type transistor 4 becomes on-state.

[59] Since the input data Din is 2.5V during the period from the instant t2 to the instant t3 (the data valid period Pv1), the voltage of 2.5V is applied to the gate G of the n-type transistor 3. The voltage Vs on the source S of the n-type transistor 3 is 0V since the n-type transistor 4 is in the on-state. Therefore, with regard to n-type transistor 3, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[60]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 2.5V - V_{SS} \\ &= 2.5V \end{aligned}$$

[61] In this case, since the voltage V_{GS} (= 2.5V) is larger than the threshold voltage Vth (= +1V to +2V) of the n-type transistor 3, the n-type transistor 3 becomes on-state.

[62] Therefore, during the period from the instant t2 to the instant t3, the node N1 is not connected to the power supply Vdd (= 5V) since the transistor 2 is in the off-state, but is connected to the power supply Vss (= 0V) since the transistors 3 and 4 are in the on-states. As a result of this, the node N1 is discharged from 5V to 0V at the instant t2, so that the voltage of the level shift data Dshift becomes 0V (the instant t2 to the instant t3).

[63] In this way, the voltage level of the input data Din during the data valid period Pv1 (the instant t2 to the instant t3) is shifted from 2.5V to 0V.

[64] Next, during a period from the instant t3 to the instant t4 (the data invalid period Pi2), the clock signal CLK has the low level voltage (= 0V), so that the voltage of 0V is applied to the gates G of the p-type and n-type transistors 2 and 4. Therefore, with regard to p-type transistor 2, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[65]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0V - V_{DD} \\ &= -5V \end{aligned}$$

[66] In this case, since the voltage V_{GS} (= -5V) is smaller than the threshold voltage Vth (= -1V to -2V) of the p-type transistor 2, the p-type transistor 2 becomes on-state.

[67] On the other hand, with regard to n-type transistor 4, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[68]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0V - V_{SS} \\ &= 0V \end{aligned}$$

[69] In this case, since the voltage V_{GS} (= 0V) is smaller than the threshold voltage Vth

(= +1V to +2V) of the n-type transistor 4, the n-type transistor 4 becomes off-state.

[70] Therefore, the transistors 2 and 4 are in on-state and off-state, respectively, during the period from the instant t3 to the instant t4. The node N1 is connected to the power supply Vdd (= 5V) since the transistor 2 is ON, but is not connected to the power supply Vss (= 0V) irrespective of whether the transistor 3 is ON or OFF since the transistor 4 is OFF. Therefore, the node N1 is pre-charged to the voltage Vdd (= 5V) during the period from the instant t3 to the instant t4 (the data invalid period Pi2), so that the voltage of the level shift data Dshift is set to 5V.

[71] The node N1 is pre-charged to 5V during the data invalid period Pi2 in this way, and then a transition is made to a data valid period Pv2 (the instant t4 to the instant t5).

[72] During the period from the instant t4 to the instant t5, the clock signal CLK has the high level voltage (= 5V), so that the transistors 2 and 4 are in the off-state and on-state, respectively. Since the input data Din is 0V, the voltage of 0V is applied to the gate G of the n-type transistor 3. The voltage on the source S of the n-type transistor 3 is 0V since the n-type transistor 4 is in the on-state. Therefore, with regard to n-type transistor 3, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[73]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 0V - V_{SS} \\ &= 0V \end{aligned}$$

[74] In this case, since the voltage V_{GS} (= 0V) is smaller than the threshold voltage Vth (+1V to +2V) of the n-type transistor 3, the n-type transistor 3 becomes off-state. Therefore, the node N1 is not connected to the power supply Vss. During the data valid period Pv2 (the instant t4 to the instant t5), the node N1 also is not connected to the power supply Vdd (= 5V) since the transistor 2 is in the off-state. As a result of this, the node N1 continuously holds 5V of the data invalid period Pi2 (the instant t3 to the instant t4) during the data valid period Pv2 (the instant t4 to the instant t5), so that the voltage of the level shift data Dshift remains 5V.

[75] Therefore, the voltage 0V of the input data Din during the data valid period Pv2 (the instant t4 to the instant t5) is shifted to 5V.

[76] As described above, the node N1 is not connected to the power supplies Vdd and Vss during the instant t4 to the instant t5. Therefore, the voltage on the node N1 may change because of occurrence of a leak current and a change of the load capacitance Cload, so that the voltage of 5V may not be substantially held. Within a region A in Fig. 3, a situation in which the voltage on the node N1 changes and thus the voltage at the instant t5 deviates from the voltage at the instant t4 by Vva is illustrated with a

broken line. If such amount of change in voltage V_{va} can be negligible, no problem occurs. If such amount of change in voltage V_{va} can not negligible, strategies (1) or (2) described below can take depending on whether the cause of the amount of change in voltage V_{va} lies mainly in the occurrence of the leak current or the change of the load capacitor C_{load} .

[77] (1) A case in which the cause of the amount of change in voltage V_{va} lies mainly in the occurrence of the leak current.

[78] In this case, a manner in which frequencies of the clock signal CLK and the input data D_{in} are increased can be considered for example. This shortens the data valid periods and thus makes it possible that the amount of change in voltage V_{va} becomes smaller. In another manner, the leak current can become smaller by making size of the transistor 2, 3 or 4 smaller since the smaller size of the transistor 2, 3 or 4 makes resistance of the transistor 2, 3 or 4 higher. Therefore, to make the size of the transistor smaller is one strategy if the frequency of the clock signal can not be increased.

[79] (2) A case in which the cause of the amount of change in voltage V_{va} lies mainly in the change of the load capacitor C_{load} .

[80] In this case, a manner in which an inverter is provided between the node N1 and the load capacitor C_{load} can be considered for example. By this manner, the level shifter 1 can output the level shift data D_{shift} with the level shifter 1 not being substantially affected by the change of the load capacitor C_{load} .

[81] If the cause of the amount of change in voltage V_{va} lies both in the occurrence of the leak current and in the change of the load capacitor C_{load} , both strategies (1) and (2) described above can be used in combination.

[82] Next, during the period from the instant t_5 to the instant t_6 (data invalid period Pi_3), the clock signal CLK has the low level voltage ($= 0V$), so that the transistors 2 and 4 are in the on-state and off-state, respectively. The node N1 is connected to the power supply V_{dd} ($= 5V$) since the transistor 2 is ON, but is not connected to the power supply V_{ss} ($= 0V$) irrespective of whether the transistor 3 is ON or OFF since the transistor 4 is OFF. Therefore, the node N1 is pre-charged to the voltage V_{dd} ($= 5V$) during the period from the instant t_5 to the instant t_6 (the data invalid period Pi_3), so that the voltage of the level shift data D_{shift} is set to $5V$.

[83] Next, a transition is made to a data valid period Pv_3 (the instant t_6 to the instant t_7).

[84] During the period from the instant t_6 to the instant t_7 , the clock signal CLK has the high level voltage ($= 5V$), so that the transistors 2 and 4 are in the off-state and on-state, respectively. During the period from the instant t_6 to the instant t_7 , the input data D_{in} is $2.5V$, so that the voltage of $2.5V$ is applied to the gate G of the n-type transistor 3. The voltage on the source S of the n-type transistor 3 is $0V$ since the n-type

transistor 4 is in the on-state. Therefore, the voltage V_{GS} of the n-type transistor 3 is 2.5V and is larger than the threshold voltage V_{th} ($= +2V$). As a result of this, the n-type transistor 3 becomes on-state.

[85] Therefore, during the period from the instant t_6 to the instant t_7 , the transistor 2 is in the off-state, but the transistors 3 and 4 are in the on-state, so that the node N1 is connected to the power supply V_{ss} ($= 0V$). As a result of this, the node N1 is discharged from 5V to 0V at the instant t_6 , so that the voltage of the level shift data Dshift becomes 0V (the instant t_6 to the instant t_7). In this way, the voltage 2.5V of the input data Din during the data valid period Pv3 (the instant t_6 to the instant t_7) is shifted to 0V.

[86] As described above, the level shifter 1 shown in Fig. 2 shifts the voltage 0V of the input data Din to 5V and shifts the voltage 2.5V of the input data Din to 0V and outputs the level-shifted input data Din as the level shift data Dshift.

[87] The level shifter 1 shown in Fig. 2 can output the level shift data Dshift without an inverted input data Din_inv used for shifting a level of the input data Din. In the level shifter 1, the p-type transistor 2 at the side of the voltage Vdd and the n-type transistor 4 at the side of the voltage Vss with respect to the node N1 are controlled by the clock signal CLK, so that if one of these transistors is in the on-state, the other is in the off-state (see Fig. 3). Therefore, during the operation of the level shifter 1, the power supply Vdd and the power supply Vss are prevented from becoming shorted to each other. As a result of this, it is prevented that DC current flows from the power supply Vdd to Vss, so that lower power consumption is achieved.

[88] The clock signal CLK has the voltage levels of 0V and 5V and the input data Din has the voltage levels of 0V and 2.5V in the first embodiment, but it is noted that the voltage levels of the clock signal CLK and the input data Din are not limited to the values described above as long as the level shifter 1 shown in Fig. 2 carries out the level shift operation. The power supply Vdd and the power supply Vss supply the voltages 5V and 0V in the first embodiment, respectively, but it is noted that the power supply Vdd and the power supply Vss are not limited to 5V and 0V, respectively, as long as the level shifter 1 shown in Fig. 2 carries out the level shift operation.

[89] Fig. 4 shows a level shifter 11 of second embodiment according to the present invention.

[90] The level shifter 11 receives a digital signal of 1 bit as an input data Din, and the digital signal is represented by voltage levels of e.g. 0V and 1.5V. The level shifter 11 shifts the voltage level 0V of the input data Din to 2.5V and shifts the voltage level 1.5V of the input data Din to 0V and outputs the shifted input data Din as a level shift data Dshift. In order to shift the voltage level as described above, the level shifter 11 comprises two p-type transistors 12 and 13 and one n-type transistor 14. Each of the

transistors 12 and 13 has a threshold voltage V_{th} of substantially $-1.5V$ and the transistor 14 has a threshold voltage V_{th} of substantially $+1.5V$. The transistors 12, 13, and 14 are connected in series. The source S of the transistor 12 is connected to the power supply V_{dd} ($= 2.5$) and the source S of the transistor 14 is connected to the power supply V_{ss} ($= 0V$). A node N2 between the transistors 13 and 14 is connected to load capacitance C_{load} .

[91] It is noted that, in the level shifter 11 structured as described above, on-off control of the transistor 13 is carried out using the input data D_{in} , but on-off control of the other transistors 12 and 14 is carried out not using the input data D_{in} but using the clock signal CLK.

[92] Operation of the level shifter 11 is described below.

[93] Fig. 5 is a timing chart of the level shifter 11 shown in Fig. 4 .

[94] The input data D_{in} received by the level shifter 11 comprises data valid periods $Pv1, Pv2, Pv3, \dots$ and data invalid periods $Pi1, Pi2, Pi3, \dots$. The data valid period and the data invalid period alternate. The data valid period is a period during which a voltage to be shifted is present, so that the voltage of the data valid period is an object to be shifted. On the other hand, the data invalid period is a period during which a voltage level of a data valid period is changed to a voltage level of the next data valid period, and the voltage of the data invalid period is not an object to be shifted. The clock signal CLK received by the level shifter 11 has a low level voltage ($0V$) during data valid periods $Pv1, Pv2, Pv3, \dots$ and has a high level voltage ($2.5V$) during data invalid periods $Pi1, Pi2, Pi3, \dots$

[95] Basic operation of the level shifter 11 is as follows. That is, the level shifter 11 operates during the data invalid period so as to discharge the node N2 to the voltage V_{ss} ($= 0V$), and then operates during the next data valid period so as to hold the voltage V_{ss} on the discharged node N2 or so as to charge the node N2 from the voltage V_{ss} ($= 0V$) to the V_{dd} ($= 5V$) on the basis of the voltage level of the input data D_{in} . For example, as shown in Fig. 5, the level shifter 11 discharges the node N2 to the voltage V_{ss} ($= 0V$) during the data invalid period $Pi1$ and then charges the node N2 from the voltage V_{ss} ($= 0V$) to the V_{dd} ($= 2.5V$) during the data valid period $Pv1$. And, the level shifter 11 discharges the node N2 to the voltage V_{ss} ($= 0V$) during the data invalid period $Pi2$ and then holds the voltage V_{ss} on the node N2 during the next data valid period $Pv2$. In such a manner, the level shifter 11 shifts the voltage $0V$ of the input data D_{in} to $2.5V$ and shifts the voltage $1.5V$ of the input data D_{in} to $0V$ and then outputs the level shift data D_{shift} .

[96] Operation when the level shifter 11 outputs the level shift data D_{shift} will be in detail described below with respect to Figs. 4 and 5.

[97] During a period from an instant $t1$ to an instant $t2$, the clock signal CLK has the

high level voltage (= 2.5V), so that the voltage of 2.5V is applied to the gates G of the p-type and n-type transistors 12 and 14. Therefore, with regard to p-type transistor 12, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[98]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 2.5V - V_{dd} \\ &= 0V \end{aligned}$$

[99] In this case, since the voltage V_{GS} (= 0V) is larger than the threshold voltage V_{th} ($\approx -1.5V$) of the p-type transistor 12, the p-type transistor 12 becomes off-state.

[100] On the other hand, with regard to n-type transistor 14, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[101]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 2.5V - V_{ss} \\ &= 2.5V \end{aligned}$$

[102] In this case, since the voltage V_{GS} (= 2.5V) is larger than the threshold voltage V_{th} ($\approx +1.5V$) of the n-type transistor 14, the n-type transistor 14 becomes on-state.

[103] Therefore, the transistors 12 and 14 are in off-state and on-state, respectively, during the period from the instant t1 to the instant t2 (data invalid period Pi1). The node N2 is connected to the power supply V_{ss} (= 0V) since the transistor 12 is ON, but is not connected to the power supply V_{dd} (= 2.5V) irrespective of whether the transistor 13 is ON or OFF since the transistor 12 is OFF. Therefore, the node N2 is discharged to the voltage V_{ss} (= 0V) during the period from the instant t1 to the instant t2 (the data invalid period Pi1), so that the voltage of the level shift data Dshift is set to 0V.

[104] The node N1 is discharged to 0V during the data invalid period Pi1 in this way, and then a transition is made to a data valid period Pv1 (the instant t2 to the instant t3).

[105] Since the clock signal CLK has the low level voltage (= 0V) during the period from the instant t2 to the instant t3, the voltage of 0V is applied to the gates G of the p-type and the n-type transistors 12 and 14. Therefore, with regard to p-type transistor 12, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[106]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 0V - V_{dd} \\ &= -2.5V \end{aligned}$$

[107] In this case, since the voltage V_{GS} (= -2.5V) is smaller than the threshold voltage V_{th} ($\approx -1.5V$) of the p-type transistor 12, the p-type transistor 12 becomes on-state.

[108] On the other hand, with regard to n-type transistor 14, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[109]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 0V - V_{SS} \\ &= 0V \end{aligned}$$

[110] In this case, since the voltage V_{GS} ($= 0V$) is smaller than the threshold voltage V_{th} ($\approx +1.5V$) of the n-type transistor 14, the n-type transistor 14 becomes off-state.

[111] Since the input data D_{in} is $0V$ during the period from the instant t_2 to the instant t_3 (the data valid period $Pv1$), the voltage of $0V$ is applied to the gate G of the p-type transistor 13. The voltage V_S on the source S of the p-type transistor 13 is V_{dd} ($= 2.5V$) since the n-type transistor 12 is in the on-state. Therefore, with regard to p-type transistor 13, a voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[112]

$$\begin{aligned} V_{GS} &= V_G (= \text{a voltage on the gate G}) - V_S (= \text{a voltage on the source S}) \\ &= 0V - V_{dd} \\ &= -2.5V \end{aligned}$$

[113] In this case, since the voltage V_{GS} ($= -2.5V$) is smaller than the threshold voltage V_{th} ($\approx -1.5V$) of the p-type transistor 13, the p-type transistor 13 becomes on-state.

[114] Therefore, during the period from the instant t_2 to the instant t_3 , the node N2 is not connected to the power supply V_{SS} ($= 0V$) since the transistor 14 is in the off-state, but is connected to the power supply V_{dd} ($= 2.5V$) since the transistors 12 and 13 are in the on-states. As a result of this, the node N2 is charged from $0V$ to $2.5V$ at the instant t_2 , so that the voltage of the level shift data D_{shift} becomes $2.5V$ (the instant t_2 to the instant t_3).

[115] In this way, the voltage level of the input data D_{in} during the data valid period $Pv1$ (the instant t_2 to the instant t_3) is shifted from $0V$ to $2.5V$.

[116] Next, during a period from the instant t_3 to the instant t_4 (the data invalid period $Pi2$), the clock signal CLK has the high level voltage ($= 2.5V$), so that the voltage of $2.5V$ is applied to the gates G of the p-type and n-type transistors 12 and 14. Therefore, with regard to p-type transistor 12, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[117]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 2.5V - V_{dd} \\ &= 0V \end{aligned}$$

[118] In this case, since the voltage V_{GS} ($= 0V$) is larger than the threshold voltage V_{th} ($= -1.5V$) of the p-type transistor 12, the p-type transistor 12 becomes off-state.

[119] On the other hand, with regard to n-type transistor 14, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[120]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 2.5V - V_{SS} \\ &= 2.5V \end{aligned}$$

[121] In this case, since the voltage V_{GS} ($= 2.5V$) is larger than the threshold voltage V_{th} ($= +1.5V$) of the n-type transistor 14, the n-type transistor 14 becomes on-state.

[122] Therefore, the transistors 12 and 14 are in on-state and off-state, respectively, during the period from the instant t3 to the instant t4. The node N2 is connected to the power supply V_{ss} ($= 0V$) since the transistor 14 is ON, but is not connected to the power supply V_{dd} ($= 2.5V$) irrespective of whether the transistor 13 is ON or OFF since the transistor 12 is OFF. Therefore, the node N2 is discharged to the voltage V_{ss} ($= 0V$) during the period from the instant t3 to the instant t4 (the data invalid period Pi2), so that the voltage of the level shift data Dshift is set to 0V.

[123] The node N2 is discharged to 0V during the data invalid period Pi2 in this way, and then a transition is made to a data valid period Pv2 (the instant t4 to the instant t5).

[124] During the period from the instant t4 to the instant t5, the clock signal CLK has the low level voltage ($= 0V$), so that the transistors 12 and 14 are in the on-state and off-state, respectively. Since the input data Din is 1.5V, the voltage of 1.5V is applied to the gate G of the p-type transistor 13. The voltage on the source S of the p-type transistor 13 is V_{dd} ($= 2.5V$) since the p-type transistor 12 is in the on-state. Therefore, with regard to p-type transistor 13, the voltage V_{GS} between source S and gate G viewed from the source S is as follows.

[125]

$$\begin{aligned} V_{GS} &= V_G - V_S \\ &= 1.5V - V_{dd} \\ &= -1V \end{aligned}$$

[126] In this case, since the voltage V_{GS} ($= -1V$) is larger than the threshold voltage V_{th} ($= -1.5V$) of the p-type transistor 13, the p-type transistor 13 becomes off-state. Therefore, the node N2 is not connected to the power supply V_{dd} ($= 2.5V$). During the data valid period Pv2 (the instant t4 to the instant t5), the node N2 also is not connected to the power supply V_{ss} ($= 0V$) since the transistor 14 is in the off-state. As a result of this, the node N2 continuously holds 0V of the data invalid period Pi2 (the instant t3 to the instant t4) during the data valid period Pv2, so that the voltage of the

level shift data Dshift becomes 0V (the instant t4 to the instant t5).

- [127] As described above, the node N2 is not connected to the power supplies Vdd and Vss during the instant t4 to the instant t5. Therefore, the voltage on the node N2 may change because of an occurrence of a leak current and a change of the load capacitance Cload, so that the voltage of 0V may not be substantially held. In this case, the same strategies as (1) and/or (2) explained with reference to Fig. 3 can be used.
- [128] Next, during the period from the instant t5 to the instant t6 (data invalid period Pi3), the clock signal CLK has the high level voltage (= 2.5V), so that the transistors 12 and 14 are in the off-state and on-state, respectively. The node N2 is connected to the power supply Vss (= 0V) since the transistor 14 is ON, but is not connected to the power supply Vdd (= 2.5V) irrespective of whether the transistor 13 is ON or OFF since the transistor 12 is OFF. Therefore, the node N2 is discharged to the voltage Vss (= 0V) during the period from the instant t5 to the instant t6 (the data invalid period Pi3), so that the voltage of the level shift data Dshift is set to 0V.
- [129] Next, a transition is made to a data valid period Pv3 (the instant t6 to the instant t7).
- [130] During the period from the instant t6 to the instant t7, the clock signal CLK has the low level voltage (= 0V), so that the transistors 12 and 14 are in the on-state and off-state, respectively. During the period from the instant t6 to the instant t7, the input data Din is 0V, so that the voltage of 0V is applied to the gate G of the p-type transistor 13. The voltage on the source S of the p-type transistor 13 is 2.5V since the n-type transistor 12 is in the on-state. Therefore, the voltage V_{GS} of the p-type transistor 13 is -2.5V and is smaller than the threshold voltage Vth (= -1.5V). As a result of this, the p-type transistor 13 becomes on-state.
- [131] Therefore, during the period from the instant t6 to the instant t7, the transistor 14 is off-state, but the transistors 12 and 13 are on-state, so that the node N2 is connected to the power supply Vdd (= 2.5V). As a result of this, the node N2 is charged from 0V to 2.5V at the instant t6, so that the voltage of the level shift data Dshift becomes 2.5V (the instant t6 to the instant t7).
- [132] In this way, the level shifter 11 shown in Fig. 4 shifts the voltage level 0V of the input data Din to 2.5V and shifts the voltage level 1.5V of the input data Din to 0V and outputs the level-shifted input data Din as the level shift data Dshift.
- [133] The level shifter 11 shown in Fig. 4 can output the level shift data Dshift without an inverted input data Din_inv used for shifting a level of the input data Din. In the level shifter 11, the p-type transistor 12 at the side of the voltage Vdd and the n-type transistor 14 at the side of the voltage Vss with respect to the node N2 are controlled by the clock signal CLK, so that if one of these transistors is in the on-state, the other is in the off-state (see Fig. 5). Therefore, during the operation of the level shifter 11, the

power supply Vdd and the power supply Vss are prevented from becoming shorted to each other. As a result of this, it is prevented that DC current flows from the power supply Vdd to Vss, so that low power consumption is achieved.

- [134] It is possible that the input data Din having the voltages 1.5V and 0V is shifted to the level shift data Dshift having the voltages 5V and 0V by combining the level shifters 11 and 1 shown in Figs. 4 and 2.
- [135] Fig. 6 shows a level shifter 10 of the third embodiment according to the present invention. Fig. 7 is a timing chart of the level shifter 10 shown in Fig. 6.
- [136] It is noted that the level shifter 10 shown in Fig. 6 does not comprise the transistor 4 shown in Fig. 2, but instead comprises an AND circuit 5. The AND circuit 5 receives an input data Din and an clock signal CLK' and outputs an input data Din' into a gate G of the transistor 3. The input data Din' represents a logical sum of the input data Din and the clock signal CLK'.
- [137] In the following, operation of the level shifter 10 will be described using a timing chart of the level shifter 10 (see Fig. 7).
- [138] Basic operation of the level shifter 10 is the same as that of the level shifter 1 shown in Fig. 2. That is, the level shifter 10 pre-charges the node N1 to the voltage Vdd (= 5V) during the data invalid period. Next, if the voltage of the input data Din during the data valid period is 0V, the voltage Vdd on the pre-charged node N1 is held, and if the voltage of the input data Din is 5V, the node N1 is discharged from the Vdd (= 5V) to Vss (= 0V). Therefore, the Dshift outputted from the level shifter 10 shown in Fig. 6 is the same as the Dshift outputted from the level shifter 1 shown in Fig. 2 (see timing charts shown in Figs. 7 and 3). However, the level shifter 10 shown in Fig. 6 shifts level of the input data Din by not only using the first clock signal CLK but also using the second clock signal CLK'. A difference between the clock signals CLK and CLK' is that the high level voltage of the first clock signal CLK is 5V, while the high level voltage of the second clock signal CLK' is 2.5V. The second clock signal CLK' and the input data Din are received by the AND circuit 5.
- [139] The AND circuit 5 changes the input data Din to the input data Din' on the basis on the second clock signal CLK' and then outputs the input data Din' (hereinafter, the input data Din' is referred to as "changed input data Din' "). More specifically, the AND circuit 5 outputs the voltage level of the input data Din when the second clock signal CLK' is high level voltage (= 2.5V), and outputs low level voltage (= 0V) as the changed input data Din' when one of the second clock signal CLK' and the input data Din is low level voltage (=0V). As shown in the timing chart of Fig. 7, during the data valid periods Pv1, Pv2, ..., the voltage of the second clock signal CLK' is high level (= 2.5V), so that the AND circuit 5 outputs the voltages of the input data Din of the data valid periods Pv1, Pv2, ... as the voltages of the changed input data Din'. During the

data invalid periods $Pi1$, $Pi2$, ..., the second clock signal CLK' is low level voltage (= 0V), so that the AND circuit 5 outputs voltage of 0V as the changed input data Din' irrespective of the voltage level of the input data Din of the data invalid periods $Pi1$, $Pi2$,...

- [140] Such changed input data Din' controls the transistor 3, so that the level shifter 10 operates as follows.
- [141] During the period from the instant $t1$ to the instant $t2$, the first clock signal CLK has the low level voltage (= 0V), so that the voltage of 0V is applied to the gate G of the p-type transistor 2. Therefore, the voltage V_{GS} of the p-type transistor 2 is -5V and thus is smaller than the threshold voltage V_{th} (= -1V to -2V) of the p-type transistor 2. As a result, the p-type transistor 2 becomes on-state.
- [142] Since the second clock signal CLK' is 0V during the period from the instant $t1$ to the instant $t2$, it is noted that the AND circuit 5 outputs the voltage of 0V as the changed input data Din' . Therefore, the voltage V_{GS} of the n-type transistor 3 is 0V and thus is smaller than the threshold voltage V_{th} (= +1V to +2V) of the n-type transistor 3, so that the n-type transistor 3 becomes off-state.
- [143] Since the p-type transistor 2 is in the on-state and the n-type transistor 3 is in the off-state, the node N1 is connected to the power supply V_{dd} (= 5V). Therefore, the node N1 is pre-charged to the voltage V_{dd} (= 5V) during the period from the instant $t1$ to the instant $t2$ (the data invalid period $Pi1$), so that the voltage of the level shift data $Dshift$ is set to 5V.
- [144] The node N1 is pre-charged to 5V during the data invalid period $Pi1$ in this way, and next, a transition is made to the data valid period $Pv1$ (the instant $t2$ to the instant $t3$).
- [145] During the period from the instant $t2$ to the instant $t3$, the first clock signal CLK is the high level voltage (= 5V), so that the voltage of 5V is applied to the gate G of the p-type transistor 2. Therefore, the voltage V_{GS} of the p-type transistor 2 is 0V and thus is larger than the threshold voltage V_{th} (= -1V to -2V) of the p-type transistor 2. As a result, the p-type transistor 2 becomes off-state.
- [146] Further, since the second clock signal CLK' is 2.5V and the input data Din also is 2.5V during the period from the instant $t2$ to the instant $t3$, the AND circuit 5 outputs the voltage of 2.5V as the changed input data Din' , so that the voltage of 2.5V is applied to the gate G of the n-type transistor 3. Therefore, the voltage V_{GS} of the n-type transistor 3 is 2.5V and thus is larger than the threshold voltage V_{th} (= +1V to +2V) of the n-type transistor 3, so that the n-type transistor 3 becomes on-state.
- [147] During the period from the instant $t2$ to the instant $t3$, the node N1 is not connected to the power supply V_{dd} (= 5V) since the transistor 2 is in the off-state, but is connected to the power supply V_{ss} (= 0V) since the transistor 3 is in the on-state. As a

result, the node N1 is discharged from 5V to 0V at the instant t2, so that the voltage of the level shift data Dshift becomes 0V (the instant t2 to the instant t3).

[148] In this way, the voltage level of the input data Din during the data valid period Pv1 (the instant t2 to the instant t3) is shifted from 2.5V to 0V.

[149] Next, during the period from the instant t3 to the instant t4, the first clock signal CLK has the low level voltage (= 0V), so that the voltage of 0V is applied to the gate G of the p-type transistor 2. Therefore, the voltage V_{gs} of the p-type transistor 2 is -5V and thus is smaller than the threshold voltage V_{th} (= -1V to -2V) of the p-type transistor 2. As a result, the p-type transistor 2 becomes on-state.

[150] Since the second clock signal CLK' is 0V during the period from the instant t3 to the instant t4, it is noted that the AND circuit 5 outputs the voltage of 0V as the changed input data Din'. Therefore, the voltage V_{gs} of the n-type transistor 3 is 0V and thus is smaller than the threshold voltage V_{th} (= +1V to +2V) of the n-type transistor 3, so that the n-type transistor 3 becomes off-state.

[151] Therefore, the transistors 2 and 3 are in the on-state and off-state, respectively, during the period from the instant t3 to the instant t4. The node N1 is connected to the power supply Vdd (= 5V) since the transistor 2 is ON, but is not connected to the power supply Vss (=0V) since the transistor 3 is OFF. Therefore, during the period from the instant t3 to the instant t4 (the data invalid period Pi2), the node N1 is pre-charged to the voltage Vdd (=5V), so that the voltage of the level shift data Dshift is set to 5V.

[152] The node N1 is pre-charged to 5V during the data invalid period Pi2 in this way, and next, a transition is made to the data valid period Pv2 (the instant t4 to the instant t5).

[153] During the period from the instant t4 to the instant t5, the AND circuit 5 outputs the voltage of 0V as the changed input data Din' since the second clock signal CLK' is 2.5V and the input data Din is 0V, so that the voltage of 0V is applied to the gate G of the n-type transistor 3. Therefore, the n-type transistor 3 becomes off-state.

[154] During the period from the instant t4 to the instant t5, the first clock signal CLK is the high level voltage (= 5V), so that the voltage of 5V is applied to the gate G of the p-type transistor 2. Therefore, the p-type transistor 2 becomes off-state.

[155] Since the transistors 2 and 3 are both off-state as described above, the node N1 is not connected to the power supplies Vdd and Vss. As a result of this, the node N1 continuously holds the voltage 5V of the data invalid period Pi2 (the instant t3 to the instant t4) during the data valid period Pv2 (the instant t4 to the instant t5), so that the voltage of the level shift data Dshift remains 5V. In this way, the voltage 0V of the input data Din during the data valid period Pv2 (the instant t4 to the instant t5) is shifted to 5V.

- [156] In a case in which the voltage of 5V on the node N1 changes because of an occurrence of a leak current and a change of the load capacitance C_{load} and consequently the amount of change in voltage during the data valid period $Pv2$ can not be negligible, the strategies (1) and/or (2) explained with reference to Fig. 3 can be used.
- [157] Next, during the period from the instant $t5$ to the instant $t6$, the first clock signal CLK has the low level voltage ($= 0V$) and thus the voltage of 0V is applied to the gate G of the p-type transistor 2, so that the p-type transistor 2 becomes on-state.
- [158] Further, since the second clock signal CLK' is 0V during the period from the instant $t5$ to the instant $t6$, the AND circuit 5 outputs the voltage of 0V as the changed input data Din' , so that the n-type transistor 3 becomes off-state.
- [159] Since the p-type transistor 2 is in the on-state and the n-type transistor 3 is in the off-state, the node N1 is connected to the power supply V_{dd} ($= 5V$), so that the voltage of the level shift data $Dshift$ is kept 5V (the instant $t5$ to the instant $t6$).
- [160] Next, during the period from the instant $t6$ to the instant $t7$, the first clock signal CLK is the high level voltage ($= 5V$), so that the transistor 2 becomes off-state. And, since the input data Din is 2.5V during the period from the instant $t6$ to the instant $t7$, the AND circuit 5 outputs the voltage of 2.5V as the changed input data Din' , so that the n-type transistor 3 becomes on-state.
- [161] During the period from the instant $t6$ to the instant $t7$, the transistor 2 is in the off-state but the transistor 3 is in the on-state, so that the node N1 is connected to the power supply V_{ss} ($= 0V$). As a result of this, the node N1 is discharged from 5V to 0V at the instant $t6$, so that the voltage of the level shift data $Dshift$ becomes 0V (the instant $t6$ to the instant $t7$). In this way, the voltage 2.5V of the input data Din during the data valid period $Pv3$ (the instant $t6$ to the instant $t7$) is shifted to 0V.
- [162] As described above, the level shifter 1 shown in Fig. 2 shifts the voltage 0V of the input data Din to 5V and shifts the voltage 2.5V of the input data Din to 0V, and outputs the level-shifted input data Din as the level shift data $Dshift$. Therefore, the $Dshift$ outputted from the level shifter 10 shown in Fig. 6 is the same as the $Dshift$ outputted from the level shifter 1 shown in Fig. 2 (see the timing charts shown in Figs. 7 and 3).
- [163] The level shifter 10 shown in Fig. 6 can output the level shift data $Dshift$ without an inverted input data Din_{inv} used for shifting a level of the input data Din . Further, the level shifter 10 comprises two transistors 2 and 3. The transistor 2 is controlled by the clock signal CLK, so that the transistor 2 is in the on-state during the data invalid periods. On the other hand, it is noted that the transistor 3 is controlled by the changed input data Din' outputted from the AND circuit 5. The AND circuit 5 changes the voltages of the input data Din of the data invalid periods to 0V and then outputs the input data Din as the changed input data Din' , so that the transistor 3 is always in the

off-state during the data invalid periods. Therefore, the transistor 3 is in the off-state while the transistor 2 is in the on-state, so that the power supply Vdd and the power supply Vss are prevented from becoming shorted to each other during the operation of the level shifter 10 and thus lower power consumption is achieved.

- [164] In the third embodiment, to provide the means for changing the input data Din (2.5V/0V), the AND circuit 5, realizes the level shifter 10 (see Fig. 6) in which the transistor 4 required for the level shifter 1 shown in Fig. 2 is omitted. This concept can be applied to the level shifter 11 shown in Fig. 4, so that to provide the means for changing the input data Din (1.5V/0V) can realize a different level shifter in which the transistor 12 required for the level shifter 11 is omitted.
- [165] Fig. 8 is a schematic diagram showing a voltage converting device 50 in which the level shifter 1 shown in Fig. 2 is used. Fig. 9 shows a timing chart of the voltage converting device 50.
- [166] The voltage converting device 50 comprises the level shifter 1 shown in Fig. 2 and a latch 102. The latch 102 shown in Fig. 8 has the same structure as the latch 102 shown in Fig. 1 has.
- [167] The level shifter Dshift outputted from the level shifter 1 is processed by the latch 102 and is outputted as an output data Dout. An detailed explanation of an operation of the latch 102 is omitted since the latch 102 itself is known. If the voltage of the input data Din is 2.5V, this voltage of 2.5V is shifted to the voltage of 0V by the level shifter 1 as explained with respect to Figs. 2 and 3, so that the voltage of the level shift data Dshift is 0V. The voltage of 0V of the level shift data Dshift is converted into a voltage of 5V by the latch 102, so that the output data Dout is 5V. On the other hand, if the voltage of the input data Din is 0V, this voltage of 0V is shifted to the voltage of 5V by the level shifter 1, so that the voltage of the level shift data Dshift is 5V. The voltage of 5V of the level shift data Dshift is converted into a voltage of 0V by the latch 102, so that the output data Dout is 0V. Therefore, the voltage converting device 50 outputs the voltage of 5V if the input data Din is 2.5V, but outputs the voltage of 0V if the input data Din is 0V.
- [168] It is noted that, in the voltage converting device 50 shown in Fig. 8, both transistors 2 and 3 of the level shifter 1 are in the off-state during the period of instant t4 to the instant t5 (see Fig. 3) and thus the node N1 is not connected to both the power supply Vdd and the power supply Vss. Therefore, if an input capacitance of the latch 102 is changed by a rising or a falling of the clock signal CLK or CLK_inv, the voltage on the node N1 (the level shift data Dshift) during the period from the instant t4 to the instant t5 may change with the change in this input capacitance. In this case, there is no problem if an amount of change in voltage is negligible. However, if the voltage on the node N1 is changed to an extent that the latch 102 incorrectly recognizes the voltage

on the node N1 as 0V instead of 5V, the voltage converting device 50 can not output the correct output data Dout. For this reason, if the amount of change in voltage on the node N1 may not be negligible, the voltage converting device 50 shown in Fig. 8 can be configured, for example, as shown in Fig. 10.

[169] Fig. 10 is schematic diagram showing a voltage converting device 60 of a different example from the voltage converting device 50 shown in Fig. 8. Fig. 11 is a timing chart of the voltage converting device 60.

[170] The voltage converting device 60 comprises a level shifter 20 and a latch 103. The level shifter 20 comprises a first portion 21. The first portion 21 has the same structure as the level shifter 1 shown in Fig. 8 has. Therefore, an intermediate shift data Dimm on the node N1 of the first portion 21 has the same waveform as the level shift data Dshift shown in Fig. 9 has. It is noted that the level shifter 20 shown in Fig. 10 comprises a second portion 22 in a succeeding stage of the first portion 21. Therefore, the intermediate shift data Dimm outputted from the first portion 21 is not supplied to the latch 103, but supplied to the second portion 22. Since the second portion 22 is an inverter, the intermediate shift data Dimm is inverted by the second portion 22 and the inverted intermediate shift data Dimm appears on the node N2 of the second portion 22 as a level shift data Dshift.

[171] Since the node N2 is connected to the power supply Vdd when the voltage of the intermediate shift data Dimm is 0V and the node N2 is connected to the power supply Vss when the voltage of the intermediate shift data Dimm is 5V, it is noted that the node N2 is substantially always connected to the power supply Vdd or the power supply Vss. Therefore, even if the voltage on the node N2 changes because of the change in the input capacitance of the latch 103, the changed voltage on the node N2 can be immediately returned to the original voltage. As a result, the level shift data Dshift outputted from the level shifter 20 is received by the latch 103 without being substantially affected by the change in the input capacitance of the latch 103.

[172] It is noted that a relationship between the level shift data Dshift received by the latch 103 shown in Fig. 10 and the level shift data Dshift received by the latch 102 shown in Fig. 8 is an inverted relationship (see the timing charts of Figs. 9 and 11). Therefore, assuming that a voltage on a node X is taken from the latch 103 shown in Fig. 10 as the output data Dout in the same manner as the latch 102 shown in Fig. 8 carries out, the output data Dout of the voltage converting device 60 shown in Fig. 10 is represented by inverting the output data Dout of the voltage converting device 50 shown in Fig. 8. In order that the voltage converting device 60 shown in Fig. 10 can output the substantially same output data Dout as the voltage converting device 50 shown in Fig. 8 outputs, the voltage converting device 60 outputs a voltage on a node Y instead of the node X as the output data Dout. This makes it possible that the voltage

converting device 60 shown in Fig. 10 outputs the substantially same output data Dout as the voltage converting device 50 shown in Fig. 8 outputs although the level shifter 20 comprises the second portion 22 (inverter).

[173] In Figs. 8 to 11, the level shifter 1 shown in Fig. 2 is applied to the voltage converting device. However, even if the level shifter 10 shown in Fig. 6 is used instead of the level shifter 1, the same output data Dout as Figs. 9 and 11 illustrate are outputted.

[174] A voltage converting device can be obtained by combining the level shifter 11 shown in Fig. 4 and a latch.

[175] Fig. 12 shows an example in which the voltage converting device 50 shown in Fig. 8 is applied to a mobile phone 200.

[176] Fig. 12 schematically illustrates a part of a liquid crystal cell at a side of a glass substrate 80 and a part of a TCP 70, and the TCP 70 is attached to the glass substrate 80 with an anisotropic conductive film (not shown). On the glass substrate 80, the voltage converting device 50 shown in Fig. 8 is provided. On the TCP 70, an IC chip 71 is mounted. The IC chip 71 outputs a clock signal (hereinafter, referred to as "IC clock signal") CLK', an inverted clock signal (hereinafter, referred to as "inverted IC clock signal") CLK'_inv, and digital data of 1bit (Data). The voltage converting device 50 receives this Data outputted from the IC chip 71 as an input data Din and then outputs an output data Dout. It is noted that, for the purpose of controlling a transistor 2, the voltage converting device 50 does not receive the IC clock signal CLK' but receives a clock signal CLK obtained by shifting a level of the IC clock signal CLK' with a level shifter 81. This reason will be described below.

[177] Transistors used in the IC chip 71 is usually formed on a silicon substrate, but the transistors 2, 3, and 4 of the voltage converting device 50 are formed on the glass substrate 80. Therefore, the transistors 2, 3, and 4 formed on the glass substrate 80 are usually different in threshold voltage from the transistors used in the IC chip 71. As one example, p-type and n-type transistors used in the IC chip 71 has threshold voltage of approximately -1V and +1V, respectively, but the p-type transistor 2 formed on the glass substrate 80 has a threshold voltage of -1V to -2V and the n-type transistors 3 and 4 formed on the glass substrate 80 have a threshold voltage of +1V to +2V. For this reason, power supply voltages Vss and Vdd required for the voltage converting device 50 are different from those required for the IC chip 71 (for example, the voltage Vdd required for the voltage converting device 50 must be higher than the voltage Vdd required for the IC chip 71). As one example, the power supply voltages Vss and Vdd required for the IC chip 71 is 0V and 2.5V, respectively, but the power supply voltages Vss and Vdd required for the voltage converting device 50 is 0V and 5V, respectively. In the case that the power supply voltages of the IC chip 71 are Vss=0V and

V_{dd}=2.5V, the IC clock signal CLK' has the voltages of 0V and 2.5V, whereas in the case that the power supply voltages of the voltage converting device 50 are V_{ss}=0V and V_{dd}=5V, the source S of the transistor 2 is connected to power supply V_{dd} (=5V). Under such situation, if the IC clock signal CLK' itself is applied to the gate G of the transistor 2 of the level shifter 1, the V_{GS} of the transistor 2 becomes -2.5V or -5V. Therefore, if the threshold voltage V_{th} of the transistor 2 is -1V to -2V, the V_{GS} of the transistor 2 does not exceed the threshold voltage V_{th}, so that the transistor 2 can be turned on but can not be turned off. In order to ensure ON and OFF of the transistor 2, a different clock signal from the IC clock signal CLK' can be applied to the gate G of the transistor 2, for example. This different clock signal may be, for example, a clock signal having a low level voltage of 0V and a high level voltage of 5V. If the clock signal having the voltages of 0V and 5V, the V_{GS} of the transistor 2 becomes 0V and -5V, so that the transistor 2 can be reliably turned on and off even if the transistor 2 has the threshold voltage of -1V to -2V. In order to generate such different clock signal, the level shifter 81 for shifting the voltage level of the IC clock signal CLK' is provided in Fig. 12. The level shifter 81 may be, for example, the level shifter 101 shown in Fig. 1. By supplying the level shifter 101 shown in Fig. 1 with the IC clock signal CLK' and the inverted IC clock signal CLK'_inv instead of the input data Din and the inverted input data Din_inv, the level shifter 101 outputs the clock signal CLK having the voltages of 0V and 5V. Therefore, the transistor 2 can be surely turned on and off by supplying the clock signal CLK to the transistor 2 of the level shifter 1.

- [178] In this way, the voltage converting device 50 can convert the input data Din received from the IC chip 71 into the desired output data Dout as shown in the timing chart of Fig. 9.
- [179] In Fig. 12, in order to be able to shift the voltage level of the digital data of 1 bit Data outputted from the IC chip 71, one voltage converting device 50 shown in Fig. 8 is provided. If it is necessary that the IC chip 71 outputs digital data of a plurality of bits and that voltage levels of the digital data of the plurality of bits are shifted, a plurality of voltage converting devices each of which is the voltage converting device shown in Fig. 8 may be accordingly provided. A case in which the plurality of voltage converting devices are provided and each of the voltage converting devices is the voltage converting devices shown in Fig. 8 will be described below.
- [180] Fig. 13 shows an example in which a mobile phone 201 comprises a plurality of voltage converting devices 50 and each of the voltage converting devices 50 is the voltage converting device 50 shown in Fig. 8.
- [181] An IC chip 71 mounted on a TCP 70 outputs M digital data Data1, Data2, ..., DataM. In order to shift the voltage levels of the M digital data Data1, Data2, ..., DataM, M voltage converting devices 50 are formed on the glass substrate 80, and

each of the voltage converting devices 50 is the voltage converting device shown in Fig. 8. Each of M digital data Data1, Data2, ..., DataM outputted from the IC chip 71 is supplied to a respective one of the voltage converting devices 50 as a respective one of input data Din1, Din2, ..., DinM. The voltage converting devices 50 are supplied with the clock signal CLK (5V/0V) outputted from the level shifter 81 instead of the IC clock signal CLK' (2.5V/0V) outputted from the IC chip 71 in order to surely control the transistor 2 of the level shifter 1 of each of the voltage converting devices 50.

[182] In Fig. 13, each of M digital data Data1, Data2, ..., DataM outputted from the IC chip 71 is received by a respective one of voltage converting devices 50, so that the voltage levels of M digital data are shifted and then the shifted M digital data are outputted as output data Dout 1, Dout 2, ..., DoutM.

[183] In Fig. 13, since each of the voltage converting devices 50 is provided with the level shifter 1 according to the present invention, the power supply Vdd and the power supply Vss are prevented from becoming shorted to each other, and thus low power consumption of the mobile phone 201 is achieved.

[184] Now, assuming in Fig. 13 that the conventional level shifter 101 shown in Fig. 1 is used instead of each of the level shifters 1. In this case, it is noted that, in order for the level shifters 101 to shift the digital data Data1, Data2, ..., DataM, each of the level shifters 101 must additionally receive a respective one of the inverted digital data Data1_inv, Data2_inv, ..., DataM_inv. Therefore, in the case that the conventional level shifter 101 shown in Fig. 1 is used instead of each of the level shifters 1, the IC chip 71 must be provided with output portions of the inverted digital data Data1_inv, Data2_inv, ..., DataM_inv in addition to the output portions of the digital data Data1, Data2, ..., DataM. In contrast, in the case of the mobile phone 201 shown in Fig. 13, the clock signal CLK outputted from the level shifter 81 is commonly used for M level shifters 1 according to the present invention, so that the voltage levels of M input data Din1 to DinM can be shifted using one clock signal CLK and can be shifted without using M inverted input data for the level shifters. Therefore, the IC chip 71 need not have M output portions for the inverted digital data Data1_inv, Data2_inv, ..., DataM_inv corresponding to the M digital data Data1, Data2, ..., DataM, so that an interface for connecting the IC chip 71 and the level shifters 1 is simplified.

[185] Fig. 14 shows an example in which the level shifter 10 shown in Fig. 6 is applied to a mobile phone 300.

[186] Fig. 14 schematically illustrates a part of a liquid crystal cell at a side of a glass substrate 80 and a part of a TCP 70, and the TCP 70 is attached to the glass substrate 80 with an anisotropic conductive film (not shown). On the glass substrate 80, the level shifter 10 shown in Fig. 6 and the latch 102 shown in Fig. 1 are provided. The voltage converting device 82 consists of the level shifter 10 and the latch 102. On the TCP 70,

an IC chip 71 is mounted. Like the mobile phone 200 shown in Fig. 12, the mobile phone 300 comprises the level shifter 81 in order to control the transistor 2 of the level shifter 10.

- [187] The transistor 3 of the level shifter 10 is controlled by the changed input data Din' outputted from the AND circuit 5. Since the voltage levels of the changed input data Din' is 0V and 2.5V (see Fig. 6), the changed input data Din' is generated in the IC chip 72 which operates with the power supply of 2.5V. Therefore, the AND circuit 5 is formed within the IC chip 72. The AND circuit 5 receives the input data Din and the IC clock signal CLK' and outputs the changed input data Din' having the voltage levels of 0V and 2.5V (see the timing chart of Fig. 7).
- [188] In this way, the p-type transistor 2 is controlled by the clock signal CLK having the voltage levels of 0V and 5V, and the n-type transistor 3 is controlled by the changed input data Din' having the voltage levels of 0V and 2.5V. Therefore, the level shifter 10 can convert the input data Din into the desired output data Dout as shown in the timing chart of Fig. 7.
- [189] Fig. 15 shows an example in which a mobile phone 301 comprises a plurality of voltage converting devices and each of the voltage converting devices is the voltage converting device 82 shown in Fig. 14.
- [190] In order to convert M digital data Din1, Din2,..., DinM, the IC chip 72 mounted on the TCP 70 comprises M voltage converting devices 82 each of which is the voltage converting device 82 shown in Fig. 14. In order to surely control the transistor 2 of each of the level shifters 10, each of the voltage converting devices 82 is supplied with the clock signal CLK having the voltage levels of 0V and 5V from the level shifter 81. Since each of the input data Din1', Din2',..., DinM outputted from the AND circuits 5 of the voltage converting devices 82 has the voltage levels of 0V and 2.5V, the AND circuit 5 of each of the voltage converting devices 82 is formed within the IC chip 72.
- [191] Since the mobile phone 301 comprises the level shifters 10 according to the invention, the power supply Vdd and the power supply Vss are prevented from becoming shorted to each other during the operation of the level shifter 10, so that the lower power consumption of the mobile phone 301 is achieved.
- [192] In the mobile phone 301 shown in Fig. 15, two clock signals CLK' and CLK are inputted into each of M level shifters 10, and thus two clock signals CLK' and CLK are commonly used for M level shifters 10. Therefore, the voltage levels of M input data Din1 to DinM can be shifted using two clock signals CLK' and CLK and can be shifted without using M inverted input data for the level shifters. As a result, the IC chip 72 need not have M output portions for M inverted digital data Din1_inv, Din2_inv,..., DinM_inv corresponding to M input data Din1, Din2,..., DinM, so that an interface for connecting the IC chip 72 to the level shifters 10 is simplified.

- [193] Although the level shifters 1 and 10 shown in Figs. 2 and 6 are used in the mobile phones 200, 201, 300, and 301 described above, the level shifter 11 shown in Fig. 4 can be applied to a mobile phone. Further, although the examples in which these level shifters are applied to the mobile phones are described above, the level shifter according to the invention can be applied to the other devices in which voltage levels are required to be shifted.
- [194] Although the level shifters described above receive the input data having two voltage levels (0V and 5V) and then shift two voltage levels, it is also possible that, according to the invention, a level shifter is structured so as to receive input data having one voltage level or three or more voltage levels and then shift the received one voltage level or three or more voltage levels.

Claims

- [1] A level shifter for receiving a first clock signal and data having a first voltage to shift said first voltage to a second voltage, said level shifter comprising:
a first voltage supplying means for supplying said second voltage to a pre-determined position ; and
a second voltage supplying means for supplying a third voltage to said pre-determined position,
wherein said second voltage supplying means operates so as to block supply of said third voltage to said predetermined position when said first voltage supplying means supplies said second voltage to said predetermined position.
- [2] A level shifter as claimed in claim 1, wherein during a first period, said first voltage supplying means supplies said second voltage to said predetermined position and said second voltage supplying means blocks supply of said third voltage to said predetermined position,
and wherein during a second period succeeding to said first period, said first voltage supplying means blocks supply of said second voltage to said pre-determined position and said second voltage supplying means continues to block supply of said third voltage to said predetermined position.
- [3] A level shifter as claimed in claim 2, wherein during said first period, said first voltage supplying means supplies said second voltage to said predetermined position in response to said first clock signal and said second voltage supplying means blocks supply of said third voltage to said predetermined position in response to said first clock signal and said data,
and wherein during said second period, said first voltage supplying means blocks supply of said second voltage to said predetermined position in response to said first clock signal and said second voltage supplying means continues to block supply of said third voltage to said predetermined position in response to said first clock signal and said data.
- [4] A level shifter as claimed in claim 1, wherein during a first period, said first voltage supplying means blocks supply of said second voltage to said pre-determined position and said second voltage supplying means supplies said third voltage to said predetermined position,
and wherein during a second period succeeding to said first period, said first voltage supplying means supplies said second voltage to said predetermined position and said second voltage supplying means blocks supply of said third voltage to said predetermined position.
- [5] A level shifter as claimed in claim 4, wherein during said first period, said first

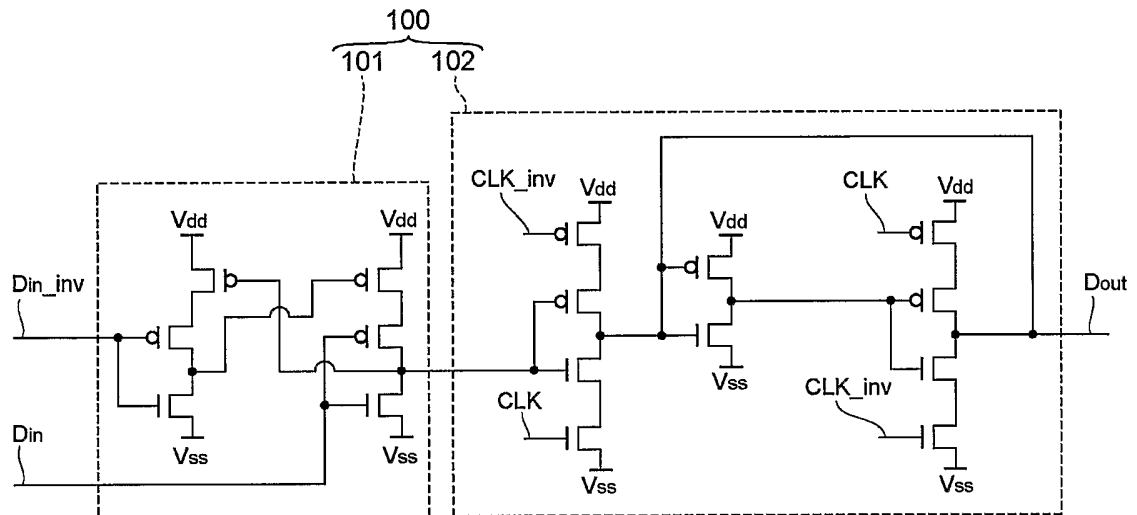
voltage supplying means blocks supply of said second voltage to said predetermined position in response to said first clock signal and said second voltage supplying means supplies said third voltage to said predetermined position in response to said first clock signal and said data,
and wherein during a second period succeeding to said first period, said first voltage supplying means supplies said second voltage to said predetermined position in response to said first clock signal and said second voltage supplying means blocks supply of said third voltage to said predetermined position in response to said first clock signal and said data.

- [6] A level shifter as claimed in any one of claims 2 to 5, wherein said first voltage supplying means comprises a first switch means, said first switch means becoming on-state and off-state in response to said first clock signal, wherein said second voltage supplying means comprises a second switch means, said second switch means becoming on-state and off-state in response to said first clock signal,
and wherein said second switch means is off-state when said first switch means is on-state, and said second switch means is on-state when said first switch means is off-state.
- [7] A level shifter as claimed in claim 6, wherein said level shifter comprises a third switch means between said predetermined position and said second switch means, said third switch means becoming on-state and off-state in response to said data.
- [8] A level shifter as claimed in claims 2 or 4 wherein said first voltage supplying means comprises a fourth switch means, said fourth switch means becoming on-state and off-state in response to said first clock signal,
wherein said second voltage supplying means comprises a data processing means for processing said data and a fifth switch means, said fifth switch means becoming on-state and off-state in response to said processed data,
and wherein said fifth switch means is in off-state when said fourth switch means is in on-state, and said fifth switch means is in on-state when said fourth switch means is in off-state.
- [9] A level shifter as claimed in claim 8, wherein said data has a data valid period and a data invalid period,
and wherein said data processing means changes a voltage of said data of said data in valid period to a voltage used for making said fifth switch means on-state or off-state.
- [10] A level shifter as claimed in claim 9, wherein said data processing means changes a voltage of said data of said data in valid period to a voltage used for making said fifth switch means on-state or off-state by using second clock signal

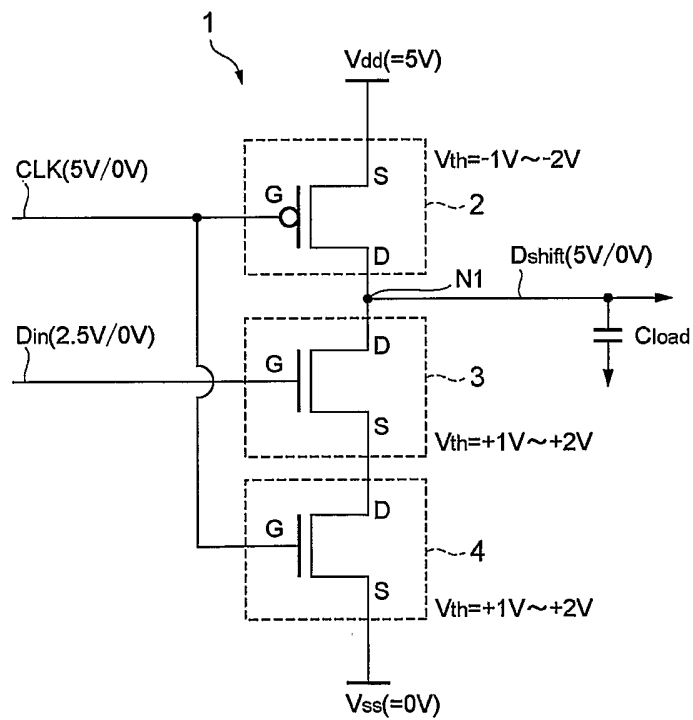
, said second clock signal having voltage levels in versed with respect to voltage levels of said first clock signal.

[11] A voltage converting device comprising said level shifter as claimed in any one of claims 1 to 10.

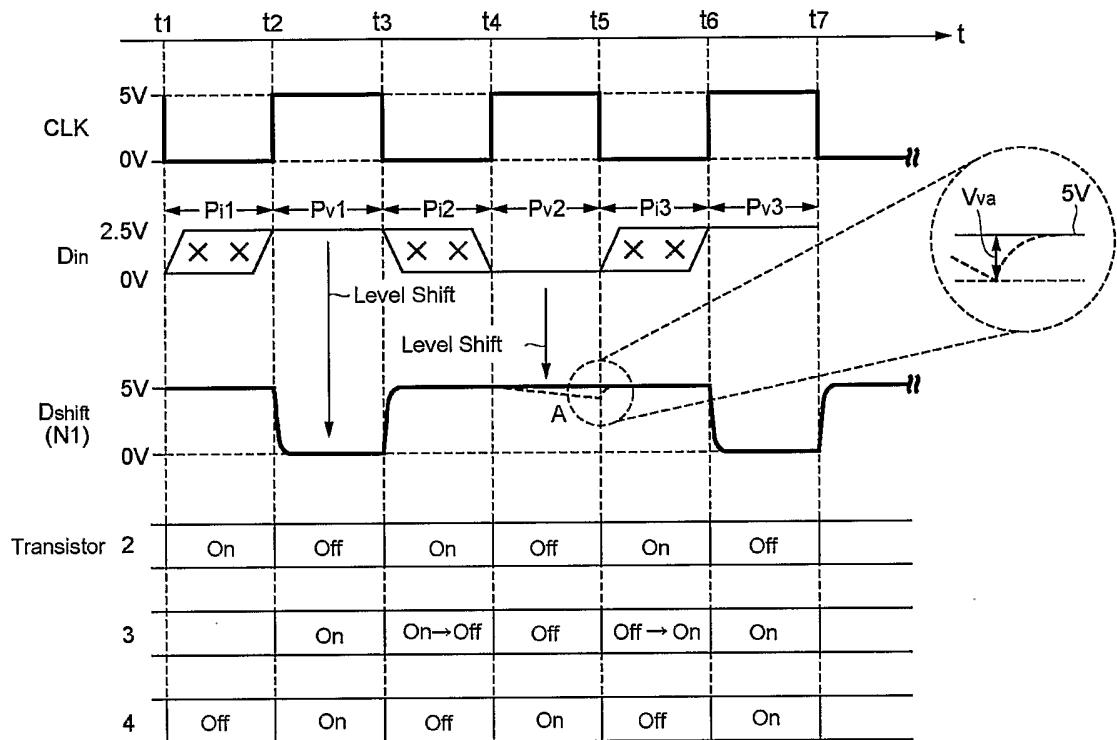
[Fig. 1]



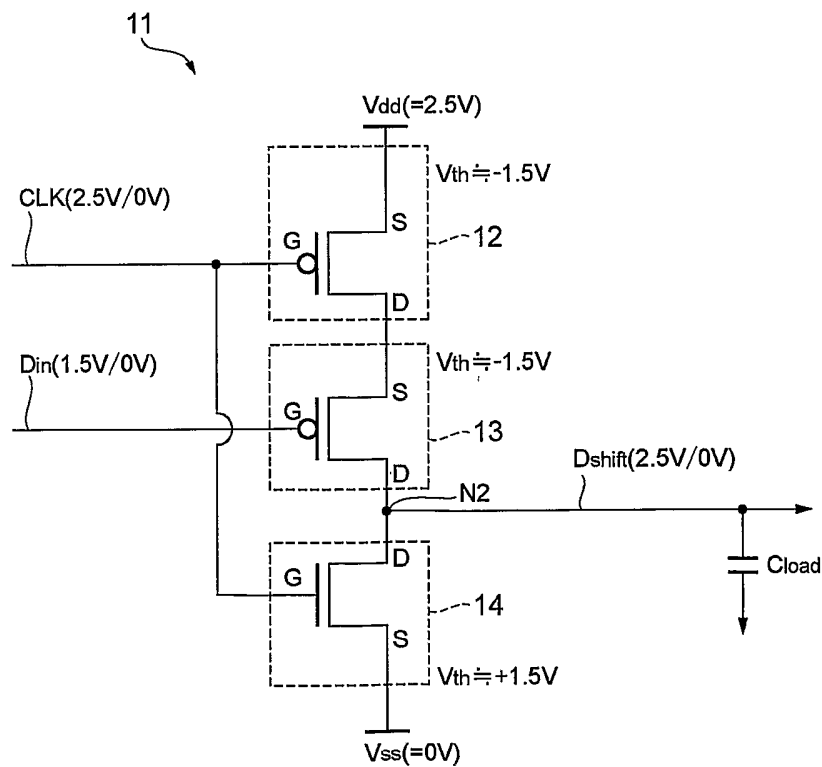
[Fig. 2]



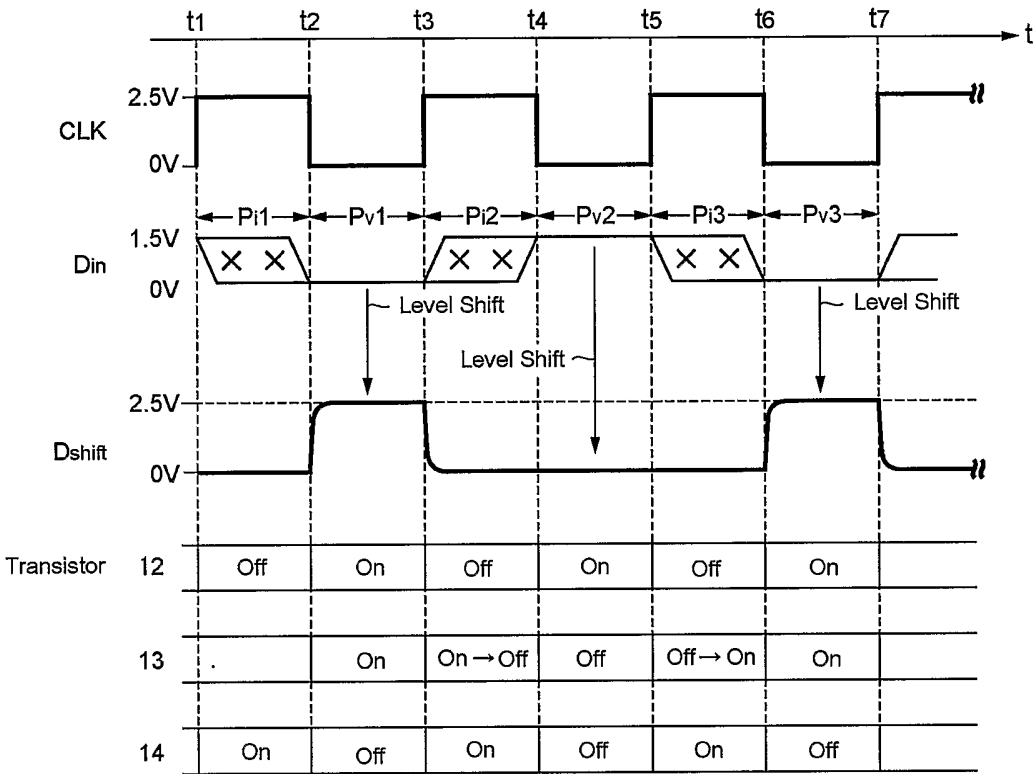
[Fig. 3]



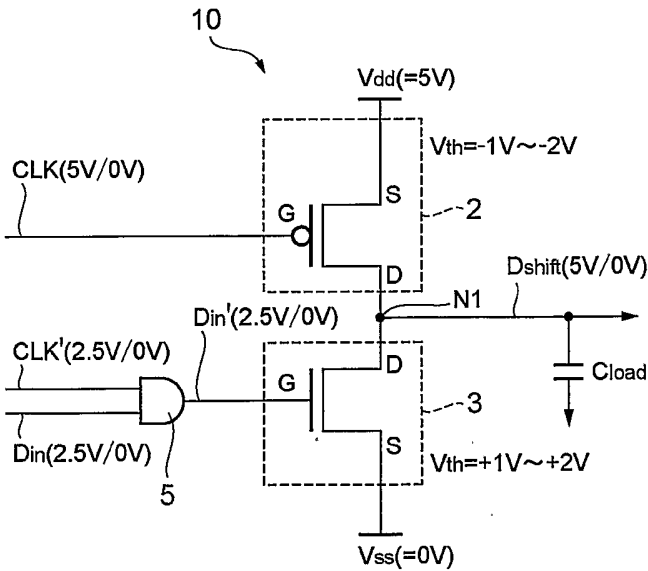
[Fig. 4]



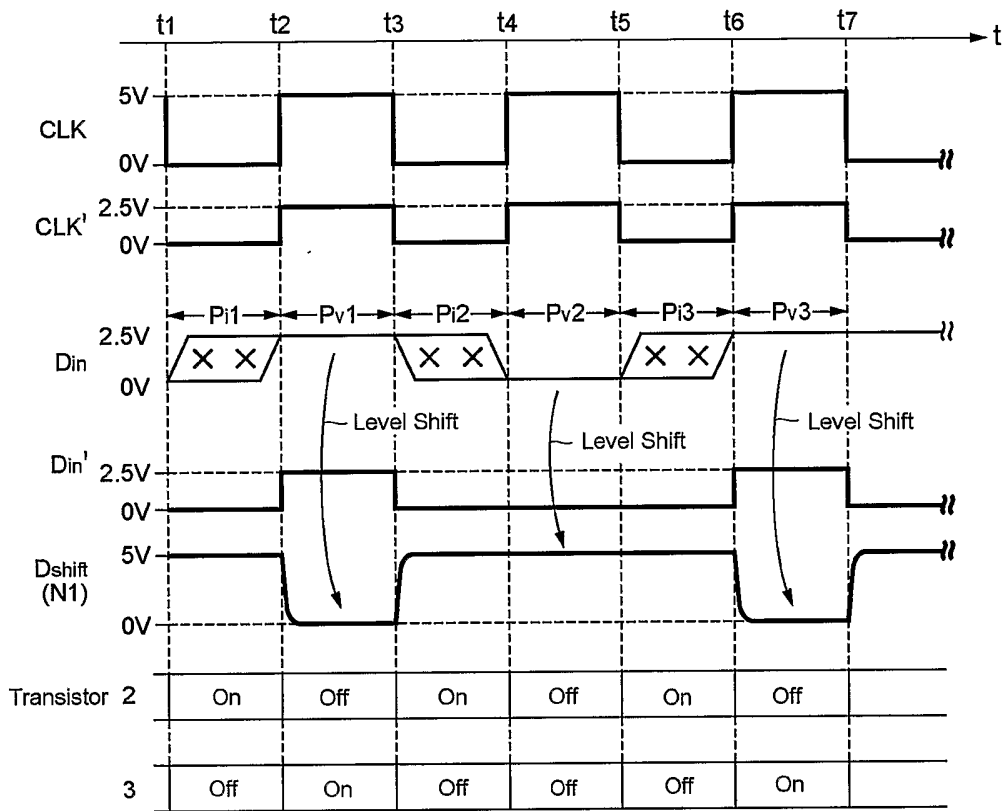
[Fig. 5]



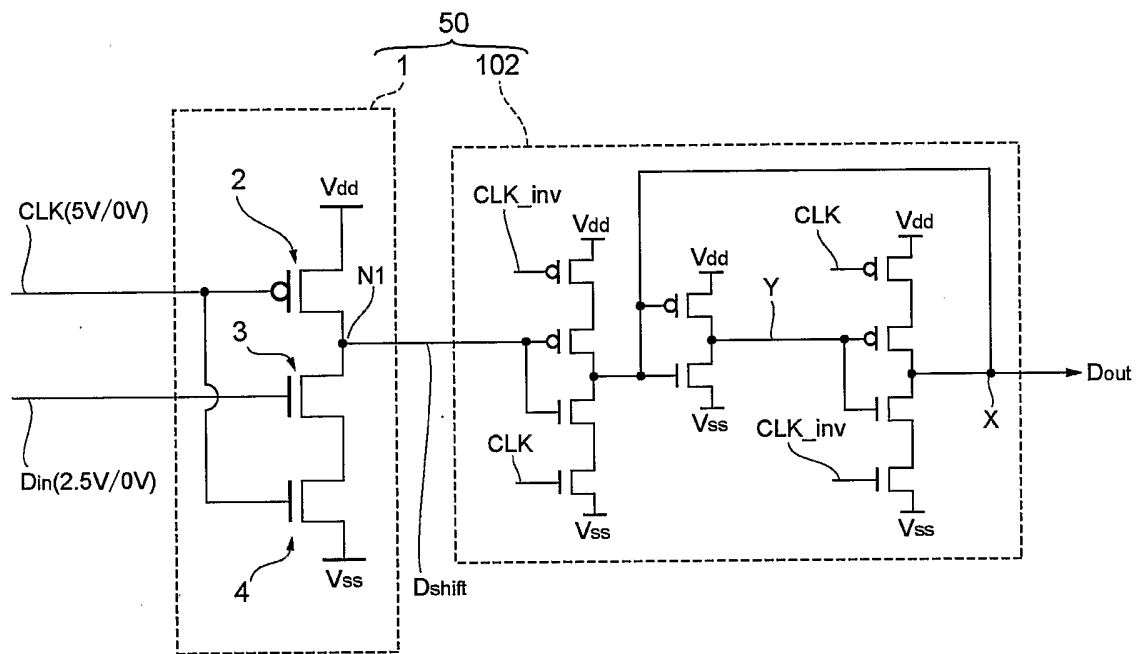
[Fig. 6]



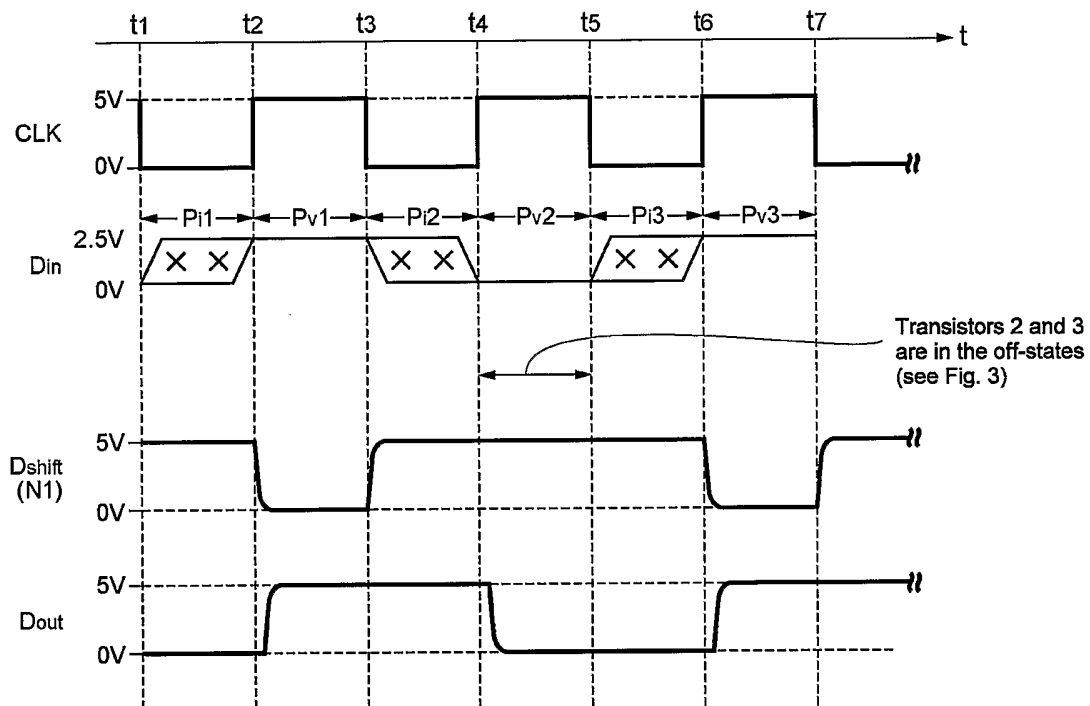
[Fig. 7]



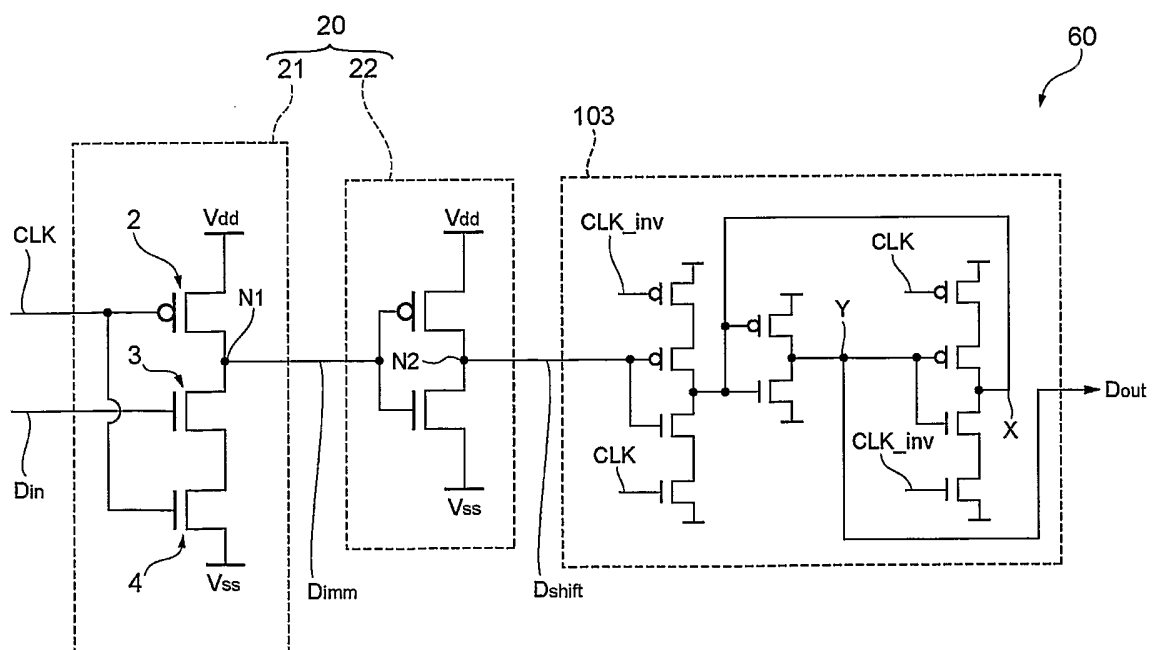
[Fig. 8]



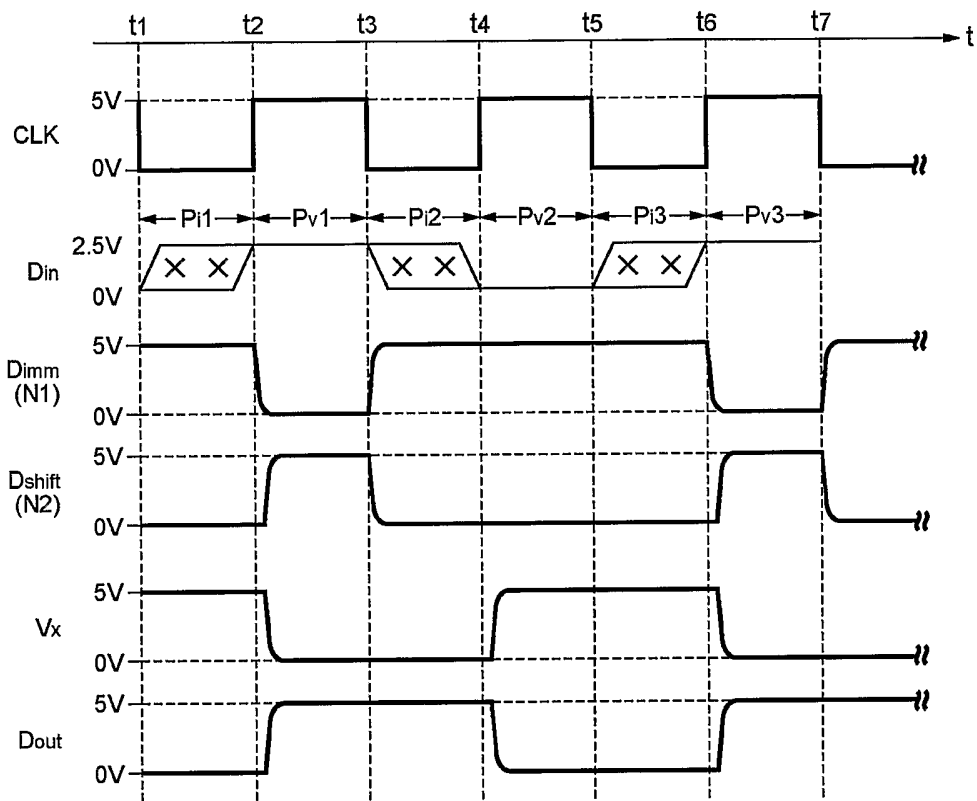
[Fig. 9]



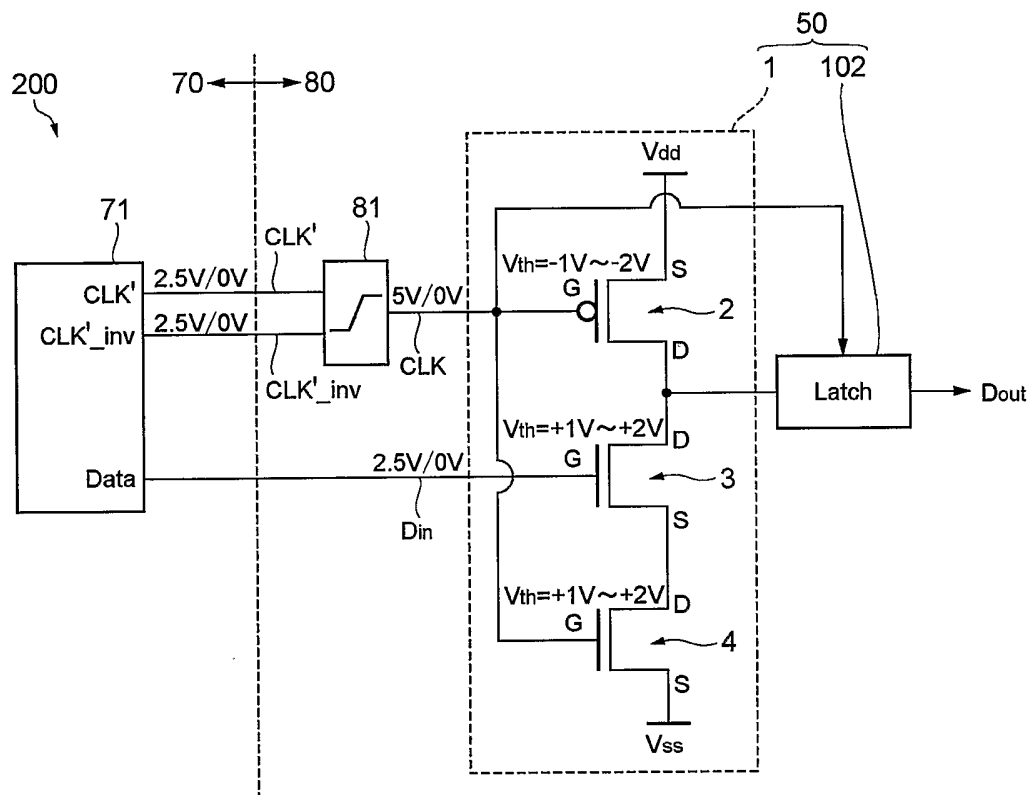
[Fig. 10]



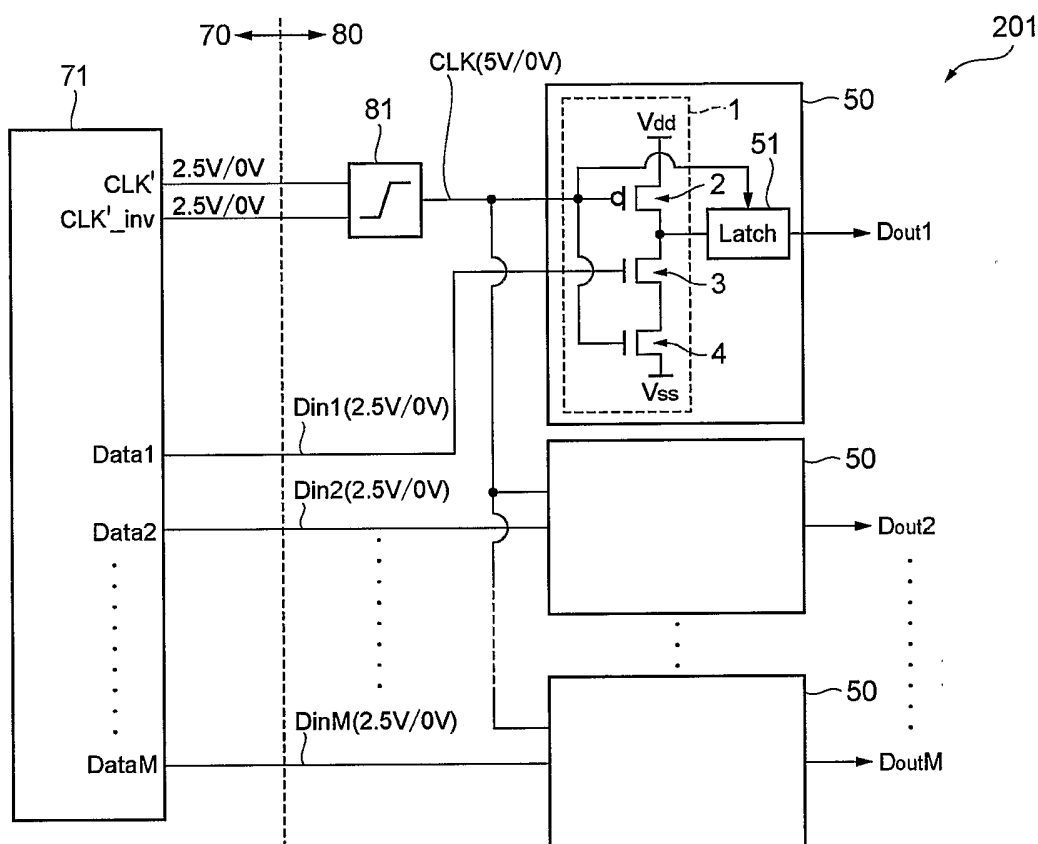
[Fig. 11]



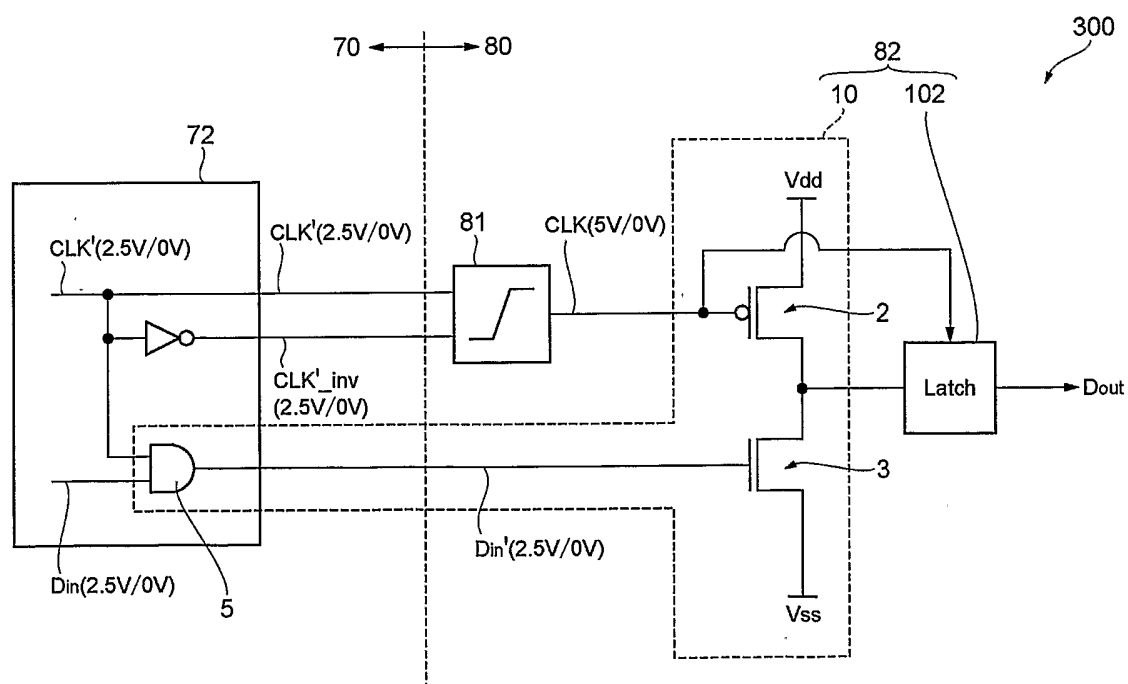
[Fig. 12]



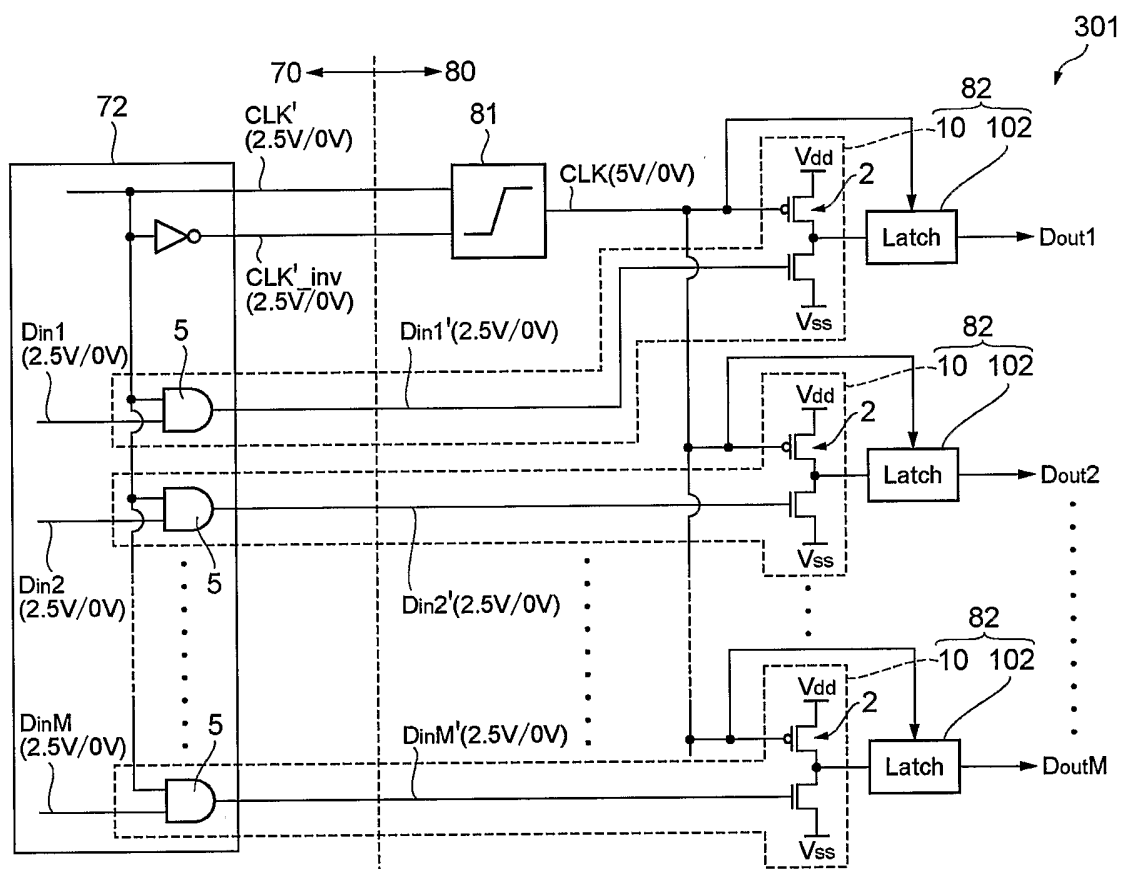
[Fig. 13]



[Fig. 14]



[Fig. 15]



INTERNATIONAL SEARCH REPORT

National Application No

T/IB2005/052843

A. CLASSIFICATION OF SUBJECT MATTER
H03K19/0185

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	MAHMOODI-MEIMAND H ET AL: "Dual-edge triggered level converting flip-flops" CIRCUITS AND SYSTEMS, 2004. ISCAS '04. PROCEEDINGS OF THE 2004 INTERNATIONAL SYMPOSIUM ON VANCOUVER, BC, CANADA 23-26 MAY 2004, PISCATAWAY, NJ, USA, IEEE, US, vol. 2, 23 May 2004 (2004-05-23), pages 661-664, XP010720423 ISBN: 0-7803-8251-X page 663, line 20 - line 40; figure 3	1-7, 11
X	US 6 545 519 B1 (CARBALLO JUAN-ANTONIO) 8 April 2003 (2003-04-08) figures 1,2	1-7, 11
X	US 3 976 984 A (HIRASAWA ET AL) 24 August 1976 (1976-08-24) column 12, line 25 - line 60; figure 26 ----- -/--	1-4, 8-11

☒ Further documents are listed in the continuation of box C.☒ Patent family members are listed in annex.

* Special categories of cited documents:

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
- *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
- *O* document referring to an oral disclosure, use, exhibition or other means
- *P* document published prior to the international filing date but later than the priority date claimed

T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

X document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

Y document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

G document member of the same patent family

Date of the actual completion of the international search

18 January 2006

Date of mailing of the international search report

26/01/2006

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

Santos, P

INTERNATIONAL SEARCH REPORT

International Application No

/IB2005/052843

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2004/041594 A1 (KANG SUNG-MO ET AL) 4 March 2004 (2004-03-04) figure 4	1-11
A	----- BECKWITH D: "A 3V-5V LEVEL SHIFTER" MOTOROLA TECHNICAL DEVELOPMENTS, MOTOROLA INC. SCHAUMBURG, ILLINOIS, US, vol. 32, September 1997 (1997-09), pages 202-203, XP000741187 ISSN: 0887-5286 the whole document -----	1-11

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

T/IB2005/052843

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6545519	B1	08-04-2003	NONE	
US 3976984	A	24-08-1976	CH 588787 A5 DE 2522341 A1 FR 2272536 A1 GB 1514964 A	15-06-1977 27-11-1975 19-12-1975 21-06-1978
US 2004041594	A1	04-03-2004	AU 2003268059 A1 CN 1679237 A EP 1537667 A2 WO 2004023240 A2	29-03-2004 05-10-2005 08-06-2005 18-03-2004