



(51) International Patent Classification:

H01L 29/786 (2006.01) H01L 29/417 (2006.01)
H01L 21/28 (2006.01) H01L 51/50 (2006.01)

(21) International Application Number:

PCT/IB2014/066146

(22) International Filing Date:

19 November 2014 (19.11.2014)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

2013-247402 29 November 2013 (29.11.2013) JP
2013-247404 29 November 2013 (29.11.2013) JP

(71) Applicant: SEMICONDUCTOR ENERGY LABORATORY CO., LTD. [JP/JP]; 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP).

(72) Inventors: NAKAZAWA, Yasutaka; c/o Semiconductor Energy Laboratory Co., LTD., 398, Hase, Atsugi-shi, Kanagawa 2430036 (JP). CHO, Takayuki. KOSHIOKA, Shunsuke. SATO, Takahiro. SAKAMOTO, Naoya. YAMAZAKI, Shunpei.

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, KE, KG, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

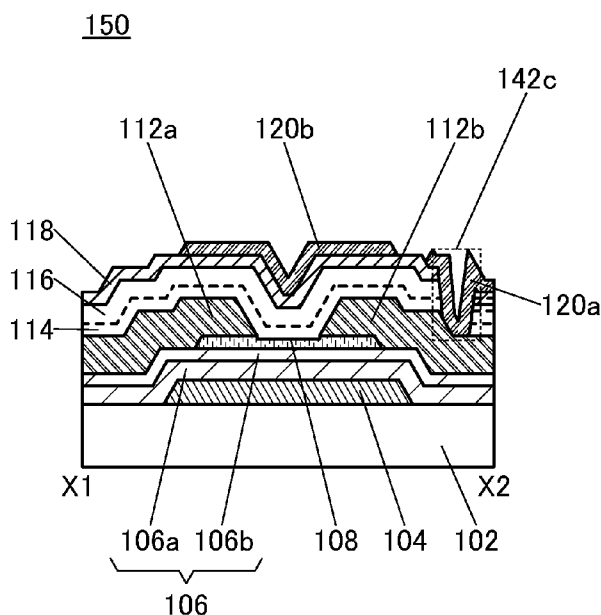
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— with international search report (Art. 21(3))

(54) Title: SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING THE SAME, AND DISPLAY DEVICE

FIG. 1C



(57) Abstract: A new semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film, and a method for manufacturing the semiconductor device are provided. The semiconductor device includes a transistor including a first gate electrode layer, a first gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the first gate insulating film to overlap the first gate electrode layer, a pair of electrode layers electrically connected to the oxide semiconductor film, a second gate insulating film over the oxide semiconductor film and the pair of electrode layers, and a second gate electrode layer that is over the second gate insulating film to overlap the oxide semiconductor film. The pair of electrode layers includes a Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti).

DESCRIPTION

**SEMICONDUCTOR DEVICE, METHOD FOR MANUFACTURING THE
SAME, AND DISPLAY DEVICE**

5

TECHNICAL FIELD

[0001]

One embodiment of the present invention relates to a semiconductor device including an oxide semiconductor and a display device including the semiconductor device. One embodiment of the present invention relates to a method for manufacturing a semiconductor device including an oxide semiconductor.

10

[0002]

Note that one embodiment of the present invention is not limited to the above technical field. The technical field of one embodiment of the invention disclosed in this specification and the like relates to an object, a method, or a manufacturing method. In addition, one embodiment of the present invention relates to a process, a machine, manufacture, or a composition of matter. Specifically, examples of the technical field of one embodiment of the present invention disclosed in this specification include a semiconductor device, a display device, a light-emitting device, a power storage device, a memory device, a method for driving any of them, and a method for manufacturing any of them.

15

20

[0003]

Note that in this specification, a semiconductor device refers to a semiconductor element itself or a device including a semiconductor element. As an example of such a semiconductor element, for example, a transistor (a thin film transistor and the like) can be given. In addition, a semiconductor device also refers to a display device such as an EL display device. In addition, a display device such as a liquid crystal panel or an organic EL panel includes a semiconductor device in some cases.

25

30

BACKGROUND ART

[0004]

Moreover, there is a trend in a display device using a transistor (e.g., a liquid crystal panel and an organic EL panel) toward a larger screen. As the screen size becomes larger, in the case of a display device using an active element such as a transistor, a voltage applied to an element varies depending on the position of a wiring which is connected to the element due to wiring resistance, which cause a problem of deterioration of display quality such as display unevenness and a defect in grayscale.

[0005]

Conventionally, an aluminum film has been widely used as a material used for the wiring, the signal line, or the like; moreover, research and development of using a copper (Cu) film as a material is extensively conducted to further reduce resistance. However, a Cu film is disadvantageous in that adhesion thereof to a base film is low and that characteristics of a transistor easily deteriorate due to diffusion of Cu in the Cu film into a semiconductor layer of the transistor. Note that a silicon-based semiconductor material is widely known as a material for a semiconductor thin film applicable to a transistor, and as another material, an oxide semiconductor has attracted attention (e.g., Patent Document 1).

[0006]

Furthermore, a Cu-Mn alloy is disclosed as a material for an ohmic electrode formed over a semiconductor layer including an oxide semiconductor material containing indium (see Patent Document 2).

[Reference]

[Patent Documents]

[0007]

[Patent Document 1] Japanese Published Patent Application No. 2007-123861

[Patent Document 2] PCT International Publication No. 2012/002573

DISCLOSURE OF INVENTION

[0008]

According to a structure disclosed in Patent Document 2, a Cu-Mn alloy film is deposited over an oxide semiconductor film, and then heat treatment is performed on the Cu-Mn alloy film to form an Mn oxide at the joint interface between the oxide semiconductor film and the Cu-Mn alloy film. The Mn oxide is formed in such a

manner that Mn in the Cu-Mn alloy film diffuses toward the oxide semiconductor film and is preferentially bonded to oxygen included in the oxide semiconductor film. A region of the oxide semiconductor film which is reduced by Mn becomes oxygen vacancy, so that the region has a high carrier density and thus has high conductivity.

5 Furthermore, Mn diffuses toward the oxide semiconductor film and thus the Cu-Mn alloy becomes pure Cu, whereby an ohmic electrode with a low electric resistance can be obtained.

[0009]

However, in the above structure, an influence of Cu that diffuses from the ohmic electrode after the ohmic electrode is formed is not considered. For example, after an electrode including a Cu-Mn alloy film is formed over an oxide semiconductor film, heat treatment is performed, whereby an Mn oxide is formed at the joint interface between the oxide semiconductor film and the Cu-Mn alloy film. Because of formation of the Mn oxide, even if the amount of Cu which can diffuse into the oxide semiconductor film from the Cu-Mn alloy film in contact with the oxide semiconductor film can be reduced, Cu which diffuses from a side surface of the Cu-Mn alloy film or a side surface or a surface of a pure Cu film obtained by release of Mn from the Cu-Mn alloy film is attached to the surface of the oxide semiconductor film.

10
15

[0010]

In the case where a bottom-gate structure is used for the transistor including an oxide semiconductor film, part of a surface of the oxide semiconductor film serves as what is called a back-channel side, and there is a problem in that the transistor characteristics obtained in a gate BT stress test, which is one kind of reliability test of a transistor, deteriorate when Cu is attached to the back-channel side.

20

25 [0011]

In the case where a copper film is used for a transistor including an oxide semiconductor film and for a wiring or a signal line connected to the transistor, to inhibit diffusion of copper from the copper film, a structure in which a barrier film is provided over and/or below the copper film can be used. However, when the barrier film is provided, there are problems in that the number of masks for forming the semiconductor device is increased and the manufacturing cost of the semiconductor device is increased.

30

[0012]

In view of the aforementioned problems, an object of one embodiment of the present invention is to provide a new semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film, and provide a method for manufacturing the semiconductor device. Another object of one embodiment of the present invention is to provide a semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film to reduce a manufacturing cost of the semiconductor device, and provide a method for manufacturing the semiconductor device. Another object of one embodiment of the present invention is to provide a semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film to improve the productivity of the semiconductor device, and provide a method for manufacturing the semiconductor device. Another object of one embodiment of the present invention is to provide a semiconductor device in which a transistor using an oxide semiconductor film includes a metal film containing Cu with a favorable shape. Another object of one embodiment of the present invention is to provide a new semiconductor device in which Cu is used for a wiring or a signal line connected to a transistor including an oxide semiconductor film, and provide a method for manufacturing the semiconductor device. Another object of one embodiment of the present invention is to provide a new semiconductor device and a method for manufacturing the new semiconductor device.

[0013]

Note that the descriptions of these objects do not disturb the existence of other objects. In one embodiment of the present invention, there is no need to achieve all the objects. Objects other than the above objects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

[0014]

One embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a first gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the first gate insulating film to overlap the first gate electrode layer, a pair of electrode layers electrically connected to the oxide semiconductor film, a second gate insulating film

over the oxide semiconductor film and the pair of electrode layers, and a second gate electrode layer that is over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers comprises a Cu-*X* alloy film, where *X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti.

5 [0015]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the gate insulating film to overlap the first gate electrode layer, a first insulating film over
10 the oxide semiconductor film, a pair of electrode layers electrically connected to the oxide semiconductor film through the first insulating film, a second insulating film over the first insulating film and the pair of electrode layers, and a second gate electrode layer that is provided over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers comprises a Cu-*X*
15 alloy film, where *X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti.

[0016]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a first gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided
20 over the first gate insulating film to overlap the first gate electrode layer, a pair of electrode layers electrically connected to the oxide semiconductor film, a second gate insulating film over the oxide semiconductor film and the pair of electrode layers, and a second gate electrode layer that is provided over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers
25 includes a Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); in the channel width direction of the transistor, the first gate electrode layer and the second gate electrode layer are connected through an opening provided in the first gate insulating film and the second gate insulating film, and surround the oxide semiconductor film with the first gate insulating film and the second gate insulating film provided between the oxide
30 semiconductor film and each of the first gate electrode layer and the second gate electrode layer.

[0017]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the gate insulating film to overlap the first gate electrode layer, a first insulating film over
5 the oxide semiconductor film, a pair of electrode layers electrically connected to the oxide semiconductor film through the first insulating film, a second insulating film over the first insulating film and the pair of electrode layers, and a second gate electrode layer that is provided over the second insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers includes a Cu-*X* alloy
10 film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); in the channel width direction of the transistor, the first gate electrode layer and the second gate electrode layer are connected through an opening provided in the gate insulating film, the first gate insulating film, and the second insulating film, and surround the oxide semiconductor film with the gate insulating film, the first insulating film, and the second insulating film provided
15 between the oxide semiconductor film and each of the first gate electrode layer and the second gate electrode layer.

[0018]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a first gate insulating
20 film over the first gate electrode layer, an oxide semiconductor film that is provided over the first gate insulating film to overlap the first gate electrode layer, a metal oxide film over the oxide semiconductor film, a pair of electrode layers electrically connected to the oxide semiconductor film through the metal oxide film, a second gate insulating film over the metal oxide film and the pair of electrode layers, and a second gate
25 electrode layer that is provided over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers includes a Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti).

[0019]

Another embodiment of the present invention is a semiconductor device
30 including a transistor which includes a first gate electrode layer, a gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the gate insulating film to overlap the first gate electrode layer, a metal oxide film over the

oxide semiconductor film, a first insulating film over the metal oxide film, a pair of electrode layers electrically connected to the oxide semiconductor film through the metal oxide film and the first insulating film, a second insulating film over the first insulating film and the pair of electrode layers, and a second gate electrode layer that is provided over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers includes a Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti).

[0020]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a first gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the first gate insulating film to overlap the first gate electrode layer, a metal oxide film over the oxide semiconductor film, a pair of electrode layers electrically connected to the oxide semiconductor film through the metal oxide film, a second gate insulating film over the metal oxide film and the pair of electrode layers, and a second gate electrode layer that is provided over the second gate insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers includes a Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); in the channel width direction of the transistor, the first gate electrode layer and the second gate electrode layer are connected through an opening provided in the first gate insulating film and the second gate insulating film, and surround the oxide semiconductor film with the first gate insulating film and the second gate insulating film provided between the oxide semiconductor film and each of the first gate electrode layer and the second gate electrode layer.

[0021]

Another embodiment of the present invention is a semiconductor device including a transistor which includes a first gate electrode layer, a gate insulating film over the first gate electrode layer, an oxide semiconductor film that is provided over the gate insulating film to overlap the first gate electrode layer, a metal oxide film over the oxide semiconductor film, a first insulating film over the metal oxide film, a pair of electrode layers electrically connected to the oxide semiconductor film through the metal oxide film and the first insulating film, a second insulating film over the first insulating film and the pair of electrode layers, and a second gate electrode layer that is

provided over the second insulating film to overlap the oxide semiconductor film. In this structure, the pair of electrode layers includes a Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); in the channel width direction of the transistor, the first gate electrode layer and the second gate electrode layer are connected through an opening provided in the gate insulating film, the first gate insulating film, and the second insulating film, and surround the oxide semiconductor film with the gate insulating film, the first insulating film, and the second insulating film provided between the oxide semiconductor film and each of the first gate electrode layer and the second gate electrode layer.

[0022]

In any of the structures, the pair of electrode layers preferably includes a Cu-Mn alloy film. In any of the structures, the pair of electrode layers preferably includes a Cu-Mn alloy film and a Cu film over the Cu-Mn alloy film. In any of the structures, the pair of electrode layers preferably includes a first Cu-Mn alloy film, a Cu film over the first Cu-Mn alloy film, and a second Cu-Mn alloy film over the Cu film. In any of the structures, it is preferable that the pair of electrode layers partly include an Mn oxide. In any of the structures, at least one of top surfaces, bottom surfaces, and side surfaces of the pair of electrode layers is preferably covered with an Mn oxide. Alternatively, in any of the structures, the top surfaces, the bottom surfaces, and the side surfaces of the pair of electrode layers are preferably covered with an Mn oxide.

[0023]

In any of the structures, the oxide semiconductor film is preferably an In-*M*-Zn oxide (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). In any of the structures, it is preferable that the oxide semiconductor film include a crystal part, and that a c-axis of the crystal part be aligned parallel to a normal vector of a surface where the oxide semiconductor film is formed.

[0024]

In any of the structures, the metal oxide film is preferably an In-*M*-Zn oxide or an In-*M* oxide (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). In any of the structures, it is preferable that the metal oxide film include a crystal part, and that a c-axis of the crystal part be aligned parallel to a normal vector of a surface where the metal oxide film is formed. In any of the structures, the energy level of the bottom of the conduction band

of the metal oxide film be closer to the vacuum level than that of the oxide semiconductor film is.

[0025]

Another embodiment of the present invention is a display device including the semiconductor device having any of the above structures.

[0026]

Another embodiment of the present invention is a method for manufacturing a semiconductor device, including the steps of: forming a first conductive film over a substrate; processing the first conductive film using a first chemical solution to form a gate electrode layer; forming a first insulating film over the gate electrode layer; forming an oxide semiconductor film over the first insulating film; processing the oxide semiconductor film using a second chemical solution to form an island-shaped oxide semiconductor film; forming a second conductive film over the first insulating film and the island-shaped oxide semiconductor film; processing the second conductive film using a third chemical solution including the same chemical solution as the first chemical solution to form a source electrode layer and a drain electrode layer; forming a second insulating film over the island-shaped oxide semiconductor film, the source electrode layer, and the drain electrode layer; processing the second insulating film to form an opening reaching the drain electrode layer; forming a third conductive film over the second insulating film to cover the opening; and processing the third conductive film using a fourth chemical solution including the same chemical solution as the second chemical solution to form a pixel electrode layer.

[0027]

Another embodiment of the present invention is a method for manufacturing a semiconductor device, including the steps of: forming a first conductive film over a substrate; processing the first conductive film using a first chemical solution to form a gate electrode layer; forming a first insulating film over the gate electrode layer; forming an oxide semiconductor film over the first insulating film; processing the oxide semiconductor film using a second chemical solution to form an island-shaped oxide semiconductor film; forming a second conductive film over the first insulating film and the island-shaped oxide semiconductor film; processing the second conductive film using a third chemical solution including the same chemical solution as the first

chemical solution to form a source electrode layer and a drain electrode layer; forming a second insulating film over the island-shaped oxide semiconductor film, the source electrode layer, and the drain electrode layer; processing the second insulating film to form a first opening reaching the drain electrode layer; processing the first insulating film and the second insulating film to form a second opening reaching the gate electrode layer; forming a third conductive film over the second insulating film to cover the first opening and the second opening; and processing the third conductive film using a fourth chemical solution including the same chemical solution as the second chemical solution to form a pixel electrode layer and a second gate electrode layer.

10 [0028]

Another embodiment of the present invention is a method for manufacturing a semiconductor device, including the steps of: forming a first conductive film over a substrate; processing the first conductive film using a first chemical solution to form a gate electrode layer; forming a first insulating film over the gate electrode layer; forming a stacked-layer oxide film over the first insulating film; processing the stacked-layer oxide film using a second chemical solution to form an island-shaped stacked-layer oxide film; forming a second conductive film over the first insulating film and the island-shaped stacked-layer oxide film; processing the second conductive film using a third chemical solution including the same chemical solution as the first chemical solution to form a source electrode layer and a drain electrode layer; forming a second insulating film over the island-shaped stacked-layer oxide film, the source electrode layer, and the drain electrode layer; processing the second insulating film to form an opening reaching the drain electrode layer; forming a third conductive film over the second insulating film to cover the opening; and processing the third conductive film using a fourth chemical solution including the same chemical solution as the second chemical solution to form a pixel electrode layer.

25 [0029]

Another embodiment of the present invention is a method for manufacturing a semiconductor device, including the steps of: forming a first conductive film over a substrate; processing the first conductive film using a first chemical solution to form a gate electrode layer; forming a first insulating film over the gate electrode layer; forming a stacked-layer oxide film over the first insulating film; processing the

stacked-layer oxide film using a second chemical solution to form an island-shaped stacked-layer oxide film; forming a second conductive film over the first insulating film and the island-shaped stacked-layer oxide film; processing the second conductive film using a third chemical solution including the chemical solution as the first chemical solution to form a source electrode layer and a drain electrode layer; forming a second insulating film over the island-shaped stacked-layer oxide film, the source electrode layer, and the drain electrode layer; processing the second insulating film to form a first opening reaching the drain electrode layer; processing the first insulating film and the second insulating film to form a second opening reaching the gate electrode layer; forming a third conductive film over the second insulating film to cover the first opening and the second opening; and processing the third conductive film using a fourth chemical solution including the same chemical solution as the second chemical solution to form a pixel electrode layer and a second gate electrode layer.

[0030]

In any of the above structures, the stacked-layer oxide film preferably includes an oxide semiconductor film and a metal oxide film. In any of the above structures, the oxide semiconductor film is preferably an In-M-Zn oxide (M is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). In any of the above structures, it is preferable that the oxide semiconductor film include a crystal part, and that a c-axis of the crystal part be aligned parallel to a normal vector of a surface where the oxide semiconductor film is formed. In any of the above structures, the metal oxide film is preferably an In-M-Zn oxide (M is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). In any of the above structures, it is preferable that the metal oxide film include a crystal part, and that a c-axis of the crystal part be aligned parallel to a normal vector of a surface where the metal oxide film is formed.

[0031]

In any of the above structure, one or both of the first conductive film and the second conductive film preferably include a Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti). In any of the above structure, it is preferable that one or both of the first conductive film and the second conductive film partly include an Mn oxide.

[0032]

In any of the above structure, the first and third chemical solutions each preferably contain an organic acid solution and a hydrogen peroxide solution. In any

of the above structure, the second and fourth chemical solutions each preferably contain oxalic acid.

[0033]

5 In any of the above structure, the second insulating film is preferably processed using a fifth chemical solution. Furthermore, the fifth chemical solution preferably contains one or both of ammonium hydrogen fluoride and ammonium fluoride.

[0034]

10 A semiconductor device, a display device, and an electronic appliance formed by any of the methods for manufacturing a semiconductor device are also embodiments of the present invention.

[0035]

15 According to one embodiment of the present invention, a new semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film can be provided. According to one embodiment of the present invention, a method for manufacturing the semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film can be provided. According to one embodiment of the present invention, a method for manufacturing a semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film to reduce a manufacturing cost of the semiconductor device can be provided. According to one embodiment of the present invention, a method for manufacturing a semiconductor device in which a metal film containing Cu is used for a transistor including an oxide semiconductor film to improve the productivity of the semiconductor device can be provided. According to one embodiment of the present invention, a semiconductor device in which a transistor including an oxide semiconductor film includes a metal film containing Cu with a favorable shape, and a method for manufacturing the semiconductor device can be provided. According to one embodiment of the present invention, a new semiconductor device with high productivity can be provided. According to one embodiment of the present invention, a new semiconductor device and a method for manufacturing the new semiconductor device can be provided.

20

25

30

[0036]

Note that the description of these effects does not disturb the existence of other

effects. One embodiment of the present invention does not necessarily achieve all the objects listed above. Other effects will be apparent from and can be derived from the description of the specification, the drawings, the claims, and the like.

BRIEF DESCRIPTION OF DRAWINGS

5 [0037]

FIG. 1A is a top view of a semiconductor device, and FIGS. 1B and 1C are cross-sectional views thereof.

FIGS. 2A and 2B are cross-sectional views of a semiconductor device.

10 FIG. 3A is a top view of a semiconductor device, and FIGS. 3B and 3C are cross-sectional views thereof.

FIG. 4 is a cross-sectional view of a semiconductor device.

FIG. 5A is a top view of a semiconductor device, and FIGS. 5B and 5C are cross-sectional views thereof.

15 FIG. 6A is a top view of a semiconductor device, and FIGS. 6B and 6C are cross-sectional views thereof.

FIGS. 7A and 7B are cross-sectional views of semiconductor devices.

FIG. 8A is a top view of a semiconductor device, and FIGS. 8B and 8C are cross-sectional views thereof.

20 FIG. 9A is a top view of a semiconductor device, and FIGS. 9B and 9C are cross-sectional views thereof.

FIGS. 10A and 10B each illustrate an energy band of a stacked-layer film.

FIGS. 11A and 11B are cross-sectional views of semiconductor devices.

FIGS. 12A and 12B are cross-sectional views of semiconductor devices.

25 FIGS. 13A to 13D are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 14A to 14C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 15A to 15C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

30 FIGS. 16A to 16D are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 17A to 17C are cross-sectional views illustrating a method for

manufacturing a semiconductor device.

FIGS. 18A and 18B are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIG. 19A is a top view of a semiconductor device, and FIGS. 19B and 19C are cross-sectional views thereof.

FIGS. 20A and 20B are cross-sectional views of semiconductor devices.

FIGS. 21A and 21B are cross-sectional views of semiconductor devices.

FIGS. 22A to 22C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 23A to 23C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 24A to 24C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 25A to 25C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 26A to 26C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 27A and 27B are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 28A to 28C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 29A and 29B are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIG. 30A is a top view of a semiconductor device, and FIGS. 30B and 30C are cross-sectional views thereof.

FIG. 31A is a top view of a semiconductor device, and FIGS. 31B and 31C are cross-sectional views thereof.

FIGS. 32A to 32C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 33A and 33B are cross-sectional views of semiconductor devices.

FIGS. 34A and 34B are cross-sectional views of semiconductor devices.

FIGS. 35A to 35C are cross-sectional views illustrating a method for

manufacturing a semiconductor device.

FIGS. 36A to 36C are cross-sectional views illustrating a method for manufacturing a semiconductor device.

FIGS. 37A to 37D are Cs-corrected high-resolution TEM images of a cross
5 section of a CAAC-OS and a cross-sectional schematic view of a CAAC-OS.

FIGS. 38A to 38D are Cs-corrected high-resolution TEM images of a plane of a CAAC-OS.

FIGS. 39A to 39C show structural analysis of a CAAC-OS and a single crystal oxide semiconductor by XRD.

10 FIGS. 40A and 40B show electron diffraction patterns of a CAAC-OS.

FIG. 41 shows a change in crystal part of an In-Ga-Zn oxide induced by electron irradiation.

FIGS. 42A and 42B are schematic views showing deposition models of a CAAC-OS and an nc-OS.

15 FIGS. 43A to 43C illustrate an InGaZnO₄ crystal and a pellet.

FIGS. 44A to 44D are schematic views showing a deposition model of a CAAC-OS.

FIGS. 45A and 45B are top views of display devices.

FIG. 46 is a cross-sectional view of a display device.

20 FIG. 47 is a cross-sectional view of a display device.

FIG. 48 is a cross-sectional view of a display device.

FIG. 49 is a cross-sectional view of a display device.

FIGS. 50A to 50D are cross-sectional views illustrating a method for manufacturing a display device.

25 FIGS. 51A and 51B are cross-sectional views illustrating a method for manufacturing a display device.

FIGS. 52A to 52D are cross-sectional views illustrating a method for manufacturing a display device.

FIG. 53 is a cross-sectional view of a display device.

30 FIG. 54 is a cross-sectional view of a display device.

FIGS. 55A to 55C are a block diagram and circuit diagrams illustrating a display device.

FIG. 56 illustrates a display module.

FIGS. 57A to 57H illustrate electronic appliances.

FIG. 58 is a cross-sectional STEM image in an example.

FIG. 59 shows EDX analysis results of conductive films in an example.

5 FIG. 60 is a cross-sectional view illustrating a sample structure in an example.

FIG. 61 shows XPS analysis results of a conductive film in an example.

BEST MODE FOR CARRYING OUT THE INVENTION

[0038]

10 Hereinafter, embodiments will be described with reference to drawings. However, the embodiments can be implemented with various modes. It will be readily appreciated by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Thus, the present invention should not be interpreted as being limited to the following description
15 of the embodiments.

[0039]

In the drawings, the size, the layer thickness, or the region is exaggerated for clarity in some cases. Therefore, embodiments of the present invention are not limited to such a scale. Note that the drawings are schematic views showing ideal examples,
20 and embodiments of the present invention are not limited to shapes or values shown in the drawings.

[0040]

Note that the ordinal numbers such as “first” and “second” in this specification and the like are used for convenience and do not denote the order of steps or the
25 stacking order of layers. Therefore, for example, description can be made even when “first” is replaced with “second” or “third”, as appropriate. In addition, the ordinal numbers in this specification and the like are not necessarily the same as those which specify one embodiment of the present invention.

[0041]

30 Note that in this specification, terms for describing arrangement, such as “over” “above”, “under”, and “below”, are used for convenience in describing a positional relation between components with reference to drawings. Further, the positional

relation between components is changed as appropriate in accordance with a direction in which each component is described. Thus, there is no limitation on terms used in this specification, and description can be made appropriately depending on the situation.

[0042]

5 In this specification and the like, a transistor is an element having at least three terminals of a gate, a drain, and a source. In addition, the transistor has a channel region between a drain (a drain terminal, a drain region, or a drain electrode layer) and a source (a source terminal, a source region, or a source electrode layer), and current can flow through the drain, the channel region, and the source. Note that in this
10 specification and the like, a channel region refers to a region through which current mainly flows.

[0043]

Further, functions of a source and a drain might be switched when transistors having different polarities are employed or a direction of current flow is changed in
15 circuit operation, for example. Therefore, the terms “source” and “drain” can be switched in this specification and the like.

[0044]

Note that in this specification and the like, the expression “electrically connected” includes the case where components are connected through an “object
20 having any electric function”. There is no particular limitation on an “object having any electric function” as long as electric signals can be transmitted and received between components that are connected through the object. Examples of an “object having any electric function” are a switching element such as a transistor, a resistor, an inductor, a capacitor, and elements with a variety of functions as well as an electrode
25 and a wiring.

[0045]

Note that in this specification, a silicon oxynitride film refers to a film that contains oxygen at a higher proportion than nitrogen, and a silicon nitride oxide film refers to a film that contains nitrogen at a higher proportion than oxygen.

30 [0046]

In this specification, the term “parallel” indicates that the angle formed between two straight lines is greater than or equal to -10° and less than or equal to 10° ,

and accordingly also includes the case where the angle is greater than or equal to -5° and less than or equal to 5° . A term “substantially parallel” indicates that the angle formed between two straight lines is greater than or equal to -30° and less than or equal to 30° . In addition, a term “perpendicular” indicates that the angle formed between two straight lines is greater than or equal to 80° and less than or equal to 100° , and accordingly includes the case where the angle is greater than or equal to 85° and less than or equal to 95° . A term “substantially perpendicular” indicates that the angle formed between two straight lines is greater than or equal to 60° and less than or equal to 120° .

[0047]
(Embodiment 1)

In this embodiment, a semiconductor device of one embodiment of the present invention is described with reference to FIGS. 1A to 1C, FIGS. 2A and 2B, FIGS. 3A to 3C, FIG. 4, FIGS. 5A to 5C, FIGS. 6A to 6C, FIGS. 7A and 7B, FIGS. 8A to 8C, FIGS. 9A to 9C, FIGS. 10A and 10B, FIGS. 11A and 11B, FIGS. 12A and 12B, FIGS. 13A to 13D, FIGS. 14A to 14C, FIGS. 15A to 15C, FIGS. 16A to 16D, FIGS. 17A to 17C, and FIGS. 18A and 18B.

[0048]

<Structure example 1 of semiconductor device>

FIG. 1A is a top view of a transistor 150 that is a semiconductor device of one embodiment of the present invention. FIG. 1B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 1A. FIG. 1C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 1A. Note that in FIG. 1A, some components of the transistor 150 (a gate insulating film and the like) are not illustrated for simplification. In a manner similar to that of the transistor 150, some components are not illustrated in some cases in top views of transistors described below. Furthermore, the direction of the dashed dotted line X1-X1 may be called a channel length direction, and the direction of the dashed dotted line Y1-Y2 may be called a channel width direction.

[0049]

The transistor 150 includes a conductive film 104 functioning as a gate electrode layer over a substrate 102; an insulating film 106 functioning as a gate

insulating film over the substrate 102 and the conductive film 104; an oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; a pair of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108; insulating films 114, 116, and 118 over the pair of electrode layers 112a and 112b and the oxide semiconductor film 108; and conductive films 120a and 120b over the insulating film 118.

[0050]

The conductive film 120a is connected to the electrode layer 112b through an opening 142c provided in the insulating films 114, 116, and 118. The conductive film 120b is formed over the insulating film 118 to overlap the oxide semiconductor film 108.

[0051]

The insulating film 106 functioning as a gate insulating film in the transistor 150 has a two-layer structure of an insulating film 106a and an insulating film 106b. Note that the structure of the insulating film 106 is not limited thereto, and for example, the insulating film 106 may have a single-layer structure or a stacked-layer structure of three or more layers. Also in the transistors described below, the insulating film 106 functioning as a gate insulating film can have a structure similar to that of the gate insulating film of the transistor 150.

[0052]

The insulating films 114, 116, and 118 in the transistor 150 function as second gate insulating films of the transistor 150. The conductive film 120a in the transistor 150 functions as, for example, a pixel electrode layer used for a display device. The conductive film 120b in the transistor 150 functions as a second gate electrode layer (also referred to as a back gate electrode layer).

[0053]

The pair of electrode layers 112a and 112b in the transistor 150 functions as a source electrode layer and a drain electrode layer. Note that the pair of electrode layers 112a and 112b includes at least a Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); for example, it is preferable that the pair of electrode layers 112a and 112b have a single-layer structure of a Cu-X alloy film or a stacked-layer structure of a Cu-X alloy film and a conductive film containing a low-resistance material such as copper

(Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a compound containing any of these materials as a main component.

[0054]

The pair of electrode layers 112a and 112b also functions as lead wirings or the like. Therefore, the pair of electrode layers 112a and 112b is formed to include a Cu-*X* alloy film, or a Cu-*X* alloy film and a conductive film containing a low-resistance material such as copper, aluminum, gold, or silver, whereby a semiconductor device with reduced wiring delay can be manufactured even when a large-sized substrate is used as the substrate 102.

[0055]

In addition, a Cu-*X* alloy film is used for the pair of electrode layers 112a and 112b in contact with the oxide semiconductor film 108, whereby *X* in the Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) might form an oxide film of *X* at the interface between the Cu-*X* alloy film and the oxide semiconductor film. The oxide film can inhibit Cu in the Cu-*X* alloy film from entering the oxide semiconductor film 108.

[0056]

For example, as the Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) used for the pair of electrode layers 112a and 112b, a Cu-Mn alloy film can be selected.

When the Cu-Mn alloy film is used for the pair of electrode layers 112a and 112b, a coating film containing Mn is formed at the interface with a base film (here, the insulating film 106b and the oxide semiconductor film 108), which can improve adhesion. Furthermore, the use of the Cu-Mn alloy film enables a favorable ohmic contact with the oxide semiconductor film 108.

[0057]

Here, FIGS. 2A and 2B are enlarged cross-sectional views of some components in the semiconductor device illustrated in FIGS. 1A to 1C.

[0058]

FIG. 2A is a cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the pair of electrode layers 112a and 112b, the insulating films 114, 116, and 118, and the conductive film 120b that are included in the transistor 150.

[0059]

As illustrated in FIG. 2A, coating films 113a and 113b might be formed at the interfaces between the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b, the interfaces between the insulating film 106b and the pair of electrode layers 112a and 112b, and the interfaces between the insulating film 114 and the pair of electrode layers 112a and 112b.

[0060]

For example, in the case where the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b are heated in the state where they are in contact with each other, the coating films 113a and 113b can be formed in the vicinity of the interface with the oxide semiconductor film 108 in such a manner that Mn in the Cu-Mn alloy film used for the pair of electrode layers 112a and 112b is segregated. Note that the coating films 113a and 113b are formed of, for example, Mn oxide, In-Mn oxide, Ga-Mn oxide, In-Ga-Mn oxide, or In-Ga-Zn-Mn oxide which can be formed by a reaction with a constituent element in the oxide semiconductor film 108.

[0061]

For example, in the case where the insulating films 106b and 114 and the pair of electrode layers 112a and 112b are heated in the state where they are in contact with each other, the coating films 113a and 113b can be formed in the vicinities of the interfaces between the insulating film 106b and the pair of electrode layers 112a and 112b and in the vicinities of the interfaces between the insulating film 114 and the pair of electrode layers 112a and 112b in such a manner that Mn in the Cu-Mn alloy film used for the pair of electrode layers 112a and 112b is segregated. Note that in addition to the above oxides, the coating films 113a and 113b can be formed of, for example, Mn hydride, Mn carbide, Mn oxide, Mn nitride, or Mn silicide when the insulating films 106b and 114 contain hydrogen, carbon, oxygen, nitrogen, silicon, or the like.

[0062]

The above structure of the pair of electrode layers 112a and 112b inhibits a Cu from entering the oxide semiconductor film 108 and enables the semiconductor device to have a conductive film with high conductivity.

[0063]

Next, details of the pair of electrode layers 112a and 112b are described below with reference to FIG. 2B. Note that FIG. 2B is a cross-sectional view taken along

dashed dotted line A-B in FIG. 1A.

[0064]

As illustrated in FIG. 2B, the coating film 113a might be formed at the interface between the insulating film 106b and the pair of electrode layers 112a and 112b, the interface between the insulating film 114 and the pair of electrode layers 112a and 112b (the electrode layer 112a in FIG. 2B). As illustrated in FIG. 2B, the periphery (the top surface, the bottom surface, and the side surface) of the electrode layer 112a is covered with the coating film 113a. In other words, at least one of the top surfaces, the bottom surfaces, and the side surfaces of the pair of electrode layers 112a and 112b is covered with the coating film 113a or 113b.

[0065]

For example, in the case where a single-layer film of a Cu-Mn alloy film or a stacked-layer film of a first Cu-Mn alloy film, a Cu film, and a second Cu-Mn alloy film is used for the pair of electrode layers 112a and 112b, an Mn oxide can be formed as the coating film 113a. The structure in which the Mn oxide covers the pair of electrode layers 112a and 112b can inhibit Cu in the Cu-Mn alloy film or Cu in the Cu film from diffusing to the outside. Therefore, a new semiconductor device in which Cu can be inhibited from entering the oxide semiconductor film 108 can be achieved. Note that in the case where a Cu-Mn alloy film is used for the pair of electrode layers 112a and 112b, at least part of the pair of electrode layers 112a and 112b includes Mn oxide.

[0066]

An In-Ga oxide, an In-Zn oxide, an In-*M*-Zn oxide (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf) can be used for the oxide semiconductor film 108. In addition, it is preferable that the oxide semiconductor film 108 include a crystal part and that the c-axis of the crystal part be aligned in a direction parallel to a normal vector of a surface where the oxide semiconductor film 108 is formed. When the oxide semiconductor film 108 includes a crystal part, Cu contained in the pair of electrode layers 112a and 112b can be further inhibited from entering the oxide semiconductor film 108. Note that it is preferable that a c-axis aligned crystalline oxide semiconductor (CAAC-OS) described later be used for the oxide semiconductor film 108 including a crystal part.

[0067]

The conductive film 120b is connected to the conductive film 104 functioning as a gate electrode layer through openings 142a and 142b provided in the insulating films 106a, 106b, 114, 116, and 118. Therefore, the same potential is applied to the conductive film 120b and the conductive film 104.

5 [0068]

As illustrated in the cross-sectional view of FIG. 1B, the oxide semiconductor film 108 is positioned to face each of the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a second gate electrode layer, and is sandwiched between the two conductive layers functioning as gate electrode layers. The lengths in the channel length direction and the channel width direction of the conductive film 120b functioning as a second gate electrode layer are longer than those in the channel length direction and the channel width direction of the oxide semiconductor film 108. The whole oxide semiconductor film 108 is covered with the conductive film 120b with the insulating films 114, 116, and 118 positioned therebetween. Since the conductive film 120b functioning as a second gate electrode layer is connected to the conductive film 104 functioning as a gate electrode layer through the opening 142a and 142b provided in the insulating films 106a, 106b, 114, 116, and 118, a side surface of the oxide semiconductor film 108 in the channel width direction faces the conductive film 120b functioning as a second gate electrode layer with the insulating films 114, 116, and 118 positioned therebetween.

[0069]

In other words, in the channel width direction of the transistor 150, the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a second gate electrode layer are connected to each other through the openings provided in the insulating film 106 functioning as a gate insulating film and the insulating films 114, 116, and 118 functioning as a gate insulating film; and the conductive film 104 and the conductive film 120b surround the oxide semiconductor film 108 with the insulating film 106 functioning as a gate insulating film and the insulating films 114, 116, and 118 functioning as a gate insulating film positioned therebetween.

[0070]

Such a structure makes it possible that the oxide semiconductor film 108

included in the transistor 150 is electrically surrounded by electric fields of the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a second gate electrode layer. A device structure of a transistor, like that of the transistor 150, in which electric fields of a gate electrode layer and a second gate electrode layer electrically surround an oxide semiconductor film where a channel region is formed can be referred to as a surrounded channel (s-channel) structure.

[0071]

Since the transistor 150 has the s-channel structure, an electric field for inducing a channel can be effectively applied to the oxide semiconductor film 108 by the conductive film 104 functioning as a gate electrode layer; therefore, the current drive capability of the transistor 150 can be improved and high on-state current characteristics can be obtained. Since the on-state current can be increased, it is possible to reduce the size of the transistor 150. In addition, since the transistor 150 is surrounded by the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a second gate electrode layer, the mechanical strength of the transistor 150 can be increased.

[0072]

Note that in the transistor 150, one of the openings 142a and 142b may be provided, and the conductive film 120b and the conductive film 104 may be connected through the opening.

[0073]

As described above, in the semiconductor device of one embodiment of the present invention, a Cu-X alloy film is used for the pair of electrode layers used as a source electrode layer and a drain electrode layer of the transistor. Furthermore, the transistor has an s-channel structure. Therefore, it is possible to obtain a new semiconductor device having reduced wiring delay and high current drive capability of a transistor.

[0074]

Other constituent elements of the semiconductor device of this embodiment are described below in detail.

[0075]

<Substrate>

There is no particular limitation on the property of a material and the like of the substrate 102 as long as the material has heat resistance enough to withstand at least heat treatment to be performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, a sapphire substrate, or the like may be used as the substrate 102. Alternatively, a single crystal semiconductor substrate or a polycrystalline semiconductor substrate made of silicon, silicon carbide, or the like, a compound semiconductor substrate made of silicon germanium or the like, an SOI substrate, or the like may be used as the substrate 102. Still alternatively, any of these substrates provided with a semiconductor element may be used as the substrate 102.

In the case where a glass substrate is used as the substrate 102, a glass substrate having any of the following sizes can be used: the 6th generation (1500 mm × 1850 mm), the 7th generation (1870 mm × 2200 mm), the 8th generation (2200 mm × 2400 mm), the 9th generation (2400 mm × 2800 mm), and the 10th generation (2950 mm × 3400 mm). Thus, a large-sized display device can be manufactured.

[0076]

Still further alternatively, a flexible substrate may be used as the substrate 102, and the transistor 150 may be provided directly on the flexible substrate. Further alternatively, a separation layer may be provided between the substrate 102 and the transistor 150. The separation layer can be used when part or the whole of a semiconductor device formed over the separation layer is separated from the substrate 102 and transferred to another substrate. In such a case, the transistor 150 can be transferred to a substrate having low heat resistance or a flexible substrate as well.

[0077]

<Conductive film>

The conductive film 104 functioning as a gate electrode layer can be formed using a metal element selected from chromium (Cr), copper (Cu), aluminum (Al), gold (Au), silver (Ag), zinc (Zn), molybdenum (Mo), tantalum (Ta), titanium (Ti), tungsten (W), manganese (Mn), nickel (Ni), iron (Fe), and cobalt (Co); an alloy containing any of these metal element as its component; an alloy containing a combination of any of these elements; or the like. The conductive film 104 may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of

an aluminum film containing silicon, a two-layer structure in which a titanium film is stacked over an aluminum film, a two-layer structure in which a titanium film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a titanium nitride film, a two-layer structure in which a tungsten film is stacked over a tantalum nitride film or a tungsten nitride film, a three-layer structure in which a titanium film, an aluminum film, and a titanium film are stacked in this order, and the like can be given. Alternatively, an alloy film or a nitride film which contains aluminum and one or more elements selected from titanium, tantalum, tungsten, molybdenum, chromium, neodymium, and scandium may be used.

[0078]

The conductive film 104 can be formed using a light-transmitting conductive material such as indium tin oxide, indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium zinc oxide, or indium tin oxide to which silicon oxide is added. It is also possible to have a stacked-layer structure formed using the above light-transmitting conductive material and the above metal element.

[0079]

The Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) included in the pair of electrode layers 112a and 112b may be used for the conductive film 104. The use of the Cu-*X* alloy film enables the manufacturing cost to be reduced because wet etching process can be used in the processing. Alternatively, the conductive film 104 can be formed using a Cu-*X* alloy film and a film containing a metal element selected from chromium (Cr), copper (Cu), aluminum (Al), gold (Au), silver (Ag), zinc (Zn), molybdenum (Mo), tantalum (Ta), titanium (Ti), tungsten (W), manganese (Mn), nickel (Ni), iron (Fe), and cobalt (Co); an alloy film containing any of these metal element as its main component; or an alloy film containing a combination of any of these elements.

[0080]

The conductive film 104 functioning as a gate electrode layer may have a single-layer structure or a stacked-layer structure of two or more layers. For example, a single-layer structure of a Cu-Mn alloy film, a two-layer structure in which a Cu film is stacked over a Cu-Mn alloy film, a three-layer structure in which a Cu film is stacked over a Cu-Mn alloy film and a Cu-Mn alloy film is stacked over the Cu film, or the like

can be used.

[0081]

Furthermore, an In-Ga-Zn-based oxynitride semiconductor film, an In-Sn-based oxynitride semiconductor film, an In-Ga-based oxynitride semiconductor film, an In-Zn-based oxynitride semiconductor film, a Sn-based oxynitride semiconductor film, an In-based oxynitride semiconductor film, or a film of a metal nitride (e.g., InN or ZnN), or the like may be provided between the conductive film 104 and the insulating film 106a. These films each have a work function higher than or equal to 5 eV, preferably higher than or equal to 5.5 eV, which is higher than the electron affinity of the oxide semiconductor. Thus, the threshold voltage of the transistor including an oxide semiconductor can be shifted in the positive direction, and what is called a normally-off switching element can be achieved. For example, in the case of using an In-Ga-Zn-based oxynitride semiconductor film, an In-Ga-Zn-based oxynitride semiconductor film having a higher nitrogen concentration than at least the oxide semiconductor film 108, specifically, an In-Ga-Zn-based oxynitride semiconductor film having a nitrogen concentration higher than or equal to 7 at.%, is used.

[0082]

<Gate insulating film>

As each of the insulating films 106a and 106b functioning as a gate insulating film of the transistor 150, an insulating layer including at least one of the following films formed by a plasma enhanced chemical vapor deposition (PE-CVD) method, a sputtering method, or the like can be used: a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film. Note that the stacked-layer structure of the insulating films 106a and 106b is not necessarily employed, and an insulating film having a single-layer structure or a three or more insulating films including any of the above materials may be used.

[0083]

It is preferable that the insulating film 106a be a nitride film containing at least

nitrogen and silicon, and that the insulating film 106b be an oxide film containing at least oxygen and silicon. Examples of the insulating film 106a include a silicon oxynitride film, a silicon nitride oxide film, and silicon nitride film. Examples of the insulating film 106b include a silicon oxynitride film, a silicon nitride oxide film, and a silicon oxide film.

[0084]

Note that the insulating film 106b that is in contact with the oxide semiconductor film 108 functioning as a channel region of the transistor 150 is preferably an oxide insulating film and preferably has a region (oxygen-excess region) containing oxygen in excess of the stoichiometric composition. In other words, the insulating film 106b is an insulating film capable of releasing oxygen. In order to provide the oxygen-excess region in the insulating film 106b, the insulating film 106b is formed in an oxygen atmosphere, for example. Alternatively, oxygen may be introduced into the deposited insulating film 106b to provide the oxygen-excess region therein. As a method for introducing oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like may be employed.

[0085]

Using hafnium oxide for the insulating films 106a and 106b has the following effects. Hafnium oxide has higher dielectric constant than silicon oxide and silicon oxynitride. Therefore, by using hafnium oxide or aluminum oxide, a physical thickness can be made larger than an equivalent oxide thickness; thus, even in the case where the equivalent oxide thickness is less than or equal to 10 nm or less than or equal to 5 nm, leakage current due to tunnel current can be low. That is, it is possible to provide a transistor with a low off-state current. Moreover, hafnium oxide with a crystalline structure has higher dielectric constant than hafnium oxide with an amorphous structure. Therefore, it is preferable to use hafnium oxide with a crystalline structure in order to provide a transistor with a low off-state current. Examples of the crystalline structure include a monoclinic crystal structure and a cubic crystal structure. Note that one embodiment of the present invention is not limited thereto.

[0086]

In this embodiment, a silicon nitride film is formed as the insulating film 106a, and a silicon oxide film is formed as the insulating film 106b. A silicon nitride film has a higher dielectric constant than a silicon oxide film and needs a larger thickness for capacitance equivalent to that of the silicon oxide. Thus, when the gate insulating film of the transistor 150 includes a silicon nitride film, the physical thickness of the gate insulating film can be increased. This makes it possible to reduce a decrease in the withstand voltage of the transistor 150 and furthermore increase the withstand voltage, thereby preventing electrostatic breakdown of the transistor 150.

[0087]

10 <Oxide semiconductor film>

The oxide semiconductor film 108 is typically In-Ga oxide film, In-Zn oxide film, or In-*M*-Zn oxide film (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf). It is particularly preferable to use an In-*M*-Zn oxide for the semiconductor film 108.

[0088]

15 In the case where the oxide semiconductor film 108 includes In-*M*-Zn oxide, it is preferable that the atomic ratio of metal elements of a sputtering target used for forming the In-*M*-Zn oxide satisfy $\text{In} \geq M$ and $\text{Zn} \geq M$. As the atomic ratio of metal elements of such a sputtering target, $\text{In}:M:\text{Zn} = 1:1:1$, $\text{In}:M:\text{Zn} = 1:1:1.2$, and $\text{In}:M:\text{Zn} = 3:1:2$ are preferable. Note that the atomic ratio of metal elements of the deposited oxide semiconductor film 108 vary from the above atomic ratio of metal elements of the sputtering target within a range of $\pm 40\%$ as an error.

[0089]

Note that when the oxide semiconductor film 108 includes In-*M*-Zn oxide, the proportion of In and the proportion of *M*, not taking Zn and O into consideration, are preferably greater than or equal to 25 atomic% and less than 75 atomic%, respectively, further preferably greater than or equal to 34 atomic% and less than 66 atomic%, respectively.

[0090]

30 The energy gap of the oxide semiconductor film 108 is 2 eV or more, preferably 2.5 eV or more, further preferably 3 eV or more. With the use of an oxide semiconductor having such a wide energy gap, the off-state current of the transistor 150

can be reduced.

[0091]

The thickness of the oxide semiconductor film 108 is greater than or equal to 3 nm and less than or equal to 200 nm, preferably greater than or equal to 3 nm and less than or equal to 100 nm, further preferably greater than or equal to 3 nm and less than or equal to 50 nm.

[0092]

An oxide semiconductor film with low carrier density is used as the oxide semiconductor film 108. For example, the carrier density of the oxide semiconductor film 108 is lower than or equal to $1 \times 10^{17} / \text{cm}^3$, preferably lower than or equal to $1 \times 10^{15} / \text{cm}^3$, further preferably lower than or equal to $1 \times 10^{13} / \text{cm}^3$, particularly preferably lower than or equal to $8 \times 10^{11} / \text{cm}^3$, still further preferably lower than or equal to $1 \times 10^{11} / \text{cm}^3$, yet further preferably higher than or equal to $1 \times 10^{-9} / \text{cm}^3$ and lower than or equal to $1 \times 10^{10} / \text{cm}^3$.

[0093]

Note that, without limitation to the compositions and materials described above, a material with an appropriate composition may be used depending on required semiconductor characteristics and electrical characteristics (e.g., field-effect mobility and threshold voltage) of a transistor. Furthermore, in order to obtain required semiconductor characteristics of a transistor, it is preferable that the carrier density, the impurity concentration, the defect density, the atomic ratio of a metal element to oxygen, the interatomic distance, the density, and the like of the oxide semiconductor film 108 be set to be appropriate.

[0094]

Note that it is preferable to use, as the oxide semiconductor film 108, an oxide semiconductor film in which the impurity concentration is low and density of defect states is low, in which case the transistor can have more excellent electrical characteristics. Here, the state in which impurity concentration is low and density of defect states is low (the amount of oxygen vacancy is small) is referred to as “highly purified intrinsic” or “substantially highly purified intrinsic”. A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has few

carrier generation sources, and thus can have a low carrier density. Thus, a transistor including the oxide semiconductor film in which a channel region is formed rarely has a negative threshold voltage (is rarely normally-on). A highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has a low density of defect states and accordingly has few carrier traps in some cases. Furthermore, the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film has an extremely low off-state current; even when an element has a channel width of $1 \times 10^6 \mu\text{m}$ and a channel length L of $10 \mu\text{m}$, the off-state current can be less than or equal to the measurement limit of a semiconductor parameter analyzer, i.e., less than or equal to $1 \times 10^{-13} \text{ A}$, at a voltage (drain voltage) between a source electrode and a drain electrode of from 1 V to 10 V.

[0095]

Accordingly, the transistor in which the channel region is formed in the highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor film can have a small variation in electrical characteristics and high reliability. Charges trapped by the trap states in the oxide semiconductor film take a long time to be released and may behave like fixed charges. Thus, the transistor whose channel region is formed in the oxide semiconductor film having a high density of trap states has unstable electrical characteristics in some cases. As examples of the impurities, hydrogen, nitrogen, alkali metal, alkaline earth metal, and the like are given.

[0096]

Hydrogen contained in the oxide semiconductor film reacts with oxygen bonded to a metal atom to be water, and also causes oxygen vacancy in a lattice from which oxygen is released (or a portion from which oxygen is released). Due to entry of hydrogen into the oxygen vacancy, an electron serving as a carrier is generated in some cases. Furthermore, in some cases, bonding of part of hydrogen to oxygen bonded to a metal element causes generation of an electron serving as a carrier. Thus, a transistor including an oxide semiconductor film which contains hydrogen is likely to be normally on. Accordingly, it is preferable that hydrogen be reduced as much as possible in the oxide semiconductor film 108. Specifically, the hydrogen concentration of the oxide semiconductor film 108, which is measured by secondary ion

mass spectrometry (SIMS), is lower than or equal to 2×10^{20} atoms/cm³, preferably lower than or equal to 5×10^{19} atoms/cm³, more preferably lower than or equal to 1×10^{19} atoms/cm³, even more preferably lower than 5×10^{18} atoms/cm³, still more preferably lower than or equal to 1×10^{18} atoms/cm³, yet still more preferably lower than or equal to 5×10^{17} atoms/cm³, even further more preferably lower than or equal to 1×10^{16} atoms/cm³.

[0097]

When silicon or carbon that is one of elements belonging to Group 14 is contained in the oxide semiconductor film 108, oxygen vacancy is increased in the oxide semiconductor film 108, and the oxide semiconductor film 108 becomes an n-type film. Thus, the concentration of silicon or carbon (the concentration is measured by SIMS) in the oxide semiconductor film 108 or the concentration of silicon or carbon (the concentration is measured by SIMS) in the vicinity of the interface with the oxide semiconductor film 108 is set to be lower than or equal to 2×10^{18} atoms/cm³, preferably lower than or equal to 2×10^{17} atoms/cm³.

[0098]

In addition, the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 108, which is measured by SIMS, is lower than or equal to 1×10^{18} atoms/cm³, preferably lower than or equal to 2×10^{16} atoms/cm³. Alkali metal and alkaline earth metal might generate carriers when bonded to an oxide semiconductor, in which case the off-state current of the transistor might be increased. Therefore, it is preferable to reduce the concentration of alkali metal or alkaline earth metal of the oxide semiconductor film 108.

[0099]

Furthermore, when containing nitrogen, the oxide semiconductor film 108 easily becomes n-type by generation of electrons serving as carriers and an increase of carrier density. Thus, a transistor including an oxide semiconductor film which contains nitrogen is likely to have normally-on characteristics. For this reason, nitrogen in the oxide semiconductor film is preferably reduced as much as possible; the concentration of nitrogen measured by SIMS is preferably, for example, lower than or equal to 5×10^{18} atoms/cm³.

[0100]

The oxide semiconductor film 108 may have a non-single-crystal structure, for example. The non-single crystal structure includes, for example, a CAAC-OS described later, a polycrystalline structure, a microcrystalline structure described later,
5 and an amorphous structure. Among the non-single crystal structure, the amorphous structure has the highest density of defect levels, whereas CAAC-OS has the lowest density of defect levels.

[0101]

The oxide semiconductor film 108 may have an amorphous structure, for
10 example. The oxide semiconductor films having the amorphous structure each have disordered atomic arrangement and no crystalline component, for example. Alternatively, the oxide films having an amorphous structure have, for example, an absolutely amorphous structure and no crystal part.

[0102]

Note that the oxide semiconductor film 108 may be a mixed film including two
15 or more of the following: a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure. The mixed film includes, for example, two or more of a region having an amorphous structure, a region having a
20 microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal structure in some cases. Furthermore, the mixed film has a stacked-layer structure of two or more of a region having an amorphous structure, a region having a microcrystalline structure, a region having a polycrystalline structure, a CAAC-OS region, and a region having a single-crystal
25 structure in some cases.

[0103]

<Electrode layers>

It is preferable that the pair of electrode layers 112a and 112b functioning as a
source electrode and a drain electrode of the transistor 150 have a single-layer structure
30 of a Cu-X alloy film or a stacked-layer structure of a Cu-X alloy film and a conductive film containing a low-resistance material such as copper (Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a compound

containing any of these materials as a main component. The pair of electrode layers 112a and 112b can be formed with a sputtering apparatus, for example. For example, a metal target containing Cu and Mn at a ratio of 90:10 [at.%) or the like can be used in the sputtering apparatus.

5 [0104]

<Insulating films>

The insulating films 114, 116, and 118 function as a second gate insulating film of the transistor 150 and also function as a protective insulating film for the oxide semiconductor film 108. For example, the insulating film 114 is an insulating film
10 which is permeable to oxygen. Note that the insulating film 114 also functions as a film which relieves damage to the oxide semiconductor film 108 at the time of forming the insulating film 116 in a later step. Note that the insulating film 114 is not necessarily provided.

[0105]

15 A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 5 nm and less than or equal to 150 nm, preferably greater than or equal to 5 nm and less than or equal to 50 nm can be used as the insulating film 114.

[0106]

Furthermore, it is preferable that the number of defects in the insulating film
20 114 be small and typically, the spin density of a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than or equal to 3×10^{17} spins/cm³ by electron spin resonance (ESR) measurement. This is because if the density of defects in the insulating film 114 is high, oxygen is bonded to the defects and the amount of oxygen that passes through the insulating film 114 is decreased.

25 [0107]

Note that all oxygen entering the insulating film 114 from the outside is not moved to the outside of the insulating film 114 and some oxygen remains in the insulating film 114 in some cases. In addition, oxygen enters the insulating film 114 and oxygen contained in the insulating film 114 is moved to the outside of the insulating
30 film 114, whereby movement of oxygen in the insulating film 114 occurs in some cases. When the oxide insulating film which is permeable to oxygen is formed as the

insulating film 114, oxygen released from the insulating film 116 provided over the insulating film 114 can be moved to the oxide semiconductor film 108 through the insulating film 114.

[0108]

5 The insulating film 116 is formed using an oxide insulating film containing oxygen in excess of the stoichiometric composition. Part of oxygen is released by heating from the oxide insulating film containing oxygen in excess of the stoichiometric composition. The oxide insulating film containing oxygen in excess of the stoichiometric composition is an oxide insulating film of which the amount of released
10 oxygen converted into oxygen atoms is greater than or equal to 1.0×10^{18} atoms/cm³, preferably greater than or equal to 3.0×10^{20} atoms/cm³ in TDS analysis. Note that the temperature of the film surface in the TDS analysis is preferably higher than or equal to 100 °C and lower than or equal to 700 °C, or higher than or equal to 100 °C and lower than or equal to 500 °C.

15 [0109]

A silicon oxide film, a silicon oxynitride film, or the like with a thickness greater than or equal to 30 nm and less than or equal to 500 nm, preferably greater than or equal to 50 nm and less than or equal to 400 nm can be used for the insulating film 116.

20 [0110]

Further, it is preferable that the amount of defects in the insulating film 116 be small, and typically the spin density of a signal that appears at $g = 2.001$ due to a dangling bond of silicon be lower than 1.5×10^{18} spins/cm³, further preferably lower than or equal to 1×10^{18} spins/cm³ by ESR measurement. Note that the insulating film
25 116 is provided more apart from the oxide semiconductor film 108 than the insulating film 114 is; thus, the insulating film 116 may have higher defect density than the insulating film 114.

[0111]

Furthermore, the insulating films 114 and 116 can be formed using insulating
30 films formed of the same kinds of materials; thus, a boundary between the insulating films 114 and 116 cannot be clearly observed in some cases. Thus, in this embodiment,

the boundary between the insulating films 114 and 116 is shown by a dashed line. Although a two-layer structure of the insulating films 114 and 116 is described in this embodiment, one embodiment of the present invention is not limited thereto. For example, a single-layer structure of the insulating film 114, a single-layer structure of the insulating film 116, or a stacked-layer structure of three or more layers may be used. [0112]

The insulating film 118 has a function of blocking oxygen, hydrogen, water, an alkali metal, an alkaline earth metal, and the like. By providing the insulating film 118, it is possible to prevent outward diffusion of oxygen from the oxide semiconductor film 108 and entry of hydrogen, water, or the like into the oxide semiconductor film 108 from the outside. The insulating film 118 can be formed using a nitride insulating film, for example. The nitride insulating film is formed using silicon nitride, silicon nitride oxide, aluminum nitride, aluminum nitride oxide, or the like. Note that instead of the nitride insulating film having a blocking effect against oxygen, hydrogen, water, an alkali metal, an alkaline earth metal, and the like, an oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, may be provided. As the oxide insulating film having a blocking effect against oxygen, hydrogen, water, and the like, an aluminum oxide film, an aluminum oxynitride film, a gallium oxide film, a gallium oxynitride film, an yttrium oxide film, an yttrium oxynitride film, a hafnium oxide film, and a hafnium oxynitride film can be given.

[0113]

<Conductive film>

For example, a material including one of indium (In), zinc (Zn), and tin (Sn) can be used for the conductive films 120a and 120b used in the transistor 150. In particular, a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide, indium tin oxide containing titanium oxide, indium tin oxide (ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added can be used for the conductive films 120a and 120b. The conductive films 120a and 120b can be formed by a sputtering method, for example.

[0114]

Although the variety of films such as the conductive films, the insulating films,

the oxide semiconductor films, and the metal oxide films which are described above can be formed by a sputtering method or a PE-CVD method, such films may be formed by another method, e.g., a thermal CVD method. A metal organic chemical vapor deposition (MOCVD) method or an atomic layer deposition (ALD) method may be employed as an example of a thermal CVD method.

[0115]

A thermal CVD method has an advantage that no defect due to plasma damage is generated since it does not utilize plasma for forming a film.

[0116]

Deposition by a thermal CVD method may be performed in such a manner that a source gas and an oxidizer are supplied to a chamber at a time so that the pressure in the chamber is set to an atmospheric pressure or a reduced pressure, and react with each other in the vicinity of the substrate or over the substrate.

[0117]

Deposition by an ALD method may be performed in such a manner that the pressure in a chamber is set to an atmospheric pressure or a reduced pressure, a source gas for reaction is sequentially introduced into the chamber, and then the sequence of the gas introduction is repeated. For example, two or more kinds of source gases are sequentially supplied to the chamber by switching respective switching valves (also referred to as high-speed valves). For example, a first source gas is introduced, an inert gas (e.g., argon or nitrogen) or the like is introduced at the same time as or after the introduction of the first gas so that the source gases are not mixed, and then a second source gas is introduced. Note that in the case where the first source gas and the inert gas are introduced at a time, the inert gas serves as a carrier gas, and the inert gas may also be introduced at the same time as the introduction of the second source gas. Alternatively, the first source gas may be exhausted by vacuum evacuation instead of the introduction of the inert gas, and then the second source gas may be introduced. The first source gas is adsorbed on the surface of the substrate to form a first layer; then the second source gas is introduced to react with the first layer; as a result, a second layer is stacked over the first layer, so that a thin film is formed. The sequence of the gas introduction is repeated plural times until a desired thickness is obtained, whereby a thin film with excellent step coverage can be formed. The thickness of the thin film

can be adjusted by the number of repetition times of the sequence of the gas introduction; therefore, an ALD method makes it possible to accurately adjust a thickness and thus is suitable for manufacturing a minute FET.

[0118]

5 The variety of films such as the conductive films, the insulating films, the oxide semiconductor films, and the metal oxide films which are described in this specification can be formed by a thermal CVD method such as a MOCVD method or an ALD method. For example, in the case where an In-Ga-Zn-O film is formed, trimethylindium, trimethylgallium, and dimethylzinc are used. Note that the chemical
10 formula of trimethylindium is $\text{In}(\text{CH}_3)_3$. The chemical formula of trimethylgallium is $\text{Ga}(\text{CH}_3)_3$. The chemical formula of dimethylzinc is $\text{Zn}(\text{CH}_3)_2$. Without limitation to the above combination, triethylgallium (chemical formula: $\text{Ga}(\text{C}_2\text{H}_5)_3$) can be used instead of trimethylgallium and diethylzinc (chemical formula: $\text{Zn}(\text{C}_2\text{H}_5)_2$) can be used instead of dimethylzinc.

15 [0119]

For example, in the case where a hafnium oxide film is formed using a deposition apparatus using an ALD method, two kinds of gases, i.e., ozone (O_3) as an oxidizer and a source gas which is obtained by vaporizing liquid containing a solvent and a hafnium precursor compound (a hafnium alkoxide solution, typically
20 tetrakis(dimethylamide)hafnium (TDMAH)) are used. Note that the chemical formula of tetrakis(dimethylamide)hafnium is $\text{Hf}[\text{N}(\text{CH}_3)_2]_4$. Examples of another material liquid include tetrakis(ethylmethyle)hafnium.

[0120]

For example, in the case where an aluminum oxide film is formed using a
25 deposition apparatus using an ALD method, two kinds of gases, e.g., H_2O as an oxidizer and a source gas which is obtained by vaporizing liquid containing a solvent and an aluminum precursor compound (e.g., trimethylaluminum (TMA)) are used. Note that the chemical formula of trimethylaluminum is $\text{Al}(\text{CH}_3)_3$. Examples of another material liquid include tris(dimethylamide)aluminum, triisobutylaluminum, and
30 aluminum tris(2,2,6,6-tetramethyl-3,5-heptanedionate).

[0121]

For example, in the case where a silicon oxide film is formed using a

deposition apparatus using an ALD method, hexachlorodisilane is adsorbed on a surface where a film is to be formed, chlorine contained in the adsorbate is removed, and radicals of an oxidizing gas (e.g., O₂ or dinitrogen monoxide) are supplied to react with the adsorbate.

5 [0122]

For example, in the case where a tungsten film is formed using a deposition apparatus employing an ALD method, a WF₆ gas and a B₂H₆ gas are sequentially introduced plural times to form an initial tungsten film, and then a WF₆ gas and an H₂ gas are introduced at a time, so that a tungsten film is formed. Note that an SiH₄ gas may be used instead of a B₂H₆ gas.

[0123]

For example, in the case where an oxide semiconductor film, e.g., an In-Ga-Zn-O film is formed using a deposition apparatus employing an ALD method, an In(CH₃)₃ gas and an O₃ gas are sequentially introduced plural times to form an InO₂ layer, a Ga(CH₃)₃ gas and an O₃ gas are introduced at a time to form a GaO layer, and then a Zn(CH₃)₂ gas and an O₃ gas are introduced at a time to form a ZnO layer. Note that the order of these layers is not limited to this example. A mixed compound layer such as an In-Ga-O layer, an In-Zn-O layer or a Ga-Zn-O layer may be formed by mixing of these gases. Note that although an H₂O gas which is obtained by bubbling with an inert gas such as Ar may be used instead of an O₃ gas, it is preferable to use an O₃ gas, which does not contain H. Furthermore, instead of an In(CH₃)₃ gas, an In(C₂H₅)₃ gas may be used. Instead of a Ga(CH₃)₃ gas, a Ga(C₂H₅)₃ gas may be used. In addition, instead of an In(CH₃)₃ gas, an In(C₂H₅)₃ gas may be used. Moreover, a Zn(CH₃)₂ gas may be used.

25 [0124]

<Structure example 2 of semiconductor device>

A transistor 152 that is a semiconductor device of one embodiment of the present invention is described FIGS. 3A to 3C.

[0125]

30 FIG. 3A is a top view of the transistor 152 that is a semiconductor device of one embodiment of the present invention. FIG. 3B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 3A. FIG. 3C is a cross-sectional view taken

along dashed dotted line X1-X2 in FIG. 3A.

[0126]

The transistor 152 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; a protective insulating film 109 over the insulating film 106 and the oxide semiconductor film 108; the pair of electrode layers 112a and 112b that is electrically connected to the oxide semiconductor film 108 through openings 140a and 140b provided in the protective insulating film 109 and functions as a source electrode layer and a drain electrode layer of the transistor 152; the insulating films 114, 116, and 118 over the pair of electrode layers 112a and 112b and the protective insulating film 109; and the conductive films 120a and 120b over the insulating film 118.

[0127]

The conductive film 120a is connected to the electrode layer 112b through the opening 142c provided in the insulating films 114, 116, and 118. The conductive film 120b is formed over the insulating film 118 to overlap the oxide semiconductor film 108.

[0128]

In the transistor 152, the protective insulating film 109 functions as a first insulating film, and the insulating films 114, 116, and 118 functions as a second insulating film. The first insulating film and the second insulating film function as a second gate insulating film of the transistor 152.

[0129]

The pair of electrode layers 112a and 112b in the transistor 152 functions as a source electrode layer and a drain electrode layer. Note that the pair of electrode layers 112a and 112b includes at least a Cu-X alloy film; for example, it is preferable that the pair of electrode layers 112a and 112b have a single-layer structure of a Cu-X alloy film or a stacked-layer structure of a Cu-X alloy film and a conductive film containing a low-resistance material such as copper (Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a compound containing any of these materials as a main component.

[0130]

The pair of electrode layers 112a and 112b also functions as lead wirings or the like. Therefore, the pair of electrode layers 112a and 112b is formed to include a Cu-*X* alloy film, or a Cu-*X* alloy film and a conductive film containing a low-resistance material such as copper, aluminum, gold, or silver, whereby a semiconductor device with reduced wiring delay can be manufactured even when a large-sized substrate is used as the substrate 102.

[0131]

In addition, a Cu-*X* alloy film is used for the pair of electrode layers 112a and 112b in contact with the oxide semiconductor film 108, whereby *X* in the Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) might form a coating film of *X* at the interface between the Cu-*X* alloy film and the oxide semiconductor film. The coating film can inhibit Cu in the Cu-*X* alloy film from entering the oxide semiconductor film 108.

[0132]

For example, as the Cu-*X* alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) used for the pair of electrode layers 112a and 112b, a Cu-Mn alloy film can be selected. When the Cu-Mn alloy film is used for the pair of electrode layers 112a and 112b, a coating film containing Mn is formed at the interface with a base film (here, the protective insulating film 109 and the oxide semiconductor film 108), which can improve adhesion. Furthermore, the use of the Cu-Mn alloy film enables a favorable ohmic contact with the oxide semiconductor film 108.

[0133]

Here, FIG. 4 is an enlarged cross-sectional view of some components in the semiconductor device illustrated in FIGS. 3A to 3C.

[0134]

FIG. 4 is a cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the protective insulating film 109, the pair of electrode layers 112a and 112b, the insulating films 114, 116, and 118, and the conductive film 120b that are included in the transistor 152.

[0135]

As illustrated in FIG. 4, coating films 113a and 113b might be formed at the

interfaces between the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b, the interfaces between the protective insulating film 109 and the pair of electrode layers 112a and 112b, and the interfaces between the insulating film 114 and the pair of electrode layers 112a and 112b. The structure of the coating films 113a and 113b is similar to that of the above-described coating films 113a and 113b.

[0136]

As illustrated in FIGS. 3B and 3C, the protective insulating film 109 covers at least a channel region and side surfaces of the oxide semiconductor film 108. In this manner, the transistor 152 is different from the transistor 150 in FIGS. 1A to 1C in that the protective insulating film 109 is provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 150 and the effect similar to that in the case of the transistor 150 can be obtained. Furthermore, in the transistor 152, the protective insulating film 109 can further inhibit an impurity (here, Cu contained in the pair of electrode layers 112a and 112b) from entering the oxide semiconductor film 108.

[0137]

As the protective insulating film 109 that can be used in the transistor 152, an insulating film including at least one of the following films formed by a PE-CVD method, a sputtering method, or the like can be used: a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, an aluminum oxide film, a hafnium oxide film, an yttrium oxide film, a zirconium oxide film, a gallium oxide film, a tantalum oxide film, a magnesium oxide film, a lanthanum oxide film, a cerium oxide film, and a neodymium oxide film. Note that the protective insulating film 109 may have a stacked-layer structure of any of these films. To improve the interface characteristics between the protective insulating film 109 and the oxide semiconductor film 108, it is particularly preferable to use a silicon oxide film or a silicon oxynitride film as the protective insulating film 109.

[0138]

Note that the protective insulating film 109 that is in contact with the oxide semiconductor film 108 is preferably an oxide insulating film and preferably has a region (oxygen-excess region) containing oxygen in excess of the stoichiometric composition. In order to provide the oxygen-excess region in the protective insulating

film 109, the protective insulating film 109 may be formed in an oxygen atmosphere, for example. Alternatively, oxygen may be introduced into the formed protective insulating film 109 to form the oxygen-excess region therein. As a method for introducing oxygen, an ion implantation method, an ion doping method, a plasma immersion ion implantation method, plasma treatment, or the like may be employed.

[0139]

The protective insulating film 109 preferably has a nitrogen concentration measured by secondary ion mass spectrometry (SIMS) of lower than or equal to 6×10^{20} atoms/cm³. In that case, nitrogen oxide is unlikely to be generated in protective insulating film 109, so that the carrier trap at the interface between the protective insulating film 109 and the oxide semiconductor film can be inhibited. Furthermore, a shift in the threshold voltage of the transistor included in the semiconductor device can be inhibited, which leads to a reduced change in the electrical characteristics of the transistor.

[0140]

Like the transistor 150 described above, the transistor 152 has an s-channel structure.

[0141]

Specifically, as illustrated in the cross-sectional view of FIG. 3B, the oxide semiconductor film 108 is positioned to face each of the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a back gate electrode layer, and is sandwiched between the two conductive layers functioning as gate electrode layers. The lengths in the channel length direction and the channel width direction of the conductive film 120b functioning as a back gate electrode layer are longer than those in the channel length direction and the channel width direction of the oxide semiconductor film 108. The whole oxide semiconductor film 108 is covered with the conductive film 120b with the protective insulating film 109 and the insulating films 114, 116, and 118 positioned therebetween. Since the conductive film 120b functioning as a back gate electrode layer is connected to the conductive film 104 functioning as a gate electrode layer through the opening 142a and 142b provided in the insulating films 106a, 106b, 114, 116, and 118 and the protective insulating film 109, a side surface of the oxide semiconductor film 108 in the channel width direction faces

the conductive film 120b functioning as a back gate electrode layer with the protective insulating film 109 positioned therebetween.

[0142]

In other words, in the channel width direction of the transistor 152, the conductive film 104 functioning as a gate electrode layer and the conductive film 120b functioning as a back gate electrode layer are connected to each other through the openings provided in the insulating film 106 functioning as a gate insulating film, the protective insulating film 109, and the insulating films 114, 116, and 118; and the conductive film 104 and the conductive film 120b surround the oxide semiconductor film 108 with the insulating film 106 functioning as a gate insulating film, the protective insulating film 109, and the insulating films 114, 116, and 118 positioned therebetween.

[0143]

<Structure example 3 of semiconductor device>

Transistors 154, 156, 158, and 160 that are semiconductor devices of one embodiment of the present invention are described using FIGS. 5A to 5C, FIGS. 6A to 6C, FIGS. 7A and 7B, FIGS. 8A to 8C, FIGS. 9A to 9C, and FIGS. 10A and 10B.

[0144]

First, the transistor 154 illustrated in FIGS. 5A to 5C is described.

[0145]

FIG. 5A is a top view of the transistor 154 that is a semiconductor device of one embodiment of the present invention. FIG. 5B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 5A. FIG. 5C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 5A.

[0146]

The transistor 154 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; a metal oxide film 108a over the oxide semiconductor film 108; a metal oxide film 108b over the metal oxide film 108a; the pair of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108 with the metal oxide film 108a and the metal oxide film 108b positioned therebetween; the insulating films 114,

116, and 118 over the pair of electrode layers 112a and 112b, the metal oxide film 108a, and the metal oxide film 108b; and the conductive films 120a and 120b over the insulating film 118.

[0147]

5 The transistor 154 is different from the transistor 150 in FIGS. 1A to 1C in that the metal oxide films 108a and 108b are provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 150 and the effect similar to that in the case of the transistor 150 can be obtained. Note that the metal oxide film 108a is provided over and in contact with the oxide semiconductor film 108.
10 The metal oxide film 108b is provided over and in contact with the metal oxide film 108a. The metal oxide films 108a and 108b function as barrier layers for preventing a constituent element of the pair of electrode layers 112a and 112b from diffusing to the oxide semiconductor film 108. Therefore, the metal oxide films 108a and 108b can further inhibit an impurity (here, Cu contained in the pair of electrode layers 112a and
15 112b) from entering the oxide semiconductor film 108.

[0148]

Note that the details of the metal oxide films 108a and 108b are described later.

[0149]

20 Next, the transistor 156 illustrated in FIGS. 6A to 6C is described.

[0150]

FIG. 6A is a top view of the transistor 156 that is a semiconductor device of one embodiment of the present invention. FIG. 6B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 6A. FIG. 6C is a cross-sectional view taken
25 along dashed dotted line X1-X2 in FIG. 6A.

[0151]

The transistor 156 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide
30 semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; the metal oxide film 108a over the oxide semiconductor film 108; the metal oxide film 108b over the metal oxide film 108a; the protective insulating film 109 over

the insulating film 106 and the metal oxide film 108b; the pair of electrode layers 112a and 112b that is electrically connected to the oxide semiconductor film 108 through the openings 140a and 140b provided in the protective insulating film 109 and functions as a source electrode layer and a drain electrode layer of the transistor 156; the insulating films 114, 116, and 118 over the pair of electrode layers 112a and 112b and the protective insulating film 109; and the conductive films 120a and 120b over the insulating film 118.

[0152]

The transistor 156 is different from the transistor 152 in FIGS. 3A to 3C in that the metal oxide films 108a and 108b are provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 152 and the effect similar to that in the case of the transistor 152 can be obtained. Note that the metal oxide film 108a is provided over and in contact with the oxide semiconductor film 108. The metal oxide film 108b is provided over and in contact with the metal oxide film 108a. The metal oxide films 108a and 108b function as barrier layers for preventing a constituent element of the pair of electrode layers 112a and 112b from diffusing to the oxide semiconductor film 108. Therefore, the metal oxide films 108a and 108b can further inhibit an impurity (here, Cu contained in the pair of electrode layers 112a and 112b) from entering the oxide semiconductor film 108.

[0153]

The oxide semiconductor film 108, the metal oxide film 108a, and the metal oxide film 108b that can be used for the transistor 154 in FIGS. 5A to 5C and the transistor 156 in FIGS. 6A to 6C are described below.

[0154]

Any of the above-described materials, such as a material formed of In-M-Zn oxide, is used for the oxide semiconductor film 108. A material which is formed of In-M-Zn oxide or In-M oxide is used for the metal oxide film 108a. A material which is formed of In-M-Zn oxide or In-M oxide is used for the metal oxide film 108b.

[0155]

Note that in the case where the metal oxide film 108a and the metal oxide film 108b are formed using the same kinds of materials, the interface between the metal oxide film 108a and the metal oxide film 108b cannot be observed in some cases.

[0156]

To increase a blocking property against a constituent element of the pair of electrode layers 112a and 112b, e.g., a copper element, it is preferable that the metal oxide film 108b be formed of CAAC-OS described later.

5 [0157]

Here, FIGS. 7A and 7B are enlarged cross-sectional views of some components in the semiconductor devices illustrated in FIGS. 5A to 5C and FIGS. 6A to 6C.

[0158]

FIG. 7A is a cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the metal oxide films 108a and 108b, the pair of electrode layers 112a and 112b, the insulating films 114, 116, and 118, and the conductive film 120b that are included in the transistor 154.

[0159]

FIG. 7B is a cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the metal oxide films 108a and 108b, the protective insulating film 109, the pair of electrode layers 112a and 112b, the insulating films 114, 116, and 118, and the conductive film 120b that are included in the transistor 156.

[0160]

As illustrated in FIG. 7A, coating films 115a and 115b might be formed at the interfaces between the metal oxide film 108b and the pair of electrode layers 112a and 112b, the interfaces between the insulating film 106b and the pair of electrode layers 112a and 112b, and the interfaces between the insulating film 114 and the pair of electrode layers 112a and 112b. As illustrated in FIG. 7B, the coating films 115a and 115b might be formed at the interfaces between the metal oxide film 108b and the pair of electrode layers 112a and 112b, the interfaces between the protective insulating film 109 and the pair of electrode layers 112a and 112b, and the interfaces between the insulating film 114 and the pair of electrode layers 112a and 112b.

[0161]

For example, in the case where the metal oxide film 108b and the pair of electrode layers 112a and 112b are heated in the state where they are in contact with each other, the coating films 115a and 115b can be formed in the vicinity of the interface with the metal oxide film 108b in such a manner that Mn in the Cu-Mn alloy

film used for the pair of electrode layers 112a and 112b is segregated. Note that the coating films 115a and 115b are formed of, for example, Mn oxide, In-Mn oxide, Ga-Mn oxide, In-Ga-Mn oxide, or In-Ga-Zn-Mn oxide which can be formed by a reaction with a constituent element in the metal oxide film 108b.

5 [0162]

For example, in the case where the insulating films 106 and 114 or the protective insulating film 109 and the pair of electrode layers 112a and 112b are heated in the state where they are in contact with each other, the coating films 115a and 115b can be formed in the vicinities of the interfaces between the insulating films 106 and 10
114 and the pair of electrode layers 112a and 112b and in the vicinity of the interfaces between the protective insulating film 109 and the pair of electrode layers 112a and 112b in such a manner that Mn in the Cu-Mn alloy film used for the pair of electrode layers 112a and 112b is segregated. Note that in addition to the above oxides, the coating films 115a and 115b can be formed of, for example, Mn hydride, Mn carbide,
15 Mn oxide, Mn nitride, or Mn silicide when the insulating films 106 and 114 or the protective insulating film 109 contains hydrogen, carbon, oxygen, nitrogen, silicon, or the like.

[0163]

Next, the transistor 158 illustrated in FIGS. 8A to 8C is described.

20 [0164]

FIG. 8A is a top view of the transistor 158 that is a semiconductor device of one embodiment of the present invention. FIG. 8B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 8A. FIG. 8C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 8A.

25 [0165]

The transistor 158 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive
30 film 104; the metal oxide film 108b over the oxide semiconductor film 108; the pair of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108 with the metal oxide film 108b positioned therebetween; the insulating films 114,

116, and 118 over the pair of electrode layers 112a and 112b and the metal oxide film 108b; and the conductive films 120a and 120b over the insulating film 118.

[0166]

The transistor 158 is different from the transistor 150 in FIGS. 1A to 1C in that the metal oxide film 108b is provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 150 and the effect similar to that in the case of the transistor 150 can be obtained. Note that the metal oxide film 108b is provided over and in contact with the oxide semiconductor film 108.

[0167]

Next, the transistor 160 illustrated in FIGS. 9A to 9C is described.

[0168]

FIG. 9A is a top view of the transistor 160 that is a semiconductor device of one embodiment of the present invention. FIG. 9B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 9A. FIG. 9C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 9A.

[0169]

The transistor 160 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; the metal oxide film 108b over the oxide semiconductor film 108; the protective insulating film 109 over the insulating film 106 and the metal oxide film 108b; the pair of electrode layers 112a and 112b that is electrically connected to the oxide semiconductor film 108 through the openings 140a and 140b provided in the protective insulating film 109 and functions as a source electrode layer and a drain electrode layer of the transistor 160; the insulating films 114, 116, and 118 over the pair of electrode layers 112a and 112b and the protective insulating film 109; and the conductive films 120a and 120b over the insulating film 118.

[0170]

The transistor 160 is different from the transistor 152 in FIGS. 3A to 3C in that the metal oxide film 108b is provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 152 and the effect similar to that

in the case of the transistor 152 can be obtained. Note that the metal oxide film 108b is provided over and in contact with the oxide semiconductor film 108.

[0171]

Since the metal oxide film 108a, the metal oxide film 108b, or the protective insulating film 109 is provided over the oxide semiconductor film 108 in the transistors 154, 156, 158, and 160, Cu can be further inhibited from entering the oxide semiconductor film 108.

[0172]

Here, a band structure of the oxide semiconductor film 108 and the metal oxide films 108a and 108b and a band structure of the oxide semiconductor film 108 and the insulating film in contact with the metal oxide films 108a and 108b are described with reference to FIGS. 10A and 10B.

[0173]

FIG. 10A shows an example of a band structure in the thickness direction of a stacked-layer structure of the insulating film 106b, the oxide semiconductor film 108, the metal oxide film 108a, the metal oxide film 108b, and the insulating film 114 (or the protective insulating film 109). FIG. 10B shows an example of a band structure in the thickness direction of a stacked-layer structure of the insulating film 106b, the oxide semiconductor film 108, the metal oxide film 108b, and the insulating film 114 (or the protective insulating film 109). For easy understanding, the energy level (E_c) of the bottom of the conduction band of each of the insulating film 106b, the oxide semiconductor film 108, the metal oxide films 108a and 108b, and the insulating film 114 (or the protective insulating film 109) is shown in the band structures.

[0174]

In the band structure of FIG. 10A, a silicon oxide film is used as each of the insulating film 106b and the insulating film 114 (or the protective insulating film 109), an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn = 1:1:1 is used as the oxide semiconductor film 108, a metal oxide film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn = 1:3:6 is used as the metal oxide film 108a, and a metal oxide film formed using a metal oxide target having an atomic ratio of metal elements of

In:Ga:Zn = 1:4:5 is used as the metal oxide film 108b.

[0175]

In the band structure of FIG. 10B, a silicon oxide film is used as each of the insulating film 106b and the insulating film 114 (or the protective insulating film 109),
5 an oxide semiconductor film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn = 1:1:1 is used as the oxide semiconductor film 108, and a metal oxide film formed using a metal oxide target having an atomic ratio of metal elements of In:Ga:Zn = 1:3:6 is used as the metal oxide film 108b.

[0176]

10 As illustrated in FIGS. 10A and 10B, the energy level of the bottom of the conduction band smoothly varies between the oxide semiconductor film 108 and the metal oxide film 108a or between the oxide semiconductor film 108 and the metal oxide film 108b. In other words, the energy level of the bottom of the conduction band is continuously varied, or a continuous junction is formed. To obtain such a band
15 structure, there exists no impurity, which forms a defect state such as a trap center or a recombination center for the oxide semiconductor, at the interface between the oxide semiconductor film 108 and the metal oxide film 108a or at the interface between the oxide semiconductor film 108 and the metal oxide film 108b.

[0177]

20 To form a continuous junction between the oxide semiconductor film 108 and the metal oxide film 108a and between the oxide semiconductor film 108 and the metal oxide film 108b, it is necessary to form the films successively without exposure to the air by using a multi-chamber deposition apparatus (sputtering apparatus) provided with a load lock chamber.

25 [0178]

With the band structure of FIG. 10A or FIG. 10B, the oxide semiconductor film 108 serves as a well, and a channel region is formed in the oxide semiconductor film 108 in the transistor with the stacked-layer structure.

[0179]

30 Note that with the above stacked-layer structure, trap states, which may be formed in the oxide semiconductor film 108 in the case where the metal oxide films

108a and 108b are not formed, are formed in the metal oxide film 108a and/or the metal oxide film 108b. Therefore, the trap states can be separated from the oxide semiconductor film 108.

[0180]

5 In addition, the trap states might be more distant from the vacuum level than the energy level (E_c) of the bottom of the conduction band of the oxide semiconductor film 108 functioning as a channel region, so that electrons are likely to be accumulated in the trap states. When the electrons are accumulated in the trap states, the electrons become negative fixed electric charge, so that the threshold voltage of the transistor is
10 shifted in the positive direction. Therefore, it is preferable that the trap states be closer to the vacuum level than the energy level (E_c) of the bottom of the conduction band of the oxide semiconductor film 108. Such a structure inhibits accumulation of electrons in the trap states. As a result, the on-state current and the field-effect mobility of the transistor can be increased.

15 [0181]

In FIGS. 10A and 10B, the energy level of the bottom of the conduction band of each of the metal oxide films 108a and 108b is closer to the vacuum level than that of the oxide semiconductor film 108. Typically, an energy difference between the bottom of the conduction band of the oxide semiconductor film 108 and the bottom of the
20 conduction band of each of the metal oxide films 108a and 108b is greater than or equal to 0.15 eV or greater than or equal to 0.5 eV, and less than or equal to 2 eV or less than or equal to 1 eV. That is, the difference between the electron affinity of each of the metal oxide films 108a and 108b and the electron affinity of the oxide semiconductor film 108 is greater than or equal to 0.15 eV or greater than or equal to 0.5 eV, and less
25 than or equal to 2 eV or less than or equal to 1 eV.

[0182]

In such a structure, the oxide semiconductor film 108 serves as a main path of current and functions as a channel region. In addition, since the metal oxide films 108a and 108b each contain one or more metal elements contained in the oxide
30 semiconductor film 108 in which a channel region is formed, interface scattering is less likely to occur at the interface between the oxide semiconductor film 108 and the metal oxide film 108a or the interface between the oxide semiconductor film 108 and the

metal oxide film 108b. Thus, the transistor can have high field-effect mobility because the movement of carriers is not hindered at the interface.

[0183]

To prevent each of the metal oxide films 108a and 108b from functioning as
5 part of a channel region, a material having sufficiently low conductivity is used for the metal oxide films 108a and 108b. Alternatively, a material which has a smaller electron affinity (a difference in energy level between the vacuum level and the bottom of the conduction band) than the oxide semiconductor film 108 and has a difference in energy level of the bottom of the conduction band from the oxide semiconductor film
10 108 (band offset) is used for the metal oxide films 108a and 108b. Furthermore, to inhibit generation of a difference between threshold voltages due to the value of the drain voltage, it is preferable to form the metal oxide films 108a and 108b using a material whose energy level of the bottom of the conduction band is closer to the vacuum level than that of the oxide semiconductor film 108 is by more than 0.2 eV,
15 preferably 0.5 eV or more.

[0184]

It is preferable that the metal oxide films 108a and 108b not have a spinel crystal structure. If the metal oxide film 108a or the metal oxide film 108b has a spinel crystal structure, constituent elements of the pair of electrode layers 112a and
20 112b might be diffused into the oxide semiconductor film 108 at the interface between the spinel structure and another region. Note that each of the metal oxide films 108a and 108b is preferably a CAAC-OS, which is described later, in which case a higher blocking property against constituent elements of the pair of electrode layers 112a and 112b, e.g., copper, is obtained.

25 [0185]

The thickness of each of the metal oxide films 108a and 108b is greater than or equal to a thickness that is capable of inhibiting diffusion of the constituent element of the pair of electrode layers 112a and 112b into the oxide semiconductor film 108, and less than a thickness that inhibits supply of oxygen from the insulating film 114 to the
30 oxide semiconductor film 108. For example, when the thickness of each of the metal oxide films 108a and 108b is greater than or equal to 10 nm, the constituent elements of the pair of electrode layers 112a and 112b can be prevented from diffusing into the

oxide semiconductor film 108. When the thickness of each of the metal oxide films 108a and 108b is less than or equal to 100 nm, oxygen can be effectively supplied from the protective insulating film 109 or the insulating films 114 and 116 to the oxide semiconductor film 108.

5 [0186]

When the metal oxide films 108a and 108b are each an In-*M*-Zn oxide in which the atomic ratio of the element *M* (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf) is higher than that of In, the energy gap of each of the metal oxide films 108a and 108b can be large and the electron affinity thereof can be small. Therefore, a difference in electron affinity between the oxide semiconductor film 108 and each of the metal oxide films 108a and 108b may be controlled by the proportion of the element *M*. Furthermore, oxygen vacancy is less likely to be generated in the metal oxide film in which the atomic ratio of Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf is higher than that of In because Ti, Ga, Y, Zr, La, Ce, Nd, Sn, and Hf are each a metal element that is strongly bonded to oxygen.

15 [0187]

When the metal oxide films 108a and 108b are each an In-*M*-Zn oxide, the proportion of In and the proportion of *M*, not taking Zn and O into consideration, are preferably less than 50 at.% and greater than or equal to 50 at.%, respectively, further preferably less than 25 at.% and greater than or equal to 75 at.%, respectively.

20 [0188]

Furthermore, in the case where the oxide semiconductor film 108 and the metal oxide films 108a and 108b are each an In-*M*-Zn oxide, the proportion of *M* (*M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf) in each of the metal oxide films 108a and 108b is larger than that in the oxide semiconductor film 108. Typically, the proportion of *M* in each of the metal oxide films 108a and 108b is 1.5 or more times, preferably two or more times, further preferably three or more times as large as that in the oxide semiconductor film 108.

25 [0189]

Furthermore, in the case where the oxide semiconductor film 108 and the metal oxide films 108a and 108b are each an In-*M*-Zn oxide, when the oxide semiconductor

film 108 has an atomic ratio of $\text{In:M:Zn} = x_1:y_1:z_1$ and the metal oxide films 108a and 108b each have an atomic ratio of $\text{In:M:Zn} = x_2:y_2:z_2$, y_2/x_2 is larger than y_1/x_1 , preferably y_2/x_2 is 1.5 or more times as large as y_1/x_1 , further preferably, y_2/x_2 is two or more times as large as y_1/x_1 , still further preferably y_2/x_2 is three or more times or four or more times as large as y_1/x_1 . In that case, it is preferable that, in the oxide semiconductor film 108, y_1 be larger than or equal to x_1 because the transistor including the oxide semiconductor film 108 can have stable electric characteristics. However, when y_1 is three or more times as large as x_1 , the field-effect mobility of the transistor including the oxide semiconductor film 108 is reduced. Accordingly, y_1 is preferably smaller than three times x_1 .

[0190]

In the case where the oxide semiconductor film 108 is an In-M-Zn oxide and a target having the atomic ratio of metal elements of $\text{In:M:Zn} = x_1:y_1:z_1$ is used for depositing the oxide semiconductor film 108, x_1/y_1 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6, and z_1/y_1 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. Note that when z_1/y_1 is greater than or equal to 1 and less than or equal to 6, a CAAC-OS film to be described later is easily formed as the oxide semiconductor film 108. Typical examples of the atomic ratio of the metal elements of the target include $\text{In:M:Zn} = 1:1:1$, $\text{In:M:Zn} = 1:1:1.2$, $\text{In:M:Zn} = 1:1:1.5$, and $\text{In:M:Zn} = 3:1:2$.

[0191]

In the case where the metal oxide films 108a and 108b are each an In-M-Zn oxide and a target having an atomic ratio of metal elements of $\text{In:M:Zn} = x_2:y_2:z_2$ is used for depositing the metal oxide films 108a and 108b, x_2/y_2 is preferably less than x_1/y_1 , and z_2/y_2 is preferably greater than or equal to 1/3 and less than or equal to 6, further preferably greater than or equal to 1 and less than or equal to 6. When the atomic ratio of M with respect to indium is high, the energy gap of each of the metal oxide films 108a and 108b can be large and the electron affinity thereof can be small; therefore, y_2/x_2 is preferably greater than or equal to 3 or greater than or equal to 4. Typical examples of the atomic ratio of the metal elements of the target include $\text{In:M:Zn} = 1:3:2$,

In:M:Zn = 1:3:4, In:M:Zn = 1:3:5, In:M:Zn = 1:3:6, In:M:Zn = 1:4:2, In:M:Zn = 1:4:4, In:M:Zn = 1:4:5, In:M:Zn = 1:4:6, In:M:Zn = 1:4:7, In:M:Zn = 1:4:8, and In:M:Zn = 1:5:5.

[0192]

Furthermore, in the case where the metal oxide films 108a and 108b are each an In-*M* oxide, when a divalent metal element (e.g., zinc) is not contained as *M*, the metal oxide films 108a and 108b which do not include a spinel crystal structure can be formed. For the metal oxide films 108a and 108b, for example, an In-Ga oxide can be used. The In-Ga oxide can be formed by a sputtering method using an In-Ga metal oxide target (In:Ga = 7:93), for example. To deposit the metal oxide films 108a and 108b by a sputtering method using DC discharge, when an atomic ratio of In:*M* is *x*:*y*, it is preferable that $y/(x + y)$ be less than or equal to 0.96, further preferably less than or equal to 0.95, for example, 0.93.

[0193]

Note that in each of the oxide semiconductor film 108 and the metal oxide films 108a and 108b, the proportions of atoms in the atomic ratio vary within a range of $\pm 40\%$ as an error.

[0194]

<Structure example 4 of semiconductor device>

Next, modification examples of the transistors 150 and 152 are described with reference to FIGS. 11A and 11B and FIGS. 12A and 12B. Note that top views of the transistors in FIG. 11A and FIG. 12A and cross-sectional views in the channel width direction thereof are similar to the top view of FIG. 1A and the cross-sectional view in the channel width direction in FIG. 1B. Furthermore, top views of the transistors in FIG. 11B and FIG. 12B and cross-sectional views in the channel width direction thereof are similar to the top view of FIG. 3A and the cross-sectional view in the channel width direction in FIG. 3B.

[0195]

FIG. 11A is a cross-sectional view of a transistor 150A that is a modification example of the transistor 150 in FIG. 1C. The transistor 150A is different from the transistor 150 in the structure of the pair of electrode layers 112a and 112b.

Specifically, the electrode layer 112a of the transistor 150A in FIG. 11A includes a conductive film 110a in contact with the oxide semiconductor film 108, a conductive film 111a over the conductive film 110a, and a conductive film 117a over the conductive film 111a. The electrode layer 112b of the transistor 150A in FIG. 11A includes a conductive film 110b in contact with the oxide semiconductor film 108, a conductive film 111b over the conductive film 110b, and a conductive film 117b over the conductive film 111b.

[0196]

FIG. 11B is a cross-sectional view of a transistor 152A that is a modification example of the transistor 152 in FIG. 3C. The transistor 152A is different from the transistor 152 in the structure of the pair of electrode layers 112a and 112b. Specifically, the electrode layer 112a of the transistor 152A in FIG. 11B includes the conductive film 110a in contact with the oxide semiconductor film 108, the conductive film 111a over the conductive film 110a, and the conductive film 117a over the conductive film 111a. The electrode layer 112b of the transistor 152A in FIG. 11B includes the conductive film 110b in contact with the oxide semiconductor film 108, the conductive film 111b over the conductive film 110b, and the conductive film 117b over the conductive film 111b.

[0197]

FIG. 12A is a cross-sectional view of a transistor 150B that is a modification example of the transistor 150 in FIG. 1C. The transistor 150B is different from the transistor 150 in the structure of the pair of electrode layers 112a and 112b. Specifically, the electrode layer 112a of the transistor 150B in FIG. 12A includes the conductive film 110a in contact with the oxide semiconductor film 108, and the conductive film 111a over the conductive film 110a. The electrode layer 112b of the transistor 150B in FIG. 12A includes the conductive film 110b in contact with the oxide semiconductor film 108, and the conductive film 111b over the conductive film 110b.

[0198]

FIG. 12B is a cross-sectional view of a transistor 152B that is a modification example of the transistor 152 in FIG. 3C. The transistor 152B is different from the transistor 152 in the structure of the pair of electrode layers 112a and 112b. Specifically, the electrode layer 112a of the transistor 152B in FIG. 12B includes the

conductive film 110a in contact with the oxide semiconductor film 108, and the conductive film 111a over the conductive film 110a. The electrode layer 112b of the transistor 152B in FIG. 12B includes the conductive film 110b in contact with the oxide semiconductor film 108, and the conductive film 111b over the conductive film 110b.

5 [0199]

For the conductive films 110a and 110b used for the transistors 150A, 150B, 152A, and 152B, the above-described Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) can be used. For the conductive films 111a and 111b, a conductive film containing a low-resistance material such as copper (Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a compound containing any of these materials as a main component can be used. To increase the conductivity of the pair of electrode layers 112a and 112b, it is preferable that the thicknesses of the conductive films 111a and 111b be larger than those of the conductive films 110a and 110b. The conductive films 117a and 117b can be formed using, for example, a material similar to that used for the conductive films 110a and 110b.

15 [0200]

A 30-nm-thick Cu-Mn alloy film is used as each of the conductive films 110a and 110b in this embodiment. Furthermore, a 200-nm-thick Cu film is used as each of the conductive films 111a and 111b. Moreover, a 50-nm-thick Cu-Mn alloy film is used as each of the conductive films 117a and 117b.

20 [0201]

When the conductive films 110a and 110b are provided in contact with the oxide semiconductor film 108 as in the structures of the transistors 150A, 150B, 152A, and 152B, a metal element (e.g., Cu) contained in the conductive films 111a and 111b can be inhibited from entering the oxide semiconductor film 108. Furthermore, when the conductive films 117a and 117b are provided in contact with top surfaces of the conductive films 111a and 111b as in the transistors 150A and 152A, heat resistance of the pair of electrode layers 112a and 112b can be improved. That is, the conductive films 117a and 117b function as barrier films for the conductive films 111a and 111b. It is preferable that the conductive films 117a and 117b be provided because they function as protective films for the conductive films 111a and 111b at the time of forming the insulating film 114.

[0202]

The other structures of the transistors 150A, 150B, 152A, and 152B are the same as those of the transistors 150 and 152 and the effect similar to that in the case of the transistors 150 and 152 can be obtained.

5 [0203]

The structures of the transistors of this embodiment can be freely combined with each other.

[0204]

<Method 1 for manufacturing semiconductor device>

10 Next, a method for manufacturing the transistor 150 that is a semiconductor device of one embodiment of the present invention is described below in detail using FIGS. 13A to 13D, FIGS. 14A to 14C, and FIGS. 15A to 15C.

[0205]

15 First, a conductive film is formed over the substrate 102 and processed through a photolithography process and an etching process, whereby the conductive film 104 functioning as a gate electrode layer is formed. Then, the insulating film 106 functioning as a gate insulating film is formed over the conductive film 104. The insulating film 106 includes the insulating films 106a and 106b (see FIG. 13A).

[0206]

20 The conductive film 104 can be formed by a sputtering method, a chemical vapor deposition (CVD) method, a vacuum evaporation method, or a pulsed laser deposition (PLD) method. Alternatively, a coating method or a printing method can be used. Although typical deposition methods are a sputtering method and a plasma chemical vapor deposition (PE-CVD) method, a thermal CVD method such as an MOCVD method, or an ALD method described above may be used.

[0207]

30 In this embodiment, a glass substrate is used as the substrate 102. Furthermore, as the conductive film 104, a 100-nm-thick tungsten film is formed by a sputtering method. Note that instead of the 100-nm-thick tungsten film, a 200-nm-thick Cu-Mn alloy film may be used as the conductive film 104. The Cu-Mn alloy film can be formed by a sputtering method using a Cu-Mn metal target (Cu:Mn =

90:10 [at.%]).

[0208]

The insulating film 106 can be formed by a sputtering method, a PE-CVD method, a thermal CVD method, a vacuum evaporation method, a PLD method, or the like. In this embodiment, a 400-nm-thick silicon nitride film as the insulating film 106a and a 50-nm-thick silicon oxynitride film as the insulating film 106b are formed by a PE-CVD method.

[0209]

Note that the insulating film 106a included in the insulating film 106 can have a stacked-layer structure of silicon nitride films. Specifically, the insulating film 106a can have a three-layer structure of a first silicon nitride film, a second silicon nitride film, and a third silicon nitride film. An example of the three-layer structure is as follows.

[0210]

For example, the first silicon nitride film can be formed to have a thickness of 50 nm under the condition where silane, nitrogen, and an ammonia gas are supplied at flow rates of 200 sccm, 2000 sccm, and 100 sccm, respectively, as a source gas to a reaction chamber of a PE-CVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is supplied using a 27.12 MHz high-frequency power source.

[0211]

The second silicon nitride film can be formed to have a thickness of 300 nm under the condition where silane, nitrogen, and an ammonia gas are supplied at flow rates of 200 sccm, 2000 sccm, and 2000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is supplied using a 27.12 MHz high-frequency power source.

[0212]

The third silicon nitride film can be formed to have a thickness of 50 nm under the condition where silane and nitrogen are supplied at flow rates of 200 sccm and 5000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus; the pressure in the reaction chamber is controlled to 100 Pa, and a power of 2000 W is

supplied using a 27.12 MHz high-frequency power source.

[0213]

Note that the first silicon nitride film, the second silicon nitride film, and the third silicon nitride film can be each formed at a substrate temperature of 350 °C.

5 [0214]

When the insulating film 106a has the three-layer structure of silicon nitride films, for example, in the case where a conductive film containing Cu is used as the conductive film 104, the following effect can be obtained.

[0215]

10 The first silicon nitride film can inhibit diffusion of Cu from the conductive film 104. The second silicon nitride film has a function of releasing hydrogen and can improve withstand voltage of the insulating film functioning as a gate insulating film. The third silicon nitride film releases a small amount of hydrogen and can inhibit diffusion of hydrogen released from the second silicon nitride film.

15 [0216]

Next, the oxide semiconductor film 108 is formed over the insulating film 106 functioning as a gate insulating film (see FIG. 13B).

[0217]

20 In this embodiment, the oxide semiconductor film 108 is formed by a sputtering method using an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:1:1).

[0218]

25 After the oxide semiconductor film 108 is formed, heat treatment may be performed at a temperature higher than or equal to 150 °C and lower than the strain point of the substrate, preferably higher than or equal to 200 °C and lower than or equal to 450 °C, further preferably higher than or equal to 300 °C and lower than or equal to 450 °C. The heat treatment performed here serves as one kind of treatment for increasing the purity of the oxide semiconductor film and can reduce hydrogen, water, and the like contained in the oxide semiconductor film 108. Note that the heat treatment for the purpose of reducing hydrogen, water, and the like may be performed
30 before the oxide semiconductor film 108 is processed into an island shape.

[0219]

An electric furnace, an RTA apparatus, or the like can be used for the heat treatment performed on the oxide semiconductor film 108. With the use of an RTA apparatus, the heat treatment can be performed at a temperature higher than or equal to the strain point of the substrate if the heating time is short. Therefore, the heat treatment time can be shortened.

[0220]

Note that the heat treatment performed on the oxide semiconductor film 108 may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air in which a water content is 20 ppm or less, preferably 1 ppm or less, further preferably 10 ppb or less), or a rare gas (argon, helium, or the like). The atmosphere of nitrogen, oxygen, ultra-dry air, or a rare gas preferably does not contain hydrogen, water, and the like. Furthermore, after heat treatment performed in a nitrogen atmosphere or a rare gas atmosphere, heat treatment may be additionally performed in an oxygen atmosphere or an ultra-dry air atmosphere. As a result, hydrogen, water, and the like can be released from the oxide semiconductor film and oxygen can be supplied to the oxide semiconductor film at the same time. Consequently, the amount of oxygen vacancies in the oxide semiconductor film can be reduced.

[0221]

In the case where the oxide semiconductor film 108 is formed by a sputtering method, as a sputtering gas, a rare gas (typically argon), oxygen, or a mixed gas of a rare gas and oxygen is used as appropriate. In the case of using the mixed gas of a rare gas and oxygen, the proportion of oxygen to a rare gas is preferably increased. In addition, increasing the purity of a sputtering gas is necessary. For example, as an oxygen gas or an argon gas used for a sputtering gas, a gas which is highly purified to have a dew point of $-40\text{ }^{\circ}\text{C}$ or lower, preferably $-80\text{ }^{\circ}\text{C}$ or lower, further preferably $-100\text{ }^{\circ}\text{C}$ or lower, still further preferably $-120\text{ }^{\circ}\text{C}$ or lower is used, whereby entry of moisture or the like into the oxide semiconductor film 108 can be minimized.

[0222]

In the case where the oxide semiconductor film 108 is formed by a sputtering method, a chamber in a sputtering apparatus is preferably evacuated to be a high vacuum state (to the degree of approximately 5×10^{-7} Pa to 1×10^{-4} Pa) with an

adsorption vacuum evacuation pump such as a cryopump in order to remove water or the like, which serves as an impurity for the oxide semiconductor film 108, as much as possible. Alternatively, a turbo molecular pump and a cold trap are preferably combined so as to prevent a backflow of a gas, especially a gas containing carbon or hydrogen from an exhaust system to the inside of the chamber.

[0223]

Next, a conductive film 112 is deposited over the insulating film 106 and the oxide semiconductor film 108 (see FIG. 13C).

[0224]

The conductive film 112 can be formed using a material selected from the above-described materials that can be used for the pair of electrode layers 112a and 112b. In this embodiment, a stacked-layer film including a 30-nm-thick Cu-Mn alloy film and a 200-nm-thick Cu film is used for the conductive film 112. The Cu-Mn alloy film is formed by a sputtering method using a Cu-Mn metal target (Cu:Mn = 90:10 [at.%]). The Cu film is formed by a sputtering method.

[0225]

Next, a resist is applied to the conductive film 112 and is patterned to form resist masks 145a and 145b in desired regions. After that a chemical solution 171 is applied over the resist masks 145a and 145b (see FIG. 13D).

[0226]

The resist masks 145a and 145b can be formed in such a manner that a photosensitive resin is applied and then is exposed and developed in desired regions. Note that the photosensitive resin may be a negative-type or positive-type photosensitive resin. The resist masks 145a and 145b can be formed by an inkjet method, in which case manufacturing costs can be reduced because a photomask is not used.

[0227]

An example of the chemical solution 171 for etching the conductive film 112 includes an etchant containing an organic acid solution and a hydrogen peroxide solution.

[0228]

Next, the resist masks 145a and 145b are removed to form the pair of electrode layers 112a and 112b (see FIG. 14A).

[0229]

The resist masks 145a and 145b can be removed using, for example, a resist peeling apparatus.

[0230]

Next, a chemical solution 173 is applied to the pair of electrode layers 112a and 112b and the oxide semiconductor film 108, and part of a surface of the oxide semiconductor film 108 which is exposed from the pair of electrode layers 112a and 112b is etched (see FIG. 14B).

[0231]

As the chemical solution 173, for example, a dilution of an acid-based chemical solution such as phosphoric acid, nitric acid, hydrofluoric acid, hydrochloric acid, sulfuric acid, acetic acid, or oxalic acid can be used. Note that the chemical solution 173 is not limited to the above acid-based chemical solutions. For example, a chemical solution with which the etching rate of the pair of electrode layers 112a and 112b is lower than that of the oxide semiconductor film 108 may be used as the chemical solution 173. Specifically, a mixed solution of phosphoric acid, a chelating agent (e.g., ethylenediaminetetraacetic acid), and aromatic-compound-based anticorrosive (e.g., benzotriazole (BTA)) can be used.

[0232]

The treatment using the chemical solution 173 can remove part of the constituent elements of the conductive film 112 which are attached to the surface of the oxide semiconductor film 108. Furthermore, the treatment using the chemical solution 173 might remove part of the oxide semiconductor film 108, so that the oxide semiconductor film 108 has a recessed portion. Note that the treatment using the chemical solution 173 is not necessarily performed.

[0233]

Next, the insulating films 114, 116, and 118 functioning as a second gate insulating film and a protective insulating film are formed to cover the insulating film 106, the oxide semiconductor film 108, and the pair of electrode layers 112a and 112b (see FIG. 14C).

[0234]

Note that after the insulating film 114 is formed, the insulating film 116 is preferably formed in succession without exposure to the air. After the insulating film 114 is formed, the insulating film 116 is formed in succession by adjusting at least one of the flow rate of a source gas, pressure, a high-frequency power, and a substrate temperature without exposure to the air, whereby the concentration of impurities attributed to the atmospheric component at the interface between the insulating film 114 and the insulating film 116 can be reduced and oxygen in the insulating film 116 can be moved to the oxide semiconductor film 108; accordingly, the amount of oxygen vacancy in the oxide semiconductor film 108 can be reduced.

[0235]

For example, as the insulating film 114, a silicon oxynitride film can be formed by a PE-CVD method. In this case, a deposition gas containing silicon and an oxidizing gas are preferably used as a source gas. Typical examples of the deposition gas containing silicon include silane, disilane, trisilane, and silane fluoride. Examples of the oxidizing gas include dinitrogen monoxide and nitrogen dioxide. An insulating film containing nitrogen and having a small number of defects can be formed as the insulating film 114 by a PE-CVD method under the condition where the ratio of the oxidizing gas to the deposition gas is higher than 20 times and lower than 100 times, preferably higher than or equal to 40 times and lower than or equal to 80 times and the pressure in a treatment chamber is lower than 100 Pa, preferably lower than or equal to 50 Pa.

[0236]

In this embodiment, a silicon oxynitride film is formed as the insulating film 114 by a PE-CVD method under the condition where the substrate 102 is held at a temperature of 220 °C, silane at a flow rate of 50 sccm and dinitrogen monoxide at a flow rate of 2000 sccm are used as a source gas, the pressure in the treatment chamber is 20 Pa, and a high-frequency power of 100 W at 13.56 MHz (1.6×10^{-2} W/cm² as the power density) is supplied to parallel-plate electrodes.

[0237]

As the insulating film 116, a silicon oxide film or a silicon oxynitride film is

formed under the following conditions: the substrate placed in a treatment chamber of the PE-CVD apparatus that is vacuum-evacuated is held at a temperature higher than or equal to 180 °C and lower than or equal to 280 °C, preferably higher than or equal to 200 °C and lower than or equal to 240 °C, the pressure is greater than or equal to 100 Pa and less than or equal to 250 Pa, preferably greater than or equal to 100 Pa and less than or equal to 200 Pa with introduction of a source gas into the treatment chamber, and a high-frequency power of greater than or equal to 0.17 W/cm² and less than or equal to 0.5 W/cm², preferably greater than or equal to 0.25 W/cm² and less than or equal to 0.35 W/cm² is supplied to an electrode provided in the treatment chamber.

10 [0238]

As the deposition conditions of the insulating film 116, the high-frequency power having the above power density is supplied to the reaction chamber having the above pressure, whereby the decomposition efficiency of the source gas in plasma is increased, oxygen radicals are increased, and oxidation of the source gas is promoted; therefore, the oxygen content of the insulating film 116 becomes higher than that in the stoichiometric composition. On the other hand, in the film formed at a substrate temperature within the above temperature range, a bond between silicon and oxygen is weak, and accordingly, part of oxygen in the film is released by heat treatment in a later step. Thus, it is possible to form an oxide insulating film which contains oxygen at a higher proportion than oxygen in the stoichiometric composition and from which part of oxygen is released by heating.

20 [0239]

Note that the insulating film 114 functions as a protective film for the oxide semiconductor film 108 in the step of forming the insulating film 116. Therefore, the insulating film 116 can be formed using the high-frequency power having a high power density while damage to the oxide semiconductor film 108 is reduced.

25 [0240]

Note that in the deposition conditions of the insulating film 116, when the flow rate of the deposition gas containing silicon with respect to the oxidizing gas is increased, the amount of defects in the insulating film 116 can be reduced. Typically, it is possible to form an oxide insulating layer in which the amount of defects is small,

30

i.e., the spin density corresponding to a signal which appears at $g = 2.001$ due to a dangling bond of silicon is lower than 6×10^{17} spins/cm³, preferably lower than or equal to 3×10^{17} spins/cm³, further preferably lower than or equal to 1.5×10^{17} spins/cm³ by ESR measurement. As a result, the reliability of the transistor can be improved.

5 [0241]

After the insulating films 114 and 116 are formed, heat treatment is performed. By the heat treatment, part of oxygen contained in the insulating films 114 and 116 can be moved to the oxide semiconductor film 108, so that the amount of oxygen vacancy contained in the oxide semiconductor film 108 can be further reduced. After the heat

10 treatment, the insulating film 118 is formed.

[0242]

The temperature of the heat treatment performed on the insulating films 114 and 116 is typically higher than or equal to 150 °C and lower than or equal to 400 °C, preferably higher than or equal to 300 °C and lower than or equal to 400 °C, further

15 preferably higher than or equal to 320 °C and lower than or equal to 370 °C. The heat treatment may be performed under an atmosphere of nitrogen, oxygen, ultra-dry air (air in which a water content is 20 ppm or less, preferably 1 ppm or less, more preferably 10 ppb or less), or a rare gas (argon, helium, or the like). Note that an electric furnace, an RTA apparatus, or the like can be used for the heat treatment, in which it is preferable

20 that hydrogen, water, and the like not be contained in the nitrogen, oxygen, ultra-dry air, or rare gas.

[0243]

In this embodiment, the heat treatment is performed at 350 °C for one hour in a mixed atmosphere of nitrogen and oxygen.

25 [0244]

In the case where water, hydrogen, or the like is contained in the insulating films 114 and 116, when the insulating film 118 having a function of blocking water, hydrogen, and the like is formed and then heat treatment is performed, water, hydrogen, or the like contained in the insulating films 114 and 116 might be moved to the oxide

30 semiconductor film 108, so that defects might be generated in the oxide semiconductor film 108. Thus, when heat treatment is performed before formation of the insulating

film 118, water or hydrogen contained in the insulating films 114 and 116 can be effectively reduced.

[0245]

Note that when the insulating film 116 is formed over the insulating film 114 while being heated, oxygen can be moved to the oxide semiconductor film 108 and oxygen vacancies in the oxide semiconductor film 108 can be reduced. For this reason, the heat treatment is not necessarily performed.

[0246]

Furthermore, by heat treatment after the insulating films 114 and 116 are formed, a coating film might be formed in the vicinity of the interface between the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b and in the vicinity of the interface between the insulating film 106b and the pair of electrode layers 112a and 112b. Examples of the coating film are the above-described coating films 113a and 113b. Even in the case where the insulating film 114 is formed during heating, the coating films 113a and 113b might be formed.

[0247]

In the case where the insulating film 118 is formed by a PE-CVD method, the substrate temperature is preferably set to higher than or equal to 300 °C and lower than or equal to 400 °C, more preferably higher than or equal to 320 °C and lower than or equal to 370 °C, so that a dense film can be formed.

[0248]

For example, in the case where a silicon nitride film is formed by a PE-CVD method as the insulating film 118, a deposition gas containing silicon, nitrogen, and ammonia are preferably used as a source gas. A small amount of ammonia compared to the amount of nitrogen is used, whereby ammonia is dissociated in the plasma and activated species are generated. The activated species cleave a bond between silicon and hydrogen which are contained in a deposition gas containing silicon and a triple bond between nitrogen molecules. As a result, a dense silicon nitride film having few defects, in which bonds between silicon and nitrogen are promoted and bonds between silicon and hydrogen is few, can be formed. On the other hand, when the amount of ammonia with respect to nitrogen is large, decomposition of a deposition gas containing

silicon and decomposition of nitrogen are not promoted, so that a sparse silicon nitride film in which bonds between silicon and hydrogen remain and defects are increased is formed. Therefore, in the source gas, a flow rate ratio of the nitrogen to the ammonia is set to be greater than or equal to 5 and less than or equal to 50, preferably greater than
5 or equal to 10 and less than or equal to 50.

[0249]

In this embodiment, with the use of a PE-CVD apparatus, a 50-nm-thick silicon nitride film is formed as the insulating film 118 using silane, nitrogen, and ammonia as a source gas. The flow rate of silane is 50 sccm, the flow rate of nitrogen is 5000 sccm,
10 and the flow rate of ammonia is 100 sccm. The pressure in the treatment chamber is 100 Pa, the substrate temperature is 350 °C, and high-frequency power of 1000 W is supplied to parallel-plate electrodes with a 27.12 MHz high-frequency power source. Note that the PE-CVD apparatus is a parallel-plate PE-CVD apparatus in which the electrode area is 6000 cm², and the power per unit area (power density) into which the
15 supplied power is converted is 1.7×10^{-1} W/cm².

[0250]

Heat treatment may be performed after the formation of the insulating film 118. The heat treatment is performed typically at a temperature of higher than or equal to 150 °C and lower than or equal to 400 °C, preferably higher than or equal to 300 °C and
20 lower than or equal to 400 °C, more preferably higher than or equal to 320 °C and lower than or equal to 370 °C. When the heat treatment is performed, the amount of hydrogen and water in the insulating films 114 and 116 is reduced and accordingly the generation of defects in the oxide semiconductor film 108 described above is inhibited.

[0251]

25 Next, the openings 142a and 142b are formed in the insulating films 106a, 106b, 114, 116, and 118. In addition, the opening 142c is formed in the insulating films 114, 116, and 118 (see FIG. 15A).

[0252]

The openings 142a and 142b reach the conductive film 104. The opening
30 142c reaches the electrode layer 112b. The openings 142a, 142b, and 142c can be formed in the same process. For example, a pattern may be formed in a desired region

using a half-tone mask (or a gray-tone mask, a phase-shift mask, or the like), and the openings 142a, 142b, and 142c can be formed with a dry-etching apparatus. Note that a half-tone mask or a gray-tone mask may be used as needed, and they are not necessarily used. The openings 142a and 142b and the opening 142c may be formed
5 in different formation processes. In such a case, the openings 142a and 142b might have two steps.

[0253]

Next, a conductive film 120 is formed over the insulating film 118 to cover the openings 142a, 142b, and 142c (see FIG. 15B).

10 [0254]

For the conductive film 120, for example, a material including one of indium (In), zinc (Zn), and tin (Sn) can be used. In particular, for the conductive film 120, a light-transmitting conductive material such as indium oxide containing tungsten oxide, indium zinc oxide containing tungsten oxide, indium oxide containing titanium oxide,
15 indium tin oxide containing titanium oxide, indium tin oxide (ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added can be used. The conductive film 120 can be formed by a sputtering method, for example.

[0255]

Then, the conductive film 120 is processed into a desired shape, whereby the
20 conductive films 120a and 120b are formed (see FIG. 15C).

[0256]

To form the conductive films 120a and 120b, for example, a dry etching method, a wet etching method, or a combination of dry etching and wet etching is used.

[0257]

25 Through the above process, the transistor 150 illustrated in FIGS. 1A to 1C can be formed.

[0258]

<Method 2 for manufacturing semiconductor device>

Next, a method for manufacturing the transistor 152 that is a semiconductor
30 device of one embodiment of the present invention is described below in detail using FIGS. 16A to 16D, FIGS. 17A to 17C, and FIGS. 18A and 18B.

[0259]

First, the steps up to the step in FIG. 13B are performed. After that, the protective insulating film 109 is formed over the insulating film 106b and the oxide semiconductor film 108 (see FIG. 16A).

[0260]

5 As the protective insulating film 109, for example, a silicon oxide film or a silicon oxynitride film is formed by a PE-CVD method, a sputtering method, or the like. In this embodiment, a 400-nm-thick silicon oxide film is deposited by a sputtering method.

[0261]

10 Next, the openings 140a and 140b reaching the oxide semiconductor film 108 are formed in the protective insulating film 109 (see FIG. 16B).

[0262]

The openings 140a and 140b are formed in such a manner that a resist mask is formed over the protective insulating film 109 through a photolithography process using a photomask, and then openings are formed in the protective film 109 using the resist mask. Note that at the time of forming the openings 140a and 140b, part of the oxide semiconductor film 108 might be etched owing to overetching, so that the oxide semiconductor film 108 might have a recessed portion. The openings 140a and 140b are formed by a wet etching method, a dry etching method, or a combination of a wet etching method and a dry etching method.

20 [0263]

Then, the conductive film 112 is formed over the protective insulating film 109 and the oxide semiconductor film 108 to cover the openings 140a and 140b (see FIG. 16C).

25 [0264]

The conductive film 112 can be formed using any of the materials and methods described above.

[0265]

Next, a resist is applied to the conductive film 112 and is patterned to form resist masks 145a and 145b in desired regions. After that the chemical solution 171 is applied over the resist masks 145a and 145b (see FIG. 16D).

30 [0266]

The resist masks 145a and 145b can be formed using any of the materials and methods described above. For the chemical solution 171, the material described above can be used.

[0267]

5 Next, the resist masks 145a and 145b are removed to form the pair of electrode layers 112a and 112b (see FIG. 17A).

[0268]

For a method for removing the resist masks 145a and 145b, the above-described method can be referred to.

10 [0269]

Next, the insulating films 114, 116, and 118 functioning as a second gate insulating film and a protective insulating film are formed to cover the protective insulating film 109 and the pair of electrode layers 112a and 112b (see FIG. 17B).

[0270]

15 The insulating films 114, 116, and 118 can be formed using any of the materials and methods described above.

[0271]

Note that the protective insulating film 109 functions as a protective film for the oxide semiconductor film 108 in the step of forming the insulating film 114.

20 Furthermore, the insulating film 114 functions as a protective film for the protective insulating film 109 in the step of forming the insulating film 116. Therefore, the insulating film 116 can be formed using the high-frequency power having a high power density while damage to the oxide semiconductor film 108 is reduced.

[0272]

25 After the insulating films 114 and 116 are formed, heat treatment is performed. By the heat treatment, part of oxygen contained in the insulating films 114 and 116 can be moved to the oxide semiconductor film 108, so that the amount of oxygen vacancy contained in the oxide semiconductor film 108 can be further reduced. After the heat treatment, the insulating film 118 is formed.

30 [0273]

In this embodiment, the heat treatment is performed at 350 °C for one hour in an atmosphere of nitrogen and oxygen.

[0274]

Next, the openings 142a and 142b are formed in the insulating films 106a, 106b, 114, 116, and 118 and the protective insulating film 109. In addition, the opening 142c is formed in the insulating films 114, 116, and 118 (see FIG. 17C).

5 [0275]

The openings 142a and 142b reach the conductive film 104. The opening 142c reaches the electrode layer 112b. The openings 142a, 142b, and 142c can be formed using the method described above.

[0276]

10 Next, the conductive film 120 is formed over the insulating film 118 to cover the openings 142a, 142b, and 142c (see FIG. 18A).

[0277]

Then, the conductive film 120 is processed into a desired shape, whereby the conductive films 120a and 120b are formed (see FIG. 18B).

15 [0278]

The conductive film 120 can be formed using the material and method described above. The conductive films 120a and 120b can be formed using the method described above.

[0279]

20 Through the above process, the transistor 152 illustrated in FIGS. 3A to 3C can be formed.

[0280]

<Method 3 for manufacturing semiconductor device>

25 Next, methods for manufacturing the transistors 154, 156, 158, 160, 150A, 150B, 152A, and 152B that are semiconductor devices of embodiments of the present invention are described below in detail.

[0281]

The metal oxide films 108a and 108b included in the transistor 154 in FIGS. 5A to 5C and the metal oxide films 108a and 108b included in the transistor 156 in
30 FIGS. 6A to 6C can be formed after the oxide semiconductor film 108 illustrated in FIG. 13B is formed.

[0282]

In this embodiment, the metal oxide film 108a is formed by a sputtering method using an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:3:6). Furthermore, the metal oxide film 108b is formed by a sputtering method using an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:4:5).

5 [0283]

In the case where the oxide semiconductor film 108 and the metal oxide films 108a and 108b are formed by a sputtering method, a power supply device for generating plasma can be an RF power supply device, an AC power supply device, a DC power supply device, or the like as appropriate. Note that it is preferable to use DC discharge applicable to a large-sized substrate in deposition because the productivity of the semiconductor device can be increased.

[0284]

The metal oxide film 108b included in the transistor 158 in FIGS. 8A to 8C and the metal oxide film 108b included in the transistor 160 in FIGS. 9A to 9C can be formed after the oxide semiconductor film 108 illustrated in FIG. 13B is formed.

[0285]

In this embodiment, the metal oxide film 108b is formed by a sputtering method using an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:3:6).

[0286]

20 In the case of the transistor 150A in FIG. 11A, in the step of forming the conductive film 112 illustrated in FIG. 13C, a conductive film to be the conductive films 110a and 110b, a conductive film to be the conductive films 111a and 111b, and a conductive film to be the conductive films 117a and 117b are stacked. After that, the conductive films are collectively etched, whereby the transistor 150A illustrated in FIG. 11A can be formed.

25 [0287]

In the case of the transistor 152A in FIG. 11B, in the step of forming the conductive film 112 illustrated in FIG. 16C, a conductive film to be the conductive films 110a and 110b, a conductive film to be the conductive films 111a and 111b, and a conductive film to be the conductive films 117a and 117b are stacked. After that, the conductive films are collectively etched, whereby the transistor 152A illustrated in FIG.

11B can be formed.

[0288]

In the case of the transistor 150B in FIG. 12A, in the step of forming the conductive film 112 illustrated in FIG. 13C, a conductive film to be the conductive films 110a and 110b and a conductive film to be the conductive films 111a and 111b are stacked. After that, the conductive films are collectively etched, whereby the transistor 150B illustrated in FIG. 12A can be formed.

[0289]

In the case of the transistor 152B in FIG. 12B, in the step of forming the conductive film 112 illustrated in FIG. 16C, a conductive film to be the conductive films 110a and 110b and a conductive film to be the conductive films 111a and 111b are stacked. After that, the conductive films are collectively etched, whereby the transistor 152B illustrated in FIG. 12B can be formed.

[0290]

For example, when a Cu-Mn alloy film is used for the conductive film to be the conductive films 110a and 110b and the conductive film to be the conductive films 117a and 117b, and a Cu film is used for the conductive film to be the conductive films 111a and 111b, these films can be collectively processed through a wet etching process; therefore the manufacturing cost can be reduced.

[0291]

The structure and method described in this embodiment can be implemented by being combined as appropriate with any of the other structures and methods described in the other embodiments.

[0292]

(Embodiment 2)

In this embodiment, a semiconductor device that is one embodiment of the present invention and is different from that in Embodiment 1 and a method of manufacturing the semiconductor device are described with reference to FIGS. 19A to 19C, FIGS. 20A and 20B, FIGS. 21A and 21B, FIGS. 22A to 22C, FIGS. 23A to 23C, FIGS. 24A to 24C, FIGS. 25A to 25C, FIGS. 26A to 26C, FIGS. 27A and 27B, FIGS. 28A to 28C, FIGS. 29A and 29B, FIGS. 30A to 30C, FIGS. 31A to 31C, FIGS. 32A to 32C, FIGS. 33A and 33B, FIGS. 34A and 34B, FIGS. 35A to 35C, and FIGS. 36A to

36C. Note that common reference numerals are used for components that have functions similar to functions of the components of the transistor 150 described in Embodiment 1, and detailed descriptions of the components are omitted.

[0293]

5 <Structure example 5 of semiconductor device>

FIG. 19A is a top view of a transistor 151 that is a semiconductor device of one embodiment of the present invention. FIG. 19B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 19A. FIG. 19C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 19A.

10 [0294]

The transistor 151 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; and the pair of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108.

[0295]

The insulating film 106 functioning as a gate insulating film in the transistor 151 has a two-layer structure of the insulating film 106a and the insulating film 106b.

20 [0296]

In FIGS. 19B and 19C, the insulating films 114, 116, and 118 functioning as a protective insulating film for the oxide semiconductor film 108 are formed over the transistor 151, specifically, over the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b. In addition, the opening 142c reaching the electrode layer 112b of the transistor 151 is formed in the insulating films 114, 116, and 118, and the conductive film 120a is formed over the insulating film 118 to cover the opening 142c. The conductive film 120a functions as, for example, a pixel electrode layer of a display device.

[0297]

30 The pair of electrode layers 112a and 112b in the transistor 151 functions as a source electrode layer and a drain electrode layer. Note that in the transistor 151, the conductive film 104 functioning as a gate electrode layer and one or both of the pair of

electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer include at least a Cu-X alloy film (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti); for example, it is preferable that the conductive film 104 and one or both of the pair of electrode layers 112a and 112b have a single-layer structure of a Cu-X alloy film or a stacked-layer structure of a Cu-X alloy film and a conductive film containing a low-resistance material such as copper (Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a compound containing any of these materials as a main component.

[0298]

The conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer also function as lead wirings or the like. Therefore, when the conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer are each formed using a Cu-X alloy film, or a Cu-X alloy film and a conductive film containing a low-resistance material such as copper, aluminum, gold, or silver, whereby a semiconductor device with reduced wiring delay can be manufactured even when a large-sized substrate is used as the substrate 102.

[0299]

Note that in the manufacturing process of the transistor 151 in FIGS. 19A to 19C, for example, the conductive film 104 functioning as a gate electrode layer, the oxide semiconductor film 108, the pair of electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer, the insulating films 114, 116, and 118 functioning as a protective insulating film, and the conductive film 120a functioning as a pixel electrode layer can each be processed by a process using a chemical solution, i.e., what is called a wet etching process. Accordingly, a method for manufacturing a semiconductor device at low manufacturing cost can be provided.

[0300]

Furthermore, the conductive film 104 used as a gate electrode layer and the pair of electrode layers 112a and 112b used as a source electrode layer and a drain electrode layer can be formed using the same kinds of materials (here, Cu-X alloy films), whereby they can be processed using the same chemical solution. Since the oxide

semiconductor film 108 and the conductive film 120a functioning as a pixel electrode layer can be formed using the same kinds of materials (here, materials including indium), they can be processed using the same chemical solution. Therefore, a method for manufacturing a semiconductor device with high reliability can be provided.

5 [0301]

Here, an effect obtained in the case where a Cu-*X* alloy film is used for the conductive film 104 functioning as a gate electrode layer is described below.

[0302]

For example, for the conductive film 104 functioning as a gate electrode layer,
10 a Cu-Mn alloy film is selected from Cu-*X* alloy films (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti). When a Cu-Mn alloy film is used for the conductive film 104 functioning as a gate electrode layer, adhesion with a base film (here, the substrate 102) can be increased. Specifically, after the Cu-Mn alloy film is formed, for example, heat treatment is performed or the insulating film 106 is deposited by substrate heating, whereby Mn in
15 the Cu-Mn alloy film is segregated; as a result, a coating film might be formed at the interface with the substrate 102. The coating film improves adhesion between the Cu-Mn alloy film and the substrate 102. Furthermore, segregation of Mn in the Cu-Mn alloy film causes a reduction in the Mn concentration of part of the Cu-Mn alloy film; as a result, the conductive film 104 can have high conductivity.

20 [0303]

An insulating film functioning as a base film may be provided between the substrate 102 and the conductive film 104 functioning as a gate electrode layer. Examples of the insulating film include a silicon oxide film, a silicon oxynitride film, a silicon nitride oxide film, a silicon nitride film, and an aluminum oxide film. The
25 insulating film can be formed with a PE-CVD apparatus or a sputtering apparatus, for example. In the case where the insulating film functioning as a base film is provided between the substrate 102 and the conductive film 104 functioning as a gate electrode layer, the coating film might be formed at the interface between the insulating film and the conductive film 104.

30 [0304]

Here, the coating film that might be formed at the interface between the insulating film and the conductive film 104 functioning as a gate electrode layer is

described below with reference to FIGS. 20A and 20B.

[0305]

FIGS. 20A and 20B are each an enlarged cross-sectional view of the substrate 102, the conductive film 104, and the insulating film 106. Note that FIG. 20A illustrates an example including the conductive film 104 having a single-layer structure, here, including a Cu-Mn alloy film having a single-layer structure. FIG. 20B illustrates an example including the conductive film 104 having a stacked-layer structure, here, a stacked-layer structure of a Cu-Mn alloy film as a conductive film 104_1, a Cu film as a conductive film 104_2, and a Cu-Mn alloy film as a conductive film 104_3.

[0306]

In FIG. 20A, a coating film 101 is formed to surround the conductive film 104. The coating film 101 covers at least one of the top surface, the bottom surface, and the side surface of the conductive film 104. The coating film 101 can be an Mn film or an Mn compound film which is formed owing to precipitation of Mn in the Cu-Mn alloy film. The Mn compound film is a compound formed by reaction with an element of the constituent elements of the substrate 102 and the insulating film 106, and examples of the compound include Mn hydride, Mn carbide, Mn oxide, Mn nitride, and Mn silicide when the substrate 102 and the insulating film 106 contain hydrogen, carbon, oxygen, nitrogen, silicon, or the like.

[0307]

In FIG. 20B, the coating film 101 is formed to surround the conductive film 104. The coating film 101 has the same structure as that described above. Note that also in the case where a Cu film is used as the conductive film 104_2, the coating film 101 might be formed at the periphery of the conductive film 104_2. For example, the coating film 101 is formed at the periphery of the conductive film 104_2 in such a manner that at the time of collectively etching the conductive film 104 including the conductive films 104_1, 104_2, and 104_3, Mn of part of the Cu-Mn alloy film used for the conductive film 104_1 or the conductive film 104_3 is attached to the periphery or sidewall of the conductive films 104_2. Alternatively, the coating film 101 is formed in such a manner that in the step of forming the insulating film 106 after formation of

the conductive film 104 or in heat treatment in a later step, Mn of part of the Cu-Mn alloy film used for the conductive film 104_1 or the conductive film 104_3 diffuses to the periphery or sidewall of the conductive film 104_2.

[0308]

5 In this manner, formation of the coating film 101 surrounding the conductive film 104 makes it possible to inhibit diffusion of a copper element contained in the conductive film 104. Note that it is preferable that the conductive film 104 partly contain an Mn oxide.

[0309]

10 Furthermore, the insulating film 106a and the insulating film 106b are formed over the conductive film 104 in the transistor 151.

[0310]

For example, a silicon nitride film can be used for the insulating film 106a, and a silicon oxynitride film can be used for the insulating film 106b. When the insulating film 106 functioning as a gate insulating film has a stacked-layer structure of the
15 insulating film 106a and the insulating film 106b, diffusion of Cu from the Cu-X alloy film, which is used for the conductive film 104 functioning as a gate electrode layer, can be further reduced. Specifically, a silicon nitride film which can be used as the insulating film 106a can inhibit diffusion of Cu from the conductive film 104. Note
20 that when a silicon nitride film is used as the insulating film 106a, the silicon nitride film may contain a large amount of hydrogen.

[0311]

In addition, when the insulating film 106 functioning as a gate insulating film has a stacked-layer structure of the insulating film 106a and the insulating film 106b,
25 hydrogen which can diffuse from the insulating film 106a can be reduced owing to the insulating film 106b.

[0312]

Therefore, use of the insulating film having the above structure as a gate insulating film can inhibit Cu contained in the conductive film 104 and hydrogen
30 contained in the insulating film 106 from diffusing to the oxide semiconductor film 108.

[0313]

In this manner, in the case where a conductive film containing Cu is used as a gate electrode layer, an impurity which can diffuse to an oxide semiconductor film can be reduced, so that a highly reliable semiconductor device can be provided. Furthermore, the conductive film containing Cu that is used as a gate electrode layer can be used for a wiring, a signal line, or the like. Therefore, a semiconductor device with reduced wiring delay can be provided.

[0314]

Next, an effect obtained in the case where a Cu-*X* alloy film is used for the pair of electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer is described below.

[0315]

For example, for the pair of electrode layers 112a and 112b, a Cu-Mn alloy film is selected from Cu-*X* alloy films (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti). When the Cu-Mn alloy film is used for the pair of electrode layers 112a and 112b, adhesion with the base film (here, the insulating film 106b and the oxide semiconductor film 108) can be improved. Furthermore, the use of the Cu-Mn alloy film enables a favorable ohmic contact with the oxide semiconductor film 108.

[0316]

In addition, a Cu-*X* alloy film is used for the pair of electrode layers 112a and 112b in contact with the oxide semiconductor film 108, whereby *X* (*X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) in the Cu-*X* alloy film might form a coating film of *X* at the interface between the Cu-*X* alloy film and the oxide semiconductor film. The coating film can inhibit Cu in the Cu-*X* alloy film from entering the oxide semiconductor film 108.

[0317]

Here, the coating film that might be formed at the interfaces between the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b is described below with reference to FIGS. 21A and 21B.

[0318]

FIG. 21A is an enlarged cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the pair of electrode layers 112a and 112b, and the insulating films 114, 116, and 118. FIG. 21B is an enlarged cross-sectional view of the insulating film 106, the oxide semiconductor film 108, the metal oxide films 108a

and 108b, the pair of electrode layers 112a and 112b, and the insulating films 114, 116, and 118. Note that FIGS. 21A and 21B each illustrate an example including the pair of electrode layers 112a and 112b having a single-layer structure, here, including a Cu-Mn alloy film having a single-layer structure.

5 [0319]

In FIG. 21A, the coating films 113a and 113b are formed to surround the pair of electrode layers 112a and 112b. The coating films 113a and 113b covers at least one of the top surfaces, the bottom surfaces, and the side surfaces of the pair of electrode layers 112a and 112b. The coating films 113a and 113b can be an Mn film
10 or an Mn compound film which is formed owing to precipitation of Mn in the Cu-Mn alloy film. The Mn compound film is a compound formed by reaction with an element contained in the oxide semiconductor film 108, and examples of the compound include Mn oxide, In-Mn oxide Ga-Mn oxide, In-Ga-Mn oxide, In-Ga-Zn-Mn oxide. Alternatively, the Mn compound film is a compound formed by reaction with an
15 element contained in the insulating film 114, and examples of the compound include Mn hydride, Mn carbide, Mn oxide, Mn nitride, and Mn silicide when the insulating film 114 contains hydrogen, carbon, oxygen, nitrogen, silicon, or the like.

[0320]

In FIG. 21B, the coating films 115a and 115b are formed to surround the pair
20 of electrode layers 112a and 112b. The coating films 115a and 115b covers at least one of the top surfaces, the bottom surfaces, and the side surfaces of the pair of electrode layers 112a and 112b. The coating films 115a and 115b can be an Mn film or an Mn compound film which is formed owing to precipitation of Mn in the Cu-Mn alloy film. The Mn compound film is a compound formed by reaction with an element
25 contained in the oxide semiconductor film 108 or the metal oxide films 108a and 108b, and examples of the compound include Mn oxide, In-Mn oxide Ga-Mn oxide, In-Ga-Mn oxide, In-Ga-Zn-Mn oxide. Alternatively, the Mn compound film is a compound formed by reaction with an element contained in the insulating film 114, and examples of the compound include Mn hydride, Mn carbide, Mn oxide, Mn nitride, and
30 Mn silicide when the insulating film 114 contains hydrogen, carbon, oxygen, nitrogen, silicon, or the like.

[0321]

In this manner, when the coating films 113a and 113b or the coating films 115a and 115b are formed to surround the pair of electrode layers 112a and 112b, it is possible to inhibit diffusion of a copper element contained in the pair of electrode layers 112a and 112b.

5 [0322]

<Method 4 for manufacturing semiconductor device>

Here, a method for manufacturing the transistor 151 that is a semiconductor device of one embodiment of the present invention is described below in detail with reference to FIGS. 22A to 22C, FIGS. 23A to 23C, FIGS. 24A to 24C, FIGS. 25A to 25C, FIGS. 26A to 26C, and FIGS. 27A and 27B.

10 [0323]

First, a conductive film 103 is formed over the substrate 102 (see FIG. 22A).

[0324]

The conductive film 103 can be formed using the material in the description of the conductive film 104. In this embodiment, a 300-nm-thick Cu-Mn alloy film is used as the conductive film 103. Note that the Cu-Mn alloy film can be formed by a sputtering method using a Cu-Mn metal target (Cu:Mn = 90:10 [at.%]). Note that the conductive film 103 may be called a first conductive film.

[0325]

20 Next, a resist is applied to the conductive film 103 and is patterned to form a resist mask 141 in a desired region. After that, the chemical solution 171 is applied over the conductive film 103 and the resist mask 141 to etch the conductive film 103 (see FIG. 22B).

[0326]

25 The resist mask 141 can be formed in such a manner that a photosensitive resin is applied and then is exposed and developed in a desired region. Note that the photosensitive resin may be a negative-type or positive-type photosensitive resin. Note that the resist mask 141 may be formed by an inkjet method, in which case manufacturing costs can be reduced because a photomask is not used.

30 [0327]

An example of the chemical solution 171 for etching the conductive film 103 includes an etchant containing an organic acid solution and a hydrogen peroxide

solution.

[0328]

When the conductive film 103 includes a Cu-Mn alloy film, adhesion with a base film (here, the substrate 102) is improved. The structure in which the conductive film 103 includes the Cu-Mn alloy film enables the manufacturing cost to be reduced because wet etching process can be used in the processing.

[0329]

Next, the resist mask 141 is removed. The conductive film 103 is processed to be the conductive film 104 functioning as a gate electrode layer, using the chemical solution 171 (see FIG. 22C).

[0330]

The resist mask 141 can be removed using, for example, a resist peeling apparatus.

[0331]

Next, the insulating film 106 functioning as a gate insulating film is formed over the substrate 102 and the conductive film 104. Note that the insulating film 106 includes the insulating films 106a and 106b (see FIG. 23A).

[0332]

The insulating film 106 can be formed by a sputtering method, a PE-CVD method, a thermal CVD method, a vacuum evaporation method, a PLD method, or the like. In this embodiment, a 400-nm-thick silicon nitride film as the insulating film 106a functioning as a gate insulating film and a 50-nm-thick silicon oxynitride film as the insulating film 106b are formed by a PE-CVD method. Note that the insulating film 106 may be called a first insulating film.

[0333]

Then, the oxide semiconductor film 108 is formed over the insulating film 106 functioning as a gate insulating film (see FIG. 23B).

[0334]

In this embodiment, the oxide semiconductor film 108 is formed by a sputtering method using an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:1:1).

[0335]

Next, a resist is applied to the oxide semiconductor film 108 and is patterned to

form a resist mask 142 in a desired region. After that, a chemical solution 172 is applied over the oxide semiconductor film 108 and the resist mask 142 to etch the oxide semiconductor film 108 (see FIG. 23C).

[0336]

5 The resist mask 142 can be formed using a method similar to that of the resist mask 141.

[0337]

As the chemical solution 172 for etching the oxide semiconductor film 108, for example, a solution containing oxalic acid can be used. An additive or the like may be
10 mixed in the chemical solution 172. A specific example of the chemical solution 172 is a mixed solution containing oxalic acid, water, and an additive. As for the composition of the mixed solution, the oxalic acid content, the water content, and the additive content are set to 5 % or less, 95 % or more, and 1 % less, respectively, so that the total of the percentages is 100 %.

15 [0338]

Next, the resist mask 142 is removed. Note that the oxide semiconductor film 108 is processed to be the island-shaped oxide semiconductor film 108, using the chemical solution 172 (see FIG. 24A).

[0339]

20 The resist mask 142 can be removed using an apparatus similar to that used for removing the resist mask 141.

[0340]

After the oxide semiconductor film 108 is formed, heat treatment may be performed at a temperature higher than or equal to 150 °C and lower than the strain
25 point of the substrate, preferably higher than or equal to 200 °C and lower than or equal to 450 °C, further preferably higher than or equal to 300 °C and lower than or equal to 450 °C.

[0341]

Next, a conductive film 111 is formed over the insulating film 106 and the
30 island-shaped oxide semiconductor film 108 (see FIG. 24B).

[0342]

The conductive film 111 can be formed using the material in the description of the pair of electrode layers 112a and 112b. In this embodiment, a 400-nm-thick Cu-Mn alloy film formed by a sputtering method is used. Note that the conductive film 111 may be called a second conductive film.

5 [0343]

Next, a resist is applied to the conductive film 111 and is patterned to form a resist mask 143 in a desired region. After that, the chemical solution 171 is applied over the conductive film 111 and the resist mask 143 to etch the conductive film 111 (see FIG. 24C).

10 [0344]

The resist mask 143 can be formed using a method similar to that of the resist mask 141.

[0345]

When the conductive film 103 and the conductive film 111 are formed using the same kinds of materials, here, formed to contain a Cu-Mn alloy film, the conductive film 103 and the conductive film 111 can be processed using the same chemical solution (here, the chemical solution 171). Therefore, a semiconductor device whose manufacturing cost is low or a semiconductor device with high productivity can be provided.

20 [0346]

Next, the resist mask 143 is removed. Note that the conductive film 111 is processed to be the pair of electrode layers 112a and 112b functioning as a source electrode layer and a drain electrode layer, using the chemical solution 171 (see FIG. 25A).

25 [0347]

The resist mask 143 can be removed using an apparatus similar to that used for removing the resist mask 141.

[0348]

Next, the chemical solution 173 is applied over the island-shaped oxide semiconductor film 108 and the pair of electrode layers 112a and 112b, and part of a surface of the island-shaped oxide semiconductor film 108 which is exposed from the pair of electrode layers 112a and 112b is etched (see FIG. 25B).

[0349]

A material which is similar to that described in Embodiment 1 can be used for the chemical solution 173.

[0350]

5 By the treatment using the chemical solution 173, part of constituent elements of the pair of electrode layers 112a and 112b which are attached to the surface of the oxide semiconductor film 108 can be removed. Note that owing to the treatment using the chemical solution 173, the thickness of part of the oxide semiconductor film 108, specifically, the thickness of the region of the oxide semiconductor film 108 which is
10 exposed from the pair of electrode layers 112a and 112b might be smaller than the thicknesses of regions of the oxide semiconductor film 108 over which the pair of electrode layers 112a and 112b is provided.

[0351]

Although a method in which part of the surface of the oxide semiconductor
15 film 108 is removed using the chemical solution 173 is described as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, part of the surface of the oxide semiconductor film 108 is not necessarily removed using the chemical solution 173. In this case, the thickness of the region of the oxide semiconductor film 108 which is exposed from the pair of electrode layers
20 112a and 112b is substantially the same as the thicknesses of the regions of the oxide semiconductor film 108 over which the pair of electrode layers 112a and 112b is provided.

[0352]

Through the above process, the transistor 151 is formed.

25 [0353]

Next, the insulating films 114, 116, and 118 functioning as a protective insulating film for the oxide semiconductor film 108 are formed to cover the transistor 151, specifically, to cover the island-shaped oxide semiconductor film 108 and the pair of electrode layers 112a and 112b of the transistor 151 (see FIG. 25C).

30 [0354]

Heat treatment is performed after the formation of the insulating films 114 and 116. By the heat treatment, part of oxygen contained in the insulating films 114 and

116 can be moved to the oxide semiconductor film 108, so that the amount of oxygen vacancy contained in the oxide semiconductor film 108 can be further reduced. After the heat treatment, the insulating film 118 is formed. Note that the insulating films 114, 116, and 118 may be called a second insulating film. In this embodiment, the heat treatment is performed at 350 °C for one hour in an atmosphere of nitrogen and oxygen.

[0355]

Next, a resist is applied to the insulating film 118 and is patterned to form a resist mask 144 in a desired region. After that, a chemical solution 174 is applied over the insulating film 118 and the resist mask 144 to etch the insulating films 114, 116, and 118 (see FIG. 26A).

[0356]

The resist mask 144 can be formed using a method similar to that of the resist mask 141.

[0357]

As the chemical solution 174, a solution containing one or both of ammonium hydrogen fluoride and ammonium fluoride can be used. Furthermore, the chemical solution 174 may contain hydrofluoric acid. In this embodiment, a mixed solution containing ammonium hydrogen fluoride and ammonium fluoride can be used as the chemical solution 174. As for the composition of the mixed solution, the ammonium hydrogen fluoride content and the ammonium fluoride content are set to 20 % and 7.1 %, respectively.

[0358]

Next, the resist mask 144 is removed. Note that the insulating films 114, 116, and 118 are processed using the chemical solution 174, whereby the opening 142c reaching the electrode layer 112b is formed (see FIG. 26B).

[0359]

Note that in the case where the opening 142c is formed using the chemical solution 174, the opening 142c may have projections and depressions at its cross section. The projections and depressions are formed when the etching rates of the insulating films 114, 116, and 118 are different from one another at the time of using the chemical

solution 174. Although a method in which the opening 142c is formed using the chemical solution 174 is described as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, the opening 142c may be formed with a dry etching apparatus. When the opening 142c is formed using the chemical solution 174, the manufacturing cost can be reduced because a wet etching apparatus or the like is used. Meanwhile, when the opening 142c has a minute pattern, it is preferable to use a dry etching apparatus.

[0360]

Next, the conductive film 120 is formed over the insulating film 118 to cover the opening 142c (see FIG. 26C).

[0361]

A material which is similar to that described in Embodiment 1 can be used for the conductive film 120.

[0362]

Next, a resist is applied to the conductive film 120 and is patterned to form a resist mask 145 in a desired region. After that, the chemical solution 172 is applied over the conductive film 120 and the resist mask 145 to etch the conductive film 120 (see FIG. 27A).

[0363]

The resist mask 145 can be formed using a method similar to that of the resist mask 141. For the chemical solution 172, a material similar to that described above can be used.

[0364]

Next, the resist mask 145 is removed. Note that the conductive film 120 is processed to be the conductive film 120a functioning as a pixel electrode layer, using the chemical solution 172 (see FIG. 27B).

[0365]

The resist mask 145 can be removed using an apparatus similar to that used for removing the resist mask 141.

[0366]

Through the above process, the semiconductor device illustrated in FIGS. 19A to 19C can be manufactured.

[0367]

As described above, in the method for manufacturing the semiconductor device of one embodiment of the present invention, a conductive film functioning as a gate electrode layer, an oxide semiconductor film, a pair of electrode layers functioning as a source electrode layer and a drain electrode layer, an insulating film functioning as a protective insulating film, and a conductive film functioning as a pixel electrode layer can each be processed through a process using a chemical solution, i.e., what is called a wet etching process. Therefore, a method for manufacturing a semiconductor device at low cost can be provided.

[0368]

Furthermore, since the conductive film used as a gate electrode layer and the pair of electrode layers used as a source electrode layer and a drain electrode layer are formed using the same kinds of materials (here, Cu-X alloy films), they can be processed using the same chemical solution. When the oxide semiconductor film and the conductive film functioning as a pixel electrode layer are formed using the same kinds of materials, here, using materials each containing indium, they can be processed using the same chemical solution. Therefore, a semiconductor device with high productivity can be provided.

[0369]

<Method 5 for manufacturing semiconductor device>

Here, a method for manufacturing the transistor 150 in FIGS. 1A to 1C which is different from the method described in Embodiment 1 is described below in detail with reference to FIGS. 28A to 28C and FIGS. 29A and 29B.

[0370]

First, the steps up to the step in FIG. 25C are performed. After that, a resist is applied to the insulating film 118 and is patterned to form a resist mask 146 in a desired region. After that, the chemical solution 174 is applied over the insulating film 118 and the resist mask 146 to etch the insulating films 106a, 106b, 114, 116, and 118 (see FIG. 28A).

[0371]

The resist mask 146 can be formed using a method similar to that of the resist mask 141.

[0372]

As the chemical solution 174, the above-described chemical solution can be used. In this embodiment, a mixed solution containing ammonium hydrogen fluoride and ammonium fluoride can be used as the chemical solution 174. As for the composition of the mixed solution, the ammonium hydrogen fluoride content and the ammonium fluoride content are set to 20 % and 7.1 %, respectively.

[0373]

Next, the resist mask 146 is removed. Note that the insulating films 114, 116, and 118 are processed using the chemical solution 174, whereby the opening 142c reaching the electrode layer 112b is formed. Furthermore, the insulating films 106a, 106b, 114, 116, and 118 are processed using the chemical solution 174, whereby the openings 142a and 142b reaching the conductive film 104 are formed (see FIG. 28B).

[0374]

Although a method in which the openings 142a, 142b, and 142c are formed using the chemical solution 174 is described as an example in this embodiment, one embodiment of the present invention is not limited thereto. For example, the openings 142a, 142b, and 142c may be formed with a dry etching apparatus. When the openings 142a, 142b, and 142c are formed using the chemical solution 174, the manufacturing cost can be reduced because a wet etching apparatus or the like is used. Meanwhile, when the openings 142a, 142b, and 142c each have a minute pattern, it is preferable to use a dry etching apparatus. Note that the opening 142c may be called a first opening, and the openings 142a and 142b may be called second openings.

[0375]

Next, the conductive film 120 is formed over the insulating film 118 to cover the openings 142a, 142b, and 142c (see FIG. 28C).

[0376]

A material which is similar to that described above can be used for the conductive film 120.

[0377]

Next, a resist is applied to the conductive film 120 and is patterned to form a resist mask 147 in a desired region. After that, the chemical solution 172 is applied over the conductive film 120 and the resist mask 147 to etch the conductive film 120

(see FIG. 29A).

[0378]

The resist mask 147 can be formed using a method similar to that of the resist mask 141. For the chemical solution 172, a material similar to that described above
5 can be used.

[0379]

Then, the resist mask 147 is removed. Note that the conductive film 120 is processed to be the conductive film 120a functioning as a pixel electrode layer and the conductive film 120b functioning as a second gate electrode layer, using the chemical
10 solution 172 (see FIG. 29B).

[0380]

The resist mask 147 can be removed using an apparatus similar to that used for removing the resist mask 141.

[0381]

15 Through the above process, the semiconductor device illustrated in FIGS. 1A to 1C can be manufactured.

[0382]

<Structure example 6 of semiconductor device>

Next, transistors 153 and 155 that are semiconductor devices of embodiments
20 of the present invention are described with reference to FIGS. 30A to 30C, FIGS. 31A to 31C, and FIGS. 32A to 32C.

[0383]

First, the transistor 153 that is a semiconductor device of one embodiment of the present invention is described FIGS. 30A to 30C. FIG. 30A is a top view of the
25 transistor 153 that is a semiconductor device of one embodiment of the present invention. FIG. 30B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 30A. FIG. 30C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 30A.

[0384]

30 The transistor 153 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide

semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; the metal oxide film 108a over the oxide semiconductor film 108; the metal oxide film 108b over the metal oxide film 108a; and the pair of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108 with the metal oxide films 108a and 108b positioned therebetween.

[0385]

In FIGS. 30B and 30C, the insulating films 114, 116, and 118 functioning as a protective insulating film for the oxide semiconductor film 108 are formed over the transistor 153, specifically, over the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b. In addition, the opening 142c reaching the electrode layer 112b of the transistor 153 is formed in the insulating films 114, 116, and 118, and the conductive film 120a is formed over the insulating film 118 to cover the opening 142c. The conductive film 120a functions as, for example, a pixel electrode layer of a display device.

[0386]

The transistor 153 is different from the transistor 151 in FIGS. 19A to 19C in that the metal oxide films 108a and 108b are provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 151 and the effect similar to that in the case of the transistor 151 can be obtained.

[0387]

Next, the transistor 155 that is a semiconductor device of one embodiment of the present invention is described FIGS. 31A to 31C. FIG. 31A is a top view of the transistor 155 that is a semiconductor device of one embodiment of the present invention. FIG. 31B is a cross-sectional view taken along dashed dotted line Y1-Y2 in FIG. 31A. FIG. 31C is a cross-sectional view taken along dashed dotted line X1-X2 in FIG. 31A.

[0388]

The transistor 155 includes the conductive film 104 functioning as a gate electrode layer over the substrate 102; the insulating film 106 functioning as a gate insulating film over the substrate 102 and the conductive film 104; the oxide semiconductor film 108 provided over the insulating film 106 to overlap the conductive film 104; the metal oxide film 108b over the oxide semiconductor film 108; and the pair

of electrode layers 112a and 112b electrically connected to the oxide semiconductor film 108 with the metal oxide film 108b positioned therebetween.

[0389]

In FIGS. 31B and 31C, the insulating films 114, 116, and 118 functioning as a protective insulating film for the oxide semiconductor film 108 are formed over the transistor 155, specifically, over the oxide semiconductor film 108 and the pair of electrode layers 112a and 112b. In addition, the opening 142c reaching the electrode layer 112b of the transistor 155 is formed in the insulating films 114, 116, and 118, and the conductive film 120a is formed over the insulating film 118 to cover the opening 142c. The conductive film 120a functions as, for example, a pixel electrode layer of a display device.

[0390]

The transistor 155 is different from the transistor 151 in FIGS. 19A to 19C in that the metal oxide film 108b is provided over the oxide semiconductor film 108. The other structures are the same as those of the transistor 151 and the effect similar to that in the case of the transistor 151 can be obtained.

[0391]

<Method 6 for manufacturing semiconductor device>

Next, methods for manufacturing the transistors 153 and 155 that are semiconductor devices of embodiments of the present invention are described below in detail using FIGS. 32A to 32C.

[0392]

First, the steps up to the step in FIG. 23A are performed. After that, the oxide semiconductor film 108 and the metal oxide films 108a and 108b are formed over the insulating film 106 (see FIG. 32A).

[0393]

In this embodiment, the oxide semiconductor film 108 and the metal oxide films 108a and 108b are stacked successively using a multi-chamber deposition apparatus (sputtering apparatus) having a load lock chamber. Note that an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:1:1) is used for forming the oxide semiconductor film 108. Furthermore, an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:3:6) is used for

forming the metal oxide film 108a, and an In-Ga-Zn metal oxide target (In:Ga:Zn = 1:4:5) is used for forming the metal oxide film 108b. Note that a stacked-layer structure of the oxide semiconductor film 108, the metal oxide film 108a, and the metal oxide film 108b or a stacked-layer structure of the oxide semiconductor film 108 and the metal oxide film 108b is referred to as a stacked-layer oxide film in some cases.

[0394]

Next, a resist is applied to the metal oxide film 108b and is patterned to form the resist mask 142 in a desired region. After that, the chemical solution 172 is applied over the metal oxide film 108b and the resist mask 142, and the oxide semiconductor film 108 and the metal oxide films 108a and 108b are etched (see FIG. 32B).

[0395]

The resist mask 142 can be formed using a method similar to that of the resist mask 141.

[0396]

As the chemical solution 172 for etching the oxide semiconductor film 108 and the metal oxide films 108a and 108b, for example, a solution containing oxalic acid can be used. An additive or the like may be mixed in the chemical solution 172. A specific example of the chemical solution 172 is a mixed solution containing oxalic acid, water, and an additive. As for the composition of the mixed solution, the oxalic acid content, the water content, and the additive content are set to 5 % or less, 95 % or more, and 1 % less, respectively, so that the total of the percentages is 100 %.

[0397]

Since the oxide semiconductor film 108 and the metal oxide films 108a and 108b are formed using the same kinds of materials, they can be collectively etched using the chemical solution 172.

[0398]

Next, the resist mask 142 is removed. Note that the oxide semiconductor film 108 is processed to be the island-shaped oxide semiconductor film 108, using the chemical solution 172. The metal oxide film 108a is processed to be the island-shaped metal oxide film 108a, using the chemical solution 172. The metal oxide film 108b is processed to be the island-shaped metal oxide film 108b, using the

chemical solution 172 (see FIG. 32C).

[0399]

The resist mask 142 can be removed using an apparatus similar to that used for removing the resist mask 141.

5 [0400]

Subsequently, a process similar to that of the transistor 151 is performed, whereby the transistor 153 can be manufactured. The transistor 155 can be manufactured without the formation of the metal oxide film 108a.

[0401]

10 <Structure example 7 of semiconductor device>

Next, transistors 151A, 150C, 151B, and 150D that are semiconductor devices of embodiments of the present invention are described with reference to FIGS. 33A and 33B, FIGS. 32A and 34B, FIGS. 35A to 35C, and FIGS. 36A to 36C.

[0402]

15 FIGS. 33A and 33B and FIGS. 34A and 34B are each a cross-sectional view in the channel length direction of the transistor. Note that top views of the transistors in FIG. 33A and FIG. 34A and cross-sectional views in the channel width direction thereof are similar to the top view of FIG. 19A and the cross-sectional view in the channel width direction in FIG. 19B. Furthermore, top views of the transistors in FIG. 33B and
20 FIG. 34B and cross-sectional views in the channel width direction thereof are similar to the top view of FIG. 1A and the cross-sectional view in the channel width direction in FIG. 1B.

[0403]

FIG. 33A is a cross-sectional view of the transistor 151A that is a modification
25 example of the transistor 151 illustrated in FIG. 19C. The conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 151A have a different structure from the conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 151. Specifically, the conductive film 104 of the
30 transistor 151A in FIG. 33A includes the conductive film 104_1 in contact with the substrate 102, the conductive film 104_2 over the conductive film 104_1, and the

conductive film 104_3 over the conductive film 104_2. The electrode layer 112a of the transistor 151A in FIG. 33A includes a conductive film 112a_1 in contact with the oxide semiconductor film 108, a conductive film 112a_2 over the conductive film 112a_1, and a conductive film 112a_3 over the conductive film 112a_2. The electrode layer 112b of the transistor 151A in FIG. 33A includes a conductive film 112b_1 in contact with the oxide semiconductor film 108, a conductive film 112b_2 over the conductive film 112b_1, and a conductive film 112b_3 over the conductive film 112b_2.

[0404]

FIG. 33B is a cross-sectional view of the transistor 150C that is a modification example of the transistor 150 illustrated in FIG. 1C. The conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 150C have a different structure from the conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 150. Specifically, the conductive film 104 of the transistor 150C in FIG. 33B includes the conductive film 104_1 in contact with the substrate 102, the conductive film 104_2 over the conductive film 104_1, and the conductive film 104_3 over the conductive film 104_2. The electrode layer 112a of the transistor 150C in FIG. 33B includes the conductive film 112a_1 in contact with the oxide semiconductor film 108, the conductive film 112a_2 over the conductive film 112a_1, and the conductive film 112a_3 over the conductive film 112a_2. The electrode layer 112b of the transistor 150C in FIG. 33B includes the conductive film 112b_1 in contact with the oxide semiconductor film 108, the conductive film 112b_2 over the conductive film 112b_1, and the conductive film 112b_3 over the conductive film 112b_2.

[0405]

FIG. 34A is a cross-sectional view of the transistor 151B that is a modification example of the transistor 151 illustrated in FIG. 19C. The conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 151B have a different structure from the conductive film

104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 151. Specifically, the conductive film 104 of the transistor 151B in FIG. 34A includes the conductive film 104_1 in contact with the substrate 102 and the conductive film 104_2 over the conductive film 104_1. The electrode layer 112a of the transistor 151B in FIG. 34A includes the conductive film 112a_1 in contact with the oxide semiconductor film 108 and the conductive film 112a_2 over the conductive film 112a_1. The electrode layer 112b of the transistor 151B in FIG. 34A includes the conductive film 112b_1 in contact with the oxide semiconductor film 108 and the conductive film 112b_2 over the conductive film 112b_1.

[0406]

FIG. 34B is a cross-sectional view of the transistor 150D that is a modification example of the transistor 150 illustrated in FIG. 1C. The conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 150D have a different structure from the conductive film 104 functioning as a gate electrode layer and the pair of electrode layers 112a and 112b that are included in the transistor 150. Specifically, the conductive film 104 of the transistor 150D in FIG. 34B includes the conductive film 104_1 in contact with the substrate 102 and the conductive film 104_2 over the conductive film 104_1. The electrode layer 112a of the transistor 150D in FIG. 34B includes the conductive film 112a_1 in contact with the oxide semiconductor film 108 and the conductive film 112a_2 over the conductive film 112a_1. The electrode layer 112b of the transistor 150D in FIG. 34B includes the conductive film 112b_1 in contact with the oxide semiconductor film 108 and the conductive film 112b_2 over the conductive film 112b_1.

[0407]

For the conductive films 104_1, 112a_1, and 112b_1 used for the transistors 151A, 150C, 151B, and 150D, the above-described Cu-X alloy film (X is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti) can be used. For the conductive films 104_2, 112a_2, and 112b_2, a conductive film containing a low-resistance material such as copper (Cu), aluminum (Al), gold (Au), or silver (Ag), an alloy containing any of these materials, or a

compound containing any of these materials as a main component can be used. To increase the conductivity of each of the conductive film 104 and the pair of electrode layers 112a and 112b, it is preferable that the thicknesses of the conductive films 104_2, 112a_2, and 112b be larger than those of the conductive films 104_1, 112a_1, and 112b_1. The conductive films 104_3, 112a_3, and 112b_3 provided in each of the transistors 151A and 152A can be formed using, for example, materials similar to those used for the conductive films 104_1, 112a_1, and 112b_1.

[0408]

A 30-nm-thick Cu-Mn alloy film is used as each of the conductive films 104_1, 112a_1, and 112b_1 in this embodiment. Furthermore, a 200-nm-thick Cu film is used as each of the conductive films 104_2, 112a_2, and 112b_2. Moreover, a 50-nm-thick Cu-Mn alloy film is used as each of the conductive films 104_3, 112a_3, and 112b_3.

[0409]

When the conductive film 104_1 is provided in contact with the substrate 102 as in the structures of the transistors 151A, 150C, 151B, and 150D, adhesion with the substrate 102 can be improved. When the conductive film 104_3 is provided over and in contact with the conductive film 104_2 as in the structures of the transistors 151A and 152A, heat resistance of the conductive film 104 can be improved. When the conductive film 104_3 is provided over and in contact with the conductive film 104_2 as in the structures of the transistors 151A and 152A, a metal element (e.g., Cu) contained in the conductive film 104_2 can be inhibited from diffusing upward.

[0410]

When the conductive films 112a_1 and 112b_1 are provided in contact with the oxide semiconductor film 108 as in the structures of the transistors 151A, 150C, 151B, and 150D, a metal element (e.g., Cu) contained in the conductive films 112a_2, and 112b_2 can be inhibited from entering the oxide semiconductor film 108. Furthermore, when the conductive films 112a_3 and 112b_3 are provided in contact with top surfaces of the conductive films 112a_2 and 112b_2 as in the transistors 151A and 150C, heat resistance of the pair of electrode layers 112a and 112b can be improved. That is, the conductive films 112a_3 and 112b_3 function as barrier films for the conductive films

112a_2 and 112b_2. It is preferable that the conductive films 112a_3 and 112b_3 be provided because they function as protective films for the conductive films 112a_2 and 112b_2 at the time of forming the insulating film 114.

[0411]

5 The other structures of the transistors 151A, 150C, 151B, and 150D are the same as those of the transistors 151 and 150 and the effect similar to that in the case of the transistors 151 and 150 can be obtained.

[0412]

<Method 7 for manufacturing semiconductor device>

10 Next, methods for manufacturing the transistors 151A and 150C that are semiconductor devices of embodiments of the present invention are described below in detail with reference to FIGS. 35A to 35C and FIGS. 36A to 36C.

[0413]

15 First, conductive films 103_1, 103_2, and 103_3 are formed over the substrate 102 (see FIG. 35A).

[0414]

20 The conductive films 103_1, 103_2, and 103_3 each can be formed using the material in the description of the conductive film 104. In this embodiment, a 30-nm-thick Cu-Mn alloy film is used as the conductive film 103_1, a 200-nm-thick Cu film is used as the conductive film 103_2, and a 50-nm-thick Cu-Mn alloy film is used as the conductive film 103_3. Note that the Cu-Mn alloy films can be formed by a sputtering method using a Cu-Mn metal target (Cu:Mn = 90:10 [at.%]).

[0415]

25 Next, a resist is applied to the conductive film 103_3 and is patterned to form the resist mask 141 in a desired region. After that, the chemical solution 171 is applied over the conductive film 103_3 and the resist mask 141 to etch the conductive films 103_1, 103_2, and 103_3 (see FIG. 35B).

[0416]

30 For the resist mask 141 and the chemical solution 171, materials similar to the above-described materials can be used. Note that in this embodiment, an etchant containing an organic acid solution and a hydrogen peroxide solution is used as the

chemical solution 171 for etching the conductive films 103_1, 103_2, and 103_3.

[0417]

In this manner, in the case of the three-layer structure in which a Cu-Mn alloy film is used as the conductive films 103_1 and 103_3 and a Cu film is used as the
5 conductive film 103_2, since the three layers are formed using the same kinds of materials, they can be collectively etched using the chemical solution 171. Furthermore, in the case of the above three-layer structure, a favorable cross-sectional shape can be obtained. Accordingly, coverage with the insulating film 106 formed later is improved, so that a highly reliable semiconductor device can be obtained.

10 [0418]

Next, the resist mask 141 is removed. Note that the conductive films 103_1, 103_2, and 103_3 are processed to be the conductive films 104_1, 104_2, and 104_3, using the chemical solution 171. Note that the conductive film 104 functioning as a gate electrode layer is formed of the conductive films 104_1, 104_2, and 104_3 (see
15 FIG. 35C).

[0419]

Next, through a process similar to that of the transistor 151 or the transistor 150 described above, the oxide semiconductor film 108 is formed over the insulating film 106. After that, conductive films 111_1, 111_2, and 111_3 are formed over the
20 insulating film 106 and the oxide semiconductor film 108 (see FIG. 36A).

[0420]

The conductive films 111_1, 111_2, and 111_3 each can be formed using the material in the description of the pair of electrode layers 112a and 112b. In this embodiment, a 30-nm-thick Cu-Mn alloy film is used as the conductive film 111_1, a
25 200-nm-thick Cu film is used as the conductive film 111_2, and a 50-nm-thick Cu-Mn alloy film is used as the conductive film 111_3. Note that the Cu-Mn alloy films can be formed by a sputtering method using a Cu-Mn metal target (Cu:Mn = 90:10 [at.%]).

[0421]

Next, a resist is applied to the conductive film 111_3 and is patterned to form a
30 resist mask 143 in a desired region. After that, the chemical solution 171 is applied over the conductive film 111_3 and the resist mask 143 to etch the conductive films

111_1, 111_2, and 111_3 (see FIG. 36B).

[0422]

For the resist mask 143 and the chemical solution 171, materials similar to the above-described materials can be used.

5 [0423]

Next, the resist mask 143 is removed. Note that the conductive films 111_1, 111_2, and 111_3 are processed to be the conductive films 102a_1, 102b_1, 102a_2, 102b_2, 102a_3, and 102b_3, using the chemical solution 171. Note that the electrode layer 112a is formed of the conductive films 102a_1, 102a_2, and 102a_3. The electrode layer 112b is formed of the conductive films 102b_1, 102b_2, and 102b_3 (see FIG. 36C).

[0424]

Subsequently, a process similar to that of the transistor 151 or 150 is performed, whereby the transistor 151A or 150C can be manufactured. The transistors 151B and 150D can each be manufactured without the formation of the conductive films 103_3 and 111_3.

[0425]

Note that the structures of the transistors and the methods for manufacturing the transistors in this embodiment can be freely combined with each other.

20 [0426]

(Embodiment 3)

In this embodiment, the structure of an oxide semiconductor film included in a semiconductor device of one embodiment of the present invention is described below in detail.

25 [0427]

First a structure which can be included in an oxide semiconductor film is described below.

[0428]

An oxide semiconductor is classified into a single crystal oxide semiconductor and a non-single-crystal oxide semiconductor.

[0429]

Examples of a non-single-crystal oxide semiconductor include a c-axis aligned crystalline oxide semiconductor (CAAC-OS), a polycrystalline oxide semiconductor, a microcrystalline oxide semiconductor, and an amorphous oxide semiconductor.

[0430]

5 From another perspective, an oxide semiconductor is classified into an amorphous oxide semiconductor and a crystalline oxide semiconductor. Examples of a crystalline oxide semiconductor include a single crystal oxide semiconductor, a CAAC-OS, a polycrystalline oxide semiconductor, and a microcrystalline oxide semiconductor.

10 [0431]

<CAAC-OS>

First, a CAAC-OS is described. Note that a CAAC-OS can be referred to as an oxide semiconductor including c-axis aligned nanocrystals (CANC).

[0432]

15 A CAAC-OS is one of oxide semiconductors having a plurality of c-axis aligned crystal parts (also referred to as pellets).

[0433]

In a combined analysis image (also referred to as a high-resolution TEM image) of a bright-field image and a diffraction pattern of a CAAC-OS, which is
20 obtained using a transmission electron microscope (TEM), a plurality of pellets can be observed. However, in the high-resolution TEM image, a boundary between pellets, that is, a grain boundary is not clearly observed. Thus, in the CAAC-OS, a reduction in electron mobility due to the grain boundary is less likely to occur.

[0434]

25 A CAAC-OS observed with TEM is described below. FIG. 37A shows a high-resolution TEM image of a cross section of the CAAC-OS which is observed from a direction substantially parallel to the sample surface. The high-resolution TEM image is obtained with a spherical aberration corrector function. The high-resolution TEM image obtained with a spherical aberration corrector function is particularly
30 referred to as a Cs-corrected high-resolution TEM image. The Cs-corrected high-resolution TEM image can be obtained with, for example, an atomic resolution analytical electron microscope JEM-ARM200F manufactured by JEOL Ltd.

[0435]

FIG. 37B is an enlarged Cs-corrected high-resolution TEM image of a region (1) in FIG. 37A. FIG. 37B shows that metal atoms are arranged in a layered manner in a pellet. Each metal atom layer has a configuration reflecting unevenness of a surface over which the CAAC-OS is formed (hereinafter, the surface is referred to as a formation surface) or a top surface of the CAAC-OS, and is arranged parallel to the formation surface or the top surface of the CAAC-OS.

[0436]

As shown in FIG. 37B, the CAAC-OS has a characteristic atomic arrangement. The characteristic atomic arrangement is denoted by an auxiliary line in FIG. 37C. FIGS. 37B and 37C prove that the size of a pellet is approximately 1 nm to 3 nm, and the size of a space caused by tilt of the pellets is approximately 0.8 nm. Therefore, the pellet can also be referred to as a nanocrystal (nc).

[0437]

Here, according to the Cs-corrected high-resolution TEM images, the schematic arrangement of pellets 5100 of a CAAC-OS over a substrate 5120 is illustrated by such a structure in which bricks or blocks are stacked (see FIG. 37D). The part in which the pellets are tilted as observed in FIG. 37C corresponds to a region 5161 shown in FIG. 37D.

[0438]

FIG. 38A shows a Cs-corrected high-resolution TEM image of a plane of the CAAC-OS observed from a direction substantially perpendicular to the sample surface. FIGS. 38B, 38C, and 38D are enlarged Cs-corrected high-resolution TEM images of regions (1), (2), and (3) in FIG. 38A, respectively. FIGS. 38B, 38C, and 38D indicate that metal atoms are arranged in a triangular, quadrangular, or hexagonal configuration in a pellet. However, there is no regularity of arrangement of metal atoms between different pellets.

[0439]

Next, a CAAC-OS analyzed by X-ray diffraction (XRD) is described. For example, when the structure of a CAAC-OS including an InGaZnO_4 crystal is analyzed by an out-of-plane method, a peak appears at a diffraction angle (2θ) of around 31° as shown in FIG. 39A. This peak is derived from the (009) plane of the InGaZnO_4

crystal, which indicates that crystals in the CAAC-OS have c-axis alignment, and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or the top surface of the CAAC-OS.

[0440]

5 Note that in structural analysis of the CAAC-OS by an out-of-plane method, another peak may appear when 2θ is around 36° , in addition to the peak at 2θ of around 31° . The peak at 2θ of around 36° indicates that a crystal having no c-axis alignment is included in part of the CAAC-OS. It is preferable that in the CAAC-OS analyzed by an out-of-plane method, a peak appear when 2θ is around 31° and that a peak not appear
10 when 2θ is around 36° .

[0441]

On the other hand, in structural analysis of the CAAC-OS by an in-plane method in which an X-ray is incident on a sample in a direction substantially perpendicular to the c-axis, a peak appears when 2θ is around 56° . This peak is
15 attributed to the (110) plane of the InGaZnO₄ crystal. In the case of the CAAC-OS, when analysis (ϕ scan) is performed with 2θ fixed at around 56° and with the sample rotated using a normal vector of the sample surface as an axis (ϕ axis), as shown in FIG. 39B, a peak is not clearly observed. In contrast, in the case of a single crystal oxide semiconductor of InGaZnO₄, when ϕ scan is performed with 2θ fixed at around 56° , as
20 shown in FIG. 39C, six peaks which are derived from crystal planes equivalent to the (110) plane are observed. Accordingly, the structural analysis using XRD shows that the directions of a-axes and b-axes are different in the CAAC-OS.

[0442]

Next, a CAAC-OS analyzed by electron diffraction is described. For example,
25 when an electron beam with a probe diameter of 300 nm is incident on a CAAC-OS including an InGaZnO₄ crystal in a direction parallel to the sample surface, a diffraction pattern (also referred to as a selected-area transmission electron diffraction pattern) shown in FIG. 40A might be obtained. In this diffraction pattern, spots derived from the (009) plane of an InGaZnO₄ crystal are included. Thus, the electron diffraction
30 also indicates that pellets included in the CAAC-OS have c-axis alignment and that the c-axes are aligned in a direction substantially perpendicular to the formation surface or

the top surface of the CAAC-OS. Meanwhile, FIG. 40B shows a diffraction pattern obtained in such a manner that an electron beam with a probe diameter of 300 nm is incident on the same sample in a direction perpendicular to the sample surface. As shown in FIG. 40B, a ring-like diffraction pattern is observed. Thus, the electron
5 diffraction also indicates that the a-axes and b-axes of the pellets included in the CAAC-OS do not have regular alignment. The first ring in FIG. 40B is considered to be derived from the (010) plane, the (100) plane, and the like of the InGaZnO₄ crystal. The second ring in FIG. 40B is considered to be derived from the (110) plane and the like.

10 [0443]

Moreover, the CAAC-OS is an oxide semiconductor having a low density of defect states. Defects in the oxide semiconductor are, for example, a defect due to impurity and oxygen vacancy. Therefore, the CAAC-OS can be regarded as an oxide semiconductor with a low impurity concentration, or an oxide semiconductor having a
15 small number of oxygen vacancy.

[0444]

The impurity contained in the oxide semiconductor might serve as a carrier trap or serve as a carrier generation source. Furthermore, oxygen vacancies in the oxide semiconductor serve as carrier traps or serve as carrier generation sources when
20 hydrogen is captured therein.

[0445]

Note that the impurity means an element other than the main components of the oxide semiconductor, such as hydrogen, carbon, silicon, or a transition metal element. For example, an element (specifically, silicon or the like) having higher strength of
25 bonding to oxygen than a metal element included in an oxide semiconductor extracts oxygen from the oxide semiconductor, which results in disorder of the atomic arrangement and reduced crystallinity of the oxide semiconductor. A heavy metal such as iron or nickel, argon, carbon dioxide, or the like has a large atomic radius (or molecular radius), and thus disturbs the atomic arrangement of the oxide semiconductor
30 and decreases crystallinity.

[0446]

An oxide semiconductor having a low density of defect states (a small amount

of oxygen vacancy) can have a low carrier density. Such an oxide semiconductor is referred to as a highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. A CAAC-OS has a low impurity concentration and a low density of defect states. That is, a CAAC-OS is likely to be highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor. Thus, a transistor including a CAAC-OS rarely has negative threshold voltage (is rarely normally on). The highly purified intrinsic or substantially highly purified intrinsic oxide semiconductor has few carrier traps. An electric charge trapped by the carrier traps in the oxide semiconductor takes a long time to be released. The trapped electric charge may behave like a fixed electric charge. Thus, the transistor which includes the oxide semiconductor having a high impurity concentration and a high density of defect states might have unstable electrical characteristics. However, a transistor including a CAAC-OS has small variation in electrical characteristics and high reliability.

[0447]

Since the CAAC-OS has a low density of defect states, carriers generated by light irradiation or the like are less likely to be trapped in defect states. Therefore, in a transistor using the CAAC-OS, change in electrical characteristics due to irradiation with visible light or ultraviolet light is small.

[0448]

<Microcrystalline oxide semiconductor>

Next, a microcrystalline oxide semiconductor is described.

[0449]

A microcrystalline oxide semiconductor has a region in which a crystal part is observed and a region in which a crystal part is not clearly observed in a high-resolution TEM image. In most cases, the size of a crystal part included in the microcrystalline oxide semiconductor is greater than or equal to 1 nm and less than or equal to 100 nm, or greater than or equal to 1 nm and less than or equal to 10 nm. An oxide semiconductor including a nanocrystal (nc) that is a microcrystal with a size greater than or equal to 1 nm and less than or equal to 10 nm, or a size greater than or equal to 1 nm and less than or equal to 3 nm is specifically referred to as a nanocrystalline oxide semiconductor (nc-OS). In a high-resolution TEM image of the nc-OS, for example, a grain boundary is not clearly observed in some cases. Note that there is a possibility

that the origin of the nanocrystal is the same as that of a pellet in a CAAC-OS. Therefore, a crystal part of the nc-OS may be referred to as a pellet in the following description.

[0450]

5 In the nc-OS, a microscopic region (for example, a region with a size greater than or equal to 1 nm and less than or equal to 10 nm, in particular, a region with a size greater than or equal to 1 nm and less than or equal to 3 nm) has a periodic atomic arrangement. There is no regularity of crystal orientation between different pellets in the nc-OS. Thus, the orientation of the whole film is not ordered. Accordingly, the
10 nc-OS cannot be distinguished from an amorphous oxide semiconductor, depending on an analysis method. For example, when the nc-OS is subjected to structural analysis by an out-of-plane method with an XRD apparatus using an X-ray having a diameter larger than the size of a pellet, a peak which shows a crystal plane does not appear. Furthermore, a diffraction pattern like a halo pattern is observed when the nc-OS is
15 subjected to electron diffraction using an electron beam with a probe diameter (e.g., 50 nm or larger) that is larger than the size of a pellet (the electron diffraction is also referred to as selected-area electron diffraction). Meanwhile, spots appear in a nanobeam electron diffraction pattern of the nc-OS when an electron beam having a probe diameter close to or smaller than the size of a pellet is applied. Moreover, in a
20 nanobeam electron diffraction pattern of the nc-OS, regions with high luminance in a circular (ring) pattern are shown in some cases. Also in a nanobeam electron diffraction pattern of the nc-OS, a plurality of spots is shown in a ring-like region in some cases.

[0451]

25 Since there is no regularity of crystal orientation between the pellets (nanocrystals) as mentioned above, the nc-OS can also be referred to as an oxide semiconductor including random aligned nanocrystals (RANC) or an oxide semiconductor including non-aligned nanocrystals (NANC).

[0452]

30 The nc-OS is an oxide semiconductor that has high regularity as compared with an amorphous oxide semiconductor. Therefore, the nc-OS is likely to have a lower density of defect states than an amorphous oxide semiconductor. Note that there is no

regularity of crystal orientation between different pellets in the nc-OS. Therefore, the nc-OS has a higher density of defect states than the CAAC-OS.

[0453]

<Amorphous oxide semiconductor>

5 Next, an amorphous oxide semiconductor is described.

[0454]

The amorphous oxide semiconductor is an oxide semiconductor having disordered atomic arrangement and no crystal part and exemplified by an oxide semiconductor which exists in an amorphous state as quartz.

[0455]

In a high-resolution TEM image of the amorphous oxide semiconductor, crystal parts cannot be found.

[0456]

15 When the amorphous oxide semiconductor is subjected to structural analysis by an out-of-plane method with an XRD apparatus, a peak which shows a crystal plane does not appear. A halo pattern is observed when the amorphous oxide semiconductor is subjected to electron diffraction. Furthermore, a spot is not observed and only a halo pattern appears when the amorphous oxide semiconductor is subjected to nanobeam electron diffraction.

[0457]

There are various understandings of an amorphous structure. For example, a structure whose atomic arrangement does not have ordering at all is called a completely amorphous structure. Meanwhile, a structure which has ordering until the nearest neighbor atomic distance or the second-nearest neighbor atomic distance but does not have long-range ordering is also called an amorphous structure. Therefore, the strictest definition does not permit an oxide semiconductor to be called an amorphous oxide semiconductor as long as even a negligible degree of ordering is present in an atomic arrangement. At least an oxide semiconductor having long-term ordering cannot be called an amorphous oxide semiconductor. Accordingly, because of the presence of crystal part, for example, a CAAC-OS and an nc-OS cannot be called an amorphous oxide semiconductor or a completely amorphous oxide semiconductor.

[0458]

<Amorphous-like oxide semiconductor>

Note that an oxide semiconductor may have a structure intermediate between the nc-OS and the amorphous oxide semiconductor. The oxide semiconductor having
5 such a structure is specifically referred to as an amorphous-like oxide semiconductor (a-like OS).

[0459]

In a high-resolution TEM image of the a-like OS, a void may be observed. Furthermore, in the high-resolution TEM image, there are a region where a crystal part
10 is clearly observed and a region where a crystal part is not observed.

[0460]

The a-like OS has an unstable structure because it includes a void. To verify that an a-like OS has an unstable structure as compared with a CAAC-OS and an nc-OS, a change in structure caused by electron irradiation is described below.

15 [0461]

An a-like OS (referred to as Sample A), an nc-OS (referred to as Sample B), and a CAAC-OS (referred to as Sample C) are prepared as samples subjected to electron irradiation. Each of the samples is an In-Ga-Zn oxide.

[0462]

20 First, a high-resolution cross-sectional TEM image of each sample is obtained. The high-resolution cross-sectional TEM images show that all the samples have crystal parts.

[0463]

Note that which part is regarded as a crystal part is determined as follows. It
25 is known that a unit cell of an InGaZnO₄ crystal has a structure in which nine layers including three In-O layers and six Ga-Zn-O layers are stacked in the c-axis direction. The distance between the adjacent layers is equivalent to the lattice spacing on the (009) plane (also referred to as d value). The value is calculated to be 0.29 nm from crystal structural analysis. Accordingly, a portion where the lattice spacing between lattice
30 fringes is greater than or equal to 0.28 nm and less than or equal to 0.30 nm is regarded as a crystal part of InGaZnO₄. Each of lattice fringes corresponds to the a-b plane of the InGaZnO₄ crystal.

[0464]

FIG. 41 shows change in the average size of crystal parts (at 22 points to 45 points) in each sample. Note that the crystal part size corresponds to the length of a lattice fringe. FIG. 41 indicates that the crystal part size in the a-like OS increases with an increase in the cumulative electron dose. Specifically, as shown by (1) in FIG. 41, a crystal part of approximately 1.2 nm (also referred to as an initial nucleus) at the start of TEM observation grows to a size of approximately 2.6 nm at a cumulative electron dose of $4.2 \times 10^8 \text{ e}^-/\text{nm}^2$. In contrast, the crystal part size in the nc-OS and the CAAC-OS shows little change from the start of electron irradiation to a cumulative electron dose of $4.2 \times 10^8 \text{ e}^-/\text{nm}^2$. Specifically, as shown by (2) and (3) in FIG. 41, the average crystal sizes in an nc-OS and a CAAC-OS are approximately 1.4 nm and approximately 2.1 nm, respectively, regardless of the cumulative electron dose.

[0465]

In this manner, growth of the crystal part in the a-like OS is induced by electron irradiation. In contrast, in the nc-OS and the CAAC-OS, growth of the crystal part is hardly induced by electron irradiation. Therefore, the a-like OS has an unstable structure as compared with the nc-OS and the CAAC-OS.

[0466]

The a-like OS has a lower density than the nc-OS and the CAAC-OS because it includes a void. Specifically, the density of the a-like OS is higher than or equal to 78.6% and lower than 92.3% of the density of the single crystal oxide semiconductor having the same composition. The density of each of the nc-OS and the CAAC-OS is higher than or equal to 92.3% and lower than 100% of the density of the single crystal oxide semiconductor having the same composition. Note that it is difficult to deposit an oxide semiconductor having a density of lower than 78% of the density of the single crystal oxide semiconductor.

[0467]

For example, in the case of an oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of single crystal InGaZnO₄ with a rhombohedral crystal structure is 6.357 g/cm³. Accordingly, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of the a-like OS is higher than or equal

to 5.0 g/cm^3 and lower than 5.9 g/cm^3 . For example, in the case of the oxide semiconductor having an atomic ratio of In:Ga:Zn = 1:1:1, the density of each of the nc-OS and the CAAC-OS is higher than or equal to 5.9 g/cm^3 and lower than 6.3 g/cm^3 .

[0468]

- 5 Note that there is a possibility that an oxide semiconductor having a certain composition cannot exist in a single crystal structure. In that case, single crystal oxide semiconductors with different compositions are combined at an adequate ratio, which makes it possible to calculate density equivalent to that of a single crystal oxide semiconductor with the desired composition. The density of a single crystal oxide
- 10 semiconductor having the desired composition can be calculated using a weighted average according to the combination ratio of the single crystal oxide semiconductors with different compositions. Note that it is preferable to use as few kinds of single crystal oxide semiconductors as possible to calculate the density.

[0469]

- 15 As described above, oxide semiconductors have various structures and various properties. Note that an oxide semiconductor may be a stacked layer including two or more films of an amorphous oxide semiconductor, an a-like OS, a microcrystalline oxide semiconductor, and a CAAC-OS, for example.

[0470]

- 20 <Deposition model>

Examples of deposition models of a CAAC-OS and an nc-OS are described below.

[0471]

- FIG. 42A is a schematic view of the inside of a deposition chamber where a
- 25 CAAC-OS is deposited by a sputtering method.

[0472]

- A target 5130 is attached to a backing plate. A plurality of magnets is provided to face the target 5130 with the backing plate positioned therebetween. The plurality of magnets generates a magnetic field. A sputtering method in which the
- 30 disposition rate is increased by utilizing a magnetic field of magnets is referred to as a magnetron sputtering method.

[0473]

The substrate 5120 is placed to face the target 5130, and the distance d (also referred to as a target-substrate distance (T-S distance)) is greater than or equal to 0.01 m and less than or equal to 1 m, preferably greater than or equal to 0.02 m and less than or equal to 0.5 m. The deposition chamber is mostly filled with a deposition gas (e.g.,
5 an oxygen gas, an argon gas, or a mixed gas containing oxygen at 5 vol% or higher) and the pressure in the deposition chamber is controlled to be higher than or equal to 0.01 Pa and lower than or equal to 100 Pa, preferably higher than or equal to 0.1 Pa and lower than or equal to 10 Pa. Here, discharge starts by application of a voltage at a certain value or higher to the target 5130, and plasma is observed. The magnetic field forms a
10 high-density plasma region in the vicinity of the target 5130. In the high-density plasma region, the deposition gas is ionized, so that an ion 5101 is generated. Examples of the ion 5101 include an oxygen cation (O^+) and an argon cation (Ar^+).

[0474]

Here, the target 5130 has a polycrystalline structure which includes a plurality
15 of crystal grains and in which a cleavage plane exists in at least one crystal grain. FIG. 43A shows a structure of an $InGaZnO_4$ crystal included in the target 5130 as an example. Note that FIG. 43A shows a structure of the case where the $InGaZnO_4$ crystal is observed from a direction parallel to the b-axis.

[0475]

FIG. 43A indicates that oxygen atoms in a Ga-Zn-O layer are positioned close
20 to those in an adjacent Ga-Zn-O layer. The oxygen atoms have negative charge, whereby repulsive force is generated between the two adjacent Ga-Zn-O layers. As a result, the $InGaZnO_4$ crystal has a cleavage plane between the two adjacent Ga-Zn-O layers.

25 [0476]

The ion 5101 generated in the high-density plasma region is accelerated toward
the target 5130 side by an electric field, and then collides with the target 5130. At this time, a pellet 5100a and a pellet 5100b which are flat-plate-like (pellet-like) sputtered particles are separated and sputtered from the cleavage plane. Note that structures of
30 the pellet 5100a and the pellet 5100b may be distorted by an impact of collision of the ion 5101.

[0477]

The pellet 5100a is a flat-plate-like (pellet-like) sputtered particle having a triangle plane, e.g., regular triangle plane. The pellet 5100b is a flat-plate-like (pellet-like) sputtered particle having a hexagon plane, e.g., regular hexagon plane.

5 Note that flat-plate-like (pellet-like) sputtered particles such as the pellet 5100a and the pellet 5100b are collectively called pellets 5100. The shape of a flat plane of the pellet 5100 is not limited to a triangle or a hexagon. For example, the flat plane may have a shape formed by combining two or more triangles. For example, a quadrangle (e.g., rhombus) may be formed by combining two triangles (e.g., regular triangles).

10 [0478]

The thickness of the pellet 5100 is determined depending on the kind of deposition gas and the like. The thicknesses of the pellets 5100 are preferably uniform; the reason for this is described later. In addition, the sputtered particle preferably has a pellet shape with a small thickness as compared to a dice shape with a

15 large thickness. For example, the thickness of the pellet 5100 is greater than or equal to 0.4 nm and less than or equal to 1 nm, preferably greater than or equal to 0.6 nm and less than or equal to 0.8 nm. In addition, for example, the width of the pellet 5100 is greater than or equal to 1 nm and less than or equal to 3 nm, preferably greater than or equal to 1.2 nm and less than or equal to 2.5 nm. The pellet 5100 corresponds to the

20 initial nucleus in the description of (1) in FIG. 41. For example, when the ion 5101 collides with the target 5130 including an In-Ga-Zn oxide, the pellet 5100 that includes three layers of a Ga-Zn-O layer, an In-O layer, and a Ga-Zn-O layer as shown in FIG. 43B is separated. Note that FIG. 43C shows the structure of the separated pellet 5100 which is observed from a direction parallel to the c-axis. The pellet 5100 has a

25 nanometer-sized sandwich structure including two Ga-Zn-O layers (pieces of bread) and an In-O layer (filling).

[0479]

The pellet 5100 may receive a charge when passing through the plasma, so that side surfaces thereof are negatively or positively charged. In the pellet 5100, for

30 example, an oxygen atom positioned on its side surface may be negatively charged. When the side surfaces are charged with the same polarity, charges repel each other, and accordingly, the pellet 5100 can maintain a flat-plate (pellet) shape. In the case where

a CAAC-OS is an In-Ga-Zn oxide, there is a possibility that an oxygen atom bonded to an indium atom is negatively charged. There is another possibility that an oxygen atom bonded to an indium atom, a gallium atom, or a zinc atom is negatively charged. In addition, the pellet 5100 may grow by being bonded with an indium atom, a gallium atom, a zinc atom, an oxygen atom, or the like when passing through plasma. A difference in size between (2) and (1) in FIG. 41 corresponds to the amount of growth in plasma. Here, in the case where the temperature of the substrate 5120 is at around room temperature, the pellet 5100 on the substrate 5120 hardly grows; thus, an nc-OS is formed (see FIG. 42B). An nc-OS can be deposited when the substrate 5120 has a large size because the deposition of an nc-OS can be carried out at room temperature. Note that in order that the pellet 5100 grows in plasma, it is effective to increase deposition power in sputtering. High deposition power can stabilize the structure of the pellet 5100.

[0480]

As shown in FIGS. 42A and 42B, the pellet 5100 flies like a kite in plasma and flutters up to the substrate 5120. Since the pellets 5100 are charged, when the pellet 5100 gets close to a region where another pellet 5100 has already been deposited, repulsion is generated. Here, above the substrate 5120, a magnetic field in a direction parallel to the top surface of the substrate 5120 (also referred to as a horizontal magnetic field) is generated. A potential difference is given between the substrate 5120 and the target 5130, and accordingly, current flows from the substrate 5120 toward the target 5130. Thus, the pellet 5100 is given a force (Lorentz force) on the top surface of the substrate 5120 by an effect of the magnetic field and the current. This is explainable with Fleming's left-hand rule.

[0481]

The mass of the pellet 5100 is larger than that of an atom. Therefore, to move the pellet 5100 over the top surface of the substrate 5120, it is important to apply some force to the pellet 5100 from the outside. One kind of the force may be force which is generated by the action of a magnetic field and current. In order to apply a sufficient force to the pellet 5100 so that the pellet 5100 moves over a top surface of the substrate 5120, it is preferable to provide, on the top surface, a region where the magnetic field in a direction parallel to the top surface of the substrate 5120 is 10 G or higher, preferably

20 G or higher, further preferably 30 G or higher, still further preferably 50 G or higher. Alternatively, it is preferable to provide, on the top surface, a region where the magnetic field in a direction parallel to the top surface of the substrate 5120 is 1.5 times or higher, preferably twice or higher, further preferably 3 times or higher, still further preferably 5
5 times or higher as high as the magnetic field in a direction perpendicular to the top surface of the substrate 5120.

[0482]

At this time, the magnets and the substrate 5120 are moved or rotated relatively, whereby the direction of the horizontal magnetic field on the top surface of the substrate
10 5120 continues to change. Therefore, the pellet 5100 can be moved in various directions on the top surface of the substrate 5120 by receiving forces in various directions.

[0483]

Furthermore, as shown in FIG. 42A, when the substrate 5120 is heated,
15 resistance between the pellet 5100 and the substrate 5120 due to friction or the like is low. As a result, the pellet 5100 glides above the top surface of the substrate 5120. The glide of the pellet 5100 is caused in a state where its flat plane faces the substrate 5120. Then, when the pellet 5100 reaches the side surface of another pellet 5100 that has been already deposited, the side surfaces of the pellets 5100 are bonded. At this
20 time, the oxygen atom on the side surface of the pellet 5100 is released. With the released oxygen atom, oxygen vacancies in a CAAC-OS might be filled; thus, the CAAC-OS has a low density of defect states. Note that the temperature of the top surface of the substrate 5120 is, for example, higher than or equal to 100 °C and lower than 500 °C, higher than or equal to 150 °C and lower than 450 °C, or higher than or
25 equal to 170 °C and lower than 400 °C. Hence, even when the substrate 5120 has a large size, it is possible to deposit a CAAC-OS.

[0484]

Furthermore, the pellet 5100 is heated on the substrate 5120, whereby atoms are rearranged, and the structure distortion caused by the collision of the ion 5101 can
30 be reduced. The pellet 5100 whose structure distortion is reduced is substantially single crystal. Even when the pellets 5100 are heated after being bonded, expansion

and contraction of the pellet 5100 itself hardly occur, which is caused by turning the pellet 5100 into substantially single crystal. Thus, formation of defects such as a grain boundary due to expansion of a space between the pellets 5100 can be prevented, and accordingly, generation of crevasses can be prevented.

5 [0485]

The CAAC-OS does not have a structure like a board of a single crystal oxide semiconductor but has arrangement with a group of pellets 5100 (nanocrystals) like stacked bricks or blocks. Furthermore, a grain boundary does not exist between the pellets 5100. Therefore, even when deformation such as shrink occurs in the
10 CAAC-OS owing to heating during deposition, heating or bending after deposition, it is possible to relieve local stress or release distortion. Therefore, this structure is suitable for a flexible semiconductor device. Note that the nc-OS has arrangement in which pellets 5100 (nanocrystals) are randomly stacked.

[0486]

15 When the target 5130 is sputtered with the ion 5101, in addition to the pellets 5100, zinc oxide or the like may be separated. The zinc oxide is lighter than the pellet 5100 and thus reaches the top surface of the substrate 5120 before the pellet 5100. As a result, the zinc oxide forms a zinc oxide layer 5102 with a thickness greater than or equal to 0.1 nm and less than or equal to 10 nm, greater than or equal to 0.2 nm and less
20 than or equal to 5 nm, or greater than or equal to 0.5 nm and less than or equal to 2 nm. FIGS. 44A to 44D are cross-sectional schematic views.

[0487]

As illustrated in FIG. 44A, a pellet 5105a and a pellet 5105b are deposited over the zinc oxide layer 5102. Here, side surfaces of the pellet 5105a and the pellet 5105b
25 are in contact with each other. In addition, a pellet 5105c is deposited over the pellet 5105b, and then glides over the pellet 5105b. Furthermore, a plurality of particles 5103 separated from the target together with the zinc oxide is crystallized by heat from the substrate 5120 to form a region 5105a1 on another side surface of the pellet 5105a. Note that the plurality of particles 5103 may contain oxygen, zinc, indium, gallium, or
30 the like.

[0488]

Then, as illustrated in FIG. 44B, the region 5105a1 grows to part of the pellet

5105a to form a pellet 5105a2. In addition, a side surface of the pellet 5105c is in contact with another side surface of the pellet 5105b.

[0489]

Next, as illustrated in FIG. 44C, a pellet 5105d is deposited over the pellet 5105a2 and the pellet 5105b, and then glides over the pellet 5105a2 and the pellet 5105b. Furthermore, a pellet 5105e glides toward another side surface of the pellet 5105c over the zinc oxide layer 5102.

[0490]

Then, as illustrated in FIG. 44D, the pellet 5105d is placed so that a side surface of the pellet 5105d is in contact with a side surface of the pellet 5105a2. Furthermore, a side surface of the pellet 5105e is in contact with another side surface of the pellet 5105c. A plurality of particles 5103 separated from the target 5130 together with the zinc oxide is crystallized by heat from the substrate 5120 to form a region 5105d1 on another side surface of the pellet 5105d.

[0491]

As described above, deposited pellets are placed to be in contact with each other and then growth is caused at side surfaces of the pellets, whereby a CAAC-OS is formed over the substrate 5120. Therefore, each pellet of the CAAC-OS is larger than that of the nc-OS. A difference in size between (3) and (2) in FIG. 41 corresponds to the amount of growth after deposition.

[0492]

When spaces between pellets are extremely small, the pellets may form a large pellet. The large pellet has a single crystal structure. For example, the size of the pellet may be greater than or equal to 10 nm and less than or equal to 200 nm, greater than or equal to 15 nm and less than or equal to 100 nm, or greater than or equal to 20 nm and less than or equal to 50 nm, when seen from the above. In this case, in an oxide semiconductor used for a minute transistor, a channel formation region might be fit inside the large pellet. That is, the region having a single crystal structure can be used as the channel formation region. Furthermore, when the size of the pellet is increased, the region having a single crystal structure can be used as the channel formation region, the source region, and the drain region of the transistor.

[0493]

In this manner, when the channel formation region or the like of the transistor is formed in a region having a single crystal structure, the frequency characteristics of the transistor can be increased in some cases.

[0494]

5 As shown in such a model, the pellets 5100 are considered to be deposited on the substrate 5120. Thus, a CAAC-OS can be deposited even when a formation surface does not have a crystal structure; therefore, a growth mechanism in this case is different from epitaxial growth. In addition, laser crystallization is not needed for formation of a CAAC-OS, and a uniform film can be formed even over a large-sized
10 glass substrate or the like. For example, even when the top surface (formation surface) of the substrate 5120 has an amorphous structure (e.g., the top surface is formed of amorphous silicon oxide), a CAAC-OS can be formed.

[0495]

In addition, it is found that in formation of the CAAC-OS, the pellets 5100 are
15 arranged in accordance with the top surface shape of the substrate 5120 that is the formation surface even when the formation surface has unevenness. For example, in the case where the top surface of the substrate 5120 is flat at the atomic level, the pellets 5100 are arranged so that flat planes parallel to the a-b plane face downwards. In the case where the thickness of the pellets 5100 are uniform, a layer with a uniform
20 thickness, flatness, and high crystallinity is formed. By stacking n layers (n is a natural number), the CAAC-OS can be obtained.

[0496]

In the case where the top surface of the substrate 5120 has unevenness, a CAAC-OS in which n layers (n is a natural number) in each of which the pellets 5100
25 are arranged along the unevenness are stacked is formed. Since the substrate 5120 has unevenness, a gap is easily generated between the pellets 5100 in the CAAC-OS in some cases. Note that, even in such a case, owing to intermolecular force, the pellets 5100 are arranged so that a gap between the pellets is as small as possible even on the unevenness surface. Therefore, even when the formation surface has unevenness, a
30 CAAC-OS with high crystallinity can be obtained.

[0497]

Since a CAAC-OS is deposited in accordance with such a model, the sputtered

particle preferably has a pellet shape with a small thickness. Note that when the sputtered particles have a dice shape with a large thickness, planes facing the substrate 5120 vary; thus, the thicknesses and orientations of the crystals cannot be uniform in some cases.

5 [0498]

According to the deposition model described above, a CAAC-OS with high crystallinity can be formed even on a formation surface with an amorphous structure.

[0499]

10 The semiconductor device of one embodiment of the present invention can be formed using an oxide semiconductor film having any of the above structures.

[0500]

The structure and method described in this embodiment can be implemented by being combined as appropriate with any of the other structures and methods described
15 in the other embodiments.

[0501]

(Embodiment 4)

In this embodiment, an example of a display device including any of the transistors described in Embodiment 1 and Embodiment 2 is described below with
20 reference to FIGS. 45A and 45B, FIG. 46, FIG. 47, FIG. 48, FIG. 49, FIGS. 50A to 50D, FIGS. 51A and 51B, FIGS. 52A to 52D, FIG. 53, and FIG. 54.

[0502]

FIG. 45A is a top view of an example of a display device. A display device 300 illustrated in FIG. 45A includes a pixel portion 302 provided over a first substrate 301; a source driver circuit portion 304 and a gate driver circuit portion 306 provided
25 over the first substrate 301; a sealant 312 provided to surround the pixel portion 302, the source driver circuit portion 304, and the gate driver circuit portion 306; and a second substrate 305 provided to face the first substrate 301. The first substrate 301 and the second substrate 305 are sealed with the sealant 312. That is, the pixel portion 302, the
30 source driver circuit portion 304, and the gate driver circuit portion 306 are sealed with the first substrate 301, the sealant 312, and the second substrate 305. Although not illustrated in FIG. 45A, a display element is provided between the first substrate 301

and the second substrate 305.

[0503]

In the display device 300, a flexible printed circuit (FPC) terminal portion 308 electrically connected to the pixel portion 302, the source driver circuit portion 304, and the gate driver circuit portion 306 is provided in a region different from the region which is surrounded by the sealant 312 and positioned over the first substrate 301. Furthermore, an FPC 316 is connected to the FPC terminal portion 308, and a variety of signals and the like are supplied to the pixel portion 302, the source driver circuit portion 304, and the gate driver circuit portion 306 through the FPC 316. Furthermore, a signal line 310 is connected to the pixel portion 302, the source driver circuit portion 304, the gate driver circuit portion 306, and FPC terminal portion 308. Various signals and the like are applied to the pixel portion 302, the source driver circuit portion 304, the gate driver circuit portion 306, and the FPC terminal portion 308 via the signal line 310 from the FPC 316.

[0504]

FIG. 45B is a top view of an example of a display device. In a display device 400 illustrated in FIG. 45B, a first substrate 401 is used instead of the first substrate 301 of the display device 300 in FIG. 45A, a second substrate 405 is used instead of the second substrate 305 of the display device 300, and a pixel portion 402 is used instead of the pixel portion 302.

[0505]

A plurality of gate driver circuit portions 306 may be provided in each of the display devices 300 and 400. An example in which the source driver circuit portion 304 and the gate driver circuit portion 306 are formed over the first substrate 301 or 401 where the pixel portion 302 or 402 is also formed in the display devices 300 and 400 is described; however, one embodiment of the present invention is not limited to the structure. For example, only the gate driver circuit portion 306 may be formed over the first substrate 301 or 401 or only the source driver circuit portion 304 may be formed over the first substrate 301 or 401. In this case, a substrate where a source driver circuit, a gate driver circuit, or the like is formed (e.g., a driver circuit substrate formed using a single crystal semiconductor film or a polycrystalline semiconductor film) may be mounted on the first substrate 301 or 401.

[0506]

There is no particular limitation on the connection method of a separately formed driver circuit substrate; a chip on glass (COG) method, a wire bonding method, a tape automated bonding (TAB) method, or the like can be used. Note that the display device in this specification means an image display device, a display device, or a light source (including a lighting device or the like). Furthermore, the display device also includes the following modules in its category: a module to which a connector such as an FPC or a tape carrier package (TCP) is attached; a module having a TCP at the tip of which a printed wiring board is provided; and a module in which a driver circuit substrate or an integrated circuit (IC) is directly mounted on a display element by a COG method.

[0507]

The pixel portions 302 and 402, the source driver circuit portion 304, and the gate driver circuit portion 306 included in the display devices 300 and 400 include a plurality of transistors. As the plurality of transistors, any of the transistors that are the semiconductor devices of embodiments of the present invention can be used.

[0508]

Note that the display device 300 includes a liquid crystal element as a display element, and the display device 400 includes a light-emitting element as a display element. The display device 300 and the display device 400 are described in detail with reference to FIG. 46 and FIG. 47. Note that common portions between the display device 300 and the display device 400 are described first, and then different portions are described.

[0509]

Note that a display element, a display device which is a device including a display element, a light-emitting element, and a light-emitting device which is a device including a light-emitting element can employ various modes and can include various elements. Examples of a display element, a display device, a light-emitting element, or a light-emitting device include a display medium whose contrast, luminance, reflectance, transmittance, or the like is changed by electromagnetic action, such as an electroluminescence (EL) element (e.g., an EL element including organic and inorganic materials, an organic EL element, or an inorganic EL element), an LED (e.g., a white

LED, a red LED, a green LED, or a blue LED), a transistor (a transistor that emits light depending on current), an electron emitter, a liquid crystal element, electronic ink, an electrophoretic element, a grating light valve (GLV), a plasma display panel (PDP), a display element using micro electro mechanical system (MEMS), a digital micromirror device (DMD), a digital micro shutter (DMS), MIRASOL (registered trademark), an interferometric modulator display (IMOD) element, a MEMS shutter display element, an optical-interference-type MEMS display element, an electrowetting element, a piezoelectric ceramic display, or a carbon nanotube. Examples of display devices including EL elements include an EL display. Examples of display devices including electron emitters are a field emission display (FED) and an SED-type flat panel display (SED: surface-conduction electron-emitter display). Examples of display devices including liquid crystal elements include a liquid crystal display (e.g., a transmissive liquid crystal display, a transfective liquid crystal display, a reflective liquid crystal display, a direct-view liquid crystal display, or a projection liquid crystal display). An example of a display device including electronic ink or electrophoretic elements is electronic paper. In the case of a transfective liquid crystal display or a reflective liquid crystal display, some of or all of pixel electrodes function as reflective electrodes. For example, some or all of pixel electrodes are formed to contain aluminum, silver, or the like. In such a case, a memory circuit such as an SRAM can be provided under the reflective electrodes, leading to lower power consumption.

[0510]

<Common portions in display devices>

FIG. 46 is a cross-sectional view taken along line dashed dotted line Q-R in FIG. 45A. FIG. 47 is a cross-sectional view taken along dashed dotted line V-W in FIG. 45B.

[0511]

The display devices 300 and 400 illustrated in FIG. 46 and FIG. 47 include a lead wiring portion 311, the pixel portion 302 or 402, the source driver circuit portion 304, and the FPC terminal portion 308. Note that the lead wiring portion 311 includes a signal line 310.

[0512]

The signal line 310 included in the lead wiring portion 311 is formed in the

same process as a pair of electrode layers functioning as a source electrode layer and a drain electrode layer of a transistor 350. Note that the signal line 310 may be formed using a conductive film which is formed in the same process as a conductive film functioning as a gate electrode layer of the transistor 350.

5 [0513]

The FPC terminal portion 308 includes a connection electrode 360, an anisotropic conductive film 380, and the FPC 316. Note that the connection electrode 360 is formed in the same process as the pair of electrode layers functioning as the source electrode layer and the drain electrode layer of the transistor 350. The connection electrode 360 is electrically connected to a terminal included in the FPC 316 through the anisotropic conductive film 380.

[0514]

The display devices 300 and 400 illustrated in FIG. 46 and FIG. 47 are examples in which the transistor 350 is provided in the pixel portion 302 or 402, and a transistor 352 is provided in the source driver circuit portion 304. The transistors 350 and 352 have the same structure as the transistor 152 in FIGS. 3A to 3C. Note that the structures of the transistors 350 and 352 are not limited to the structure of the transistor 152 and the transistors 350 and 352 may have any of the structures of the above-described transistors. For example, FIG. 48 illustrates a structure in which the transistor 151 is provided in the display device 300, and FIG. 49 illustrates a structure in which the transistor 151 is provided in the display device 400.

[0515]

In the transistor used in this embodiment, which includes an oxide semiconductor film which is highly purified and in which formation of oxygen vacancy is suppressed, the current in an off state (off-state current) can be made small. Accordingly, an electrical signal such as an image signal can be held for a longer period, and a writing interval can be set longer in an on state. Accordingly, frequency of refresh operation can be reduced, which leads to an effect of suppressing power consumption.

30 [0516]

The transistor used in this embodiment, which includes an oxide semiconductor film which is highly purified and in which formation of oxygen vacancy is suppressed,

can have relatively high field-effect mobility and thus can operate at high speed. For example, with such a transistor which can operate at high speed used for a liquid crystal display device, a switching transistor in a pixel portion and a driver transistor in a driver circuit portion can be formed over one substrate. That is, a semiconductor device
5 formed using a silicon wafer or the like is not additionally needed as a driver circuit, by which the number of components of the semiconductor device can be reduced. In addition, the transistor which can operate at high speed can be used also in the pixel portion, whereby a high-quality image can be provided.

[0517]

10 A wiring containing a copper element is used for the transistor of the pixel portion and the signal line connected to the transistor used in the driver circuit portion. Therefore, in the display device of one embodiment of the present invention, signal delay or the like due to wiring resistance is reduced, which enables display on a large screen.

15 [0518]

Note that in this embodiment, the transistor 350 included in the pixel portion 302 or 402 and the transistor 352 included in the source driver circuit portion 304 have in the same size; however, this embodiment is not limited to this. The sizes (L/W) or the number of the transistors used in the pixel portion 302 and the source driver circuit
20 portion 304 may vary as appropriate. The gate driver circuit portion 306 is not illustrated in FIG. 46 to FIG. 49; however, the gate driver circuit portion 306 can have a structure similar to that of the source driver circuit portion 304.

[0519]

Furthermore, in FIG. 46 to FIG. 49, a planarization insulating film 370 is
25 provided over insulating films 364, 366, and 368 included in the transistor 350 and the transistor 352.

[0520]

The insulating films 364, 366, and 368 can be formed using materials and methods similar to those of the insulating films 114, 116, and 118 described in the
30 above embodiments, respectively.

[0521]

The planarization insulating film 370 can be formed using a heat-resistant

organic material, such as a polyimide resin, an acrylic resin, a polyimide amide resin, a benzocyclobutene resin, a polyamide resin, or an epoxy resin. Note that the planarization insulating film 370 may be formed by stacking a plurality of insulating films formed using these materials. Alternatively, a structure without the planarization
5 insulating film 370 may be employed.

[0522]

A conductive film 372 or a conductive film 444 is connected to one of the pair of electrode layers included in the transistor 350. The conductive films 372 and 444 are each formed over the planarization insulating film 370 to function as a pixel
10 electrode, i.e., one electrode of the display portion. As the conductive film 372, a conductive film which transmits visible light is preferably used. For example, the conductive film is preferably formed using a material including one of indium (In), zinc (Zn), and tin (Sn). As the conductive film 444, a reflective conductive film is preferably used.

15 [0523]

<Structure example 1 of display device using liquid crystal element as display element>

The display device 300 illustrated in each of FIG. 46 and FIG. 48 includes a liquid crystal element 375. The liquid crystal element 375 includes the conductive film 372, a conductive film 374, and a liquid crystal layer 376. The conductive film
20 374 is provided on the second substrate 305 side and functions as a counter electrode. The display device 300 in each of FIG. 46 and FIG. 48 is capable of displaying an image in such a manner that transmission or non-transmission is controlled by change in the alignment state of the liquid crystal layer 376 depending on a voltage applied to the conductive film 372 and the conductive film 374.

25 [0524]

Although not illustrated in FIG. 46 to FIG. 48, an alignment film may be provided on a side of the conductive film 372 in contact with the liquid crystal layer 376 and on a side of the conductive film 374 in contact with the liquid crystal layer 376. Although not illustrated in FIG. 46 to FIG. 48, a color filter (a coloring layer); a black
30 matrix (a light-shielding layer); an optical member (an optical substrate) such as a polarizing member, a retardation member, or an anti-reflection member; and the like may be provided as appropriate. For example, circular polarization may be employed

by using a polarizing substrate and a retardation substrate. In addition, a backlight, a sidelight, or the like may be used as a light source.

[0525]

For example, a glass substrate can be used as the first substrate 301 and the
5 second substrate 305.

[0526]

A spacer 378 is provided between the first substrate 301 and the second
substrate 305. The spacer 378 is a columnar spacer obtained by selective etching of an
insulating film and is provided to control the thickness (cell gap) of the liquid crystal
10 layer 376. Note that a spherical spacer may be used as the spacer 378.

[0527]

In the case where a liquid crystal element is used as the display element, a
thermotropic liquid crystal, a low-molecular liquid crystal, a high-molecular liquid
crystal, a polymer dispersed liquid crystal, a ferroelectric liquid crystal, an
15 anti-ferroelectric liquid crystal, or the like can be used. Such a liquid crystal material
exhibits a cholesteric phase, a smectic phase, a cubic phase, a chiral nematic phase, an
isotropic phase, or the like depending on conditions.

[0528]

Alternatively, in the case of employing a horizontal electric field mode, a liquid
20 crystal exhibiting a blue phase for which an alignment film is unnecessary may be used.
A blue phase is one of liquid crystal phases, which is generated just before a cholesteric
phase changes into an isotropic phase while temperature of cholesteric liquid crystal is
increased. Since the blue phase appears only in a narrow temperature range, a liquid
crystal composition in which several weight percent or more of a chiral material is
25 mixed is used for the liquid crystal layer in order to improve the temperature range.
The liquid crystal composition which includes liquid crystal exhibiting a blue phase and
a chiral material has a short response time and has optical isotropy. In addition, the
liquid crystal composition which includes liquid crystal exhibiting a blue phase does not
need alignment treatment and has a small viewing angle dependence. An alignment
30 film does not need to be provided and rubbing treatment is thus not necessary;
accordingly, electrostatic discharge damage caused by the rubbing treatment can be
prevented and defects and damage of the liquid crystal display device in the

manufacturing process can be reduced.

[0529]

In the case where a liquid crystal element is used as the display element, a twisted nematic (TN) mode, an in-plane-switching (IPS) mode, a fringe field switching (FFS) mode, an axially symmetric aligned micro-cell (ASM) mode, an optical compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, or the like can be used.

[0530]

A normally black liquid crystal display device such as a transmissive liquid crystal display device utilizing a vertical alignment (VA) mode may be used. There are some examples of a vertical alignment mode; for example, a multi-domain vertical alignment (MVA) mode, a patterned vertical alignment (PVA) mode, an ASV mode, or the like can be employed.

[0531]

As a display method in the pixel portion 302, a progressive method, an interlace method, or the like can be employed. Furthermore, color elements controlled in a pixel at the time of color display are not limited to three colors: R, G, and B (R, G, and B correspond to red, green, and blue, respectively). For example, a display unit may be composed of four pixels of the R pixel, the G pixel, the B pixel, and a W (white) pixel. Alternatively, any one of color elements of R, G, and B may be used in common between a plurality of pixels, as in PenTile layout. Note that, the sizes of display regions may be different between respective dots of color elements. Alternatively, one or more colors of yellow, cyan, magenta, and the like may be added to RGB. Embodiments of the disclosed invention are not limited to a display device for color display; the disclosed invention can also be applied to a display device for monochrome display.

[0532]

<Display device using light-emitting element as display element>

The display device 400 illustrated in each of FIG. 47 and FIG. 49 includes a light-emitting element 480. The light-emitting element 480 includes the conductive film 444, an EL layer 446, and a conductive film 448. The display device 400 is capable of displaying an image by light emission from the EL layer 446 included in the

light-emitting element 480.

[0533]

The display device 400 in each of FIG. 47 and FIG. 49 includes the first substrate 401, an adhesive layer 418, an insulating film 420, a first element layer 410, a sealing layer 432, a second element layer 411, an insulating film 440, an adhesive layer 412, and the second substrate 405. The first element layer 410 includes the transistors 350 and 352, the insulating films 364, 366, and 368, the connection electrode 360, the light-emitting element 480, an insulating film 430, the signal line 310, and the connection electrode 360. The second element layer 411 includes an insulating film 434, a coloring layer 436, and a light-blocking layer 438. Note that the first element layer 410 and the second element layer 411 face each other with the sealing layer 432 positioned therebetween.

[0534]

Note that the first substrate 401 and the second substrate 405 each have flexibility. Therefore, the display device 400 including the first substrate 401 and the second substrate 405 has flexibility.

[0535]

For the first substrate 401 and the second substrate 405, glass which is thin enough to have flexibility, polyester resins such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN), a polyacrylonitrile resin, a polyimide resin, a polymethyl methacrylate resin, a polycarbonate (PC) resin, a polyethersulfone (PES) resin, a polyamide resin, a cycloolefin resin, a polystyrene resin, a polyamide imide resin, a polyvinyl chloride resin, and a polyether etherketone (PEEK) resin can be used, for example. In particular, a material whose thermal expansion coefficient is low is preferred, and for example, a polyamide imide resin, a polyimide resin, or PET can be suitably used. A substrate in which a glass fiber is impregnated with an organic resin or a substrate whose thermal expansion coefficient is reduced by mixing an organic resin with an inorganic filler can also be used.

[0536]

The insulating film 430 is provided over the planarization insulating film 370 and the conductive film 444. The insulating film 430 covers part of the conductive film 444. Note that the light-emitting element 480 has a top emission structure.

Therefore, the conductive film 448 has a light-transmitting property and transmits light emitted from the EL layer 446. Although the top-emission structure is described as an example in this embodiment, one embodiment of the present invention is not limited thereto. A bottom-emission structure in which light is emitted to the conductive film 444 side, or a dual-emission structure in which light is emitted to both the conductive film 444 side and the conductive film 448 side may be employed.

[0537]

The coloring layer 436 is provided to overlap the light-emitting element 480, and the light-blocking layer 438 is provided to overlap the insulating film 430 and to be included in the lead wiring portion 311 and in the source driver circuit portion 304. The coloring layer 436 and the light-blocking layer 438 are covered with the insulating film 434. A space between the light-emitting element 480 and the insulating film 434 is filled with the sealing layer 432. Although the structure of the display device 400 with the coloring layer 436 is described in this embodiment, one embodiment of the present invention is not limited thereto. For example, a structure without the coloring layer 436 may be employed in the case where the EL layer 446 is formed by separate coloring.

[0538]

The transistors 350 and 352 are provided over the insulating film 420. The insulating film 420 and the first substrate 401 are attached to each other with the adhesive layer 418. The insulating film 440 and the second substrate 405 are attached to each other with the adhesive layer 412. Examples of the insulating film 420 and the insulating film 440 include an organic resin film of an epoxy resin, an aramid resin, an acrylic resin, a polyimide resin, a polyamide resin, a polyamide-imide resin, or the like; an inorganic insulating film with low moisture permeability such as a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, or an aluminum oxide film. The method for manufacturing the display device 400 is varied depending on the materials used for the insulating film 420 and the insulating film 440. Specifically, the method for manufacturing the display device 400 when the insulating film 420 and the insulating film 440 are formed using an organic resin film is different from that when the insulating film 420 and the insulating film 440 are formed using an inorganic insulating film. The manufacturing methods are described later.

[0539]

For each of the adhesive layers 412 and 418, a resin that is curable at room temperature such as a two-component type resin, a light-curable resin, a heat-curable resin, or the like can be used, for example. The examples include an epoxy resin, an acrylic resin, a silicone resin, a phenol resin, and the like. In particular, a material with low moisture permeability, such as an epoxy resin, is preferably used.

[0540]

Furthermore, the resin may include a drying agent. For example, a substance that adsorbs moisture by chemical adsorption, such as oxide of an alkaline earth metal (e.g., calcium oxide or barium oxide), can be used. Alternatively, a substance that adsorbs moisture by physical adsorption, such as zeolite or silica gel, may be used. The drying agent is preferably included because it can prevent an impurity such as moisture from entering the light-emitting element 480, thereby improving the reliability of the display device.

[0541]

In addition, it is preferable to mix a filler with a high refractive index (e.g., titanium oxide) into the resin, in which case the efficiency of light extraction from the light-emitting element 480 can be improved.

[0542]

The adhesive layers 412 and 418 may each also include a scattering member for scattering light. For example, each of the adhesive layers 412 and 418 can be a mixture of the above resin and particles having a refractive index different from that of the resin. The particles function as the scattering member for scattering light. The difference in refractive index between the resin and the particles with a refractive index different from that of the resin is preferably 0.1 or more, further preferably 0.3 or more. Specifically, an epoxy resin, an acrylic resin, an imide resin, silicone, or the like can be used as the resin, and titanium oxide, barium oxide, zeolite, or the like can be used as the particles. Particles of titanium oxide or barium oxide are preferable because they scatter light excellently. When zeolite is used, it can adsorb water contained in the resin and the like, thereby improving the reliability of the light-emitting element.

[0543]

The display device described in this embodiment can be manufactured in such

a manner that the first element layer 410 is formed over a substrate with high heat resistance; the first element layer 410 is separated from the substrate; and the insulating film 420, the transistors 350 and 352, the light-emitting element 480, and the like are transferred over the first substrate 401 using the adhesive layer 418.

5 [0544]

In the case where, for example, a material which has high water permeability and low heat resistance (e.g., a resin) is used for the first substrate 401 and the second substrate 405, it is difficult to perform the manufacturing process at high temperature (e.g., 300 °C); therefore, conditions for forming the transistor or the insulating film over
10 the first substrate 401 and the second substrate 405 are limited. In the manufacturing method of this embodiment, a transistor and the like can be formed over a substrate with high heat resistance; thus, a highly reliable transistor and an insulating film with sufficiently low water permeability can be formed. In addition, by transferring transistor or the insulating film to the first substrate 401 or the second substrate 405, a
15 highly reliable display device can be manufactured. Thus, according to one embodiment of the present invention, a thin or/and lightweight light-emitting device with high reliability can be provided.

[0545]

A material with high toughness is preferably used for the first substrate 401 and
20 the second substrate 405. Thus, a light-emitting device with high impact resistance that is less likely to be broken can be provided. For example, when an organic resin substrate is used as the first substrate 401 and the second substrate 405, the display device 400 can be lightweight and unlikely to broken as compared to the case where a glass substrate used as the substrate.

25 [0546]

Furthermore, when a material with high thermal emissivity is used for the first substrate 401, the surface temperature of the display device can be prevented from rising, leading to prevention of breakage or a decrease in reliability of the display device. For example, the first substrate 401 may have a stacked-layer structure of a metal
30 substrate and a layer with high thermal emissivity (the layer can be formed using a metal oxide or a ceramic material, for example).

[0547]

Here, a method for manufacturing the display device 400 illustrated in each of FIG. 47 and FIG. 49 is described below in detail with reference to FIGS. 50A to 50D, FIGS. 51A and 51B, FIGS. 52A to 52D, and FIG. 53. Note that FIGS. 50A to 50D illustrate an example in which an organic resin film is used for the insulating film 420 and the insulating film 440, and FIG. 53 illustrates an example in which an inorganic insulating film is used as the insulating film 420 and the insulating film 440. In FIGS. 50A to 50D, FIGS. 51A and 51B, FIGS. 52A to 52D, and FIG. 53, to avoid complication of the drawings, the first element layer 410 and the second element layer 411 illustrated in each of FIG. 47 and FIG. 49 are not illustrated.

[0548]

<Method 1 for manufacturing display device>

First, a method for manufacturing the display device in which an organic resin film is used as each of the insulating film 420 and the insulating film 440 is described.

[0549]

First of all, the insulating film 420 is formed over a substrate 462, and the first element layer 410 is formed over the insulating film 420 (see FIG. 50A).

[0550]

It is necessary that the substrate 462 have at least heat resistance high enough to withstand heat treatment performed later. For example, a glass substrate, a ceramic substrate, a quartz substrate, or a sapphire substrate may be used as the substrate 462.

[0551]

In the case where a glass substrate is used as the substrate 462, an insulating film such as a silicon oxide film, a silicon oxynitride film, a silicon nitride film, or a silicon nitride oxide film is preferably formed between the substrate 462 and the insulating film 420, in which case contamination from the glass substrate can be prevented.

[0552]

For the insulating film 420, an organic resin film of an epoxy resin, an aramid resin, an acrylic resin, a polyimide resin, a polyamide resin, a polyamide-imide resin, or the like can be used. Among them, a polyimide resin is preferably used because it has high heat resistance. For example, in the case where a polyimide resin is used for the insulating film 420, the thickness of the polyimide resin is greater than or equal to 3 nm

and less than or equal to 20 μm , preferably greater than or equal to 500 nm and less than or equal to 2 μm . In the case where a polyimide resin is used for the insulating film 420, the insulating film 420 can be formed by a spin coating method, a dip coating method, a doctor blade method, or the like. In the case where a polyimide resin is used for the insulating film 420, for example, the polyimide resin with a desired thickness can be obtained by removing an excess resin by a doctor blade method.

[0553]

The transistor 350 and the like in the first element layer 410 can be formed according to the method for manufacturing the transistor 150 described in the above embodiment. In this embodiment, methods for forming components other than the transistor 350 are described below in detail.

[0554]

Note that formation temperatures of all the components in the first element layer 410, including the transistor 350, are preferably higher than or equal to room temperature and lower than or equal to 300 $^{\circ}\text{C}$. For example, the deposition temperature of an insulating film or a conductive film which is formed in the first element layer 410 using an inorganic material is higher than or equal to 150 $^{\circ}\text{C}$ and lower than or equal to 300 $^{\circ}\text{C}$, preferably higher than or equal to 200 $^{\circ}\text{C}$ and lower than or equal to 270 $^{\circ}\text{C}$. Furthermore, an insulating film or the like formed in the first element layer 410 using an organic resin material is preferably formed at a temperature higher than or equal to room temperature and lower than or equal to 100 $^{\circ}\text{C}$. In addition, in the formation process of the transistor 350, for example, a heating step is not necessarily performed.

[0555]

It is preferable that the CAAC-OS, which is described above, be used for a channel region of the transistor 350. In the case where the CAAC-OS is used for the channel region of the transistor 350, for example, when the display device 400 is bent, a crack or the like is less likely to be generated in the channel region, resulting in high resistance against bending.

[0556]

The insulating film 430, the conductive film 372, the EL layer 446, and the

conductive film 448 included in the first element layer 410 are formed in the following manner.

[0557]

For the insulating film 430, an organic resin or an inorganic insulating material
5 can be used. As the organic resin, for example, a polyimide resin, a polyamide resin, an acrylic resin, a siloxane resin, an epoxy resin, or a phenol resin can be used. As the inorganic insulating material, silicon oxide, silicon oxynitride, or the like can be used. In particular, a photosensitive resin is preferably used for easy formation of the insulating film 430. There is no particular limitation on the method for forming the
10 insulating film 430; for example, a photolithography method, a sputtering method, an evaporation method, a droplet discharging method (e.g., an inkjet method), a printing method (e.g., a screen printing method or an offset printing method), or the like can be used.

[0558]

15 It is preferable that a metal film which is highly reflective to visible light be used as the conductive film 444. For example, aluminum, silver, an alloy thereof, or the like can be used for the metal film. The conductive film 444 can be formed by a sputtering method, for example.

[0559]

20 A light-emitting material which can emit light by recombination of holes and electrons injected from the conductive film 444 and the conductive film 448 may be used for the EL layer 446. In addition to the light-emitting material, functional layers such as a hole-injection layer, a hole-transport layer, an electron-transport layer, and an electron-injection layer may be used as needed. The EL layer 446 can be formed by an
25 evaporation method, a coating method, or the like.

[0560]

As the conductive film 448, a conductive film which transmits visible light is preferably used, for example. For example, a material including one of indium (In), zinc (Zn), and tin (Sn) is preferably used for the conductive film. For the conductive
30 film 448, for example, a light-transmitting conductive material such as indium oxide including tungsten oxide, indium zinc oxide including tungsten oxide, indium oxide including titanium oxide, indium tin oxide including titanium oxide, indium tin oxide

(ITO), indium zinc oxide, or indium tin oxide to which silicon oxide is added can be used. In particular, indium tin oxide to which silicon oxide is added is preferably used for the conductive film 448 because a crack is less likely to be generated in the conductive film 448 when the display device 400 is bent. The conductive film 448 can
5 be formed by a sputtering method, for example.

[0561]

Next, the first element layer 410 and a temporary supporting substrate 466 are attached with an adhesive 464 for separation, and then the insulating film 420 and the first element layer 410 are separated from the substrate 462. Thus, the temporary
10 supporting substrate 466 is provided with the insulating film 420 and the first element layer 410 (see FIG. 50B).

[0562]

As the temporary supporting substrate 466, a glass substrate, a quartz substrate, a sapphire substrate, a ceramic substrate, a metal substrate, or the like can be used.
15 Alternatively, a plastic substrate that can withstand a processing temperature of this embodiment may be used, or a flexible film-like substrate may be used.

[0563]

An adhesive with which the temporary supporting substrate 466 and the element layer 410 can be chemically or physically separated when necessary, such as an
20 adhesive that is soluble in water or a solvent or an adhesive which is capable of being plasticized upon irradiation of UV light or the like, is used as the adhesive 464 for separation.

[0564]

Any of various methods can be used as appropriate as the process for
25 transferring the components to the temporary supporting substrate 466. For example, the substrate 462 and the insulating film 420 can be separated from each other in such a manner that the insulating film 420 is irradiated with laser light 468 from a side of the substrate 462 where the insulating film 420 is not formed, i.e., from the bottom side in FIG. 50B to make the insulating film 420 weak. Furthermore, a region where adhesion
30 between the substrate 462 and the insulating film 420 is low and a region where adhesion between the substrate 462 and the insulating film 420 is high may be formed by adjustment of the irradiation energy density of the laser light 468, and then the

substrate 462 and the insulating film 420 may be separated.

[0565]

Although the method in which separation is caused at the interface between the substrate 462 and the insulating film 420 is described, one embodiment of the present invention is not limited thereto. For example, separation may be caused at the interface between the insulating film 420 and the first element layer 410.

[0566]

The insulating film 420 may be separated from the substrate 462 by filling the interface between the substrate 462 and the insulating film 420 with a liquid.

Alternatively, the first element layer 410 may be separated from the insulating film 420 by filling the interface between the insulating film 420 and the first element layer 410 with a liquid. As the liquid, water, a polar solvent, or the like can be used, for example. The interface along which the insulating film 420 is separated, specifically, the interface between the substrate 462 and the insulating film 420 or the interface between the insulating film 420 and the first element layer 410 is filled with a liquid, whereby an influence of static electricity and the like which are generated owing to the separation and applied to the first element layer 410 can be reduced.

[0567]

Next, the first substrate 401 is attached to the insulating film 420 using the adhesive layer 418 (see FIG. 50C).

[0568]

Then, the adhesive 464 for separation and the temporary supporting substrate 466 are removed from the first element layer 410 by dissolving or plasticizing the adhesive 464 for separation (see FIG. 50D).

[0569]

Note that the adhesive 464 for separation is preferably removed by water, a solvent, or the like to expose the surface of the first element layer 410.

[0570]

Through the above process, the first element layer 410 can be formed over the first substrate 401.

[0571]

Next, the second substrate 405, the adhesive layer 412 over the second

substrate 405, the insulating film 440 over the adhesive layer 412, and the second element layer 411 are formed by a process similar to that illustrated in FIGS. 50A to 50D (see FIG. 51A).

[0572]

5 The insulating film 440 included in the second element layer 411 can be formed using a material similar to that of the insulating film 420, here, using an organic resin film.

[0573]

10 The coloring layer 436 included second element layer 411 is a coloring layer that transmits light in a specific wavelength range. For example, a red (R) color filter for transmitting light in a red wavelength range, a green (G) color filter for transmitting light in a green wavelength range, a blue (B) color filter for transmitting light in a blue wavelength range, or the like can be used. Each color filter is formed in a desired position with any of various materials by a printing method, an inkjet method, an
15 etching method using a photolithography technique, or the like.

[0574]

 The light-blocking layer 438 included in the second element layer 411 has a function of shielding light in a particular wavelength region, and can be a metal film or an organic insulating film including a black pigment or the like.

20 [0575]

 The insulating film 434 included in the second element layer 411 can be formed using an organic insulating film of an acrylic resin or the like. Note that the insulating film 434 is not necessarily formed.

[0576]

25 Next, a space between the first element layer 410 and the second element layer 411 is filled with the sealing layer 432 to attach the first element layer 410 and the second element layer 411 (see FIG. 51B).

[0577]

30 With the sealing layer 432, for example, solid sealing is possible. Note that the sealing layer 432 preferably has flexibility. For example, a glass material such as a glass frit, or a resin that is curable at room temperature such as a two-component type resin, a light curable resin, a heat-curable resin, and the like can be used for the sealing

layer 432.

[0578]

Finally, the anisotropic conductive film 380 and an FPC 408 are attached to the connection electrode 360. An IC chip or the like may be mounted if necessary.

5 [0579]

Through to the above process, the display device 400 illustrated in FIG. 47 can be manufactured.

[0580]

<Method 2 for manufacturing display device>

10 Next, a method for manufacturing a display device in which an inorganic insulating film is used as each of the insulating film 420 and the insulating film 440 is described below. Note that common reference numerals are used for components that have functions similar to functions described in Method 1 for manufacturing display device, and detailed descriptions of the components are omitted.

15 [0581]

First, a separation layer 463 is formed over the substrate 462. Then, the insulating film 420 is formed over the separation layer 463, and the first element layer 410 is formed over the insulating film 420 (see FIG. 52A).

[0582]

20 The separation layer 463 can have a single-layer structure or a stacked-layer structure containing an element selected from tungsten, molybdenum, titanium, tantalum, niobium, nickel, cobalt, zirconium, zinc, ruthenium, rhodium, palladium, osmium, iridium, and silicon; an alloy material containing any of the elements; or a compound material containing any of the elements, for example. In the case of a layer
25 containing silicon, a crystal structure of the layer containing silicon may be amorphous, microcrystal, polycrystal, or single crystal

[0583]

The separation layer 463 can be formed by a sputtering method, a PE-CVD method, a coating method, a printing method, or the like. Note that a coating method
30 includes a spin coating method, a droplet discharge method, and a dispensing method.

[0584]

In the case where the separation layer 463 has a single-layer structure, a

tungsten layer, a molybdenum layer, or a layer containing a mixture of tungsten and molybdenum is preferably formed. Alternatively, a layer containing an oxide or an oxynitride of tungsten, a layer containing an oxide or an oxynitride of molybdenum, or a layer containing an oxide or an oxynitride of a mixture of tungsten and molybdenum may be formed. Note that a mixture of tungsten and molybdenum is an alloy of tungsten and molybdenum, for example.

[0585]

When the separation layer 463 has a stacked-layer structure including a layer containing tungsten and a layer containing an oxide of tungsten, it may be utilized that the layer containing tungsten is formed first and an insulating layer formed of oxide is formed thereover so that a layer containing an oxide of tungsten is formed at the interface between the tungsten layer and the insulating layer. Alternatively, the layer containing an oxide of tungsten may be formed by performing thermal oxidation treatment, oxygen plasma treatment, nitrous oxide (N₂O) plasma treatment, treatment with a highly oxidizing solution such as ozone water, or the like on the surface of the layer containing tungsten. Plasma treatment or heat treatment may be performed in an atmosphere of oxygen, nitrogen, or nitrous oxide alone, or a mixed gas of any of these gasses and another gas. Surface condition of the separation layer 463 is changed by the plasma treatment or heat treatment, whereby adhesion between the separation layer 463 and the insulating film 420 formed later can be controlled.

[0586]

The insulating film 420 can be formed using an inorganic insulating film with low moisture permeability, such as a silicon oxide film, a silicon nitride film, a silicon oxynitride film, a silicon nitride oxide film, or an aluminum oxide film. The inorganic insulating film can be formed by a sputtering method or a PE-CVD method, for example.

[0587]

Next, the first element layer 410 and a temporary supporting substrate 466 are attached with an adhesive 464 for separation, and then the insulating film 420 and the first element layer 410 are separated from the separation layer 463. Thus, the temporary supporting substrate 466 is provided with the insulating film 420 and the first element layer 410 (see FIG. 52B).

[0588]

Any of various methods can be used as appropriate as the process for transferring the layer to the temporary supporting substrate 466. For example, in the case where a layer including a metal oxide film is formed at the interface between the separation layer 463 and the insulating film 420, the metal oxide film is made to be weakened by crystallization, so that the insulating film 420 can be separated from the separation layer 463. Alternatively, in the case where the separation layer 463 is formed using a tungsten film, separation is performed in such a manner that the tungsten film is etched using a mixed solution of ammonia water and a hydrogen peroxide solution.

[0589]

The insulating film 420 may be separated from the separation layer 463 by filling the interface between the separation layer 463 and the insulating film 420 with a liquid. As the liquid, water, a polar solvent, or the like can be used, for example. The interface along which the insulating film 420 is separated, specifically, the interface between the separation layer 463 and the insulating film 420 is filled with a liquid, whereby an influence of static electricity and the like which are generated owing to the separation and applied to the first element layer 410 can be reduced.

[0590]

Next, the first substrate 401 is attached to the insulating film 420 using the adhesive layer 418 (see FIG. 52C).

[0591]

Then, the adhesive 464 for separation and the temporary supporting substrate 466 are removed from the first element layer 410 by dissolving or plasticizing the adhesive 464 for separation (see FIG. 52D).

[0592]

Note that the adhesive 464 for separation is preferably removed by water, a solvent, or the like to expose the surface of the first element layer 410.

[0593]

Through the above process, the first element layer 410 can be formed over the first substrate 401.

[0594]

Next, the second substrate 405, the adhesive layer 412 over the second substrate 405, the insulating film 440 over the adhesive layer 412, and the second element layer 411 are formed by a process similar to that illustrated in FIGS. 52A to 52D. After that, a space between the first element layer 410 and the second element layer 411 is filled with the sealing layer 432, so that the first element layer 410 and the second element layer 411 are attached to each other.

[0595]

Finally, the anisotropic conductive film 380 and the FPC 408 are attached to the connection electrode 360. An IC chip or the like may be mounted if necessary.

10 [0596]

Through to the above process, the display device 400 illustrated in each of FIG. 47 and FIG. 49 can be manufactured.

[0597]

Next, a display device 300A that is a modification example of the display device 300 illustrated in each of FIG. 46 and FIG. 48 is described with reference to FIG. 53 and FIG. 54. Note that the display device 300A in FIG. 53 and the display device 300A in FIG. 54 differ in the structures of the transistors 350 and 352. The transistors 350 and 352 of the display device 300A in FIG. 53 each have a structure similar to that of the transistor 152, and the transistors 350 and 352 of the display device 300A in FIG. 54 each have a structure similar to that of the transistor 151.

20

[0598]

<Structure example 2 of display device using liquid crystal element as display element>

The display device 300A in each of FIG. 53 and FIG. 54 includes the liquid crystal element 375. The liquid crystal element 375 includes a conductive film 373, a conductive film 377, and the liquid crystal layer 376. The conductive film 373 is provided over the planarization insulating film 370 over the first substrate 301 to function as a reflective electrode. The display device 300A in each of FIG. 53 and FIG. 54 is what is called a reflective color liquid crystal display device in which external light is reflected by the conductive film 373 and transmitted through the coloring layer 436 to display an image.

30

[0599]

Note that projections and depressions are provided in part of the planarization

insulating film 370 of the pixel portion 302 in the display device 300A in each of FIG. 53 and FIG. 54. The projections and depressions can be formed in such a manner that the planarization insulating film 370 is formed using an organic resin film or the like, and projections and depressions are formed on the surface of the organic resin film.

5 The conductive film 373 functioning as a reflective electrode is formed along the projections and depressions. Therefore, when external light is incident on the conductive film 373, the light is reflected diffusely at the surface of the conductive film 373, whereby visibility can be improved.

[0600]

10 The display device 300A includes the light-blocking layer 438, the insulating film 434, and the coloring layer 436 on the second substrate 305 side. For the light-blocking layer 438, the insulating film 434, and the coloring layer 436, the materials and methods in the description of the display device 400 can be referred to. The conductive film 373 included in the display device 300A is electrically connected
15 to a source electrode layer or a drain electrode layer of the transistor 350. For the conductive film 373, the material and method in the description of the conductive film 444 can be referred to.

[0601]

The display device 300A includes a capacitor 390. The capacitor 390
20 includes a pair of electrodes and an insulating film therebetween. Specifically, in the capacitor 390, a conductive film which is formed in the same process as a conductive film functioning as a gate electrode layer of the transistor 350 is used as one electrode, a conductive film which is formed in the same process as a conductive film functioning as a source electrode layer or a drain electrode layer of the transistor 350 is used as the
25 other electrode, and a protective insulating film and an insulating film which is formed in the same process as an insulating film functioning as a gate insulating film of the transistor 350 are included.

[0602]

As described above, the transistor that is the semiconductor device of one
30 embodiment of the present invention can be applied to a variety of display devices.

[0603]

The structure described in this embodiment can be used in appropriate

combination with the structure described in any of the other embodiments.

[0604]

(Embodiment 5)

In this embodiment, a display device that can be formed using a semiconductor
5 device of one embodiment of the present invention is described with reference to FIGS.
55A to 55C.

[0605]

The display device illustrated in FIG. 55A includes a region including pixels of
display elements (hereinafter the region is referred to as a pixel portion 502), a circuit
10 portion being provided outside the pixel portion 502 and including a circuit for driving
the pixels (hereinafter the portion is referred to as a driver circuit portion 504), circuits
each having a function of protecting an element (hereinafter the circuits are referred to
as protection circuits 506), and a terminal portion 507. Note that the protection
circuits 506 are not necessarily provided.

15 [0606]

A part or the whole of the driver circuit portion 504 is preferably formed over a
substrate over which the pixel portion 502 is formed, in which case the number of
components and the number of terminals can be reduced. When a part or the whole of
the driver circuit portion 504 is not formed over the substrate over which the pixel
20 portion 502 is formed, the part or the whole of the driver circuit portion 504 can be
mounted by COG or tape automated bonding (TAB).

[0607]

The pixel portion 502 includes a plurality of circuits for driving display
elements arranged in X rows (X is a natural number of 2 or more) and Y columns (Y is a
25 natural number of 2 or more) (hereinafter, such circuits are referred to as pixel circuits
501). The driver circuit portion 504 includes driver circuits such as a circuit for
supplying a signal (scan signal) to select a pixel (hereinafter, the circuit is referred to as
a gate driver 504a) and a circuit for supplying a signal (data signal) to drive a display
element in a pixel (hereinafter, the circuit is referred to as a source driver 504b).

30 [0608]

The gate driver 504a includes a shift register or the like. The gate driver 504a
receives a signal for driving the shift register through the terminal portion 507 and

outputs a signal. For example, the gate driver 504a receives a start pulse signal, a clock signal, or the like and outputs a pulse signal. The gate driver 504a has a function of controlling the potentials of wirings supplied with scan signals (hereinafter, such wirings are referred to as scan lines GL_1 to GL_X). Note that a plurality of gate drivers 504a may be provided to control the scan lines GL_1 to GL_X separately. Alternatively, the gate driver 504a has a function of supplying an initialization signal. Without being limited thereto, the gate driver 504a can supply another signal.

[0609]

The source driver 504b includes a shift register or the like. The source driver 504b receives a signal (video signal) from which a data signal is derived, as well as a signal for driving the shift register, through the terminal portion 507. The source driver 504b has a function of generating a data signal to be written to the pixel circuit 501 which is based on the video signal. In addition, the source driver 504b has a function of controlling output of a data signal in response to a pulse signal produced by input of a start pulse signal, a clock signal, or the like. Further, the source driver 504b has a function of controlling the potentials of wirings supplied with data signals (hereinafter such wirings are referred to as data lines DL_1 to DL_Y). Alternatively, the source driver 504b has a function of supplying an initialization signal. Without being limited thereto, the source driver 504b can supply another signal.

[0610]

The source driver 504b includes a plurality of analog switches or the like, for example. The source driver 504b can output, as the data signals, signals obtained by time-dividing the video signal by sequentially turning on the plurality of analog switches. The source driver 504b may include a shift register or the like.

[0611]

A pulse signal and a data signal are input to each of the plurality of pixel circuits 501 through one of the plurality of scan lines GL supplied with scan signals and one of the plurality of data lines DL supplied with data signals, respectively. Writing and holding of the data signal to and in each of the plurality of pixel circuits 501 are controlled by the gate driver 504a. For example, to the pixel circuit 501 in the m -th row and the n -th column (m is a natural number of less than or equal to X , and n is a

natural number of less than or equal to Y), a pulse signal is input from the gate driver 504a through the scan line GL_{*m*}, and a data signal is input from the source driver 504b through the data line DL_{*n*} in accordance with the potential of the scan line GL_{*m*}.

[0612]

5 The protection circuit 506 shown in FIG. 55A is connected to, for example, the scan line GL between the gate driver 504a and the pixel circuit 501. Alternatively, the protection circuit 506 is connected to the data line DL between the source driver 504b and the pixel circuit 501. Alternatively, the protection circuit 506 can be connected to a wiring between the gate driver 504a and the terminal portion 507. Alternatively, the
10 protection circuit 506 can be connected to a wiring between the source driver 504b and the terminal portion 507. Note that the terminal portion 507 means a portion having terminals for inputting power, control signals, and video signals to the display device from external circuits.

[0613]

15 The protection circuit 506 is a circuit that electrically connects a wiring connected to the protection circuit to another wiring when a potential out of a certain range is applied to the wiring connected to the protection circuit.

[0614]

As illustrated in FIG. 55A, the protection circuits 506 are provided for the pixel
20 portion 502 and the driver circuit portion 504, so that the resistance of the display device to overcurrent generated by electrostatic discharge (ESD) or the like can be improved. Note that the configuration of the protection circuits 506 is not limited to that, and for example, the protection circuit 506 may be configured to be connected to the gate driver 504a or the protection circuit 506 may be configured to be connected to
25 the source driver 504b. Alternatively, the protection circuit 506 may be configured to be connected to the terminal portion 507.

[0615]

In FIG. 55A, an example in which the driver circuit portion 504 includes the gate driver 504a and the source driver 504b is shown; however, the structure is not
30 limited thereto. For example, only the gate driver 504a may be formed and a separately prepared substrate where a source driver circuit is formed (e.g., a driver

circuit substrate formed with a single crystal semiconductor film or a polycrystalline semiconductor film) may be mounted.

[0616]

Each of the plurality of pixel circuits 501 in FIG. 55A can have the structure
5 illustrated in FIG. 55B, for example.

[0617]

The pixel circuit 501 illustrated in FIG. 55B includes a liquid crystal element 570, a transistor 550, and a capacitor 560.

[0618]

10 The semiconductor device of one embodiment of the present invention can be used as, for example, the transistor 550. As the transistor 550, any of the transistors described in the above embodiment, for example, can be used

[0619]

The potential of one of a pair of electrodes of the liquid crystal element 570 is
15 set in accordance with the specifications of the pixel circuit 501 as appropriate. The alignment state of the liquid crystal element 570 depends on written data. A common potential may be supplied to one of the pair of electrodes of the liquid crystal element 570 included in each of the plurality of pixel circuits 501. Further, the potential supplied to one of the pair of electrodes of the liquid crystal element 570 in the pixel
20 circuit 501 in one row may be different from the potential supplied to one of the pair of electrodes of the liquid crystal element 570 in the pixel circuit 501 in another row.

[0620]

As examples of a driving method of the display device including the liquid crystal element 570, any of the following modes can be given: a TN mode, an STN
25 mode, a VA mode, an axially symmetric aligned micro-cell (ASM) mode, an optically compensated birefringence (OCB) mode, a ferroelectric liquid crystal (FLC) mode, an antiferroelectric liquid crystal (AFLC) mode, an MVA mode, a patterned vertical alignment (PVA) mode, an IPS mode, an FFS mode, a transverse bend alignment (TBA) mode, and the like. Other examples of the driving method of the display device
30 include an electrically controlled birefringence (ECB) mode, a polymer dispersed liquid crystal (PDLC) mode, a polymer network liquid crystal (PNLC) mode, and a guest-host mode. Note that the present invention is not limited to these examples, and various

liquid crystal elements and driving methods can be applied to the liquid crystal element and the driving method thereof.

[0621]

In the pixel circuit 501 in the m -th row and the n -th column, one of a source electrode and a drain electrode of the transistor 550 is electrically connected to the data line DL $_n$, and the other is electrically connected to the other of the pair of electrodes of the liquid crystal element 570. A gate electrode of the transistor 550 is electrically connected to the scan line GL $_m$. The transistor 550 has a function of controlling whether to write a data signal by being turned on or off.

[0622]

One of a pair of electrodes of the capacitor 560 is electrically connected to a wiring to which a potential is supplied (hereinafter referred to as a potential supply line VL), and the other is electrically connected to the other of the pair of electrodes of the liquid crystal element 570. The potential of the potential supply line VL is set in accordance with the specifications of the pixel circuit 501 as appropriate. The capacitor 560 functions as a storage capacitor for storing written data.

[0623]

For example, in the display device including the pixel circuit 501 in FIG. 55B, the pixel circuits 501 are sequentially selected row by row by the gate driver 504a illustrated in FIG. 55A, whereby the transistors 550 are turned on and a data signal is written.

[0624]

When the transistors 550 are turned off, the pixel circuits 501 in which the data has been written are brought into a holding state. This operation is sequentially performed row by row; thus, an image can be displayed.

[0625]

Alternatively, each of the plurality of pixel circuits 501 in FIG. 55A can have the structure illustrated in FIG. 55C, for example.

[0626]

The pixel circuit 501 illustrated in FIG. 55C includes transistors 552 and 554, a capacitor 562, and a light-emitting element 572. Here, any of the transistors described

in the above embodiment, for example, can be used as one or both of the transistors 552 and 554.

[0627]

One of a source electrode and a drain electrode of the transistor 552 is electrically connected to a wiring to which a data signal is supplied (hereinafter referred to as a signal line DL_{*n*}). A gate electrode of the transistor 552 is electrically connected to a wiring to which a gate signal is supplied (hereinafter referred to as a scan line GL_{*m*}).

[0628]

The transistor 552 has a function of controlling whether to write a data signal by being turned on or off.

[0629]

One of a pair of electrodes of the capacitor 562 is electrically connected to a wiring to which a potential is supplied (hereinafter referred to as a potential supply line VL_{*a*}), and the other is electrically connected to the other of the source electrode and the drain electrode of the transistor 552.

[0630]

The capacitor 562 functions as a storage capacitor for storing written data.

[0631]

One of a source electrode and a drain electrode of the transistor 554 is electrically connected to the potential supply line VL_{*a*}. Further, a gate electrode of the transistor 554 is electrically connected to the other of the source electrode and the drain electrode of the transistor 552.

[0632]

One of an anode and a cathode of the light-emitting element 572 is electrically connected to a potential supply line VL_{*b*}, and the other is electrically connected to the other of the source electrode and the drain electrode of the transistor 554.

[0633]

As the light-emitting element 572, an organic electroluminescent element (also referred to as an organic EL element) or the like can be used, for example. Note that the light-emitting element 572 is not limited to an organic EL element; an inorganic EL

element including an inorganic material may be used.

[0634]

A high power supply potential VDD is supplied to one of the potential supply line VL_a and the potential supply line VL_b, and a low power supply potential VSS is
5 supplied to the other.

[0635]

For example, in the display device including the pixel circuit 501 in FIG. 55C, the pixel circuits 501 are sequentially selected row by row by the gate driver 504a illustrated in FIG. 55A, whereby the transistors 552 are turned on and a data signal is
10 written.

[0636]

When the transistors 552 are turned off, the pixel circuits 501 in which the data has been written are brought into a holding state. Further, the amount of current flowing between the source electrode and the drain electrode of the transistor 554 is
15 controlled in accordance with the potential of the written data signal. The light-emitting element 572 emits light with a luminance corresponding to the amount of flowing current. This operation is sequentially performed row by row; thus, an image can be displayed.

[0637]

20 The structure described in this embodiment can be used in appropriate combination with any of the structures described in the other embodiments.

[0638]

(Embodiment 6)

In this embodiment, a display module and electronic devices that can be
25 formed using a semiconductor device of one embodiment of the present invention are described with reference to FIG. 56 and FIGS. 57A to 57H.

[0639]

In a display module 8000 illustrated in FIG. 56, a touch panel 8004 connected to an FPC 8003, a display panel 8006 connected to an FPC 8005, a backlight 8007, a
30 frame 8009, a printed board 8010, and a battery 8011 are provided between an upper cover 8001 and a lower cover 8002.

[0640]

The semiconductor device of one embodiment of the present invention can be used for, for example, the display panel 8006.

[0641]

The shapes and sizes of the upper cover 8001 and the lower cover 8002 can be changed as appropriate in accordance with the sizes of the touch panel 8004 and the display panel 8006.

[0642]

The touch panel 8004 can be a resistive touch panel or a capacitive touch panel and can be formed to overlap with the display panel 8006. A counter substrate (sealing substrate) of the display panel 8006 can have a touch panel function. A photosensor may be provided in each pixel of the display panel 8006 to form an optical touch panel.

[0643]

The backlight 8007 includes a light source 8008. Note that although a structure in which the light sources 8008 are provided over the backlight 8007 is illustrated in FIG. 56, one embodiment of the present invention is not limited to this structure. For example, a structure in which the light source 8008 is provided at an end portion of the backlight 8007 and a light diffusion plate is further provided may be employed. Note that the backlight 8007 need not be provided in the case where a self-luminous light-emitting element such as an organic EL element is used or in the case where a reflective panel or the like is employed.

[0644]

The frame 8009 protects the display panel 8006 and also functions as an electromagnetic shield for blocking electromagnetic waves generated by the operation of the printed board 8010. The frame 8009 may function as a radiator plate.

[0645]

The printed board 8010 is provided with a power supply circuit and a signal processing circuit for outputting a video signal and a clock signal. As a power source for supplying power to the power supply circuit, an external commercial power source or a power source using the battery 8011 provided separately may be used. The battery 8011 can be omitted in the case of using a commercial power source.

[0646]

The display module 8000 may be additionally provided with a member such as a polarizing plate, a retardation plate, or a prism sheet.

[0647]

FIGS. 57A to 57H illustrate electronic devices. These electronic devices can include a housing 5000, a display portion 5001, a speaker 5003, an LED lamp 5004, operation keys 5005 (including a power switch or an operation switch), a connection terminal 5006, a sensor 5007 (a sensor having a function of measuring or sensing force, displacement, position, speed, acceleration, angular velocity, rotational frequency, distance, light, liquid, magnetism, temperature, chemical substance, sound, time, hardness, electric field, current, voltage, electric power, radiation, flow rate, humidity, gradient, oscillation, odor, or infrared ray), a microphone 5008, and the like.

[0648]

FIG. 57A illustrates a mobile computer that can include a switch 5009, an infrared port 5010, and the like in addition to the above components. FIG. 57B illustrates a portable image reproducing device (e.g., a DVD player) that is provided with a memory medium and can include a second display portion 5002, a memory medium reading portion 5011, and the like in addition to the above components. FIG. 57C illustrates a goggle-type display that can include the second display portion 5002, a support 5012, an earphone 5013, and the like in addition to the above components. FIG. 57D illustrates a portable game machine that can include the memory medium reading portion 5011 and the like in addition to the above components. FIG. 57E illustrates a digital camera that has a television reception function and can include an antenna 5014, a shutter button 5015, an image receiving portion 5016, and the like in addition to the above components. FIG. 57F illustrates a portable game machine that can include the second display portion 5002, the memory medium reading portion 5011, and the like in addition to the above components. FIG. 57G illustrates a television receiver that can include a tuner, an image processing portion, and the like in addition to the above components. FIG. 57H illustrates a portable television receiver that can include a charger 5017 capable of transmitting and receiving signals, and the like in addition to the above components.

[0649]

The electronic devices illustrated in FIGS. 57A to 57H can have a variety of

functions, for example, a function of displaying a variety of data (a still image, a moving image, a text image, and the like) on the display portion, a touch panel function, a function of displaying a calendar, date, time, and the like, a function of controlling a process with a variety of software (programs), a wireless communication function, a function of being connected to a variety of computer networks with a wireless communication function, a function of transmitting and receiving a variety of data with a wireless communication function, a function of reading a program or data stored in a memory medium and displaying the program or data on the display portion, and the like. Further, the electronic device including a plurality of display portions can have a function of displaying image data mainly on one display portion while displaying text data on another display portion, a function of displaying a three-dimensional image by displaying images on a plurality of display portions with a parallax taken into account, or the like. Furthermore, the electronic device including an image receiving portion can have a function of shooting a still image, a function of taking a moving image, a function of automatically or manually correcting a shot image, a function of storing a shot image in a memory medium (an external memory medium or a memory medium incorporated in the camera), a function of displaying a shot image on the display portion, or the like. Note that functions that can be provided for the electronic devices illustrated in FIGS. 57A to 57H are not limited to those described above, and the electronic devices can have a variety of functions.

[0650]

The electronic devices described in this embodiment each include the display portion for displaying some sort of data. Note that the semiconductor device of one embodiment of the present invention can also be used for an electronic device which does not have a display portion.

[0651]

The structure described in this embodiment can be used in appropriate combination with any of the structures described in the other embodiments.

[Example 1]

[0652]

In this example, observation was performed on a cross section of a stacked-layer structure of an insulating film functioning as a gate insulating film of a

transistor of one embodiment of the present invention, a conductive film functioning as a source electrode layer or a drain electrode layer of the transistor, and an insulating film functioning as a protective film for the transistor, and the composition of the conductive film functioning as a source electrode layer or a drain electrode layer was analyzed. Details of a sample formed in this example are described below.

[0653]

First, a glass substrate was prepared. After that, insulating films 601, 602, and 603 were formed over the glass substrate. Note that the insulating films 601, 602, and 603 correspond to a gate insulating film of the transistor.

[0654]

A silicon nitride film was formed as the insulating film 601. The silicon nitride film was formed to a thickness of 300 nm under the condition where the substrate temperature was 350 °C, silane, nitrogen, and ammonia were supplied at flow rates of 200 sccm, 2000 sccm, and 2000 sccm, respectively, as a source gas to a reaction chamber of a PE-CVD apparatus, the pressure in the reaction chamber was controlled to 100 Pa, and a power of 2000 W was supplied with a 27.12 MHz high-frequency power source.

[0655]

A silicon nitride film was formed as the insulating film 602. The silicon nitride film was formed to a thickness of 50 nm under the condition where the substrate temperature was 350 °C, silane and nitrogen were supplied at flow rates of 200 sccm and 5000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus, the pressure in the reaction chamber was controlled to 100 Pa, and a power of 2000 W was supplied with a 27.12 MHz high-frequency power source.

[0656]

A silicon oxynitride film was formed as the insulating film 603. The silicon oxynitride film was formed to a thickness of 50 nm under the condition where the substrate temperature was 350 °C, silane and dinitrogen monoxide were supplied at flow rates of 20 sccm and 3000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus, the pressure in the reaction chamber was controlled to 40 Pa, and a power of 100 W was supplied with a 27.12 MHz high-frequency power

source.

[0657]

Next, a conductive film 612 was formed over the insulating film 603. Note that the conductive film 612 had a three-layer structure of a conductive film 609, a conductive film 610, and a conductive film 611. A Cu-Mn alloy film was formed as the conductive film 609. The Cu-Mn alloy film was formed to a thickness of 30 nm under the condition where the substrate temperature was room temperature, an Ar gas was supplied to a treatment chamber at a flow rate of 100 sccm, the pressure in the treatment chamber was controlled to 0.4 Pa, and a power of 2000 W was supplied to a target with a direct-current (DC) power source. The composition of the target was Cu:Mn = 90:10 [at.%]. A Cu film was formed as the conductive film 610. The Cu film was formed to a thickness of 200 nm under the condition where the substrate temperature was 100 °C, an Ar gas was supplied to a treatment chamber at a flow rate of 75 sccm, the pressure in the treatment chamber was controlled to 1.0 Pa, and a power of 15 kW was supplied to a target using a DC power source. A Cu-Mn alloy film was formed as the conductive film 611. The Cu-Mn alloy film was formed to a thickness of 100 nm under the condition where the substrate temperature was room temperature, an Ar gas was supplied to the treatment chamber at a flow rate of 100 sccm, the pressure in the treatment chamber was controlled to 0.4 Pa, and a power of 2000 W was supplied to a target using a DC power source. The composition of the target was Cu:Mn = 90:10 [at.%]

[0658]

Next, a resist mask was formed over the conductive film 611, an etchant was applied over the resist mask, and wet etching was performed to collectively process the conductive films 609, 610, and 611. As the etchant, an etchant containing an organic acid solution and a hydrogen peroxide solution was used.

[0659]

Next, the resist mask was removed, and an insulating film 614 was formed to cover the insulating film 603 and the conductive film 612. Note that the insulating film 614 corresponds to an insulating film functioning as a protective insulating film of the transistor.

[0660]

The insulating film 614 had a stacked-layer structure of a first silicon oxynitride film and a second silicon oxynitride film. The first silicon oxynitride film was formed to a thickness of 40 nm under the condition where the substrate temperature was 220 °C, silane and dinitrogen monoxide were supplied at flow rates of 50 sccm and 2000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus, the pressure in the reaction chamber was controlled to 20 Pa, and a power of 100 W was supplied with a 13.56 MHz high-frequency power source. The second silicon oxynitride film was formed to a thickness of 400 nm under the condition where the substrate temperature was 220 °C, silane and dinitrogen monoxide were supplied at flow rates of 160 sccm and 4000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus, the pressure in the reaction chamber was controlled to 200 Pa, and a power of 1500 W was supplied with a 13.56 MHz high-frequency power source.

[0661]

Next, heat treatment was performed. The heat treatment was performed for one hour in a mixed gas atmosphere of nitrogen and oxygen at a substrate temperature of 350 °C.

[0662]

An insulating film 616 was formed over the insulating film 614. Note that the insulating film 616 corresponds to an insulating film functioning as a protective insulating film for the transistor.

[0663]

A silicon nitride film was formed as the insulating film 616. The silicon nitride film was formed to a thickness of 100 nm under the condition where the substrate temperature was 350 °C, silane, nitrogen, and an ammonia gas were supplied at flow rates of 50 sccm, 5000 sccm, and 100 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus, the pressure in the reaction chamber was controlled to 100 Pa, and a power of 1000 W was supplied with a 13.56 MHz high-frequency power source.

[0664]

Through the above process, the sample of this example was fabricated.

[0665]

FIG. 58 shows a result of a cross-sectional observation of the sample of this embodiment and FIG. 59 shows results of composition analysis of the conductive films.

- 5 Note that a scanning transmission electron microscope (STEM) was used for the cross-sectional observation, and energy dispersive X-ray spectrometry (EDX, hereinafter referred to as EDX analysis) was used for the composition analysis. Points A, B, C, D, and E denoted by white circles in FIG. 58 were subjected to EDX analysis. Point A indicates the vicinity of the interface between the conductive film 611 and the
10 insulating film 614, Point B indicates a portion in the conductive film 611, Point C indicates a portion in the conductive film 610, Point D indicates the vicinity of the interface between the conductive film 609 and the insulating film 603, and Point E indicates the vicinity of the interface between the conductive film 610 and the insulating film 614. Note that the horizontal axis represents measurement points, and the vertical
15 axis represents quantitative values (at.%) in the composition analysis in FIG. 59.

[0666]

The TEM image in FIG. 58 shows that the conductive film 612 of the sample formed in this example has a favorable cross section.

[0667]

- 20 According to the results of composition analysis in FIG. 59, Mn was detected in Points A, B, D, and E. Point A is positioned at the top surface of the conductive film 612, Point D is positioned at the bottom surface of the conductive film 612, and Point E is positioned at the side surface of the conductive film 612. Therefore, Mn is present so as to surround the conductive film 612 in the sample of this example.

25 [0668]

The structure described in this example can be combined as appropriate with any of the structures described in the embodiments or the other example.

[Example 2]

[0669]

- 30 In this example, a stacked-layer structure of an oxide semiconductor film, a conductive film, and an insulating film was subjected to composition analysis. Details of a sample formed in this example are described below using FIG. 60.

[0670]

First, a substrate 622 was prepared. A glass substrate was used as the substrate 622. After that, an oxide semiconductor film 628 was formed over the substrate 622. The oxide semiconductor film 628 was formed under the condition
5 where a metal oxide sputtering target having an atomic of In:Ga:Zn = 1:1:1 was used; oxygen and argon were each supplied at a flow rate of 100 sccm, as a sputtering gas into a treatment chamber of a sputtering apparatus; the pressure in the treatment chamber was controlled to 0.6 Pa; and a direct-current power of 2.5 kW was supplied. The substrate temperature during the formation of the oxide semiconductor film 628 was set
10 to 170 °C. The thickness of the oxide semiconductor film 628 was 100 nm.

[0671]

Next, first heat treatment was performed. As the first heat treatment, heat treatment at 450°C in a nitrogen atmosphere for one hour and heat treatment at 450 °C in a mixed gas atmosphere of nitrogen and oxygen for one hour were performed.

[0672]

Next, a conductive film 632 was formed over the oxide semiconductor film 628. As the conductive film 632, a Cu-Mn alloy film was formed by a sputtering method.

[0673]

The Cu-Mn alloy film was formed to a thickness of 200 nm under the condition
20 where the substrate temperature was room temperature, an Ar gas was supplied to a treatment chamber at a flow rate of 100 sccm, the pressure in the treatment chamber was controlled to 0.4 Pa, and a power of 2000 W was supplied to the target using a DC power source. The composition of the target was Cu:Mn = 90:10 [at.%].

[0674]

Next, an insulating film 638 was formed over the conductive film 632. As the insulating film 638, a stacked-layer film including the first silicon oxynitride film and the second silicon oxynitride film was formed. The first silicon oxynitride film was formed to a thickness of 50 nm under the condition where the substrate temperature was 220 °C, silane and dinitrogen monoxide were supplied at flow rates of 30 sccm and
30 4000 sccm, respectively, as a source gas to a reaction chamber of a PE-CVD apparatus; the pressure in the reaction chamber was controlled to 40 Pa, and a power of 150 W was

supplied using a 13.56 MHz high-frequency power source. The second silicon oxynitride film was formed to a thickness of 400 nm under the condition where the substrate temperature was 220 °C, silane and dinitrogen monoxide were supplied at flow rates of 160 sccm and 4000 sccm, respectively, as a source gas to the reaction chamber of the PE-CVD apparatus; the pressure in the reaction chamber was controlled to 200 Pa, and a power of 1500 W was supplied using a 13.56 MHz high-frequency power source.

[0675]

Next, second heat treatment was performed. The second heat treatment was performed at a substrate temperature of 350 °C for one hour in a mixed gas atmosphere of nitrogen and oxygen.

[0676]

Through the above steps, the sample of this example was fabricated.

[0677]

Next, the composition analysis of the stacked-layer film of the sample formed in the above manner was performed. The composition analysis was performed by X-ray photoelectron spectroscopy (XPS) to obtain the quantitative value of each of In atoms, Ga atoms, Zn atoms, O atoms, Cu atoms, Mn atoms, and Si atoms in the depth direction of the semiconductor film 628, the conductive film 632, and the insulating film 638.

[0678]

FIG. 61 shows analysis results of XPS. The XPS analysis was performed under the condition where sputtering was performed from the substrate 622 side, a monochromatic Al X-ray source (1486.6 eV) was used, and the diameter of a detected region was 100 μm. In FIG. 61, the horizontal axis represents the sputtering time (min), and the vertical axis represents the quantitative values (at.%).

[0679]

According to the results of FIG. 61, Mn is segregated in the vicinity of the interface between the oxide semiconductor film 628 and the conductive film 632 and in the vicinity of the interface between the insulating film 638 and the conductive film 632.

[0680]

Note that the structure described in this example can be combined as appropriate with any of the structures described in the embodiments or the other example.

5

REFERENCE NUMERALS

[0681]

101: coating film, 102: substrate, 103: conductive film, 103_1: conductive film, 103_2: conductive film, 103_3: conductive film, 104: conductive film, 104_1: conductive film, 104_2: conductive film, 104_3: conductive film, 106: insulating film, 106a: insulating film, 106b: insulating film, 108: oxide semiconductor film, 108a: metal oxide film, 108b: metal oxide film, 109: protective insulating film, 110: conductive film, 110a: conductive film, 110b: conductive film, 111: conductive film, 111_1: conductive film, 111_2: conductive film, 111_3: conductive film, 111a: conductive film, 111b: conductive film, 112: conductive film, 112a: electrode layer, 112a_1: conductive film, 112a_2: conductive film, 112a_3: conductive film, 112b: electrode layer, 112b_1: conductive film, 112b_2: conductive film, 112b_3: conductive film, 113a: coating film, 113b: coating film, 114: insulating film, 115a: coating film, 115b: coating film, 116: insulating film, 117a: conductive film, 117b: conductive film, 118: insulating film, 120: conductive film, 120a: conductive film, 120b: conductive film, 140a: opening, 140b: opening, 141: resist mask, 142: resist mask, 142a: opening, 142b: opening, 142c: opening, 143: resist mask, 144: resist mask, 145: resist mask, 145a: resist mask, 145b: resist mask, 146: resist mask, 147: resist mask, 150: transistor, 150A: transistor, 150B: transistor, 150C: transistor, 150D: transistor, 151: transistor, 151A: transistor, 151B: transistor, 152: transistor, 152A: transistor, 152B: transistor, 153: transistor, 154: transistor, 155: transistor, 156: transistor, 158: transistor, 160: transistor, 171: chemical solution, 172: chemical solution, 173: chemical solution, 174: chemical solution, 300: display device, 300A: display device, 301: substrate, 302: pixel portion, 304: source driver circuit portion, 305: substrate, 306: gate driver circuit portion, 308: FPC terminal portion, 308, 310: signal line, 311: lead wiring portion, 312: sealant, 316: FPC, 350: transistor, 352: transistor, 360: connection electrode, 364: insulating film, 366:

insulating film, 368: insulating film, 370: planarization insulating film, 372: conductive film, 373: conductive film, 374: conductive film, 375: liquid crystal element, 376: liquid crystal layer, 377: conductive film, 378: spacer, 380: anisotropic conductive film, 388: insulating film, 390: capacitor, 400: display device, 401: substrate, 402: pixel portion, 5 405: substrate, 408: FPC, 410: element layer, 411: element layer, 412: adhesive layer, 414: substrate, 416: substrate, 418: adhesive layer, 420: insulating film, 430: insulating film, 432: sealing layer, 434: insulating film, 436: coloring layer, 438: light-blocking layer, 440: insulating film, 444: conductive film, 446: EL layer, 448: conductive film, 462: substrate, 463: separation layer, 464: adhesive for separation, 466: temporary supporting substrate, 468: laser light, 480: light-emitting element, 501: pixel circuit, 10 502: pixel portion, 504: driver circuit portion, 504a: gate driver, 504b: source driver, 506: protection circuit, 507: terminal portion, 550: transistor, 552: transistor, 554: transistor, 560: capacitor, 562: capacitor, 570: liquid crystal element, 572: light-emitting element, 601: insulating film, 602: insulating film, 603: insulating film, 609: conductive film, 15 610: conductive film, 611: conductive film, 612: conductive film, 614: insulating film, 616: insulating film, 622: substrate, 628: oxide semiconductor film, 632: conductive film, 638: insulating film, 5000: housing, 5001: display portion, 5002: display portion, 5003: speaker, 5004: LED lamp, 5005: operation key, 5006: connection terminal, 5007: sensor, 5008: microphone, 5009: switch, 5010: infrared port, 5011: memory medium reading portion, 5012: support, 5013: earphone, 5014: antenna, 5015: shutter button, 5016: image receiving portion, 5017: charger, 5100: pellet, 5100a: pellet, 5100b: pellet, 5101: ion, 5102: zinc oxide layer, 5103: particle, 5105a: pellet, 5105a1: region, 5105a2: pellet, 5105b: pellet, 5105c: pellet, 5105d: pellet, 5105d1: region, 5105e: pellet, 5120: substrate, 5130: target, 5161: region, 8000: display module, 8001: 25 upper cover, 8002: lower cover, 8003: FPC, 8004: touch panel, 8005: FPC, 8006: display panel, 8007: backlight, 8008: light source, 8009: frame, 8010: printed board, 8011: battery.

This application is based on Japanese Patent Application serial no. 30 2013-247402 filed with Japan Patent Office on November 29, 2013, and Japanese Patent Application serial no. 2013-247404 filed with Japan Patent Office on November 29, 2013, the entire contents of which are hereby incorporated by reference.

CLAIMS

1. A semiconductor device comprising a transistor, the transistor comprising:
a first gate electrode;
5 a first gate insulating film over the first gate electrode;
an oxide semiconductor film over the first gate insulating film, the oxide semiconductor film overlapping the first gate electrode;
a pair of electrodes electrically connected to the oxide semiconductor film;
a second gate insulating film over the oxide semiconductor film and the pair of
10 electrodes; and
a second gate electrode over the second gate insulating film, the second gate electrode overlapping the oxide semiconductor film,
wherein the pair of electrodes comprises a Cu-*X* alloy film, where *X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti.
- 15 2. The semiconductor device according to claim 1, further comprising an insulating film between the oxide semiconductor film and the pair of electrodes,
wherein the pair of electrodes is electrically connected to the oxide semiconductor film through the insulating film.
- 20 3. The semiconductor device according to claim 1, wherein in a channel width direction of the transistor, the first gate electrode and the second gate electrode are connected through an opening provided in the first gate insulating film and the second gate insulating film, and surround the oxide semiconductor film with the first gate
25 insulating film and the second gate insulating film provided between the oxide semiconductor film and each of the first gate electrode and the second gate electrode.
4. The semiconductor device according to claim 1, wherein the pair of electrodes comprises a Cu-Mn alloy film an Mn oxide.
- 30 5. The semiconductor device according to claim 1, wherein the pair of electrodes comprises a Cu-Mn alloy film and a Cu film over the Cu-Mn alloy film.

6. The semiconductor device according to claim 1, wherein at least one of top surfaces, bottom surfaces, and side surfaces of the pair of electrodes is covered with an Mn oxide.

5

7. The semiconductor device according to claim 1, wherein top surfaces, bottom surfaces, and side surfaces of the pair of electrodes are covered with an Mn oxide.

10

8. The semiconductor device according to claim 1, wherein the oxide semiconductor film is an In-*M*-Zn oxide, where *M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf.

15

9. The semiconductor device according to claim 1,
wherein the oxide semiconductor film comprises a crystal part, and
wherein a c-axis of the crystal part is aligned parallel to a normal vector of a surface where the oxide semiconductor film is formed.

20 1.

10. A display device comprising the semiconductor device according to claim

25

11. A semiconductor device comprising a transistor, the transistor comprising:
a first gate electrode;
a first gate insulating film over the first gate electrode;
an oxide semiconductor film over the first gate insulating film, the oxide semiconductor film overlapping the first gate electrode;
a metal oxide film over the oxide semiconductor film;
a pair of electrodes electrically connected to the metal oxide film;
a second gate insulating film over the metal oxide film and the pair of
electrodes; and

30

a second gate electrode over the second gate insulating film, the second gate electrode overlapping the oxide semiconductor film,

wherein the pair of electrodes comprises a Cu-*X* alloy film, where *X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti.

12. The semiconductor device according to claim 11, further comprising an
5 insulating film between the metal oxide film and the pair of electrodes,

wherein the pair of electrodes is electrically connected to the oxide semiconductor film through the insulating film and the metal oxide film.

13. The semiconductor device according to claim 11, wherein in a channel
10 width direction of the transistor, the first gate electrode and the second gate electrode are connected through an opening provided in the first gate insulating film and the second gate insulating film, and surround the oxide semiconductor film with the first gate insulating film and the second gate insulating film provided between the oxide semiconductor film and each of the first gate electrode and the second gate electrode.

15

14. The semiconductor device according to claim 11, wherein the pair of electrodes comprises a Cu-Mn alloy film and an Mn oxide.

15. The semiconductor device according to claim 11, wherein the pair of
20 electrodes comprises a Cu-Mn alloy film and a Cu film over the Cu-Mn alloy film.

16. The semiconductor device according to claim 11, wherein at least one of top surfaces, bottom surfaces, and side surfaces of the pair of electrodes is covered with an Mn oxide.

25

17. The semiconductor device according to claim 11, wherein top surfaces, bottom surfaces, and side surfaces of the pair of electrodes are covered with an Mn oxide.

18. The semiconductor device according to claim 11, wherein the oxide semiconductor film is an In-*M*-Zn oxide, where *M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf.

30

19. The semiconductor device according to claim 11, wherein the metal oxide film is an In-*M*-Zn oxide, where *M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf.

5 20. The semiconductor device according to claim 11,
 wherein the oxide semiconductor film comprises a crystal part, and
 wherein a c-axis of the crystal part is aligned parallel to a normal vector of a
surface where the oxide semiconductor film is formed.

10 21. The semiconductor device according to claim 11,
 wherein the metal oxide film comprises a crystal part, and
 wherein a c-axis of the crystal part is aligned parallel to a normal vector of a
surface where the metal oxide film is formed.

15 22. A display device comprising the semiconductor device according to claim
11.

 23. A method for manufacturing a semiconductor device, comprising the steps
of:

20 forming a first conductive film over a substrate;
 processing the first conductive film using a first chemical solution to form a
gate electrode;

 forming a first insulating film over the gate electrode;
 forming an oxide semiconductor film over the first insulating film;
25 processing the oxide semiconductor film using a second chemical solution to
form an island-shaped oxide semiconductor film;

 forming a second conductive film over the first insulating film and the
island-shaped oxide semiconductor film;

 processing the second conductive film using a third chemical solution to form a
30 source electrode and a drain electrode;

 forming a second insulating film over the island-shaped oxide semiconductor
film, the source electrode, and the drain electrode;

processing the second insulating film to form a first opening reaching the drain electrode;

forming a third conductive film over the second insulating film to cover the first opening; and

5 processing the third conductive film using a fourth chemical solution to form a pixel electrode,

wherein the first chemical solution and the third chemical solution comprises a same chemical solution, and

10 wherein the second chemical solution and the fourth chemical solution comprises a same chemical solution.

24. The method for manufacturing the semiconductor device, according to claim 23, after forming the first opening, further comprising the step of processing the first insulating film and the second insulating film to form a second opening reaching
15 the gate electrode.

25. The method for manufacturing the semiconductor device, according to claim 23, wherein the oxide semiconductor film is an In-*M*-Zn oxide, where *M* is Ti, Ga, Y, Zr, La, Ce, Nd, Sn, or Hf.

20

26. The method for manufacturing the semiconductor device, according to claim 23,

wherein the oxide semiconductor film comprises a crystal part, and

25 wherein a c-axis of the crystal part is aligned parallel to a normal vector of a surface where the oxide semiconductor film is formed.

27. The method for manufacturing the semiconductor device, according to claim 23,

30 wherein one or both of the first conductive film and the second conductive film comprise a Cu-*X* alloy film, where *X* is Mn, Ni, Cr, Fe, Co, Mo, Ta, or Ti, and

wherein one or both of the first conductive film and the second conductive film comprise an Mn oxide.

28. The method for manufacturing the semiconductor device, according to claim 23, wherein each of the first chemical solution and the third chemical solution contains an organic acid solution and a hydrogen peroxide solution.

5

29. The method for manufacturing the semiconductor device, according to claim 23, wherein each of the second chemical solution and the fourth chemical solution contains oxalic acid.

10

30. The method for manufacturing the semiconductor device, according to claim 23,

wherein the second insulating film is processed using a fifth chemical solution, and

wherein the fifth chemical solution contains one or both of ammonium hydrogen fluoride and ammonium fluoride.

15

31. The method for manufacturing the semiconductor device, according to claim 23, wherein the oxide semiconductor film is a stacked-layer oxide film.

FIG. 1A

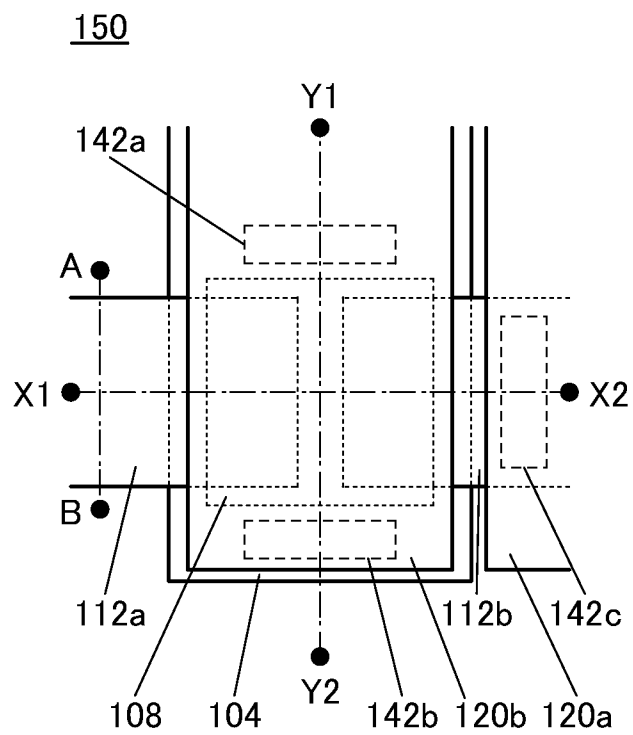


FIG. 1B

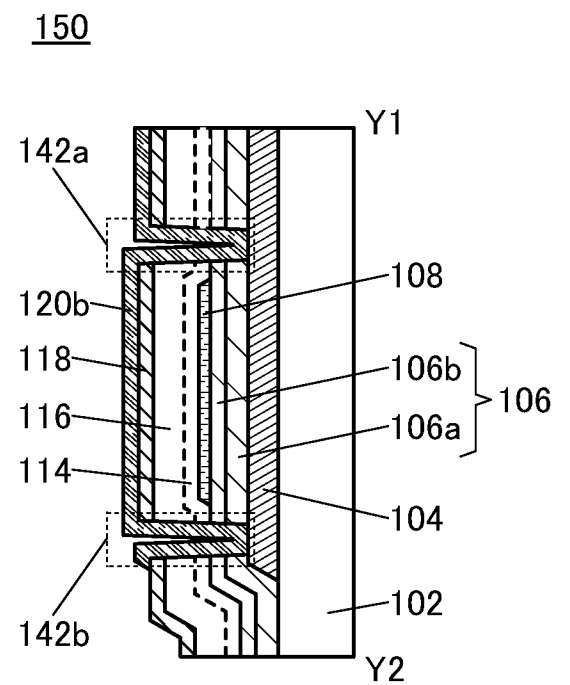


FIG. 1C

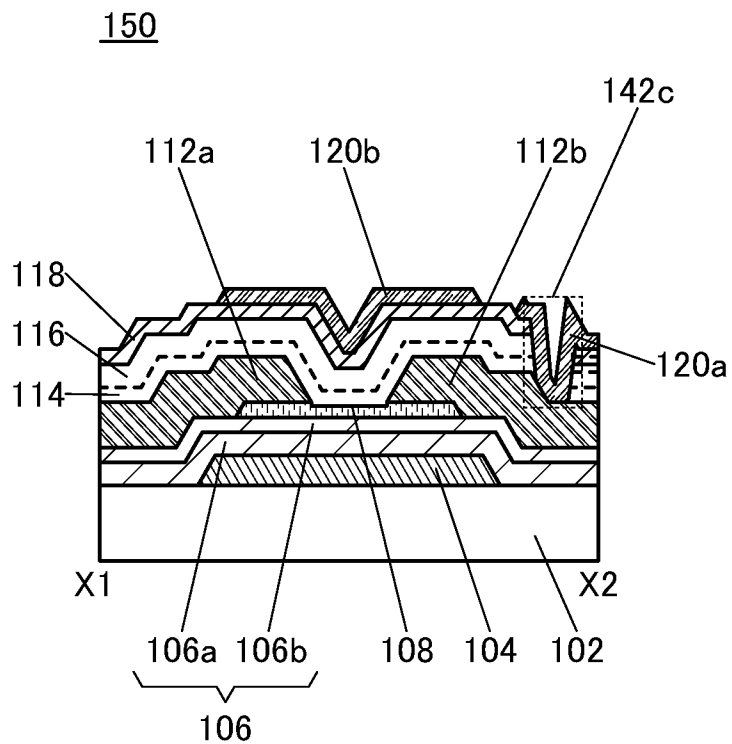


FIG. 2A

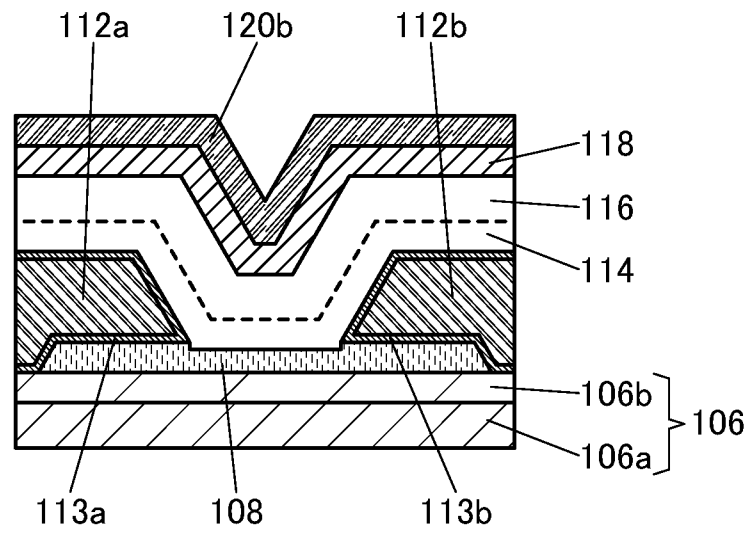


FIG. 2B

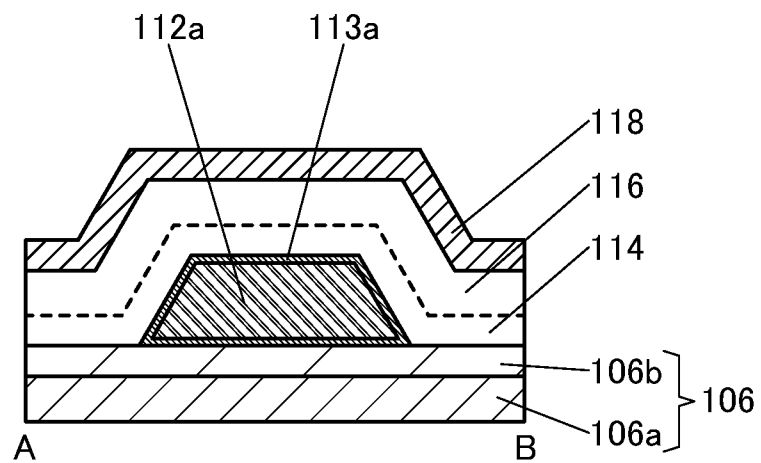


FIG. 3A

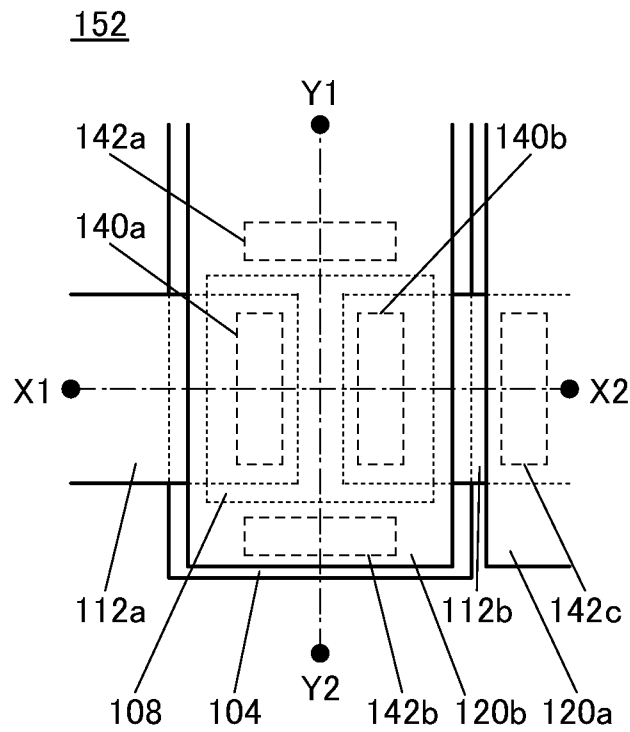


FIG. 3B

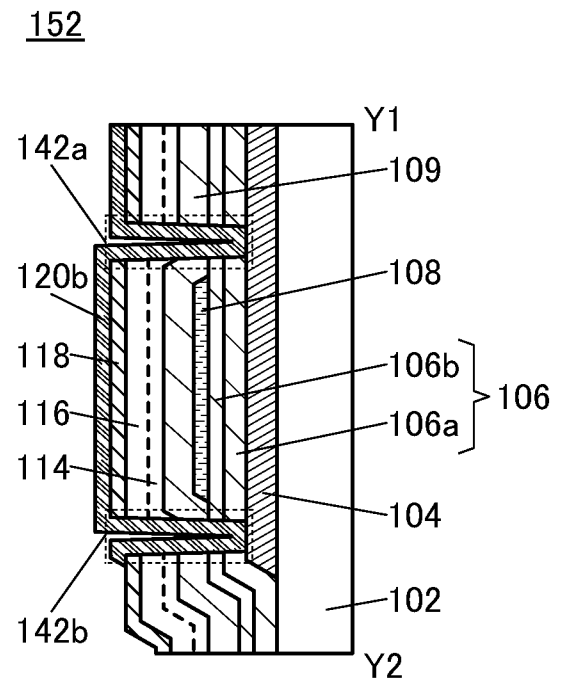


FIG. 3C

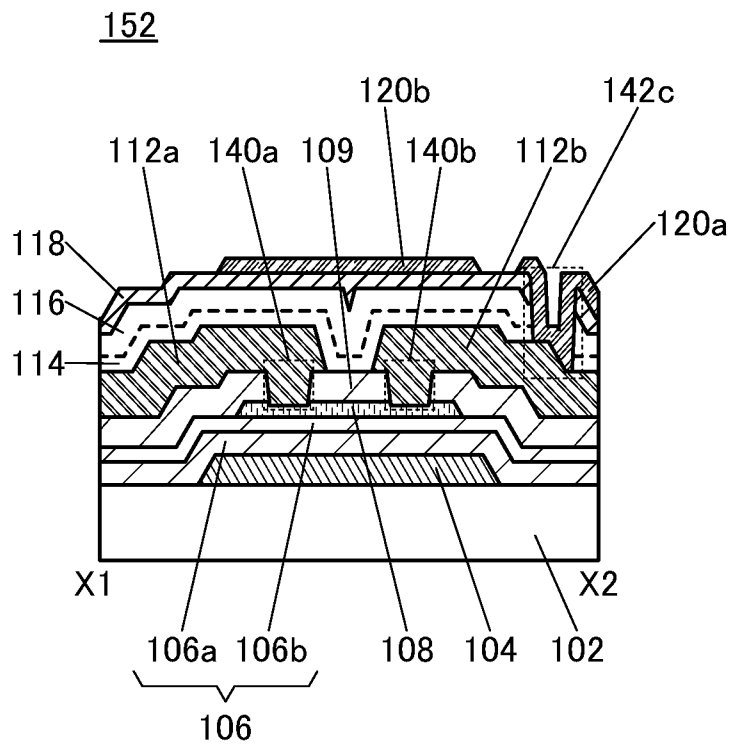


FIG. 4

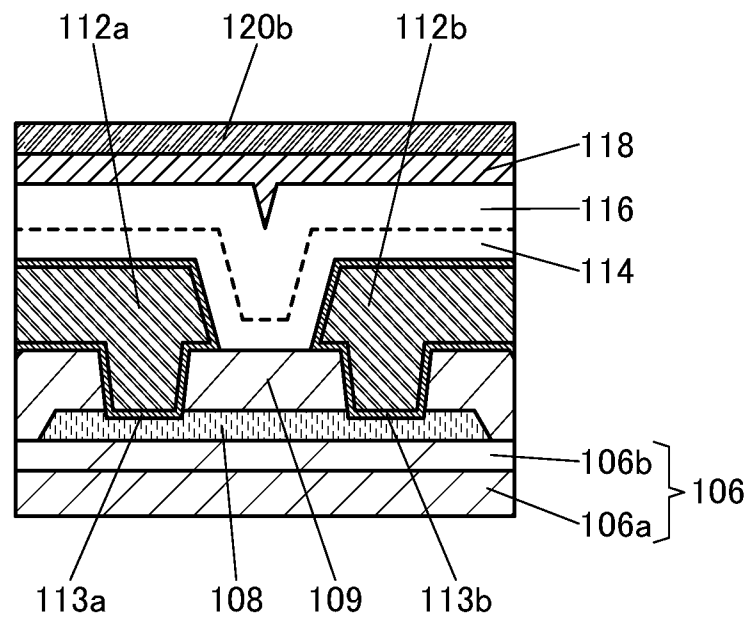


FIG. 5A

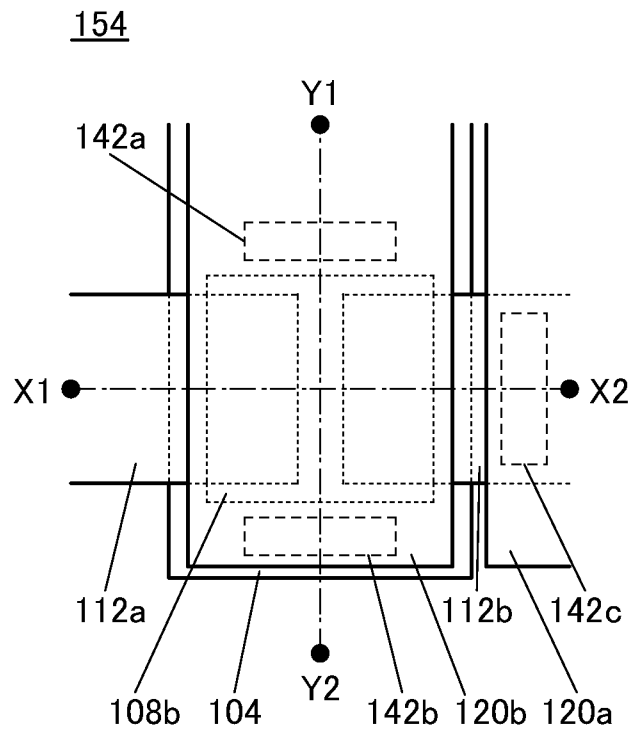


FIG. 5B

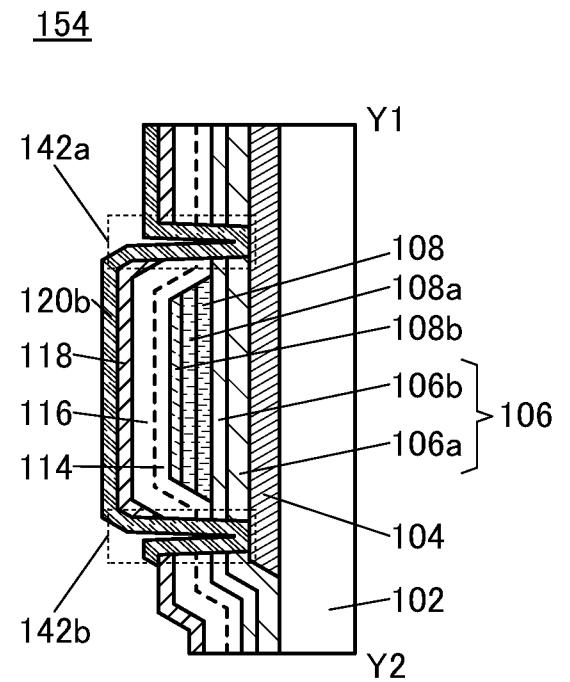


FIG. 5C

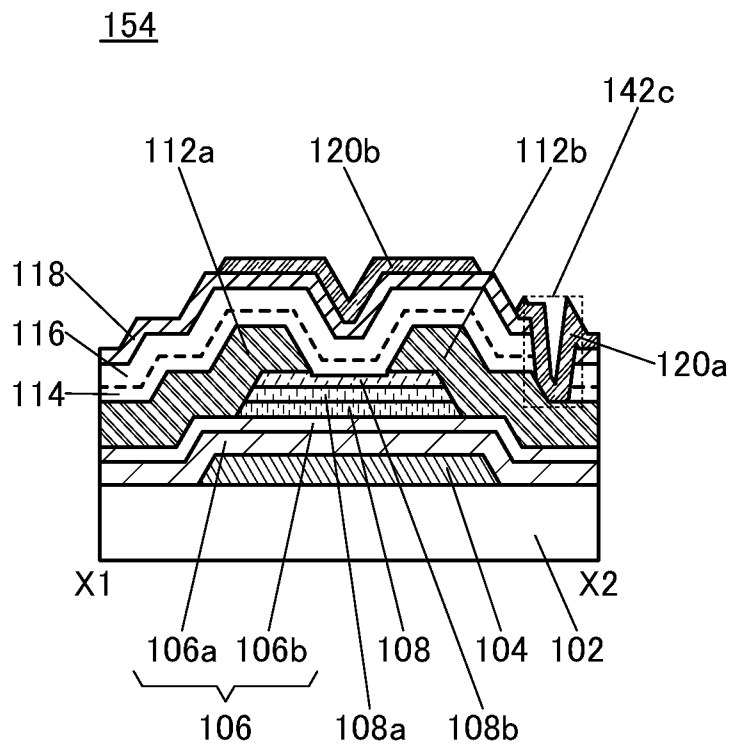


FIG. 6A

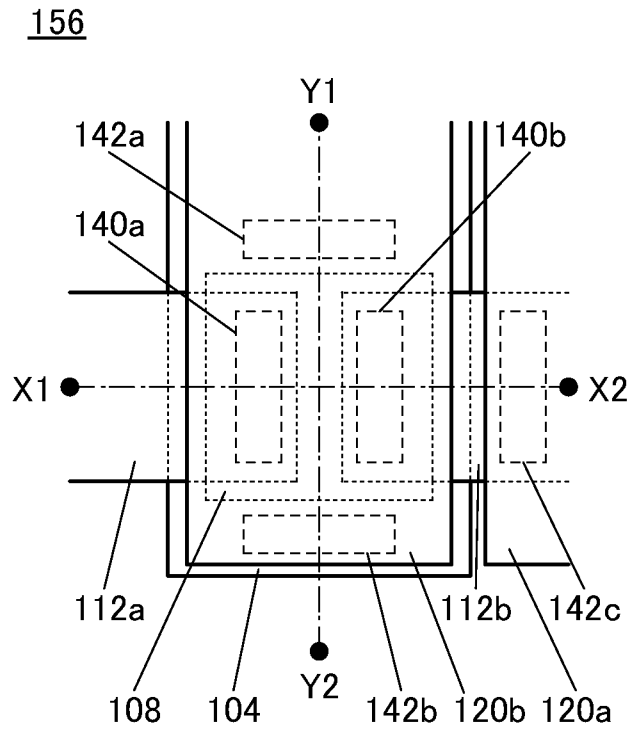


FIG. 6B

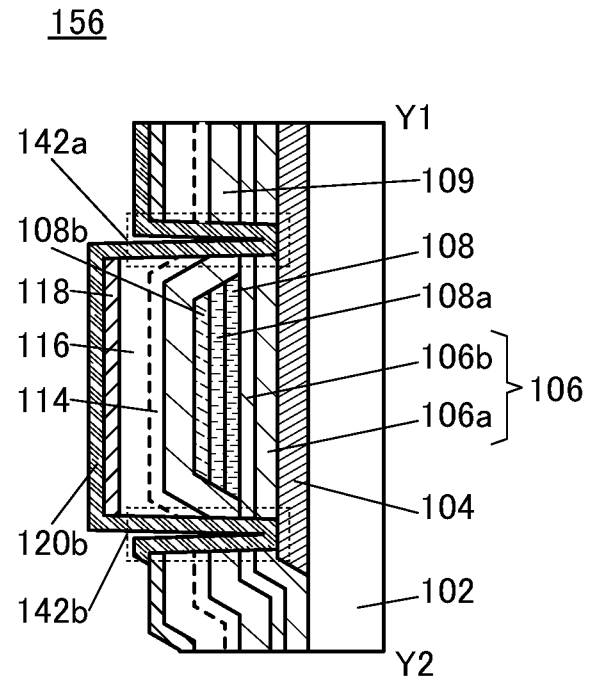


FIG. 6C

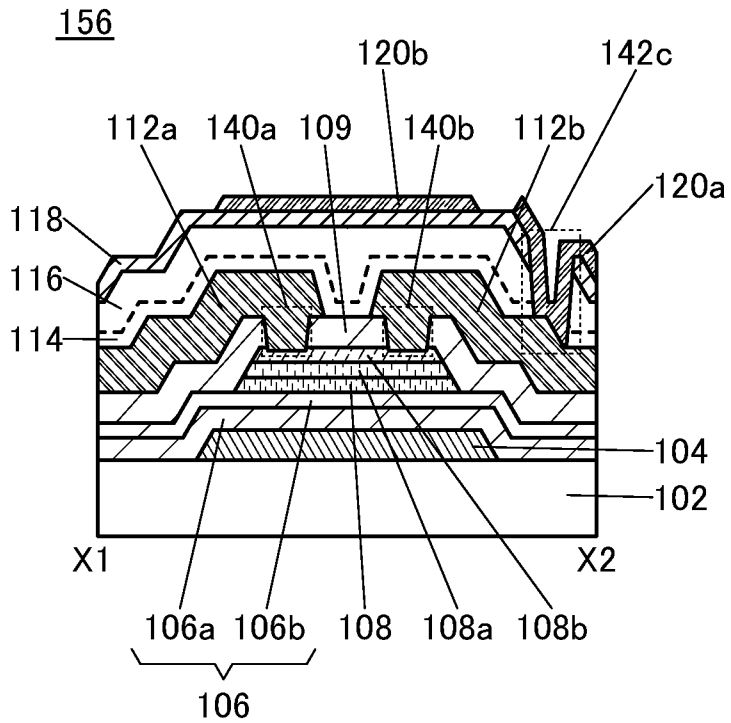


FIG. 7A

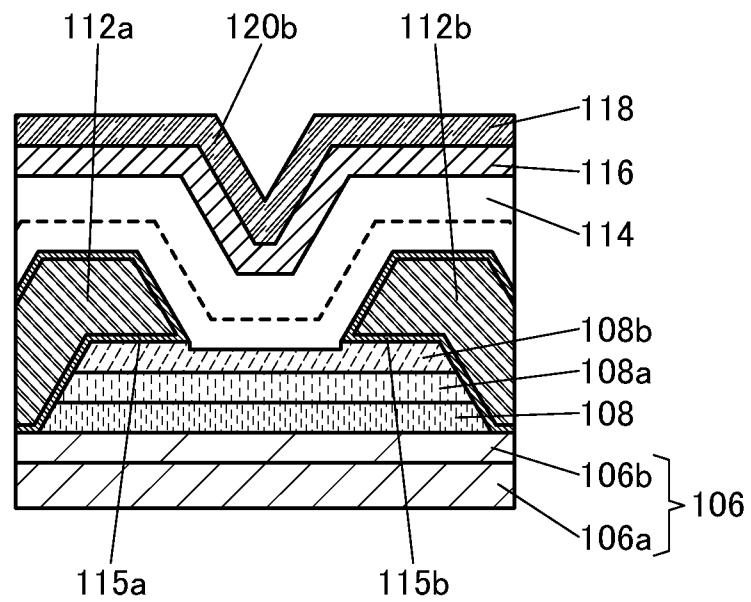


FIG. 7B

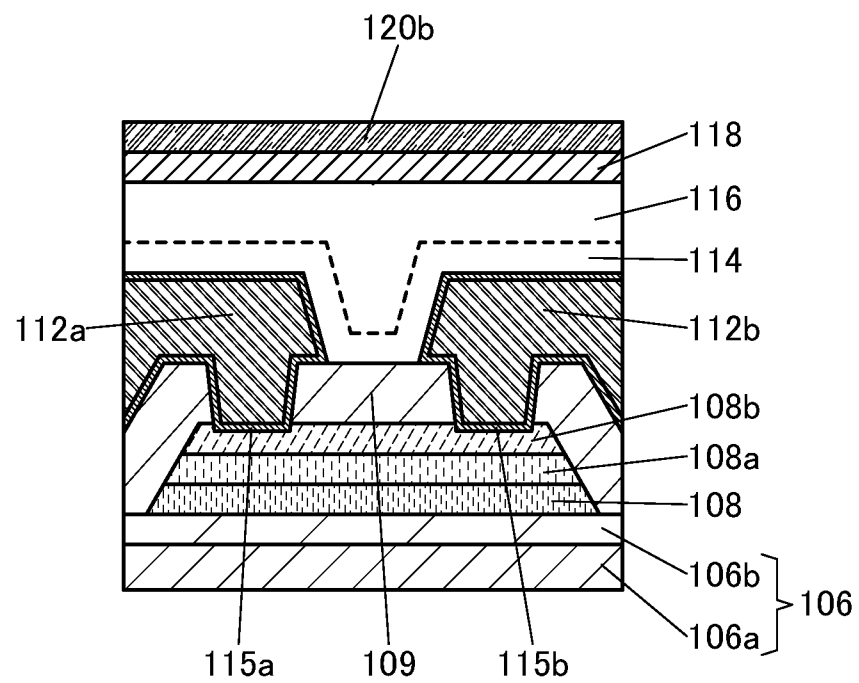


FIG. 8A

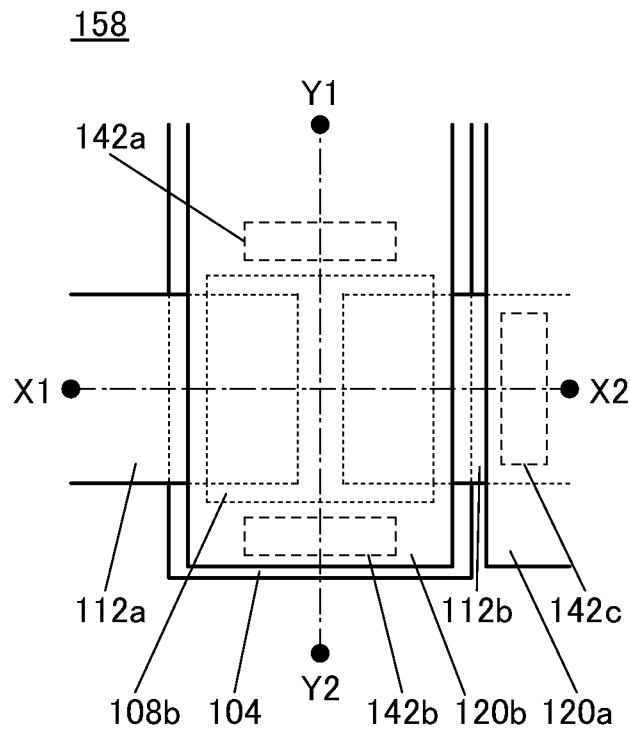


FIG. 8B

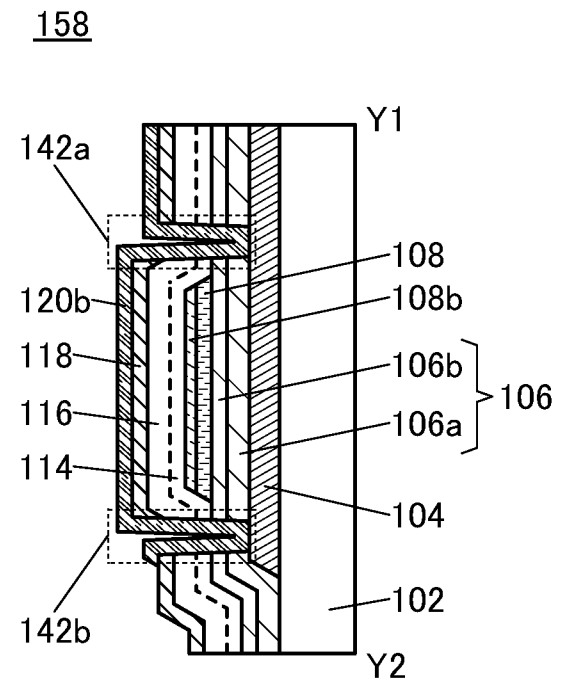


FIG. 8C

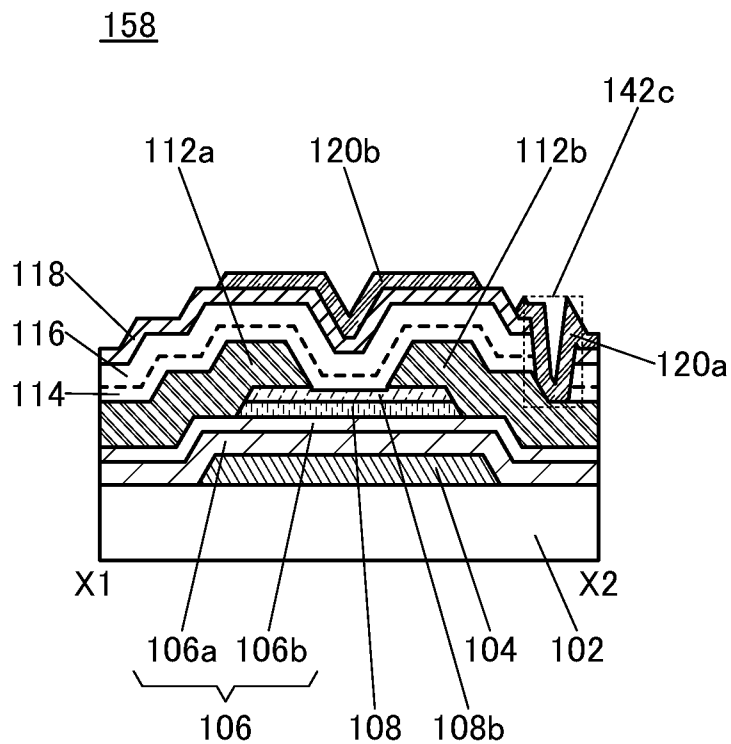


FIG. 9A

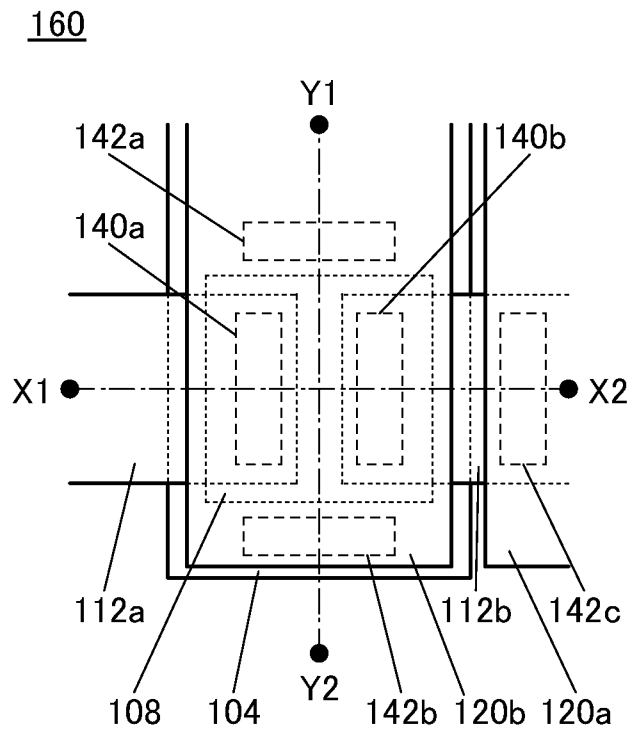


FIG. 9B

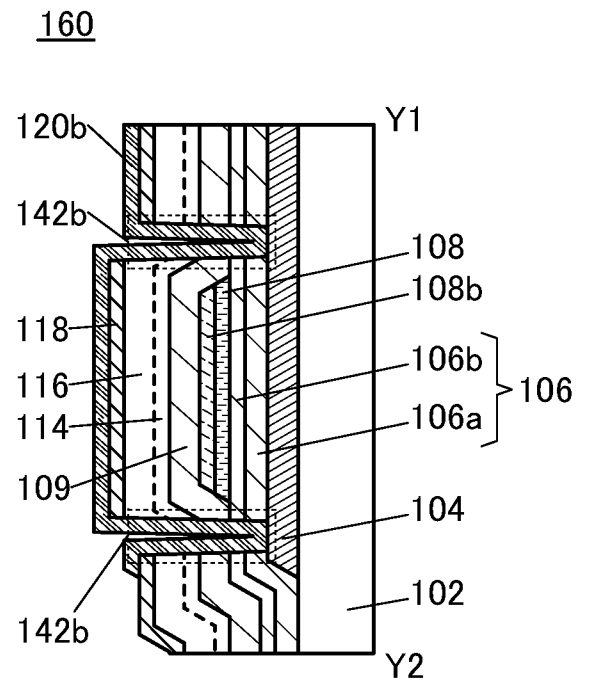


FIG. 9C

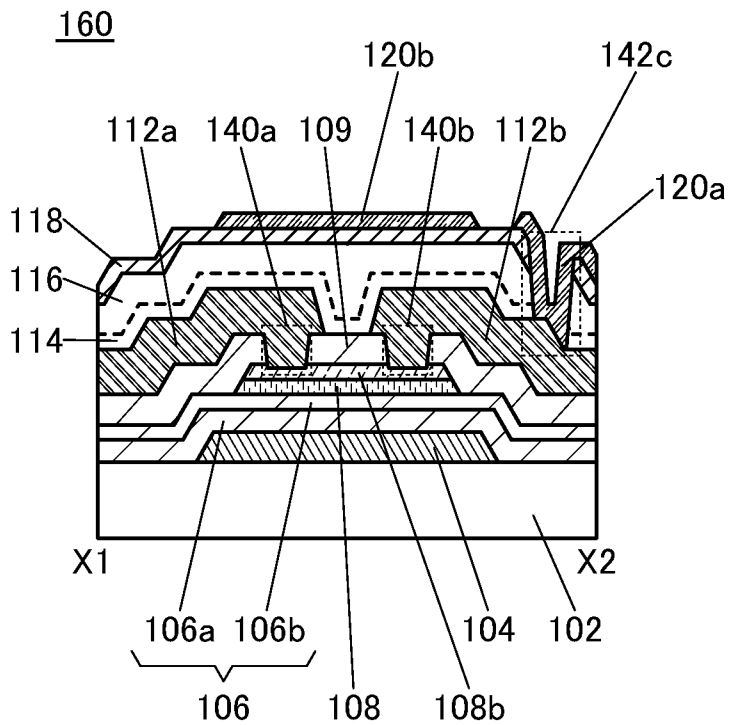


FIG. 10A

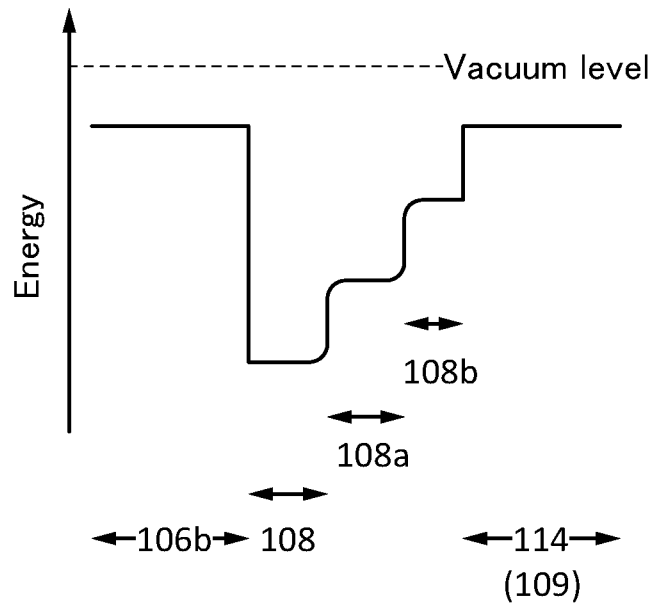


FIG. 10B

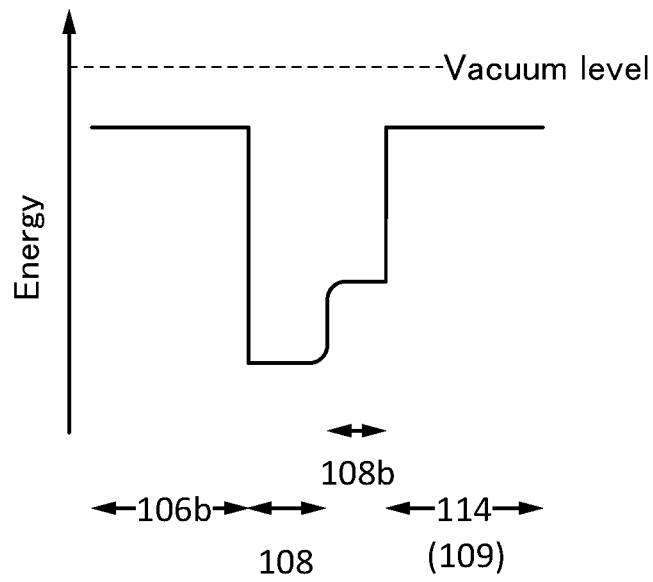


FIG. 12A

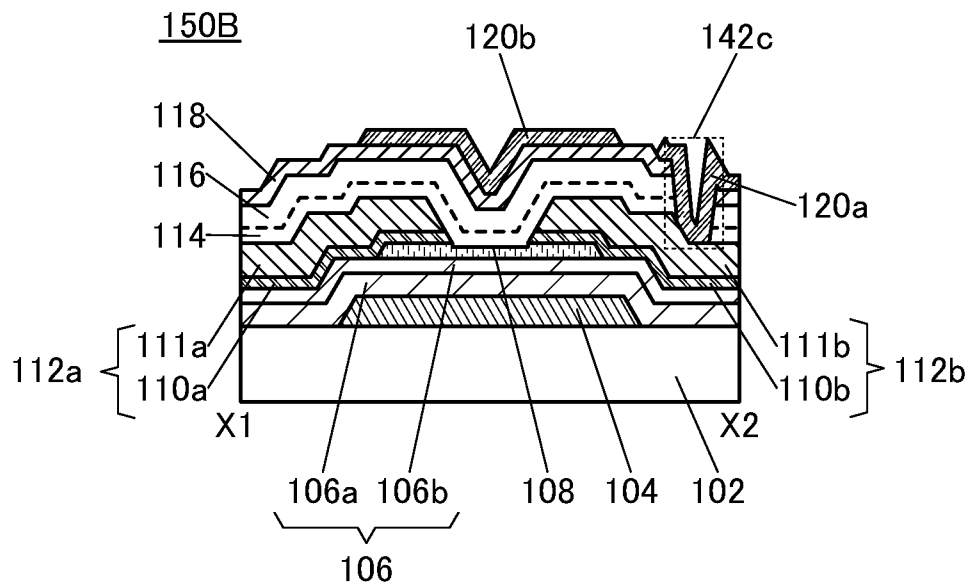


FIG. 12B

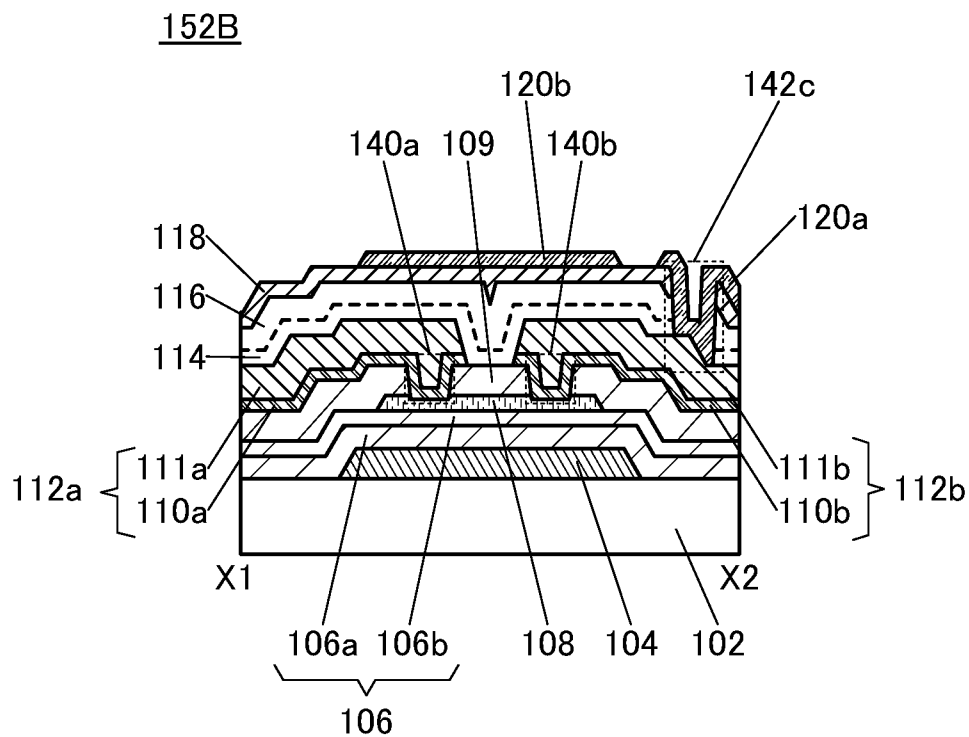


FIG. 13A

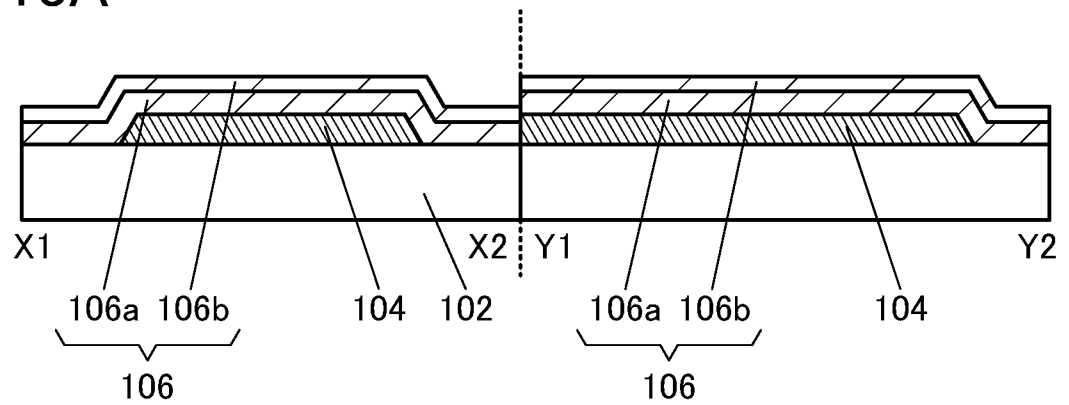


FIG. 13B

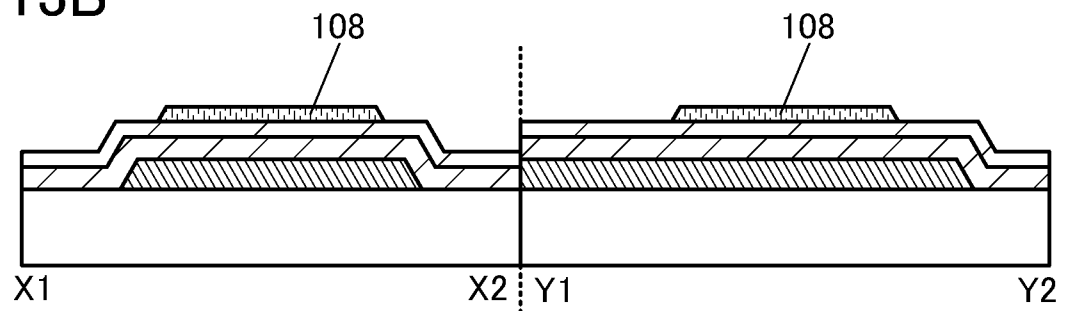


FIG. 13C

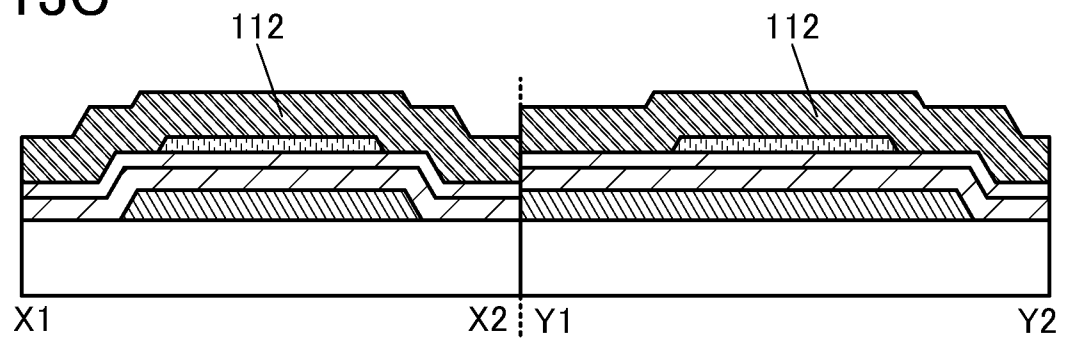


FIG. 13D

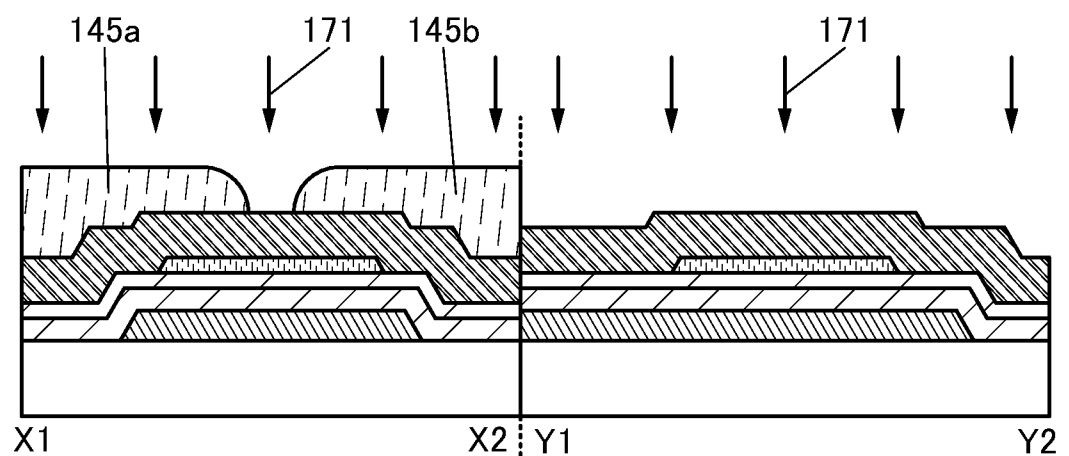


FIG. 14A

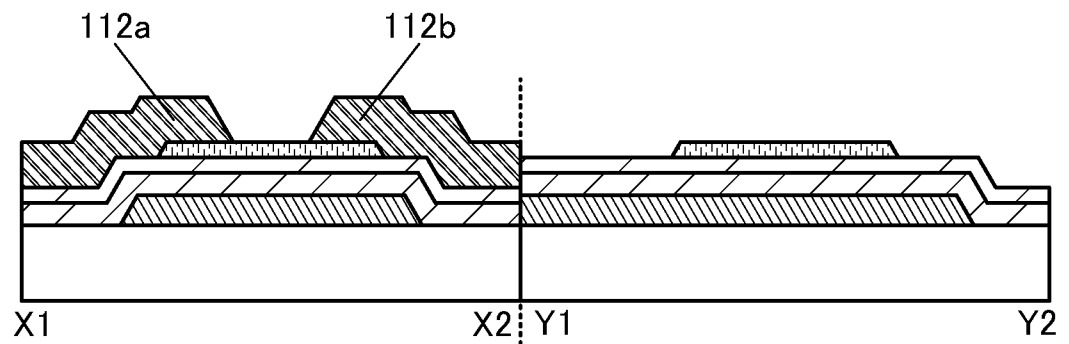


FIG. 14B

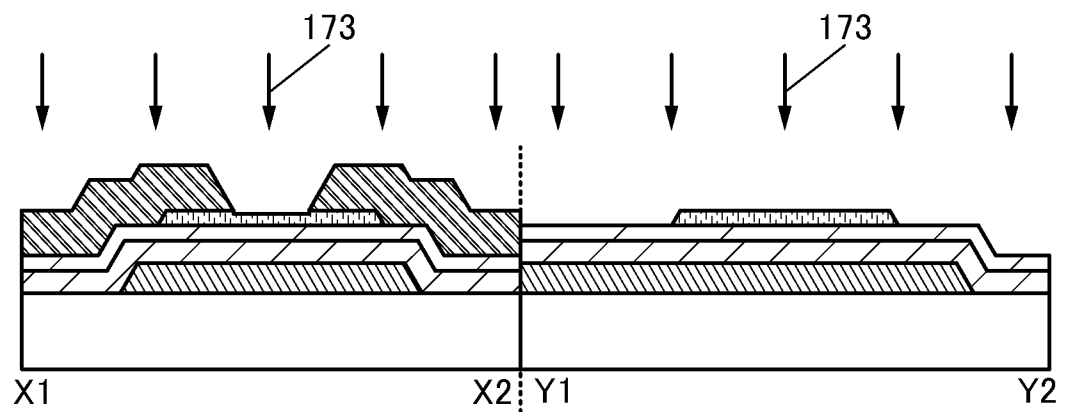


FIG. 14C

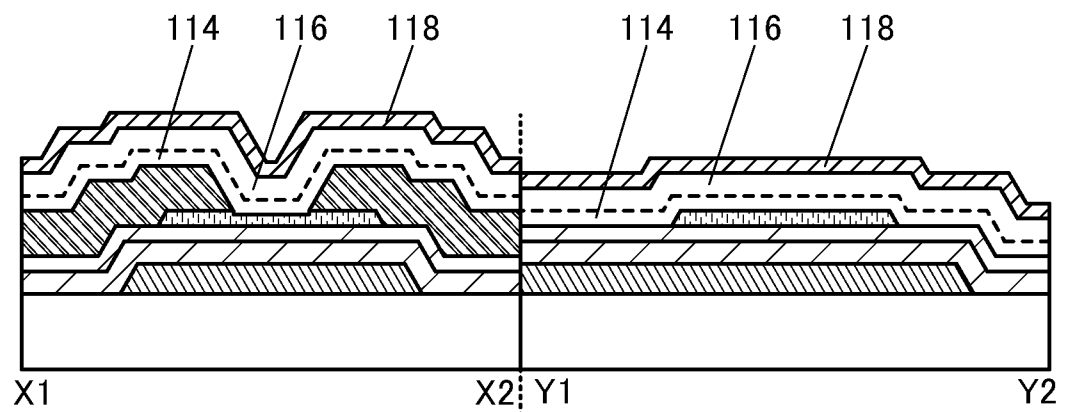


FIG. 15A

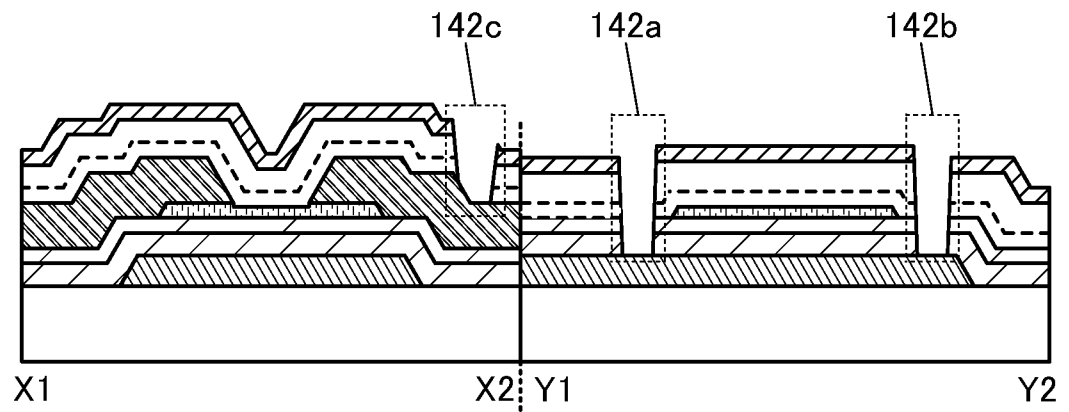


FIG. 15B

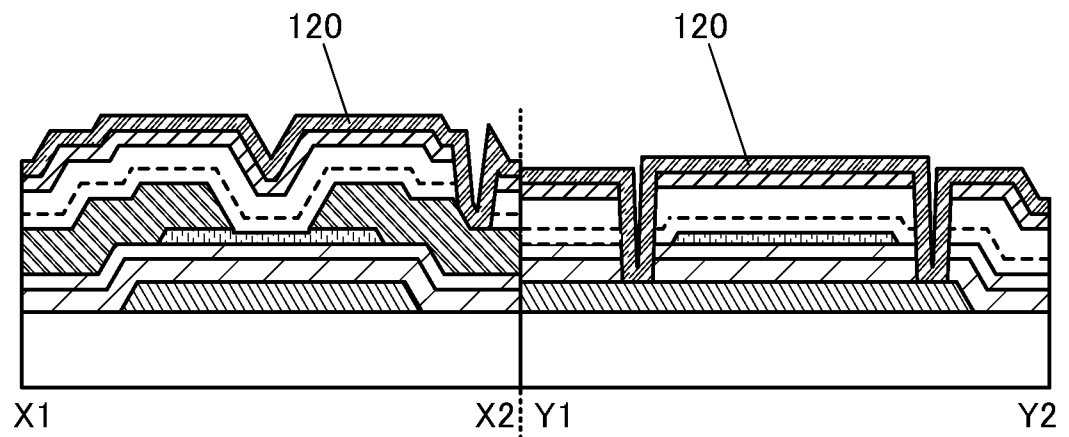


FIG. 15C

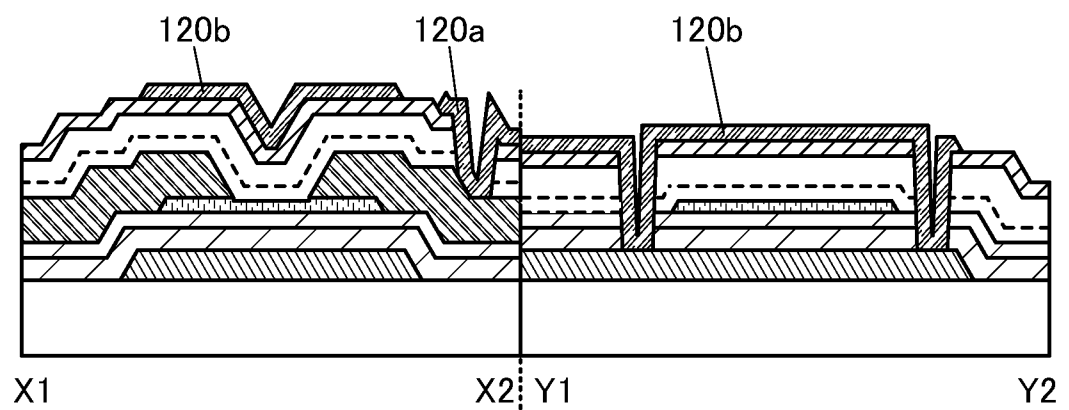


FIG. 16A

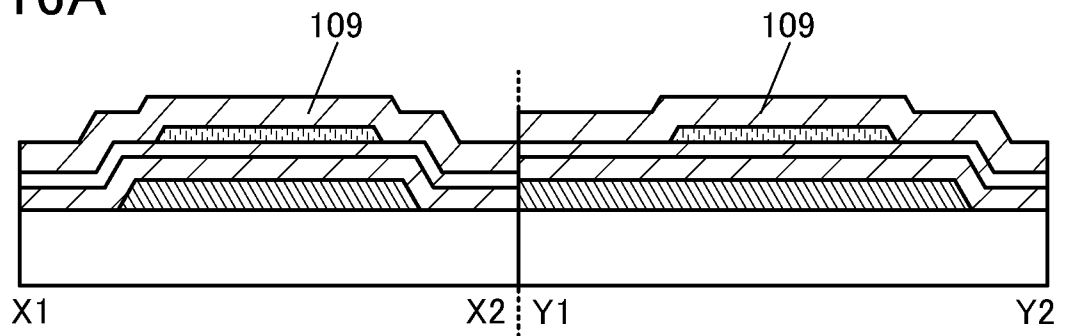


FIG. 16B

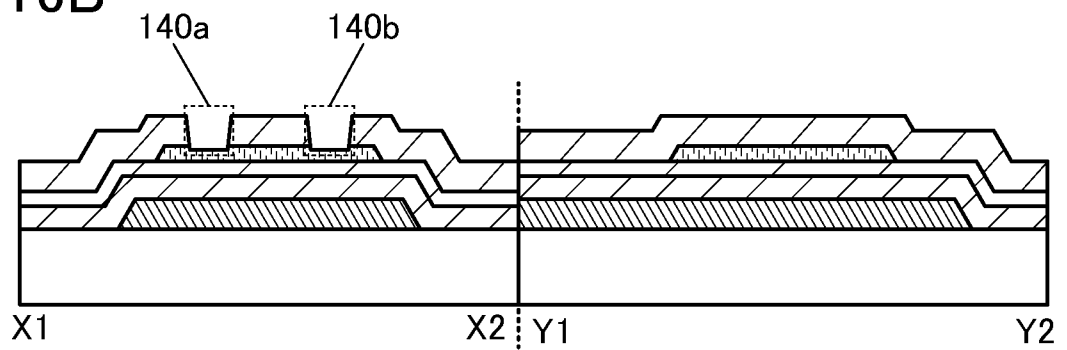


FIG. 16C

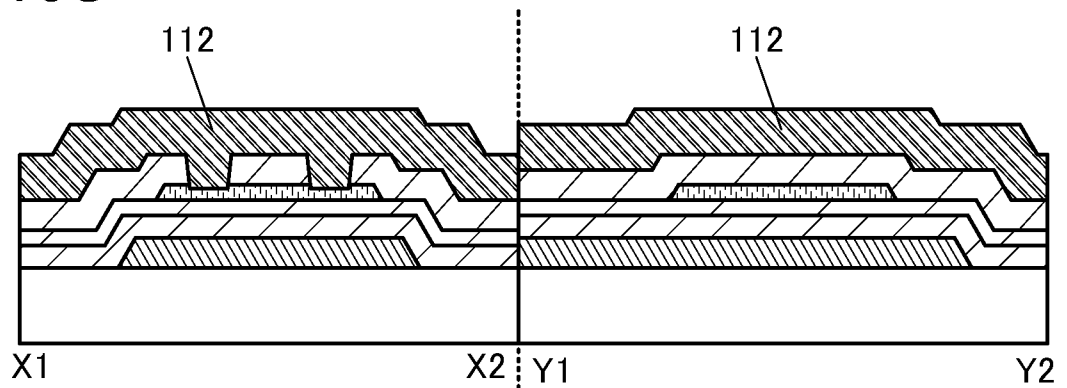


FIG. 16D

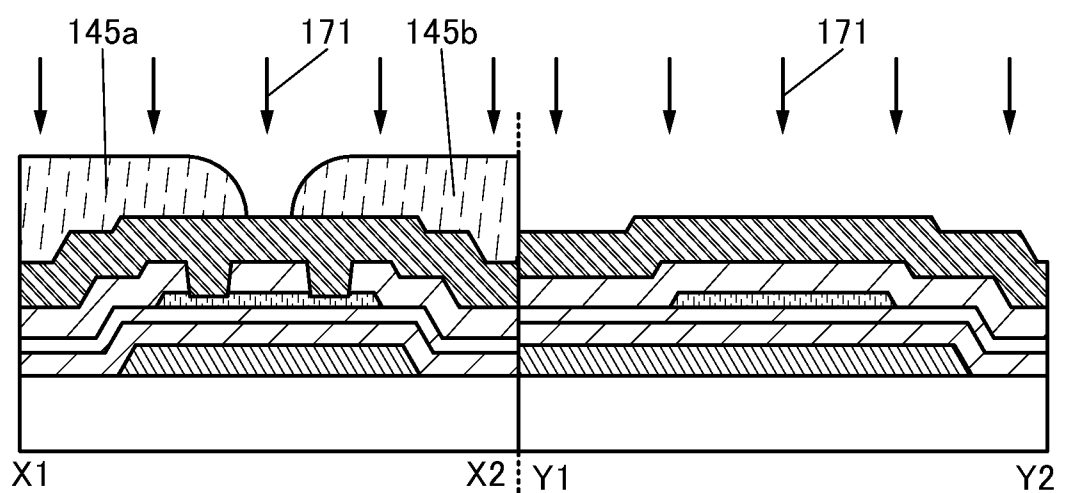


FIG. 17A

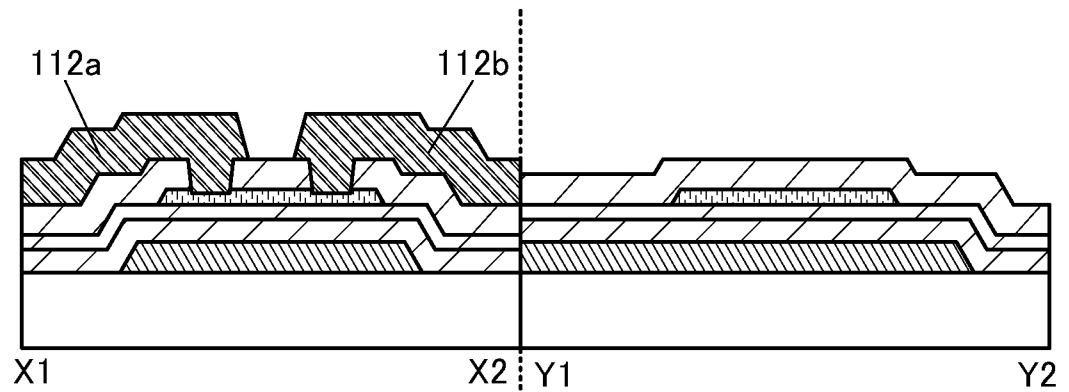


FIG. 17B

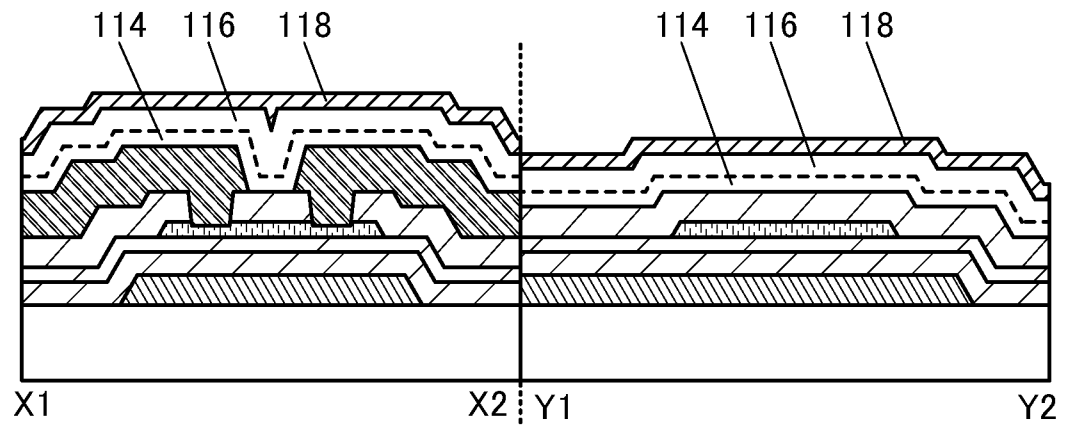


FIG. 17C

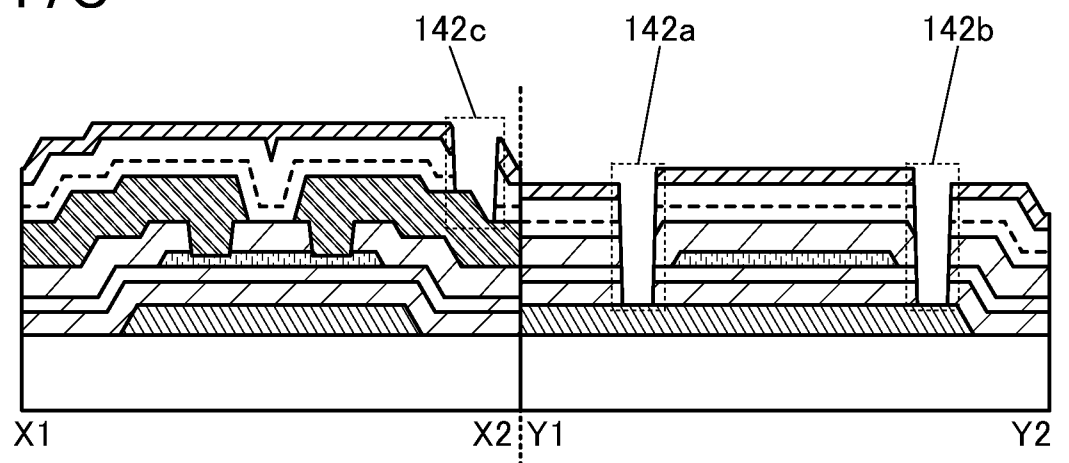


FIG. 18A

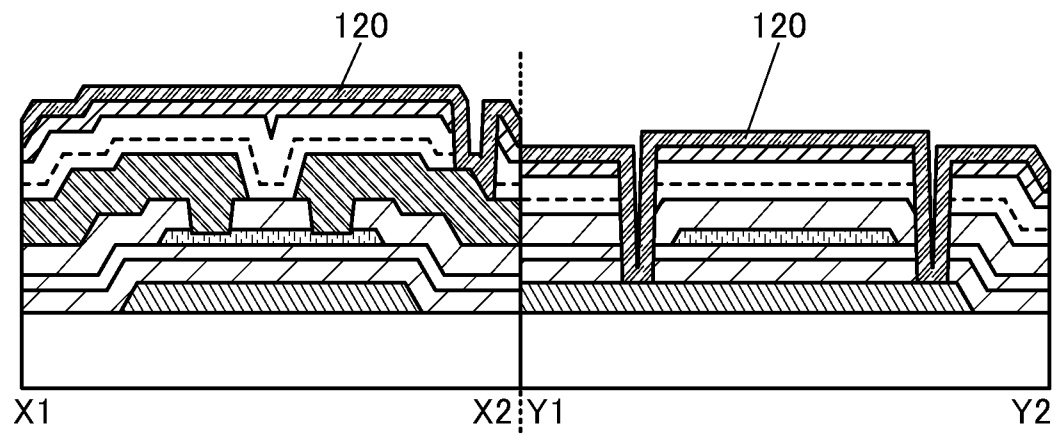


FIG. 18B

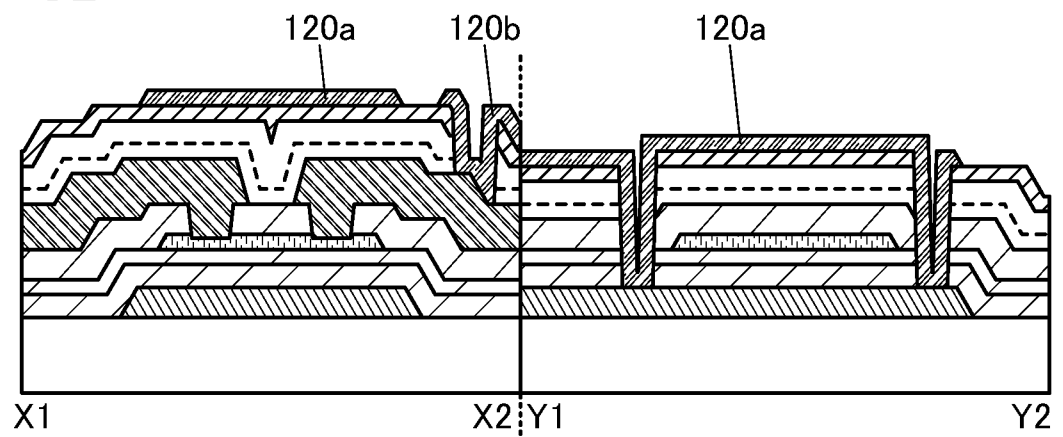


FIG. 19A

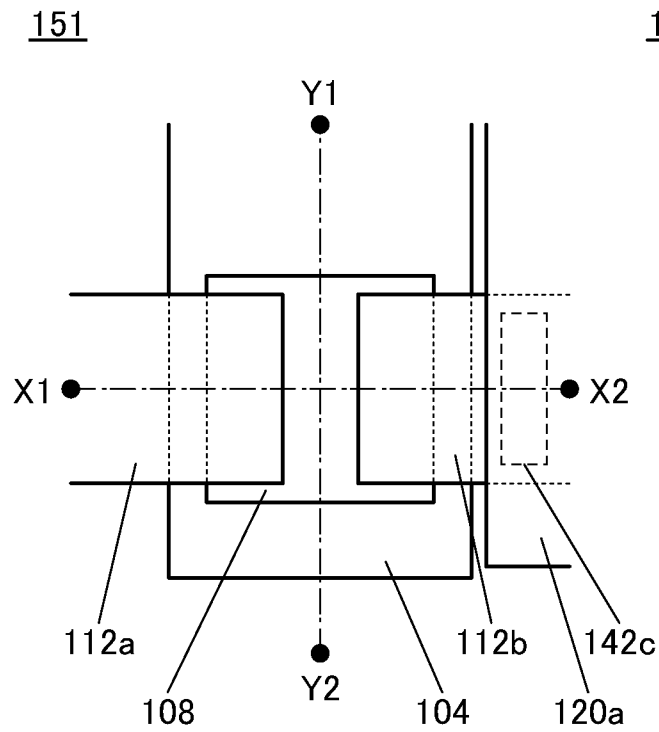


FIG. 19B

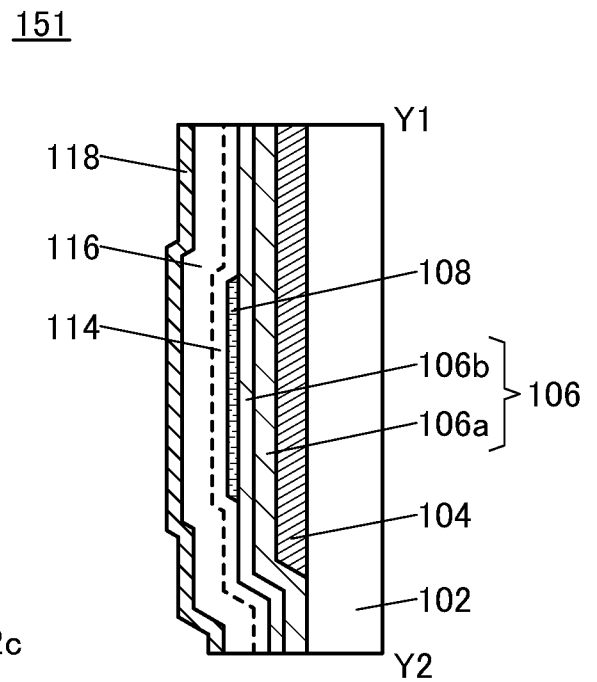


FIG. 19C

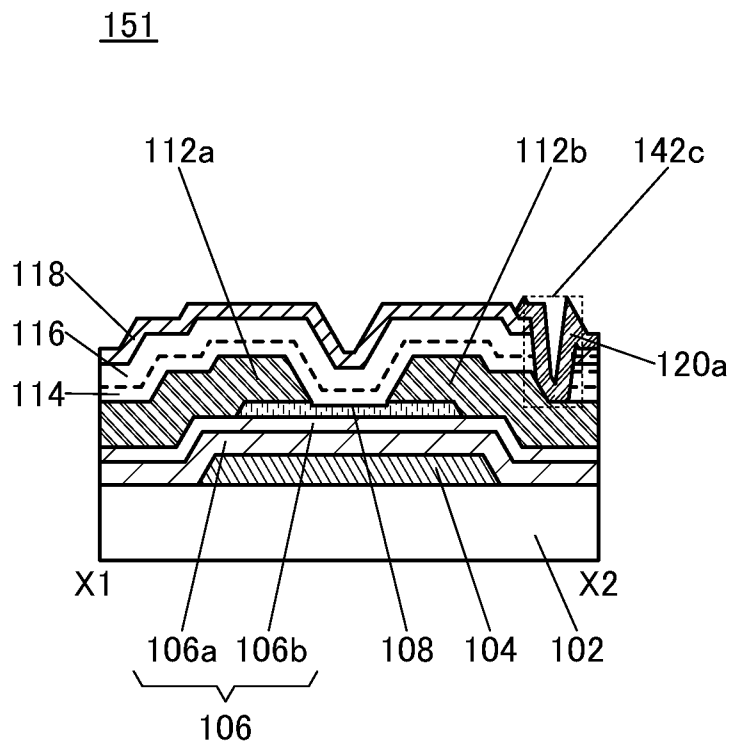


FIG. 20A

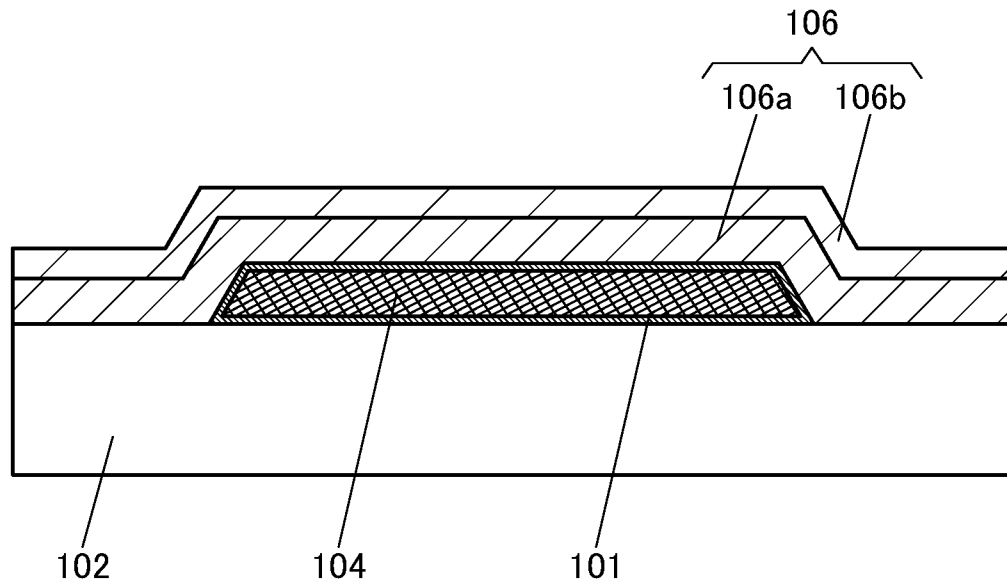


FIG. 20B

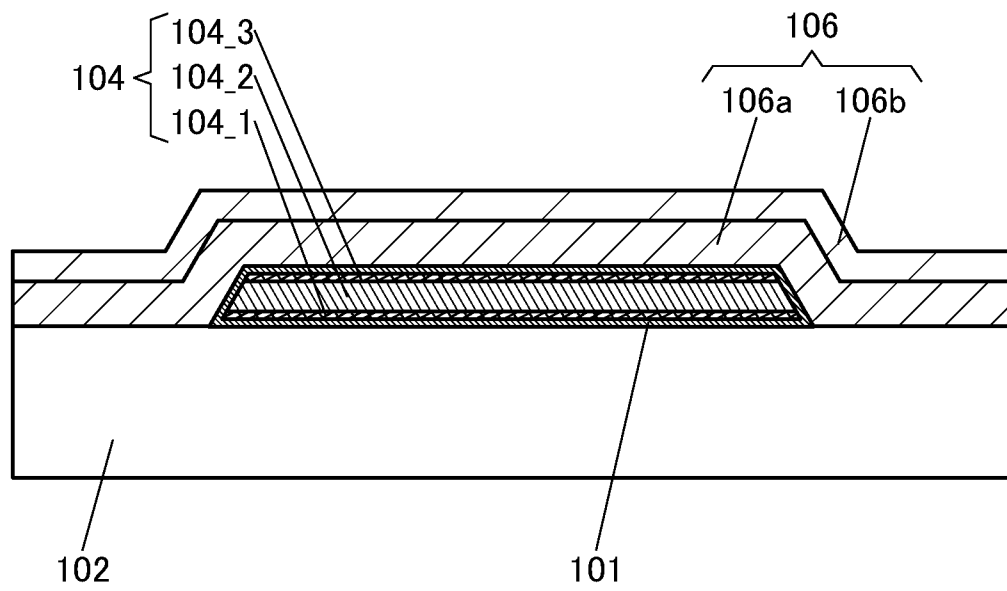


FIG. 21A

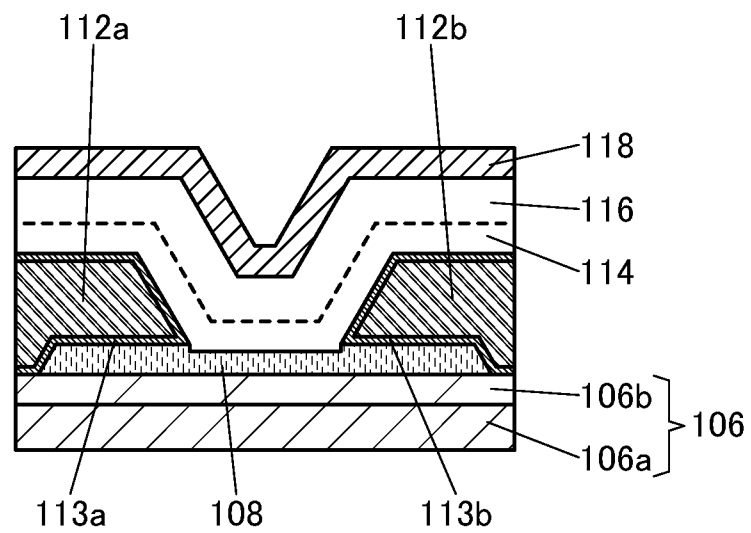


FIG. 21B

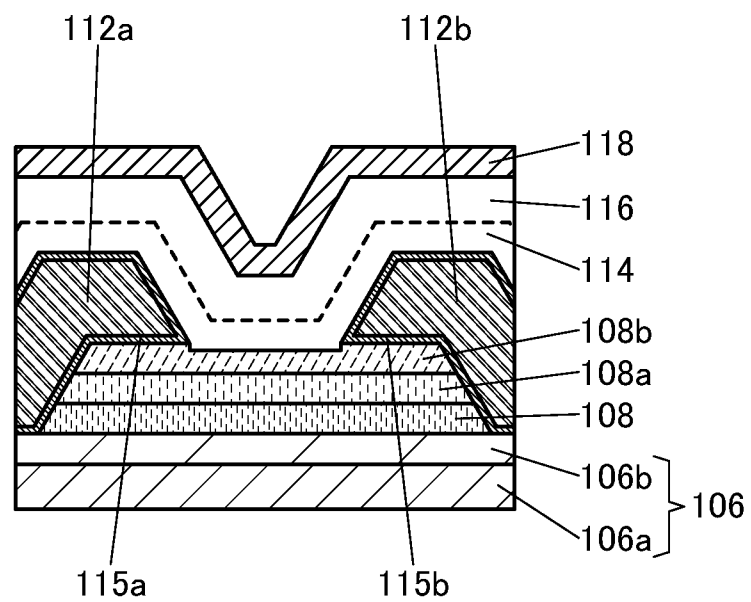


FIG. 22A

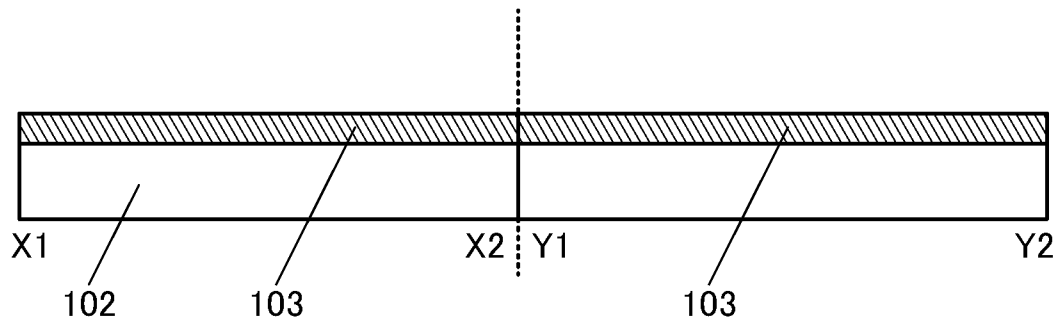


FIG. 22B

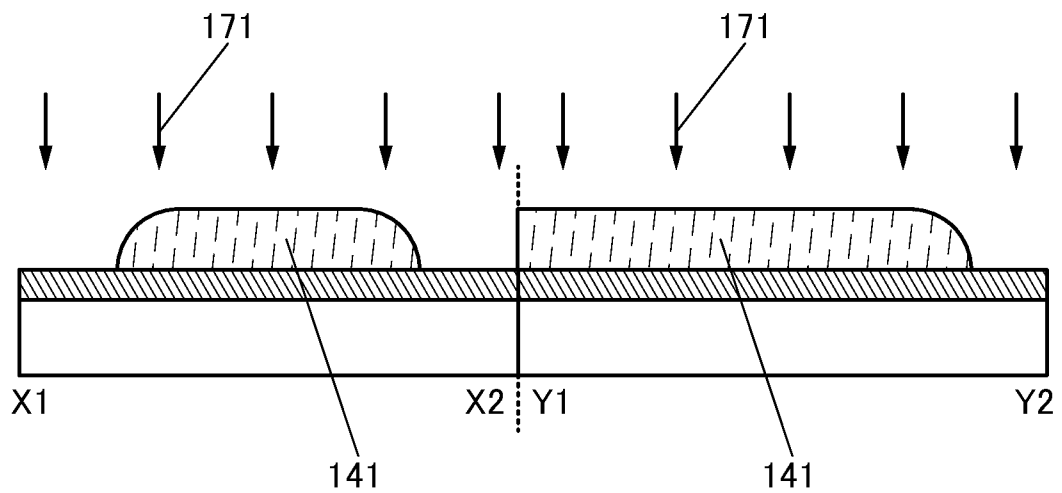


FIG. 22C

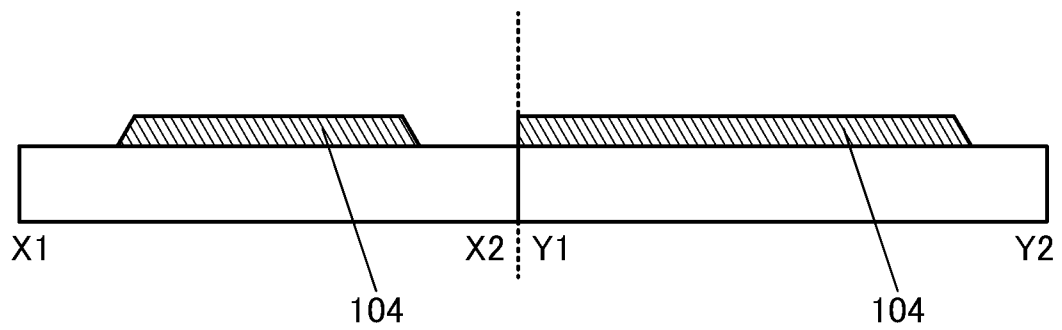


FIG. 23A

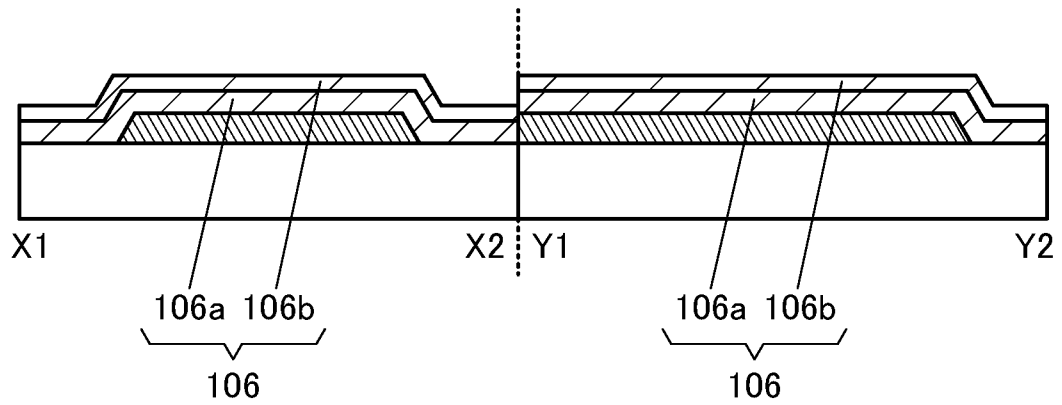


FIG. 23B

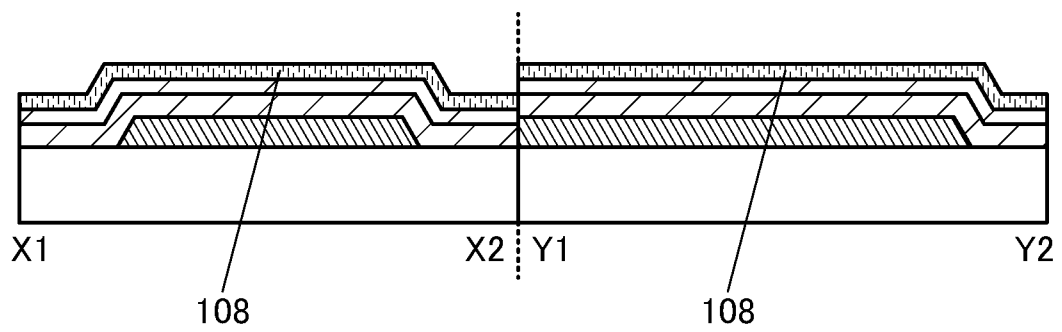


FIG. 23C

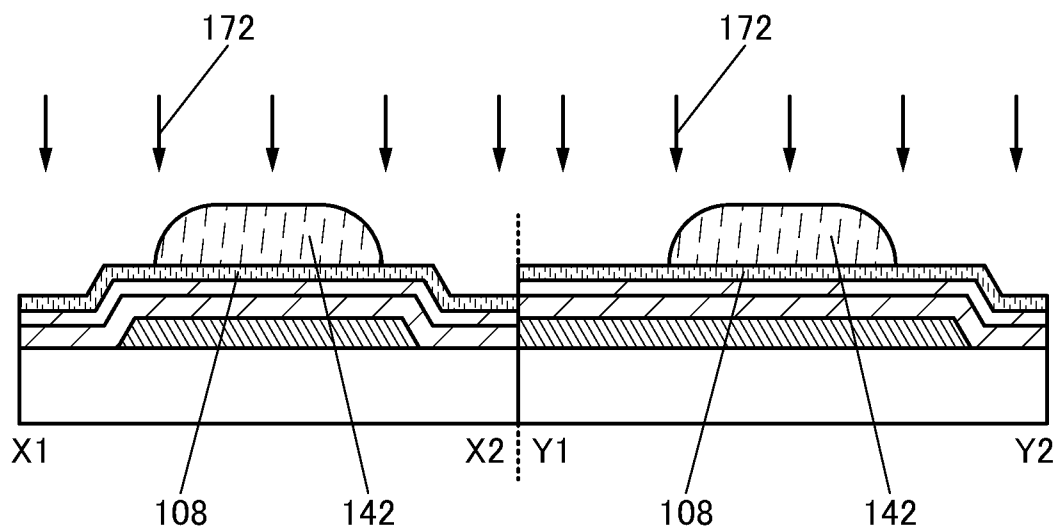


FIG. 24A

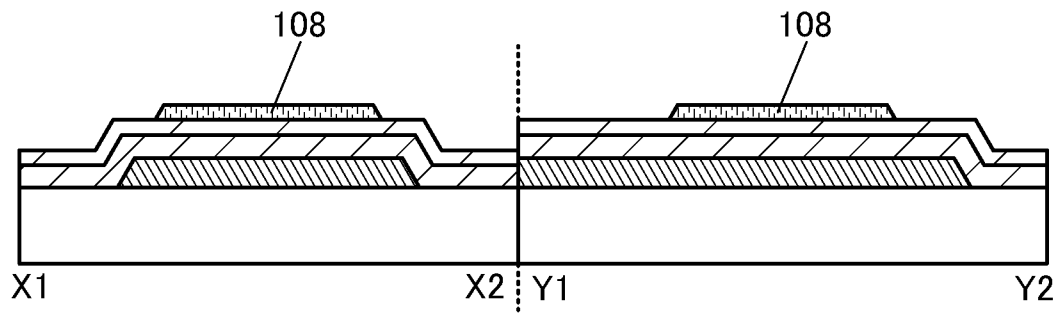


FIG. 24B

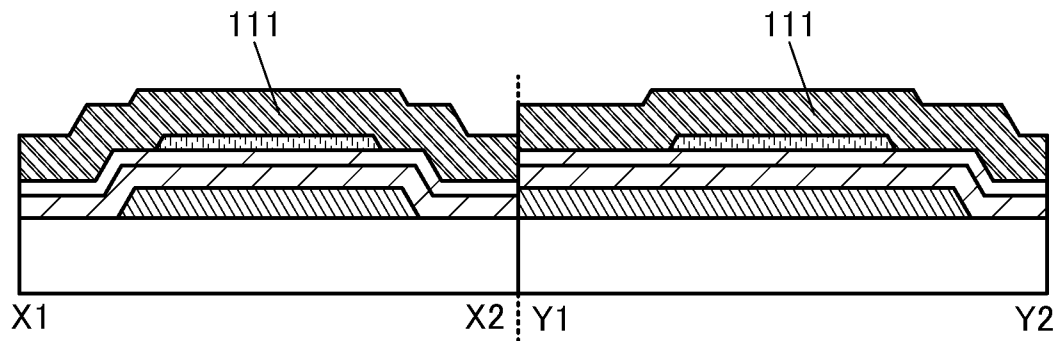


FIG. 24C

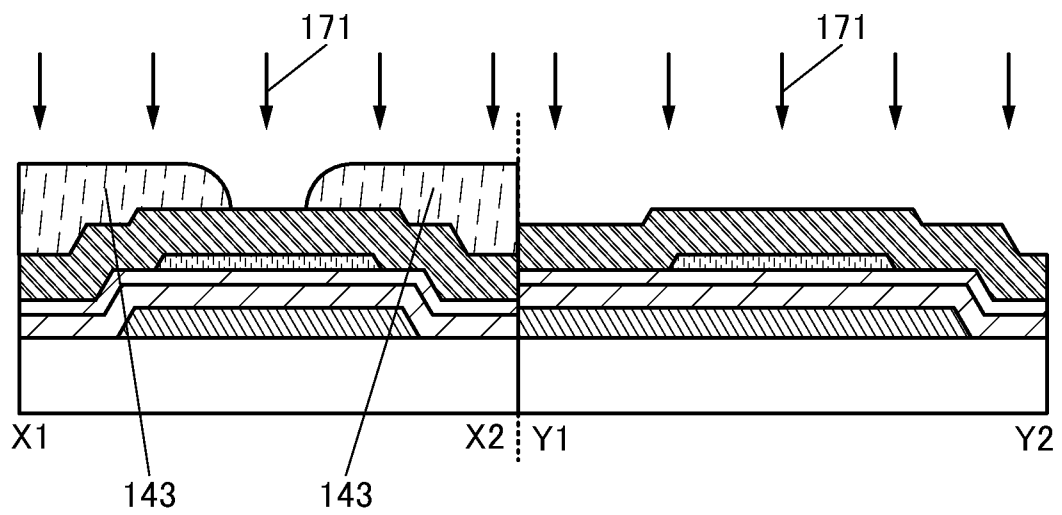


FIG. 25A

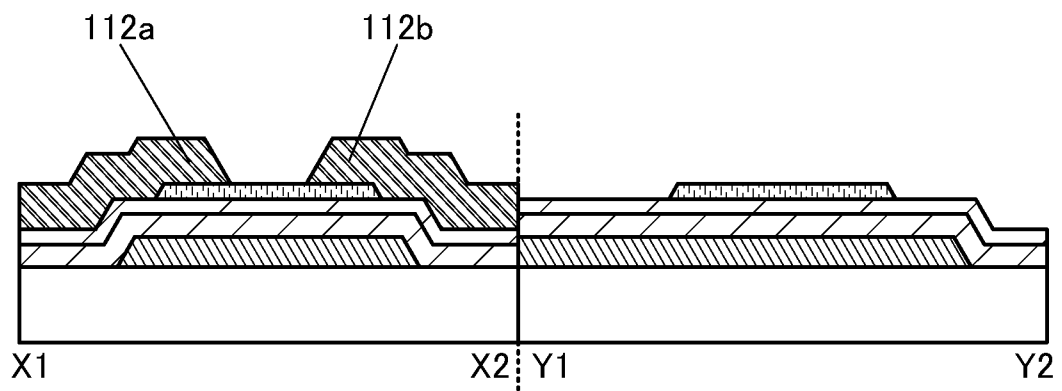


FIG. 25B

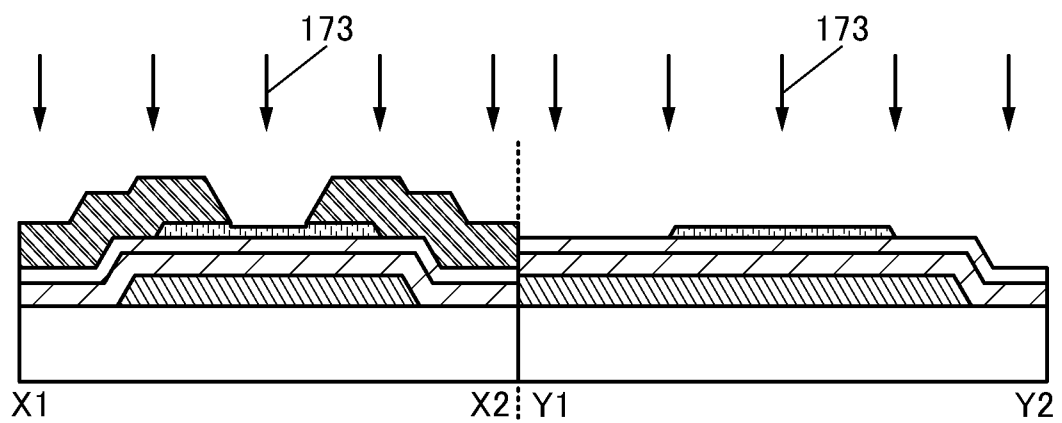


FIG. 25C

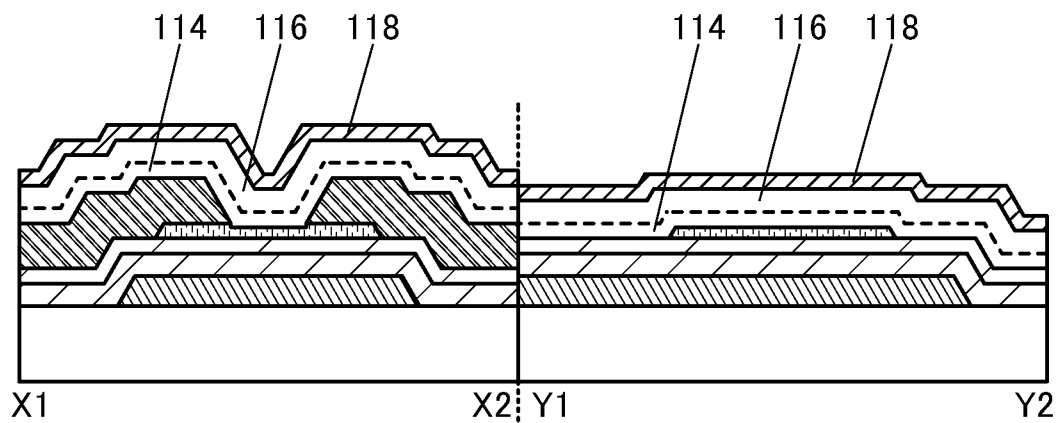


FIG. 26A

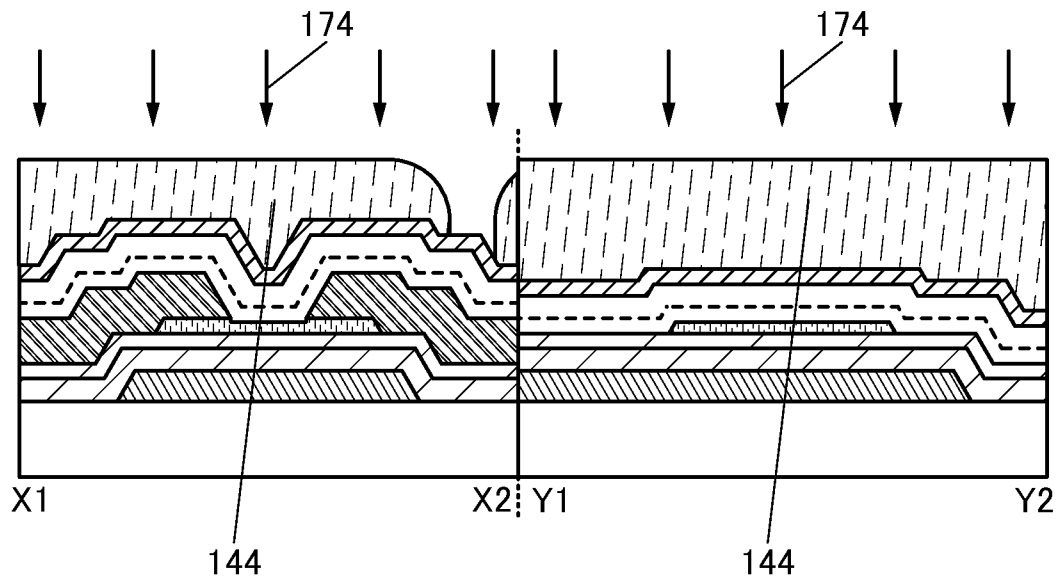


FIG. 26B

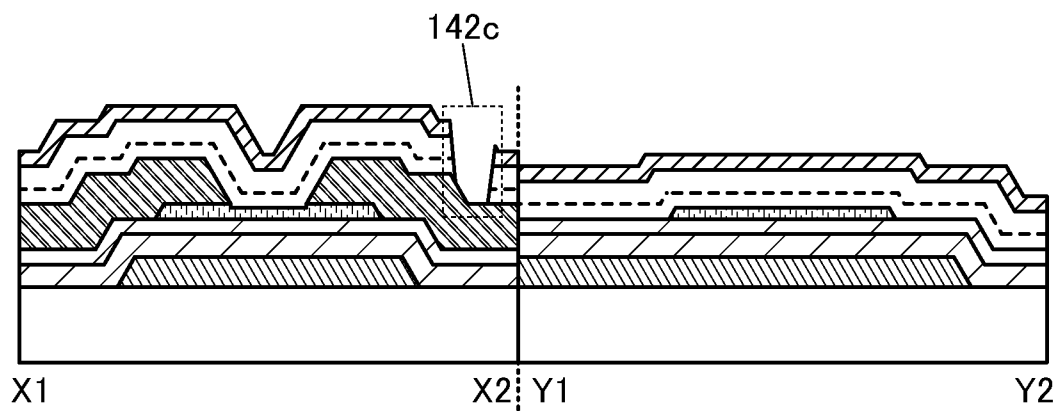


FIG. 26C

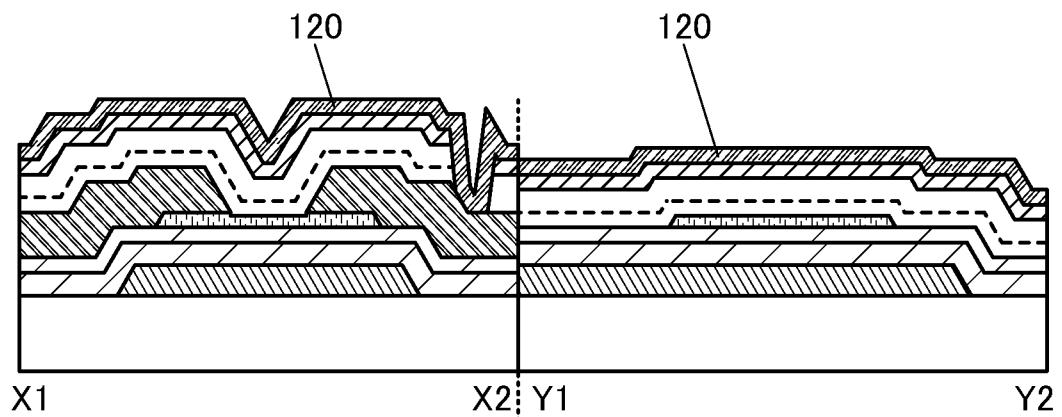


FIG. 27A

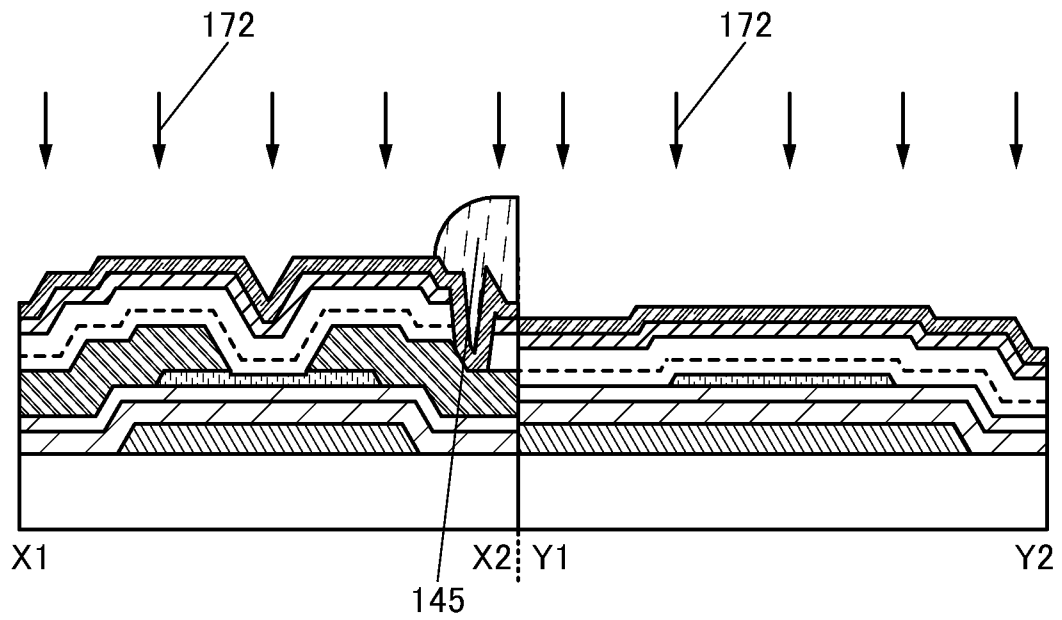


FIG. 27B

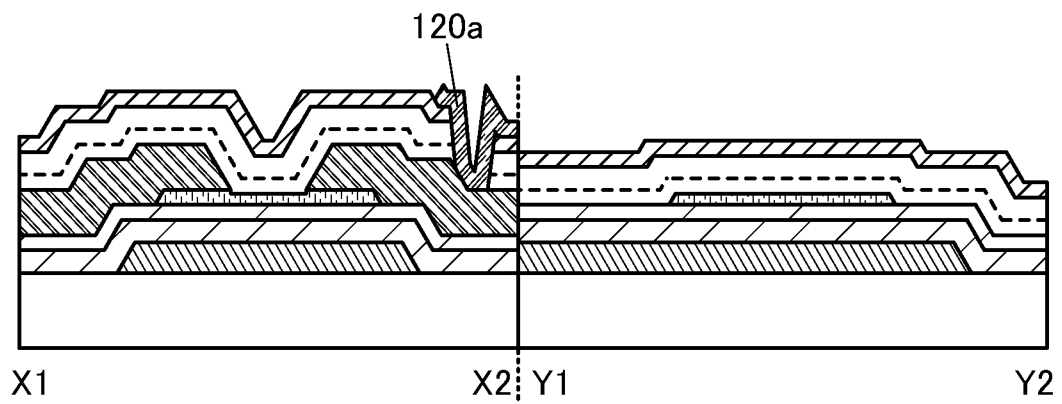


FIG. 28A

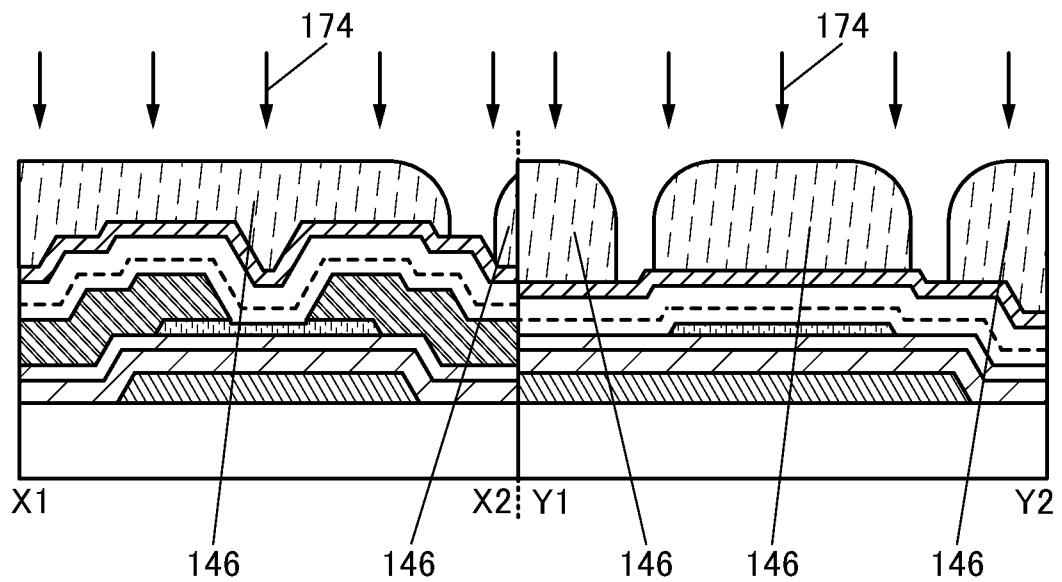


FIG. 28B

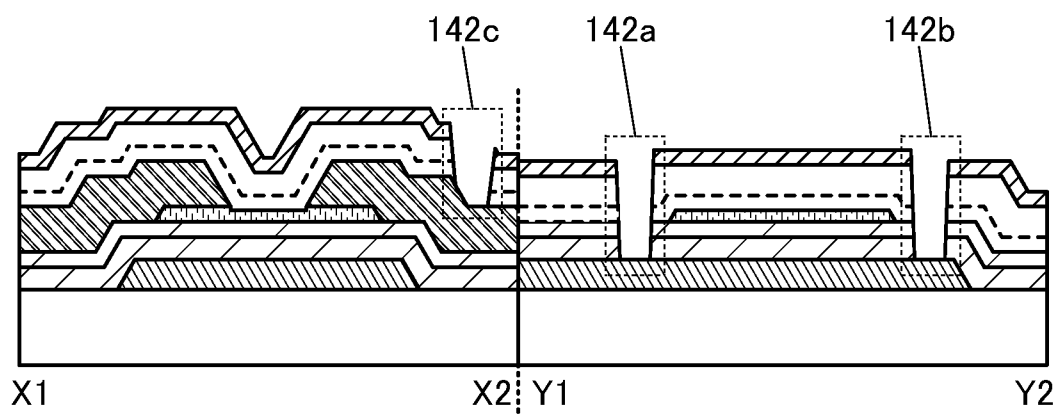


FIG. 28C

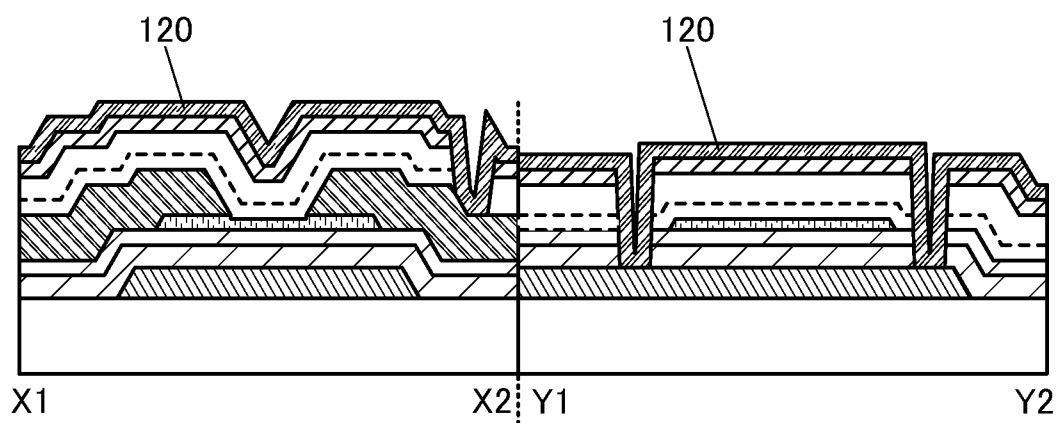


FIG. 29A

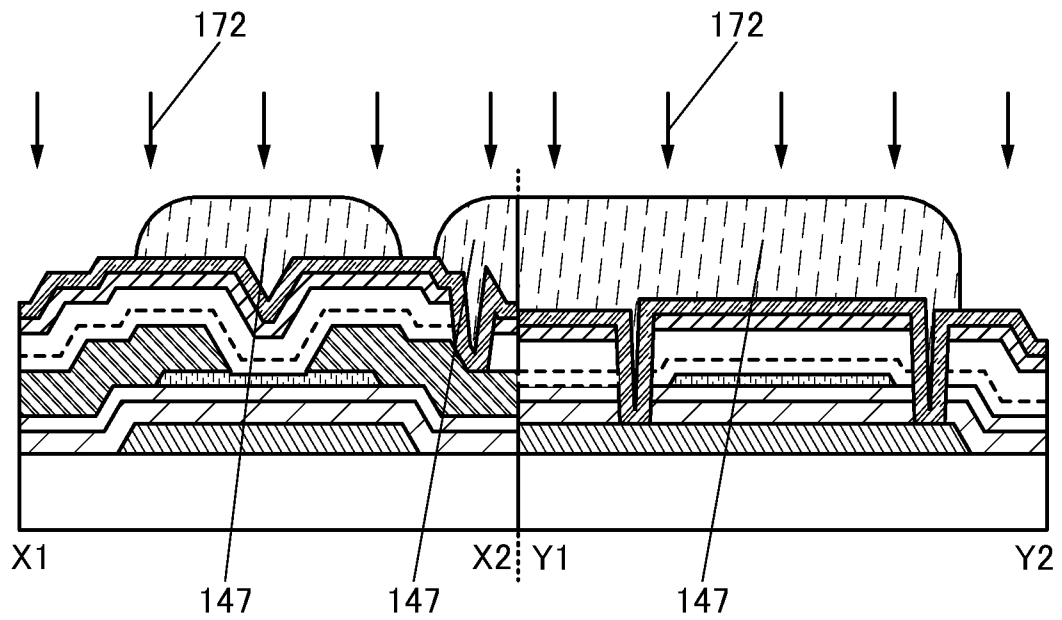


FIG. 29B

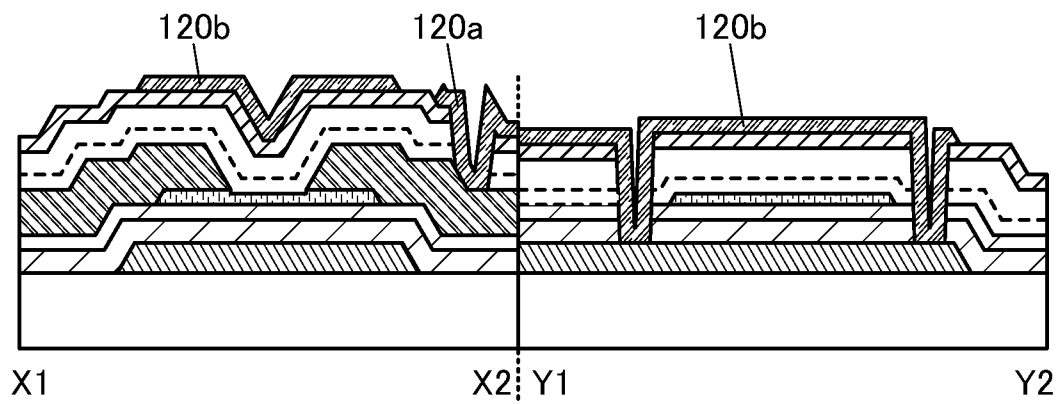


FIG. 30A

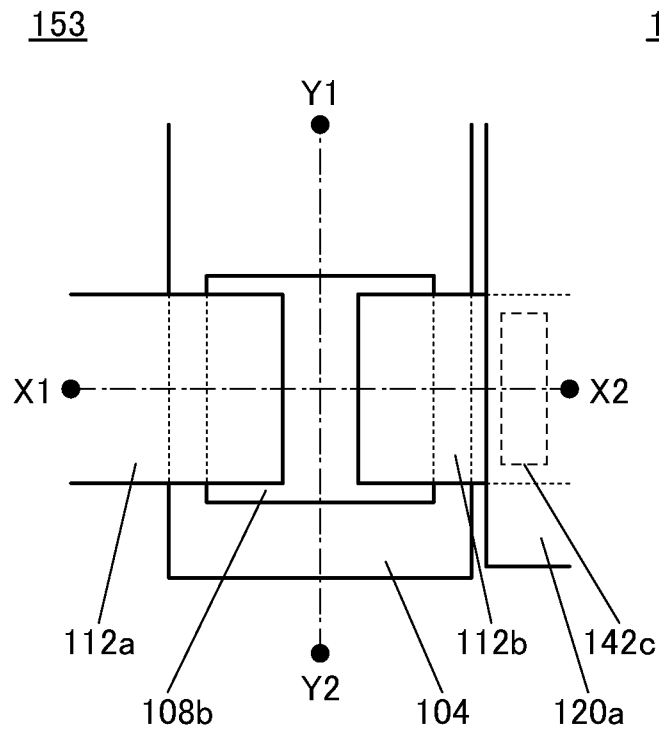


FIG. 30B

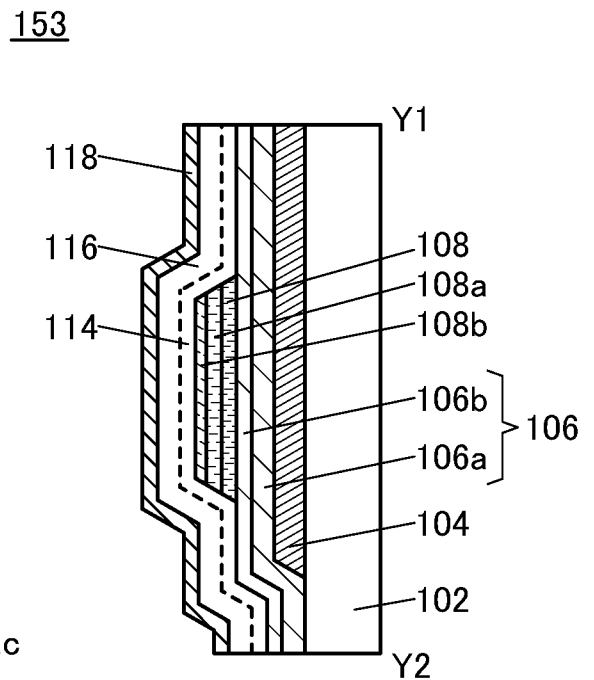


FIG. 30C

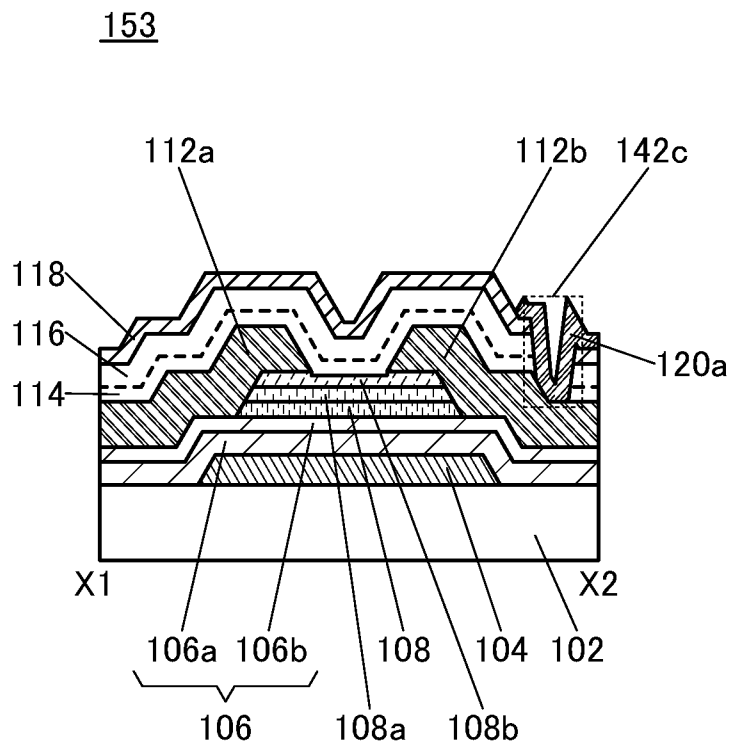


FIG. 31A

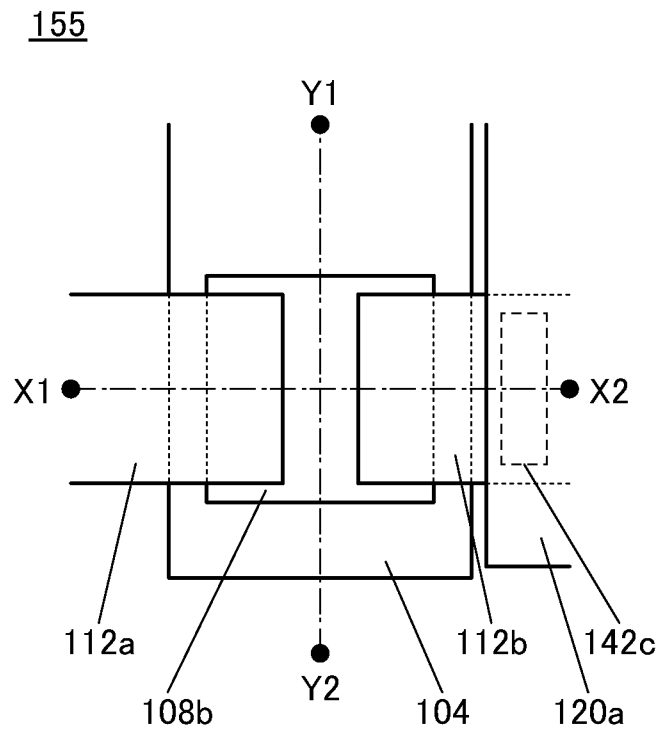


FIG. 31B

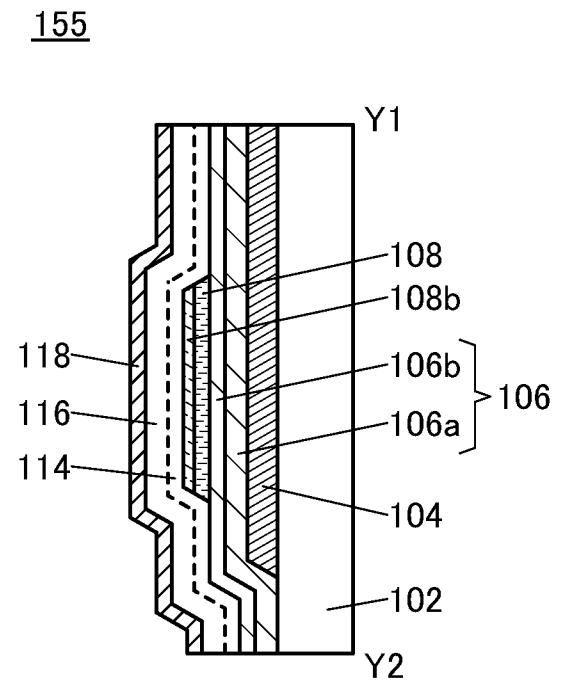


FIG. 31C

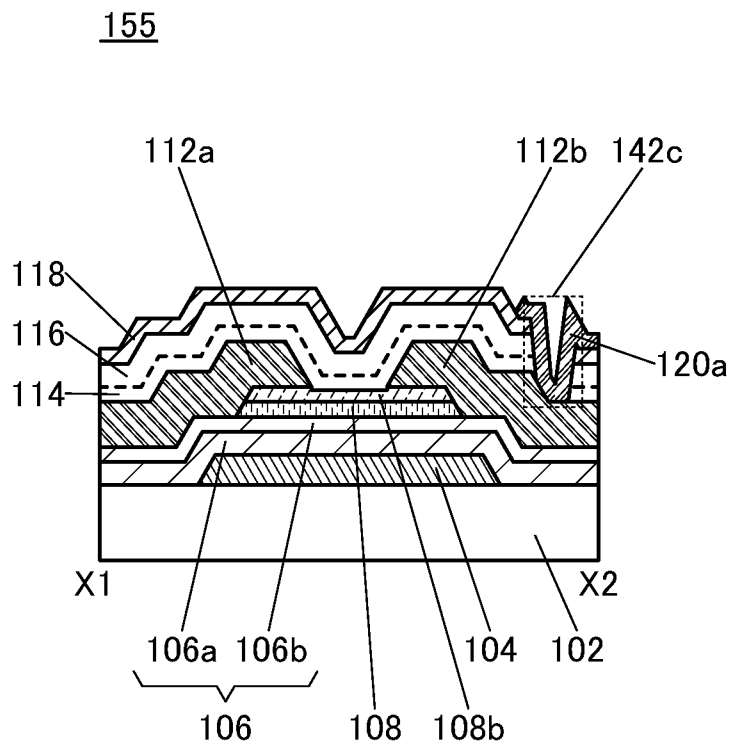


FIG. 32A

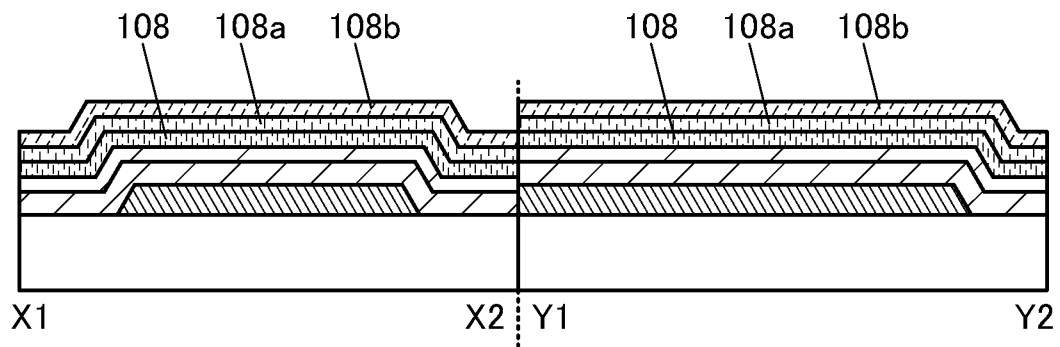


FIG. 32B

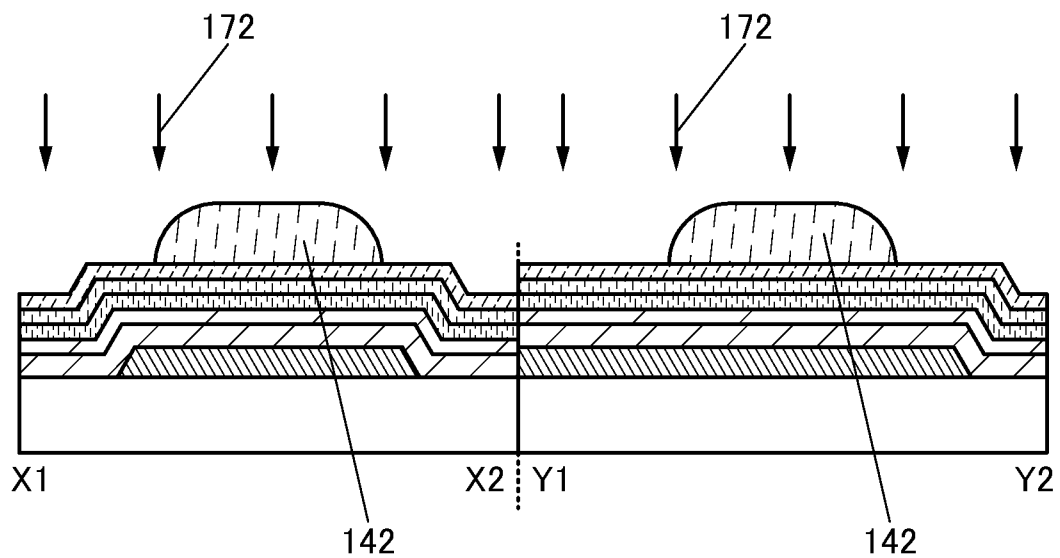


FIG. 32C

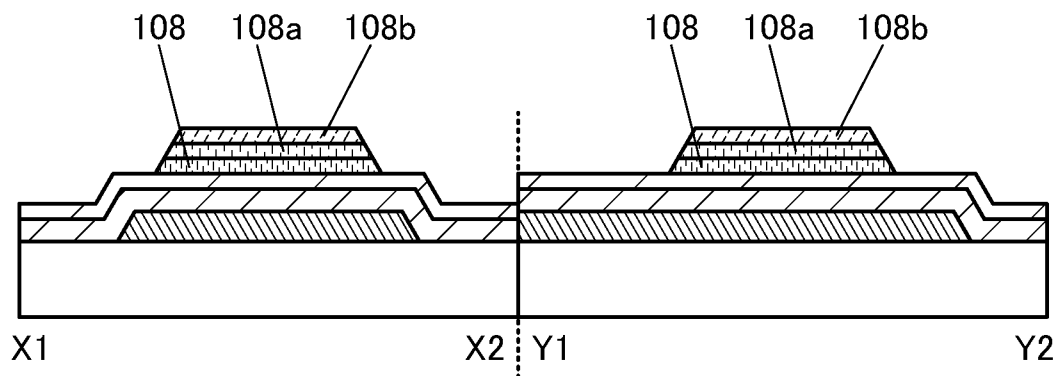


FIG. 33A

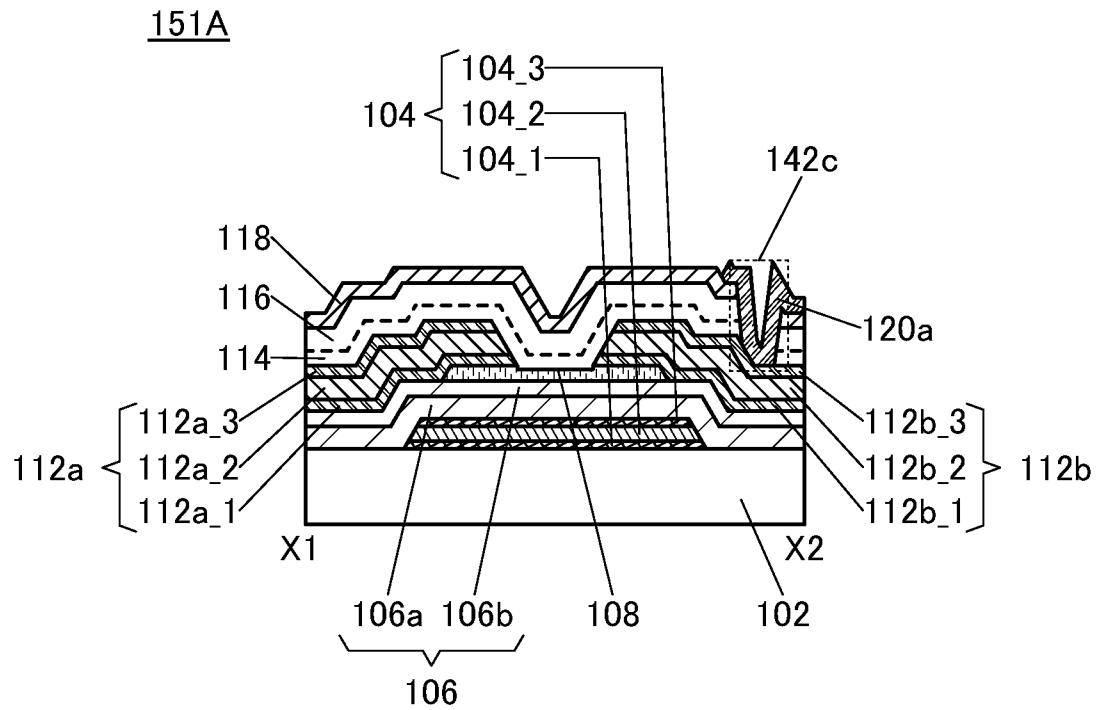


FIG. 33B

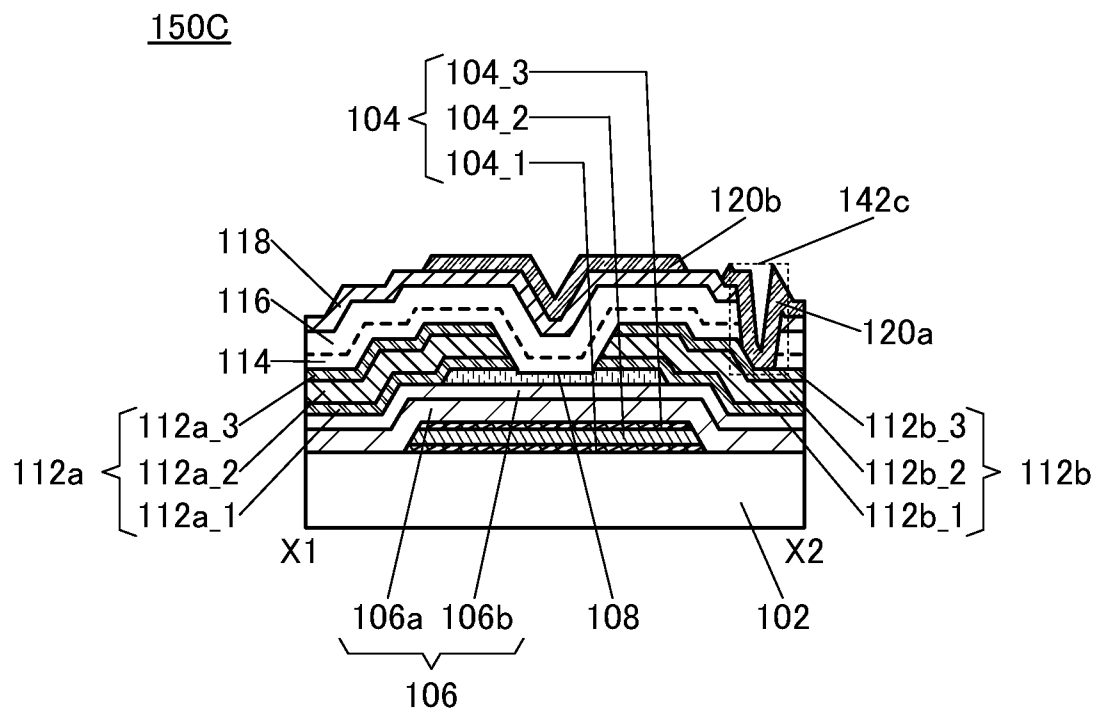


FIG. 34A

151B

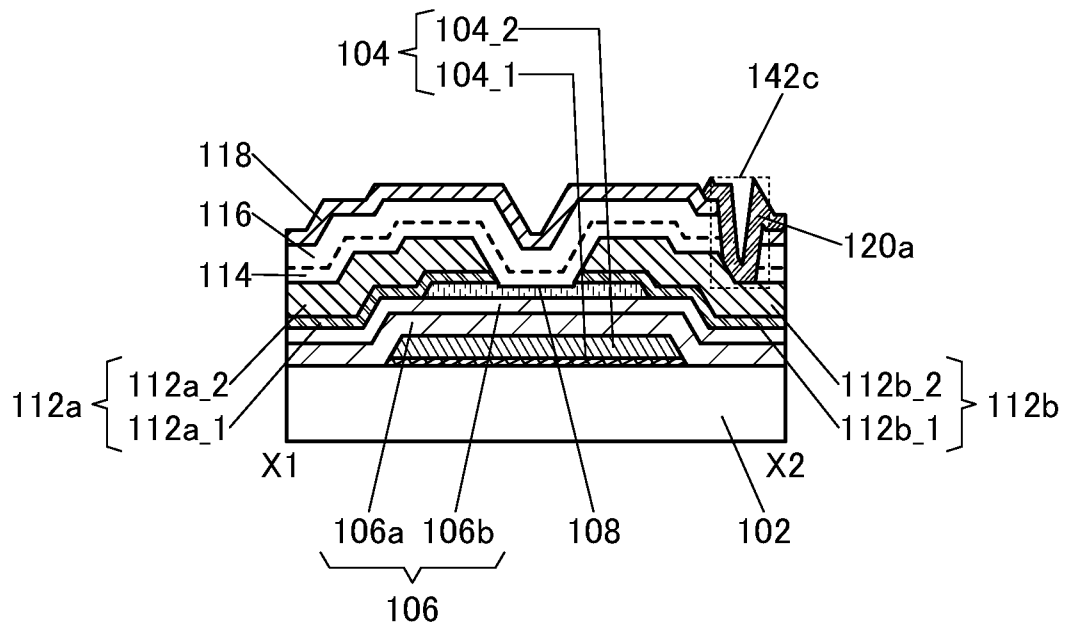


FIG. 34B

150D

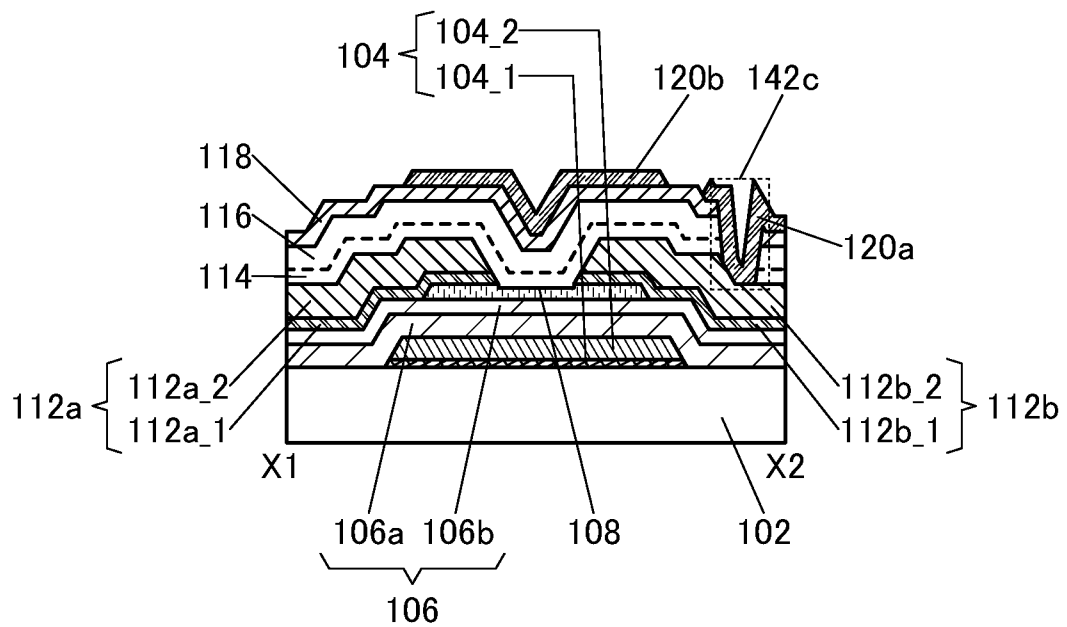


FIG. 35A

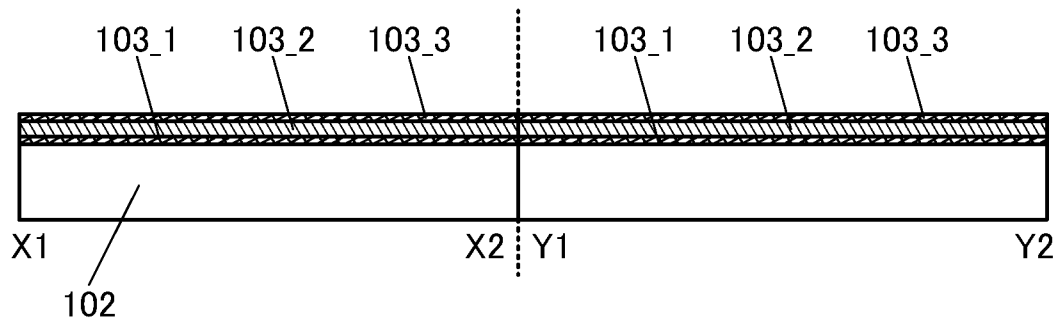


FIG. 35B

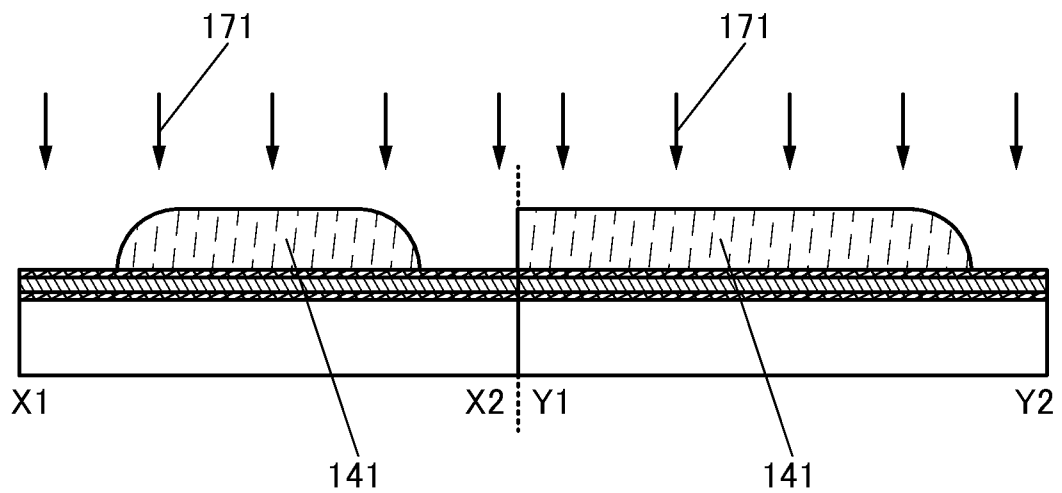


FIG. 35C

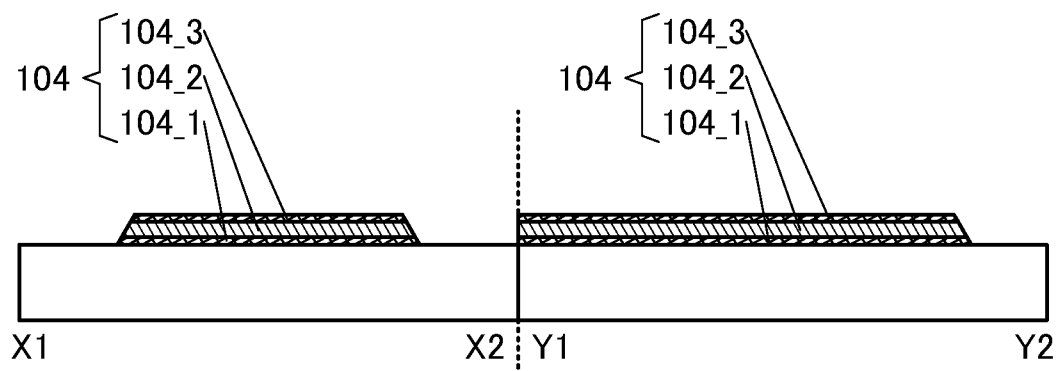


FIG. 36A

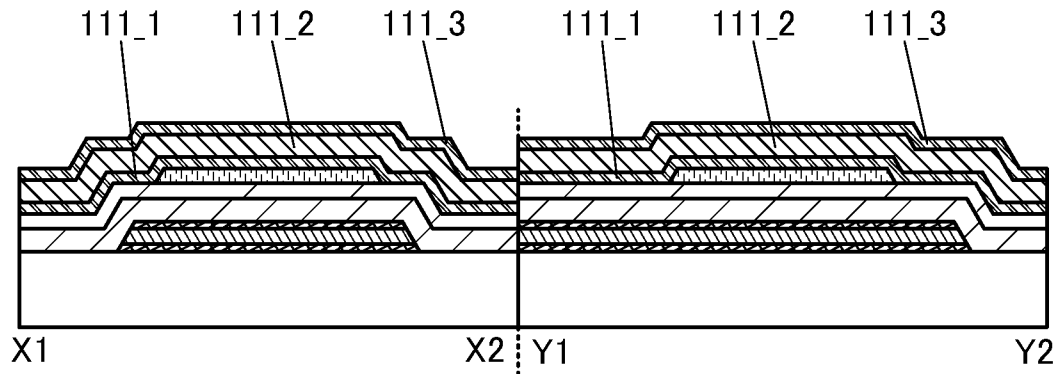


FIG. 36B

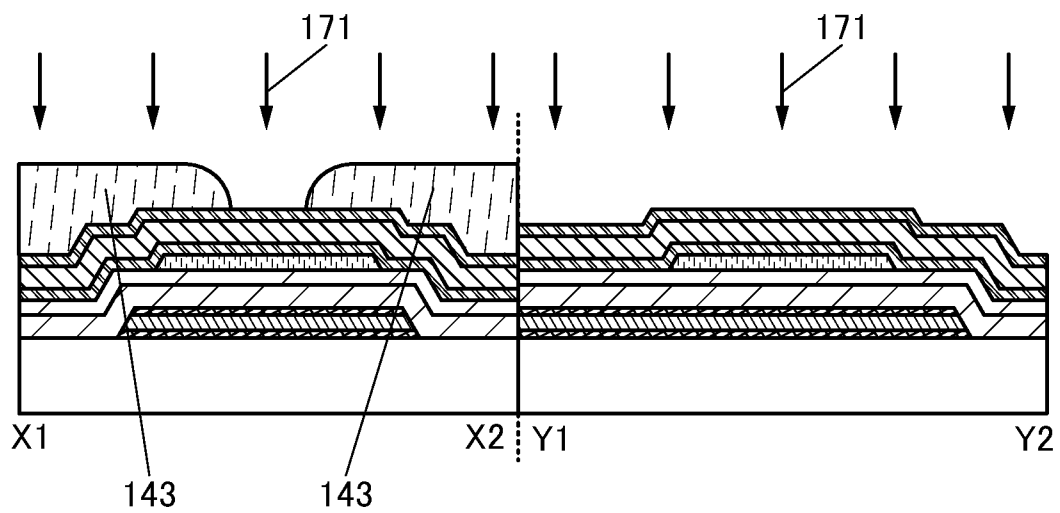


FIG. 36C

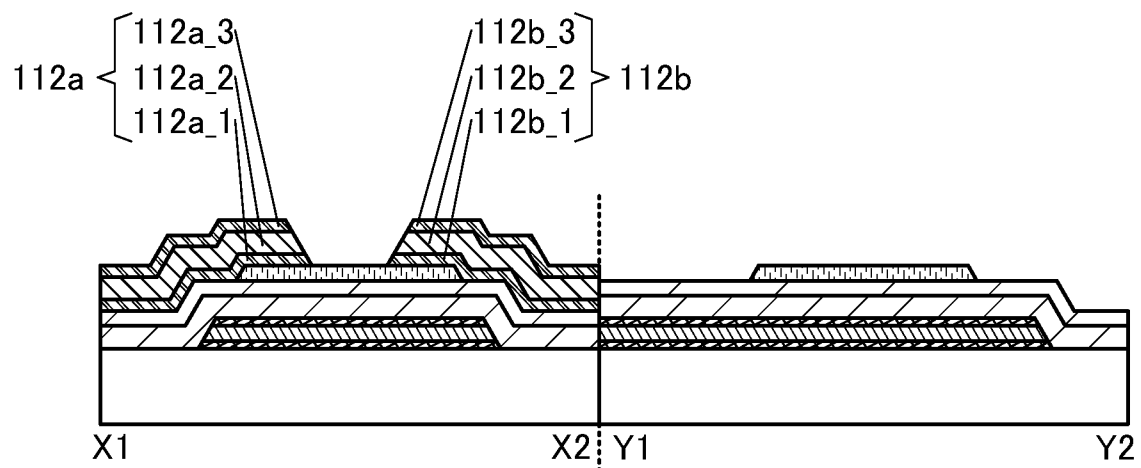


FIG. 37A

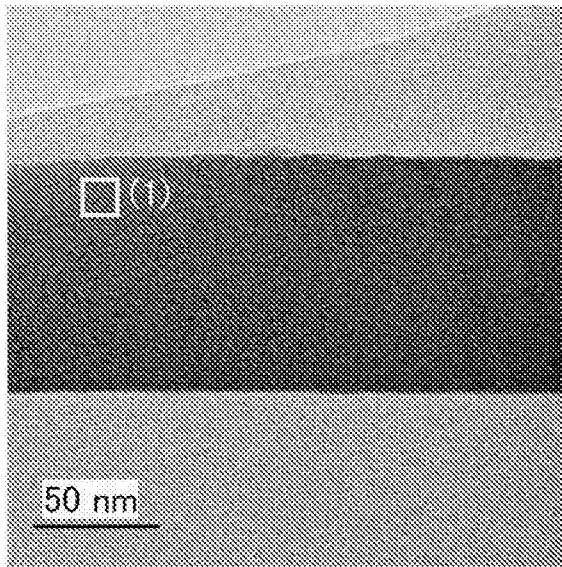


FIG. 37B

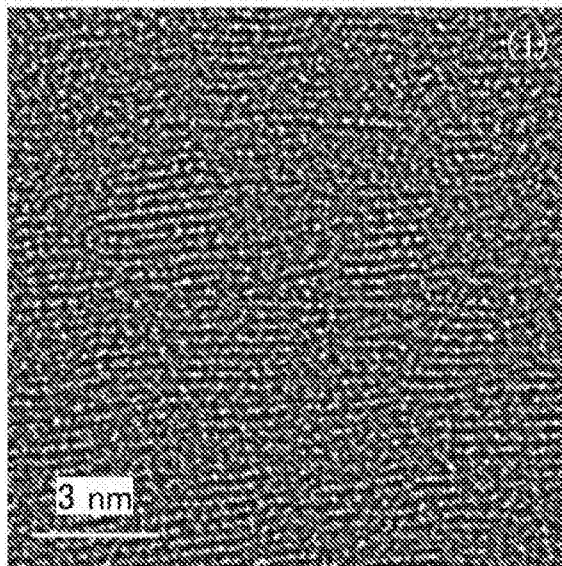


FIG. 37C

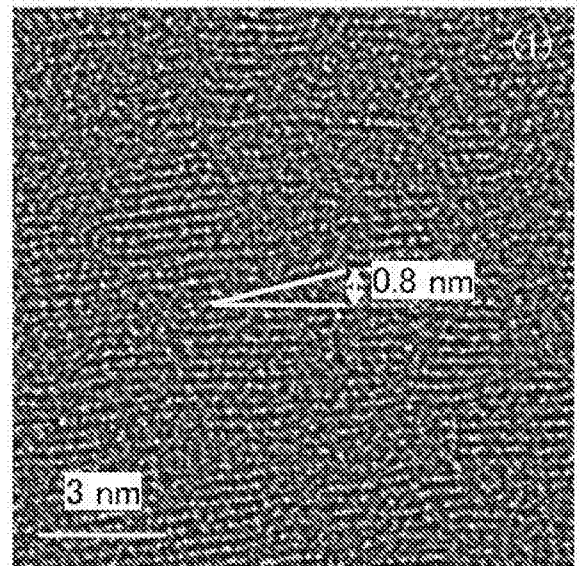


FIG. 37D

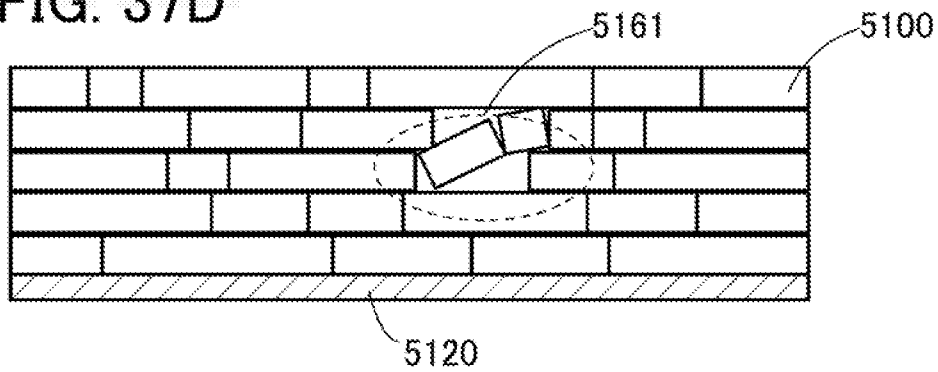


FIG. 38A

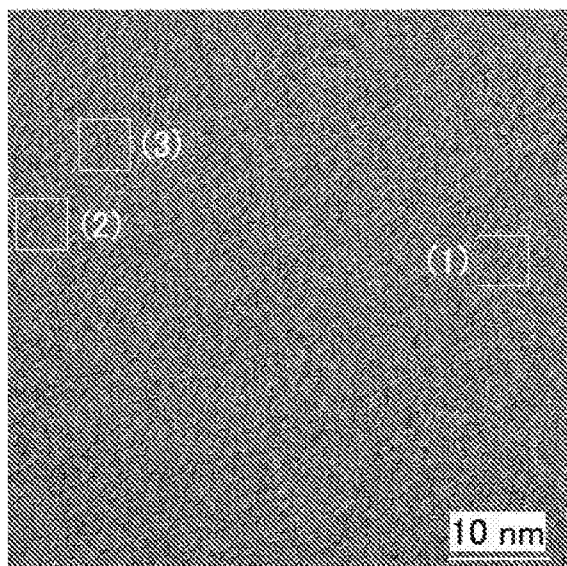


FIG. 38B

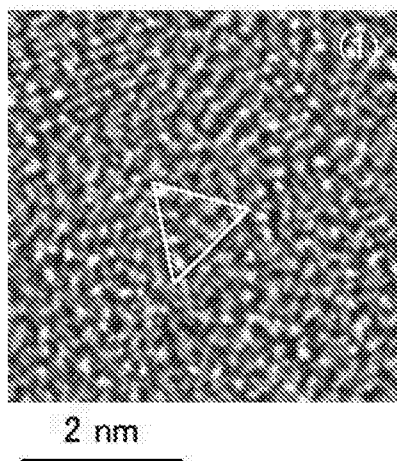


FIG. 38C

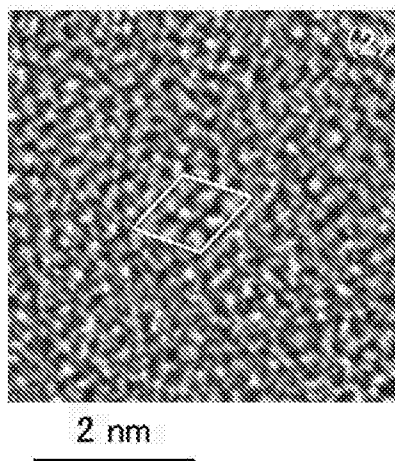


FIG. 38D

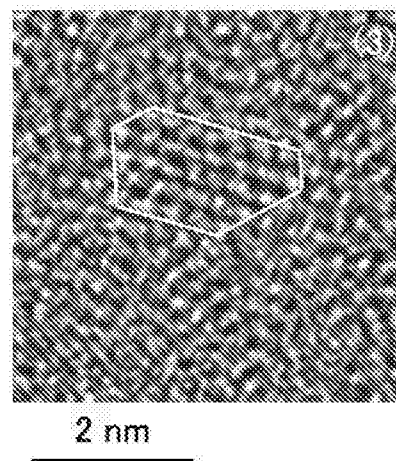


FIG. 39A

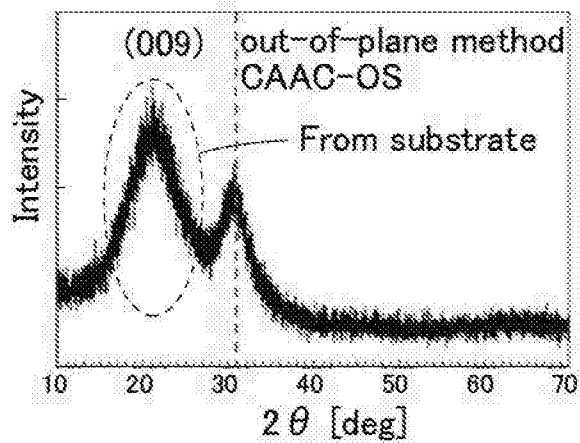


FIG. 39B

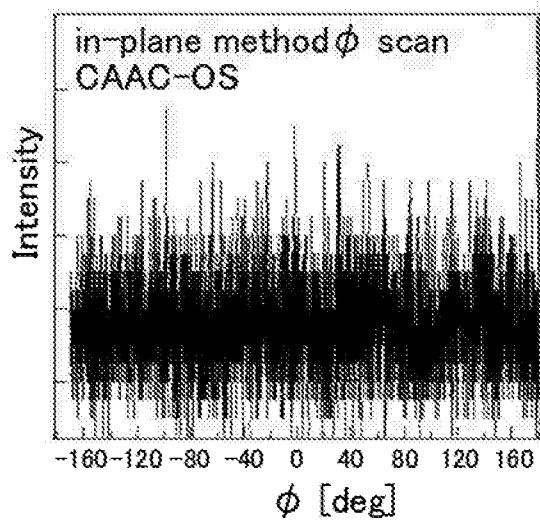


FIG. 39C

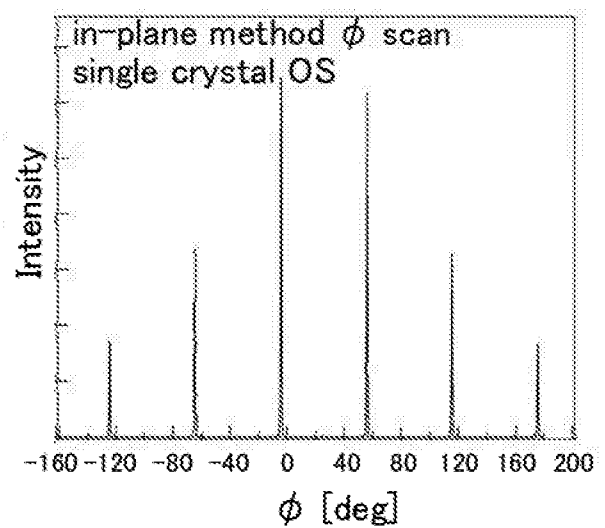
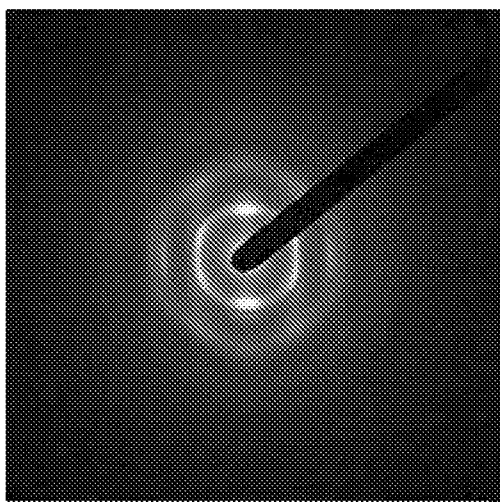
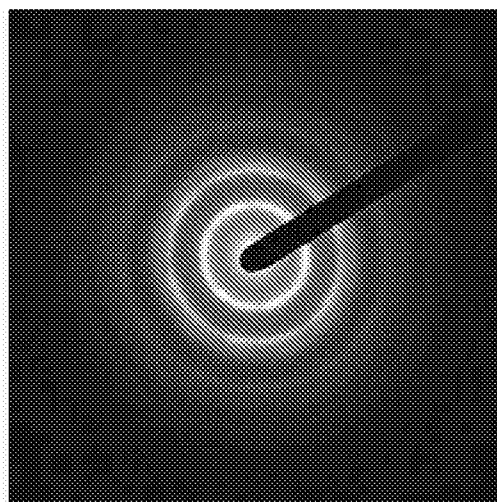


FIG. 40A



Electron beam is incident from a direction parallel to the sample surface.

FIG. 40B



Electron beam is incident from a direction vertical to the sample surface.

FIG. 41

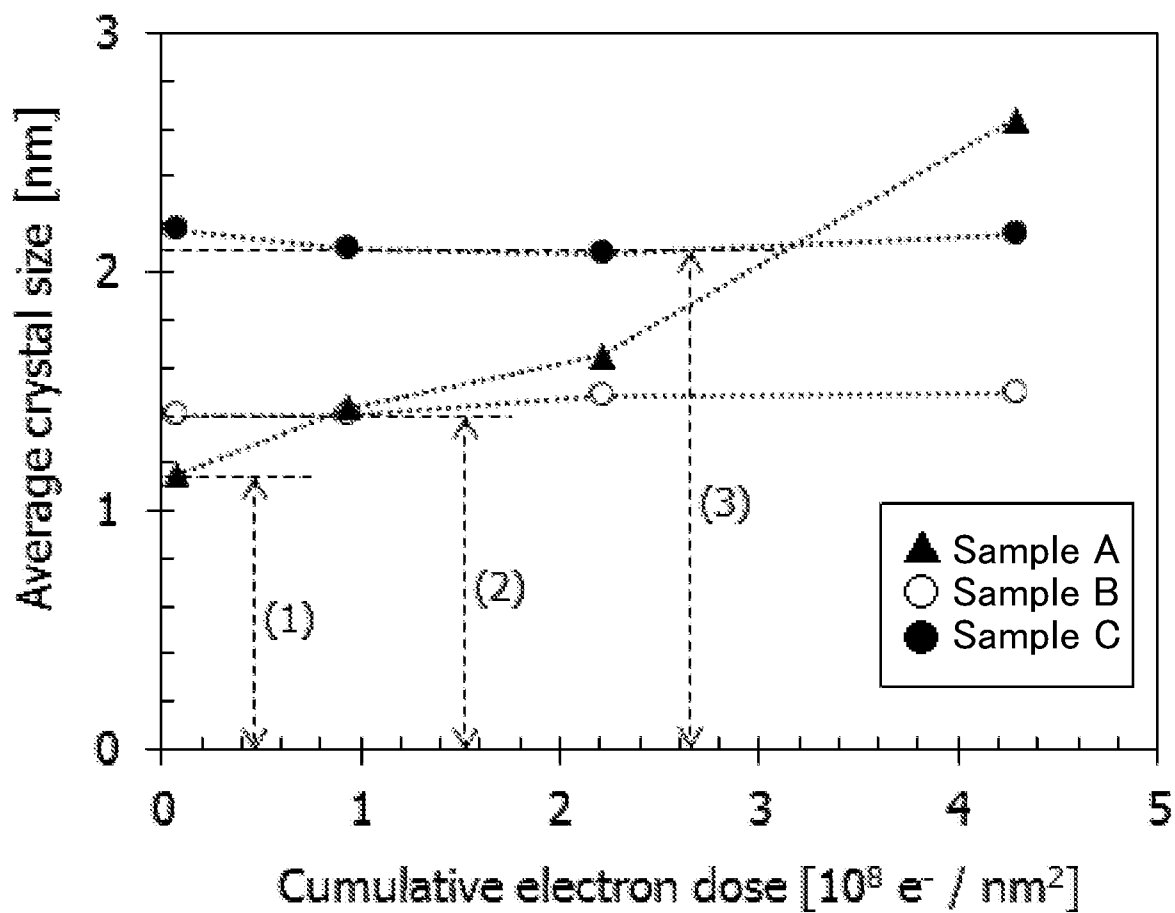


FIG. 42A

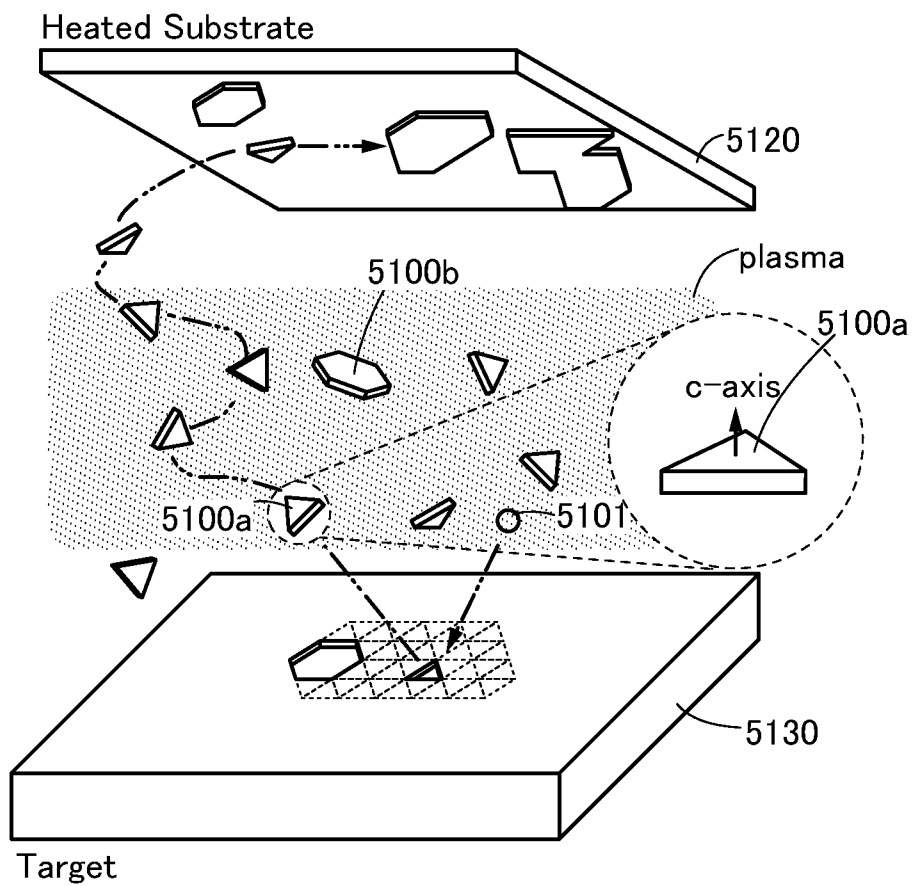


FIG. 42B

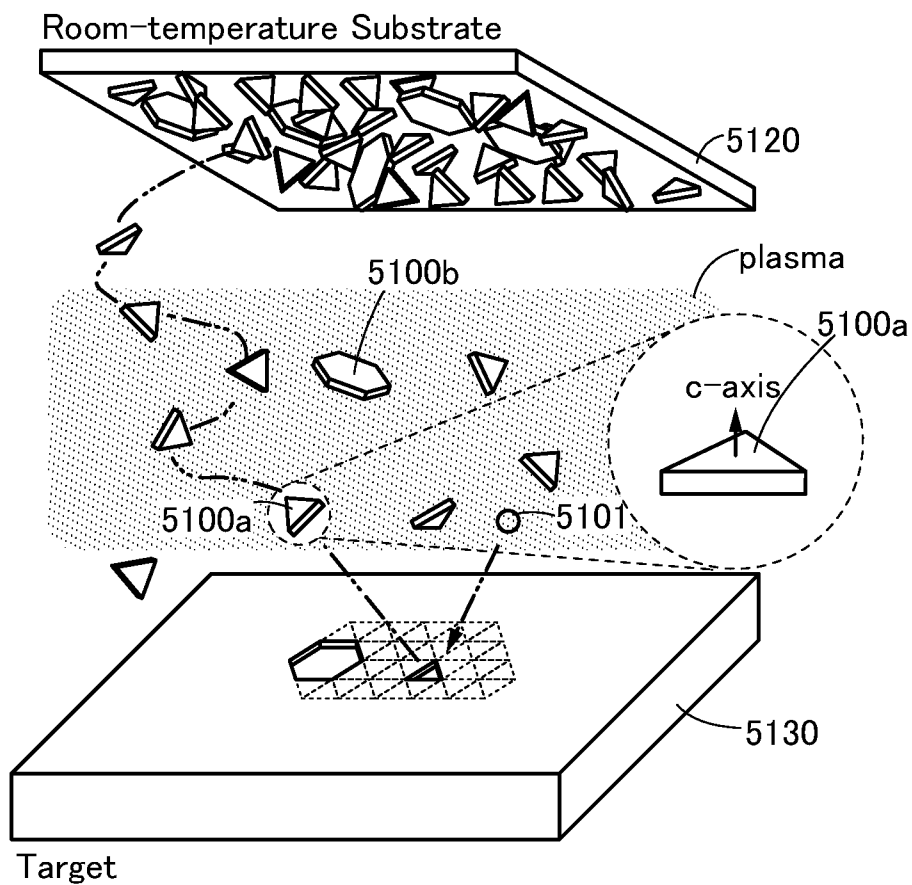


FIG. 43A

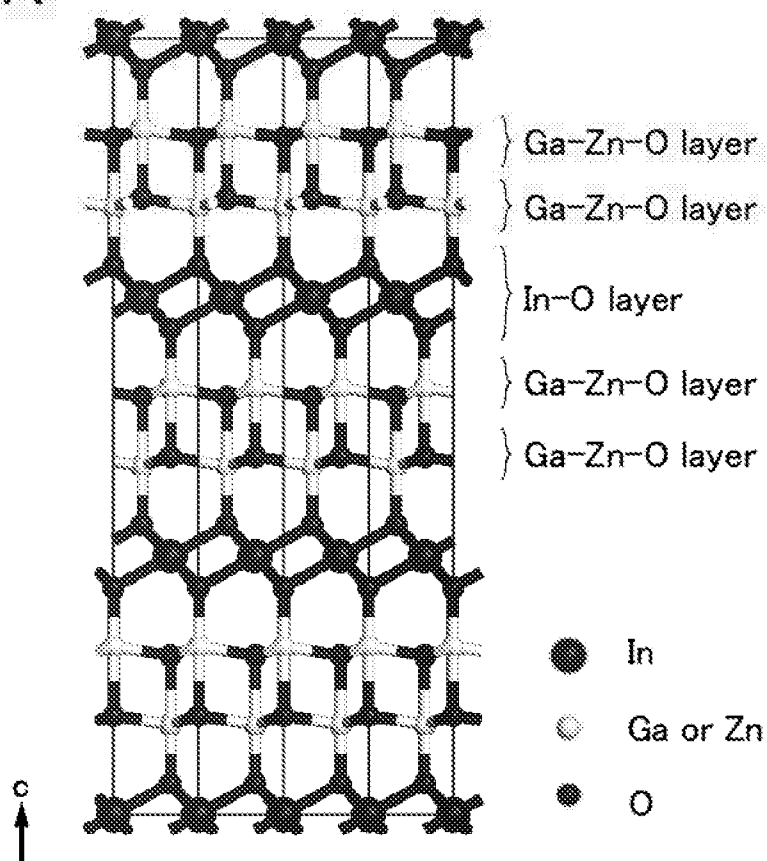
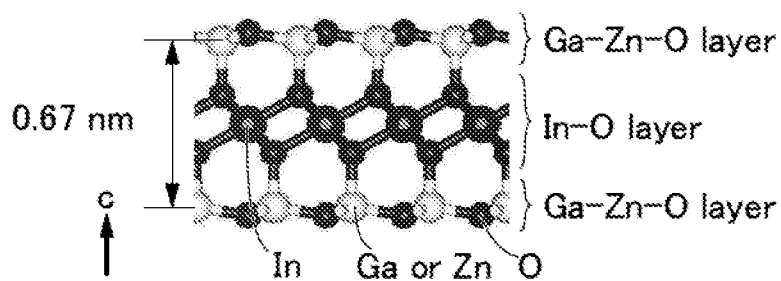
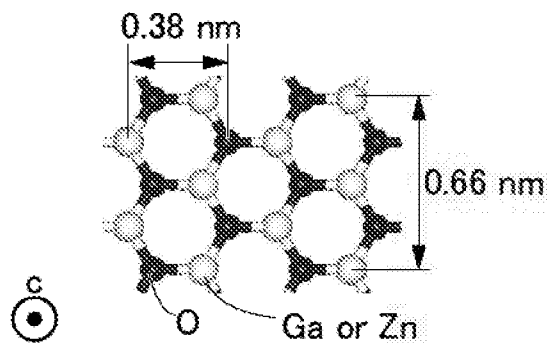


FIG. 43B



Cross sectional view of pellet

FIG. 43C



Plane view of pellet

FIG. 44A

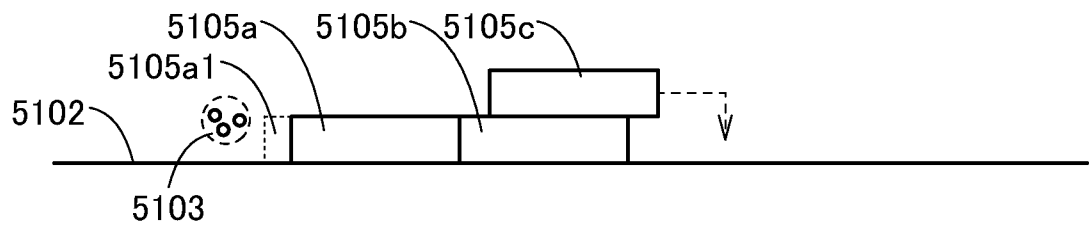


FIG. 44B

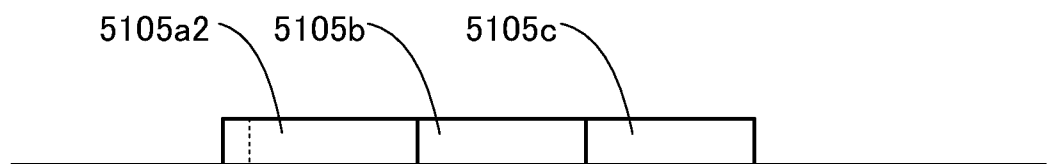


FIG. 44C

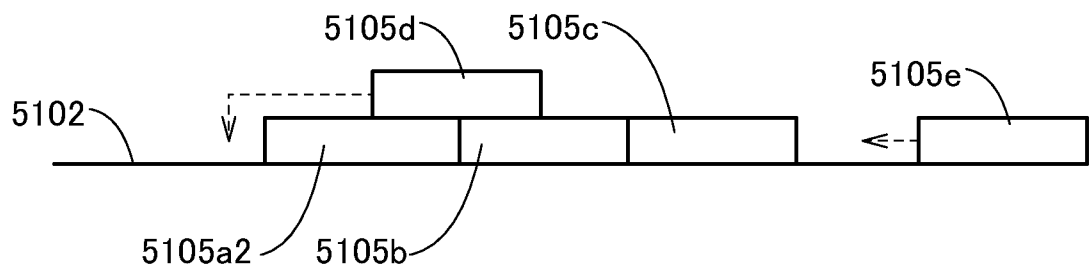


FIG. 44D

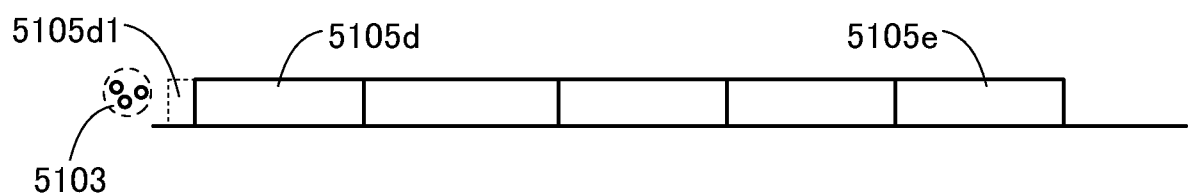


FIG. 45A

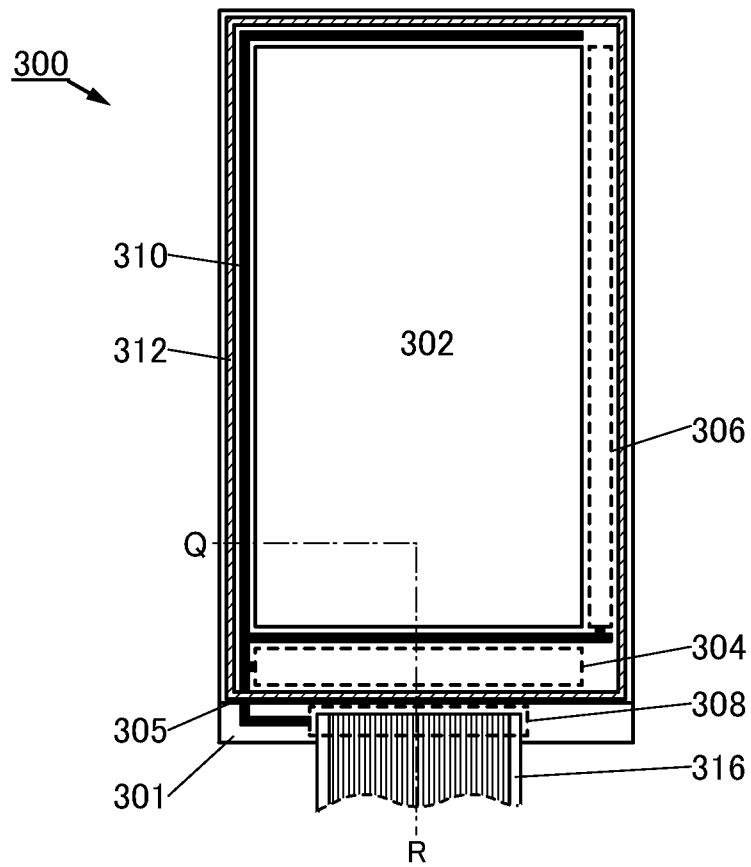


FIG. 45B

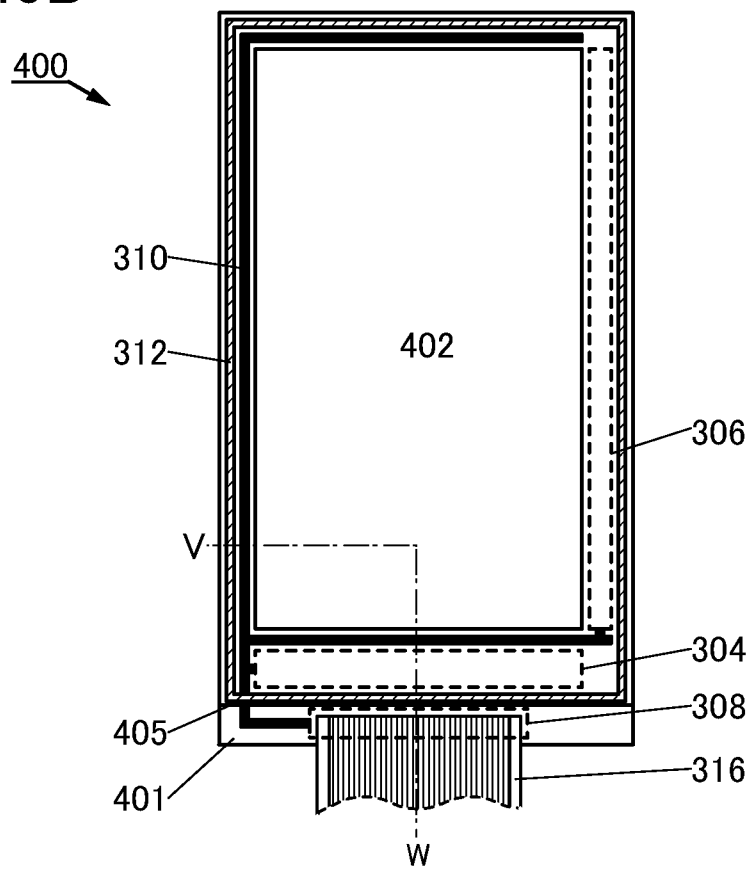


FIG. 46

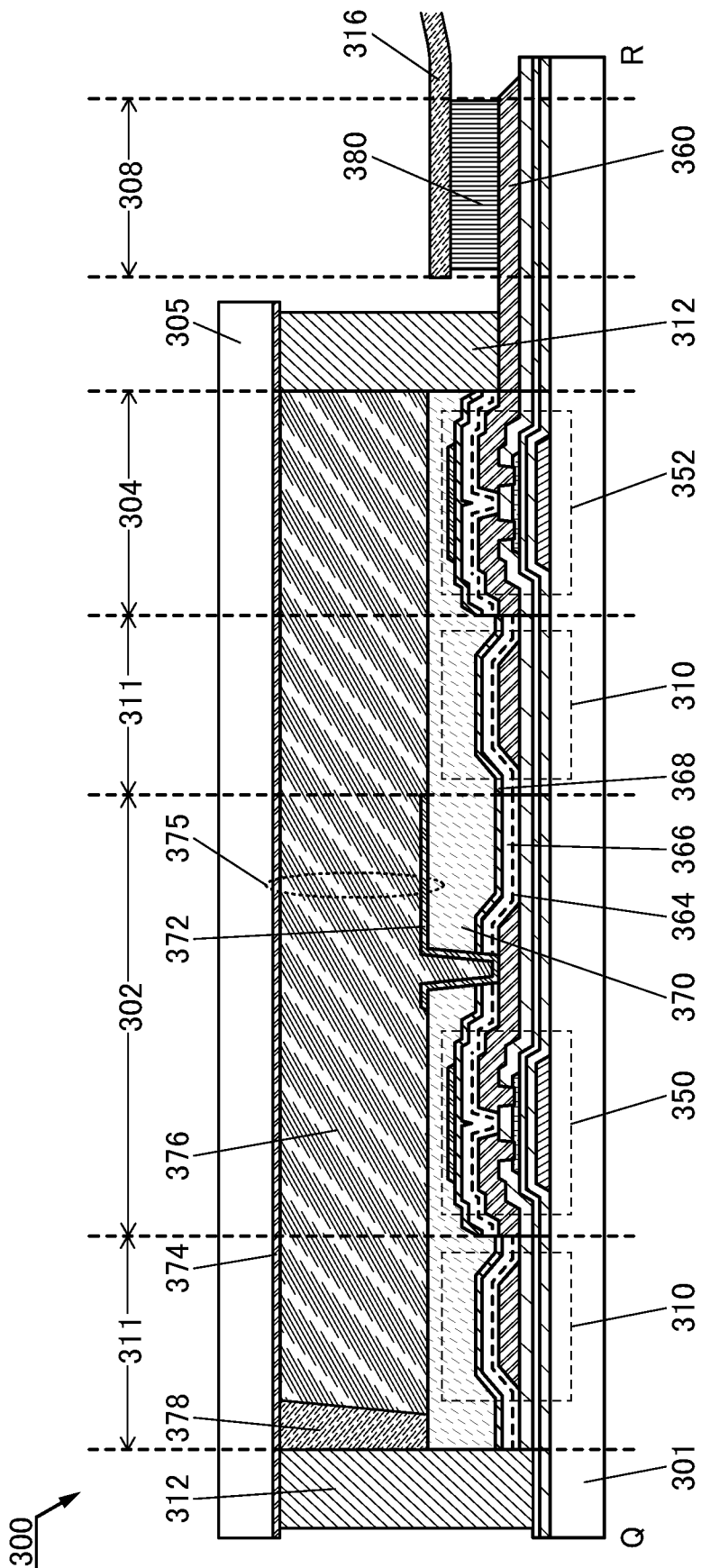


FIG. 47

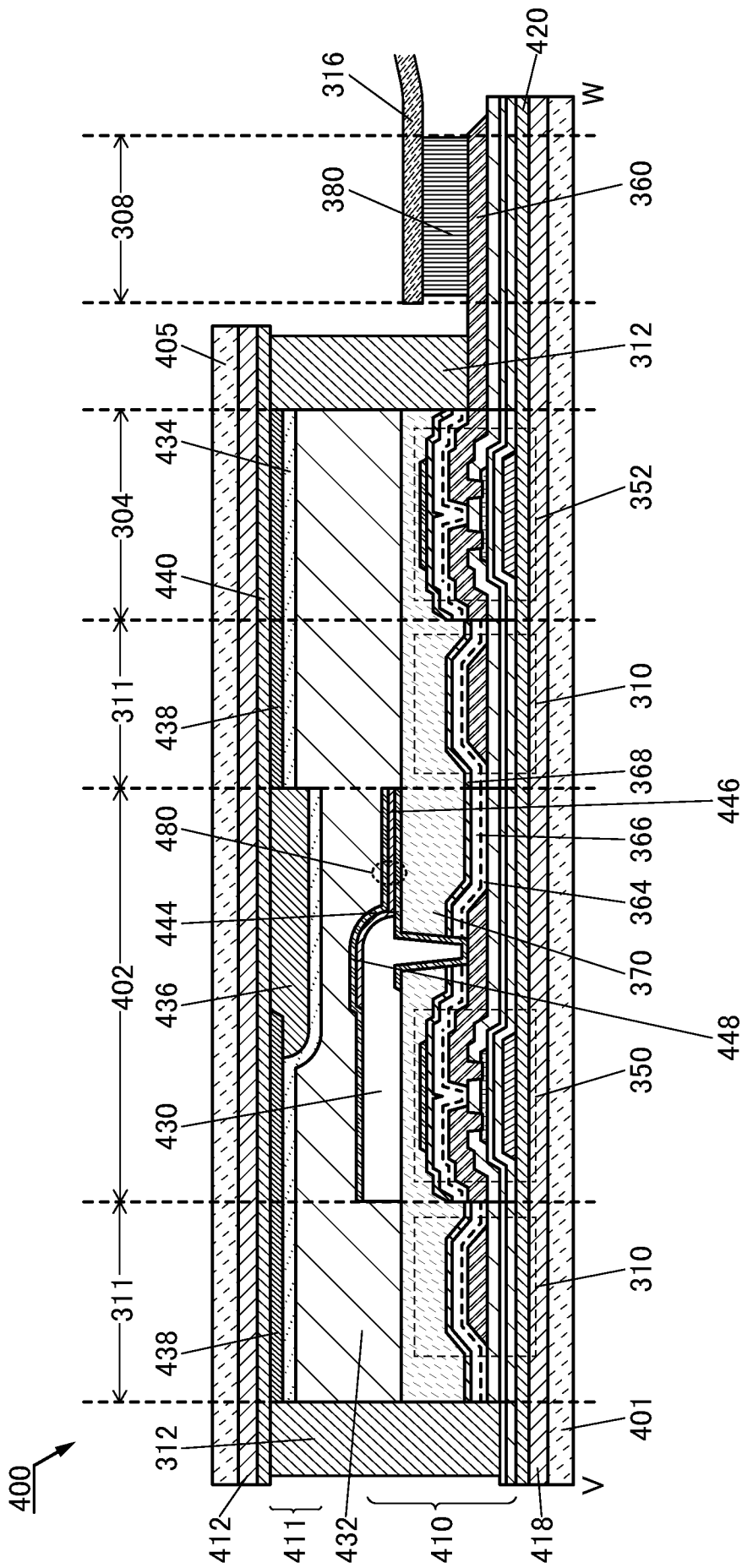


FIG. 48

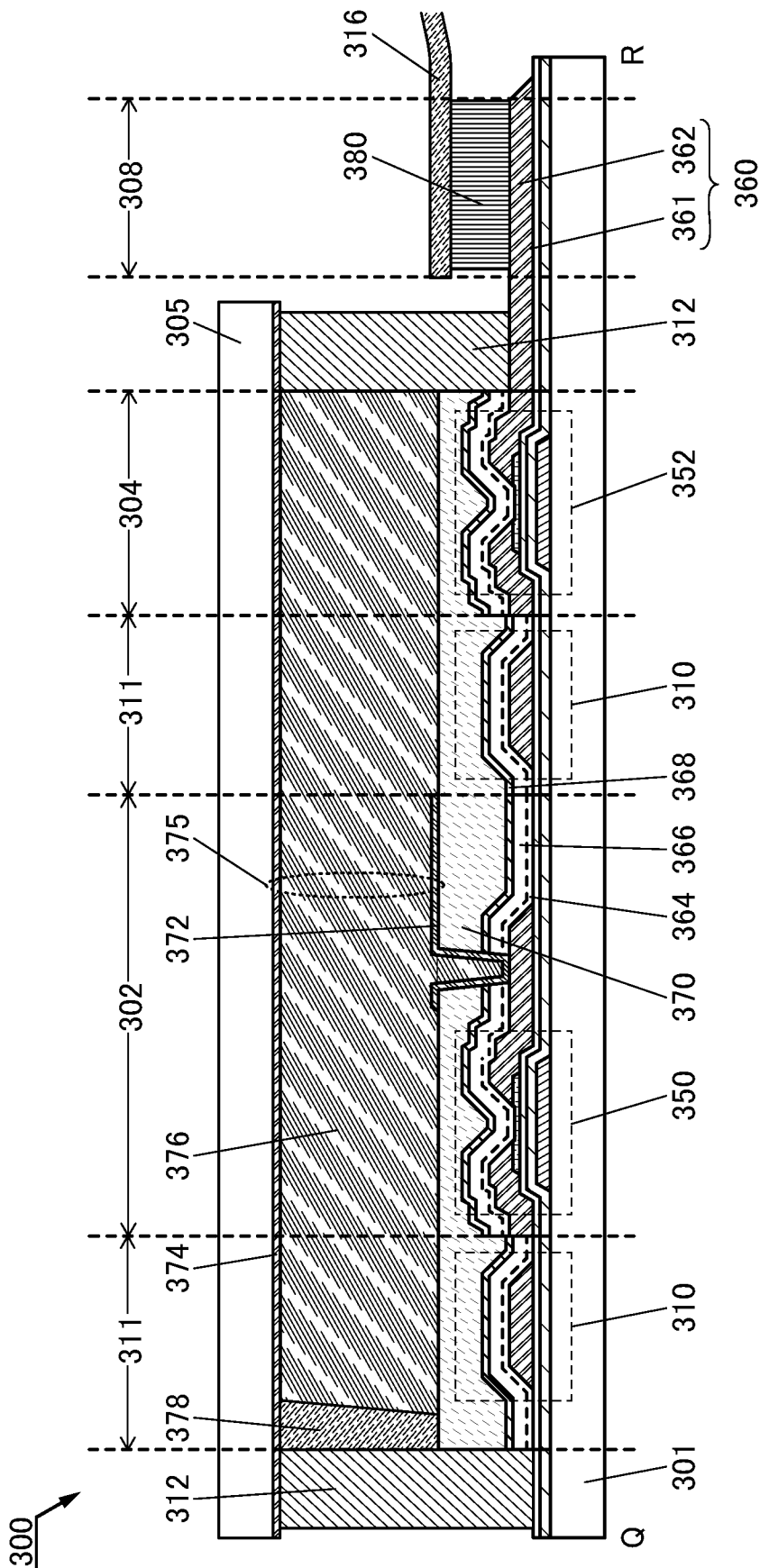


FIG. 50A

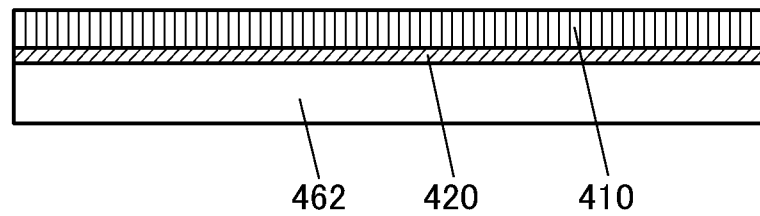


FIG. 50B

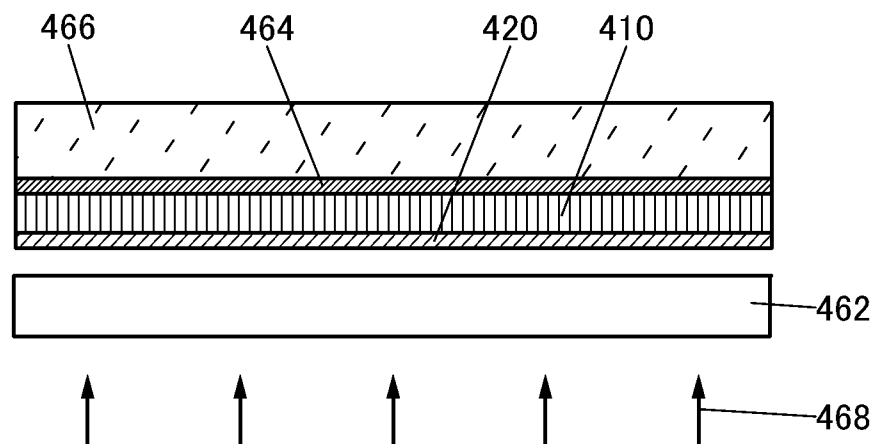


FIG. 50C

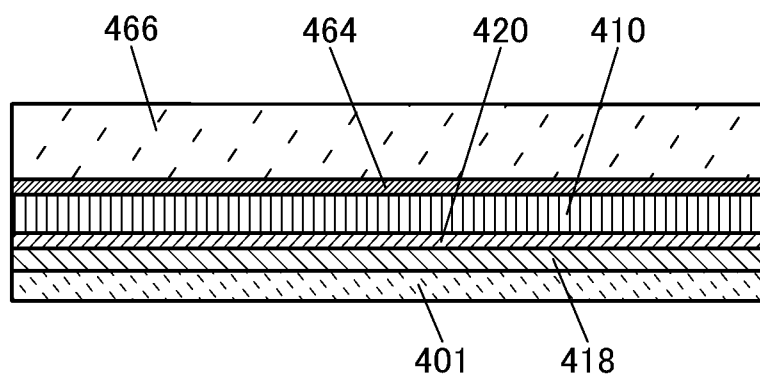


FIG. 50D

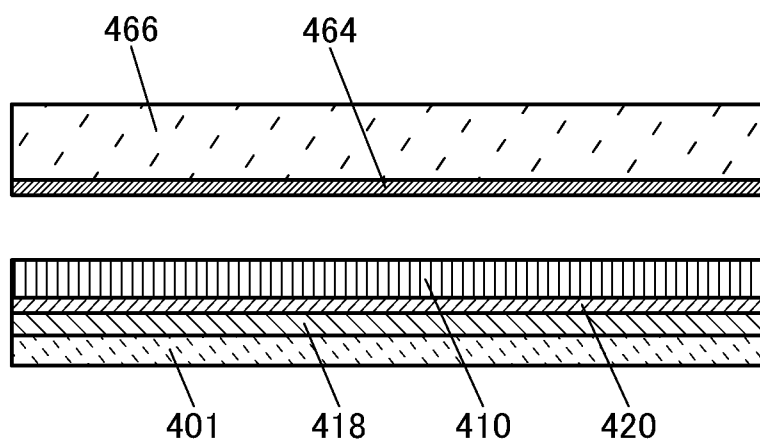


FIG. 51A

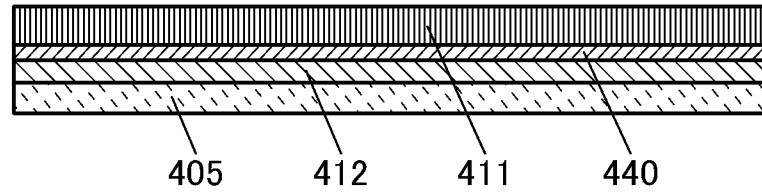


FIG. 51B

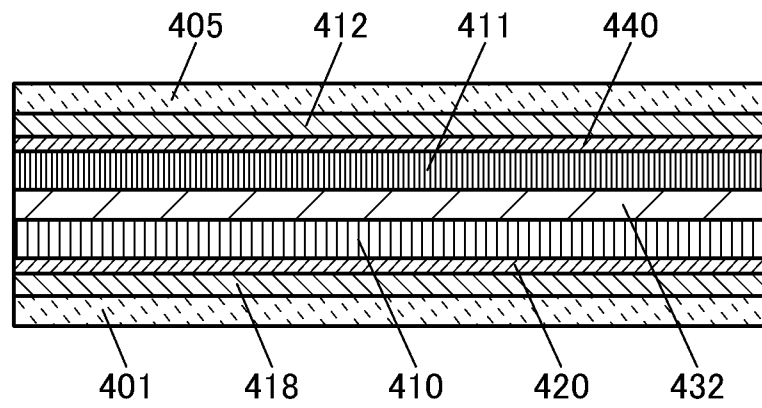


FIG. 52A

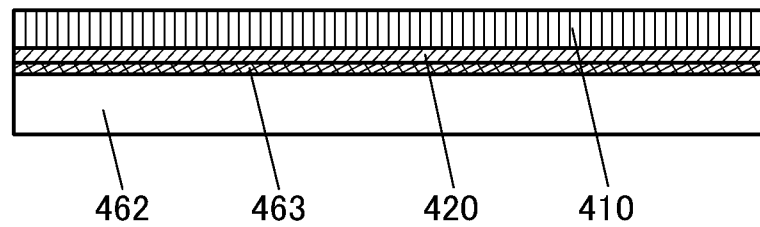


FIG. 52B

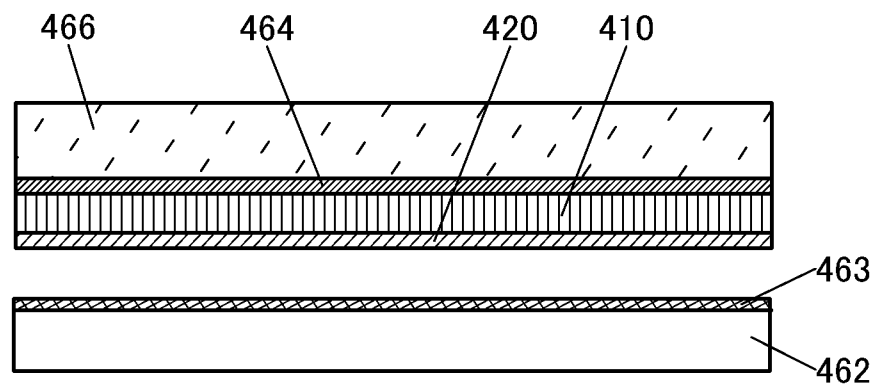


FIG. 52C

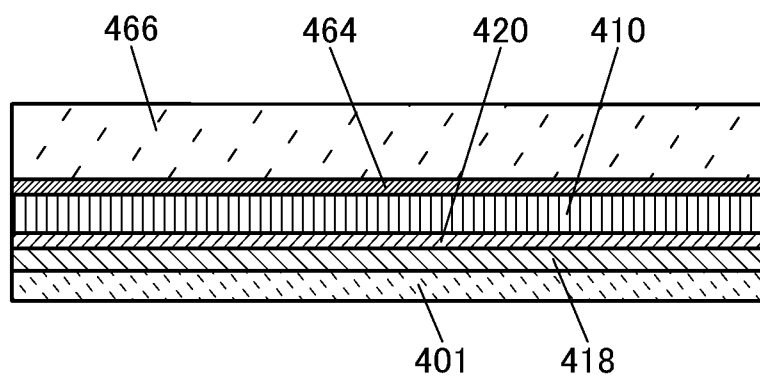


FIG. 52D

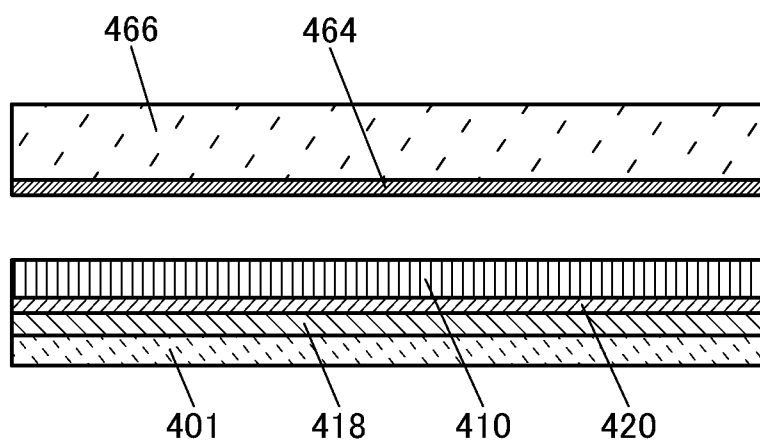


FIG. 53

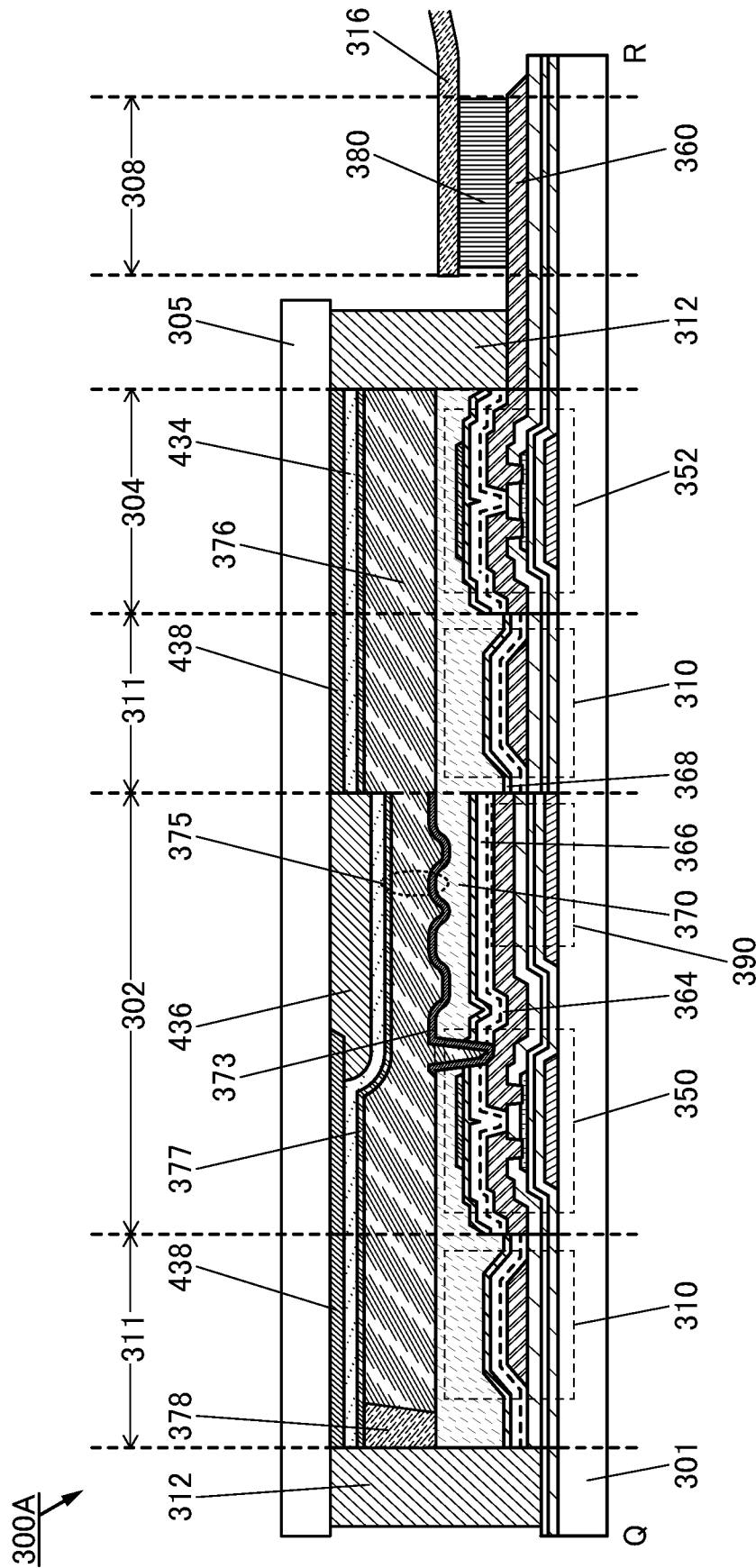


FIG. 54

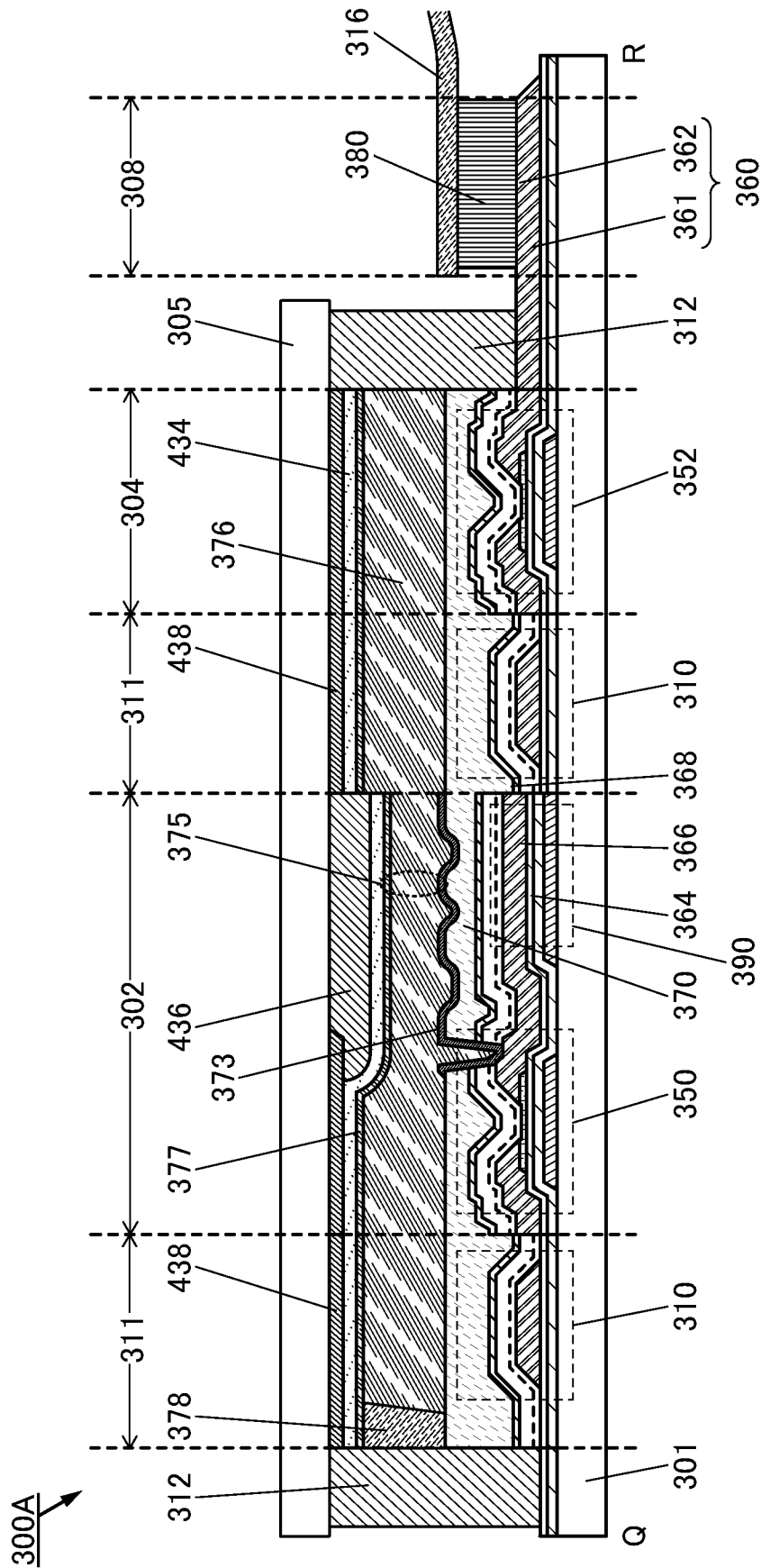


FIG. 55A

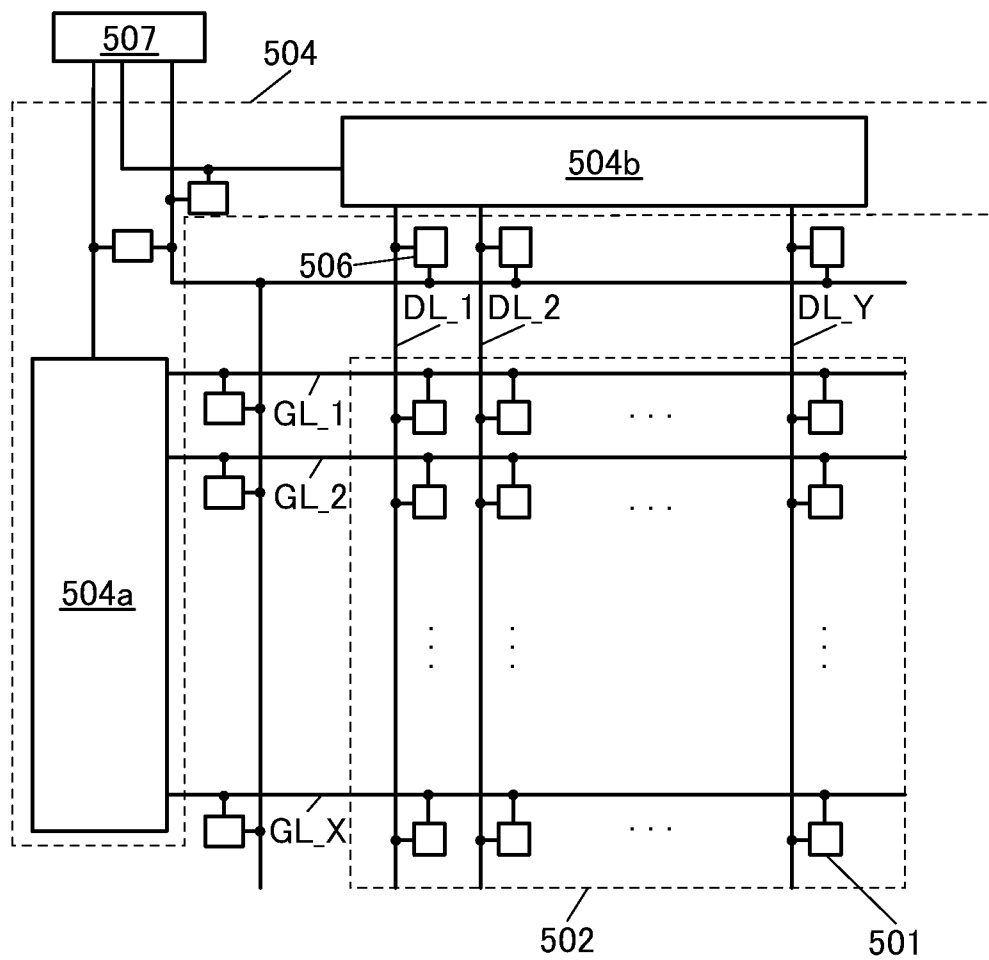


FIG. 55B

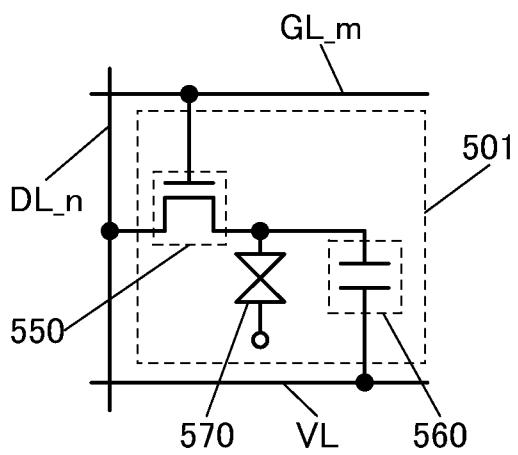


FIG. 55C

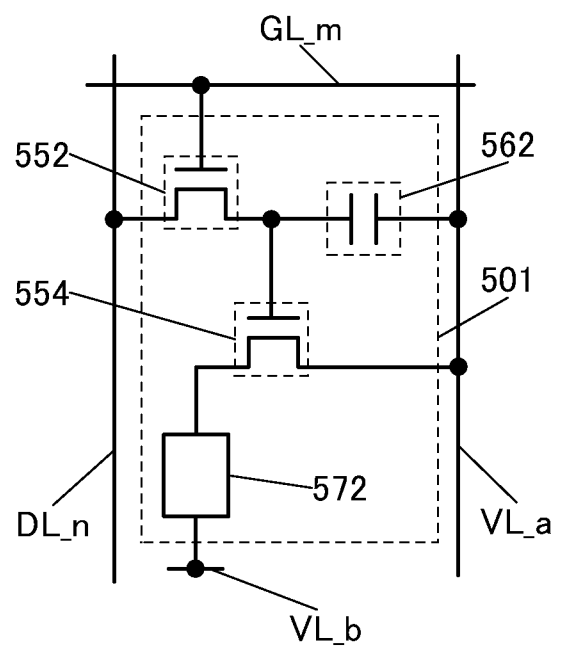


FIG. 56

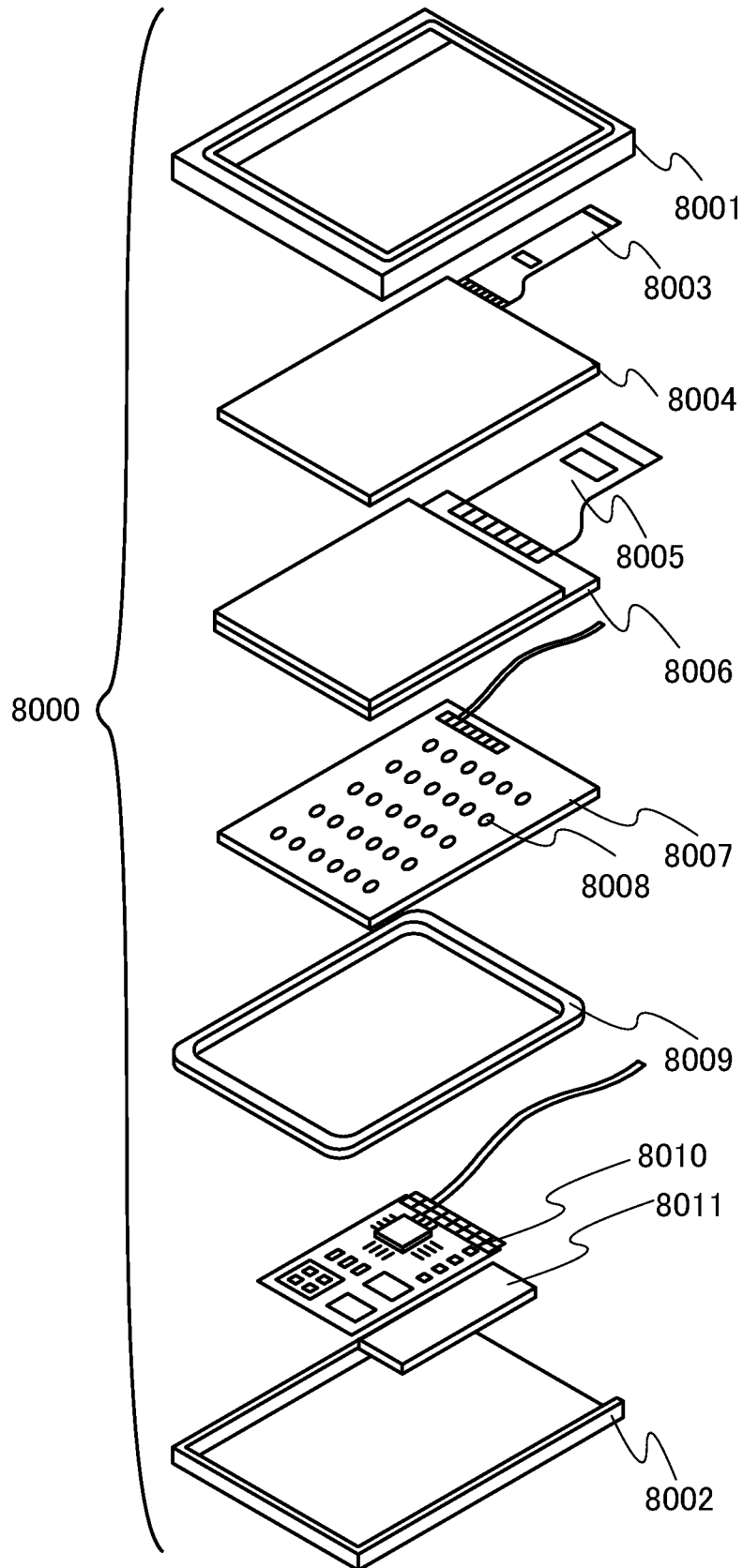


FIG. 57A

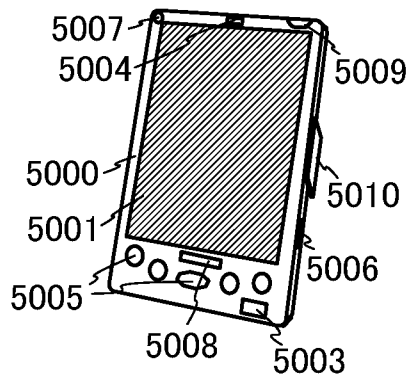


FIG. 57B

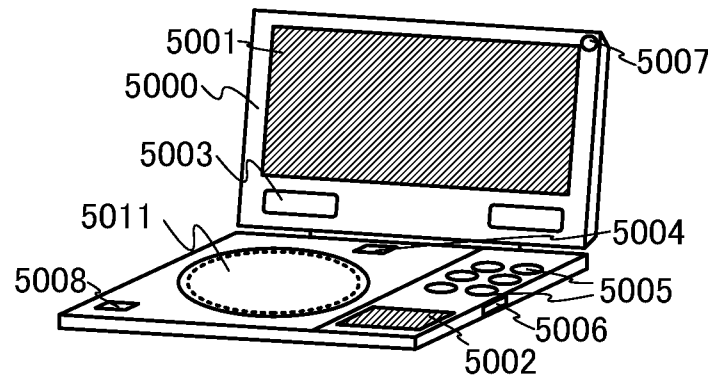


FIG. 57C

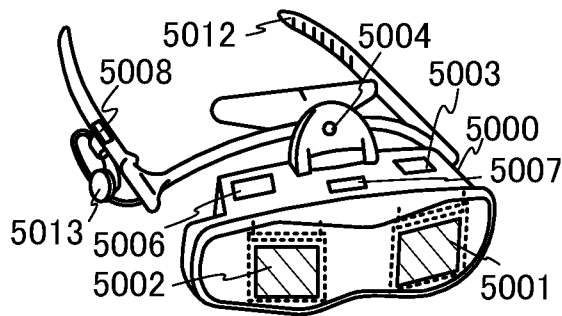


FIG. 57D

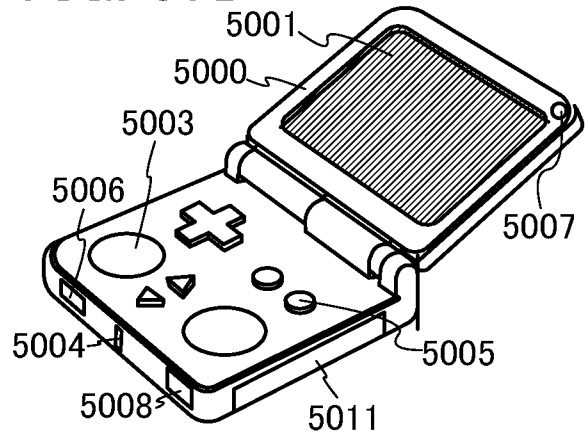


FIG. 57E

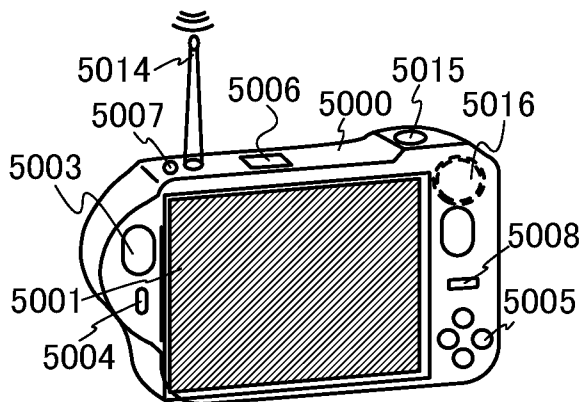


FIG. 57F

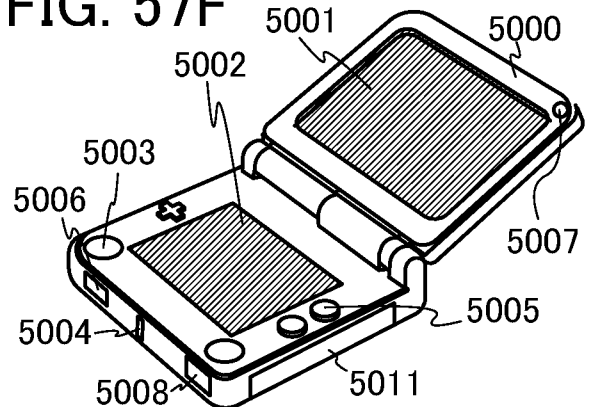


FIG. 57G

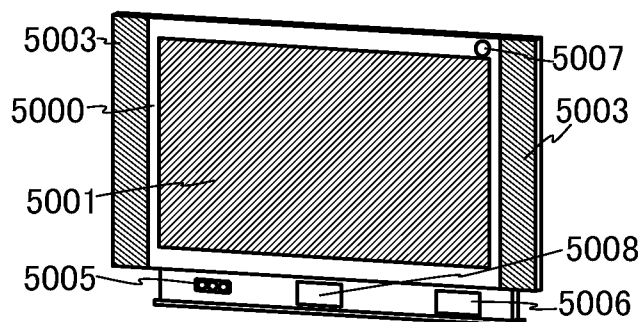


FIG. 57H

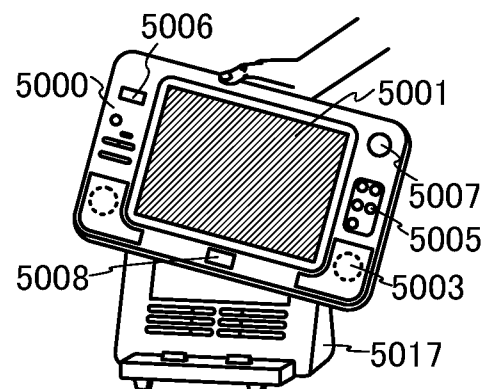


FIG. 58

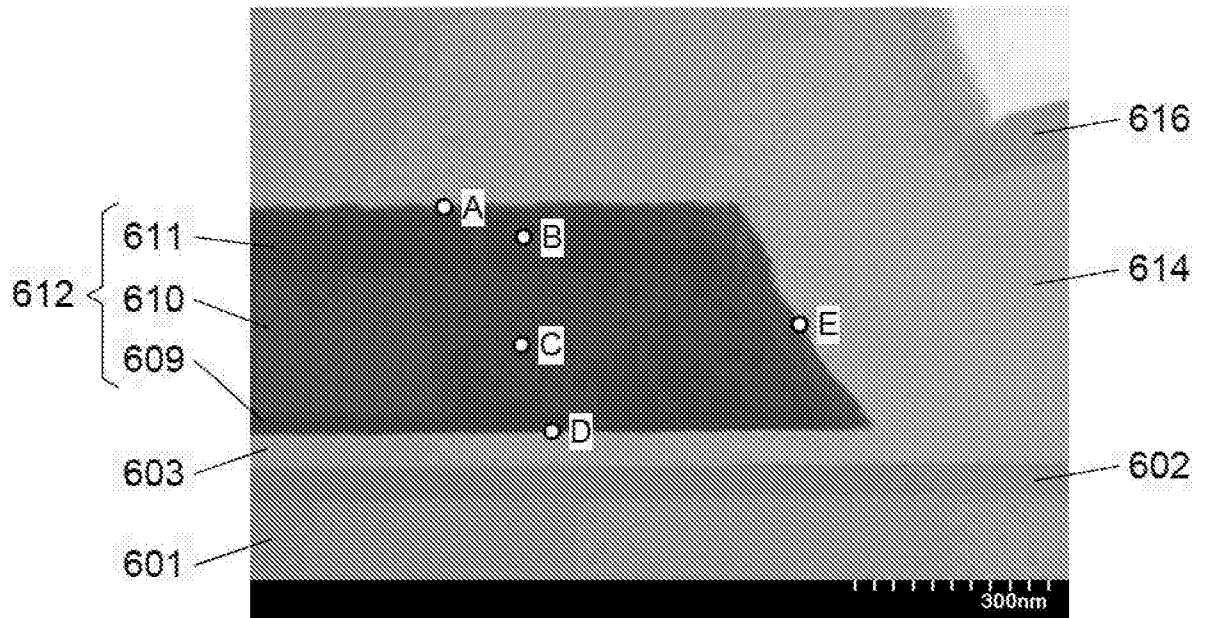


FIG. 59

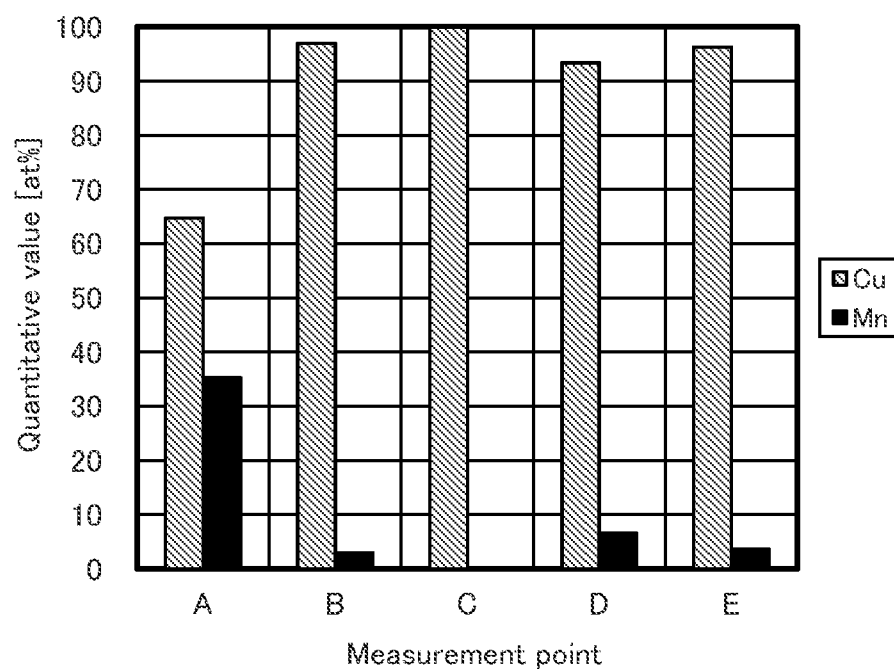


FIG. 60

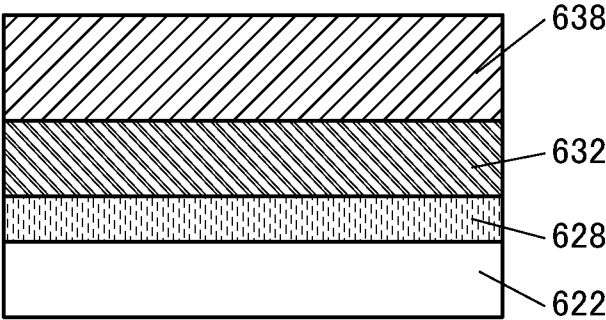
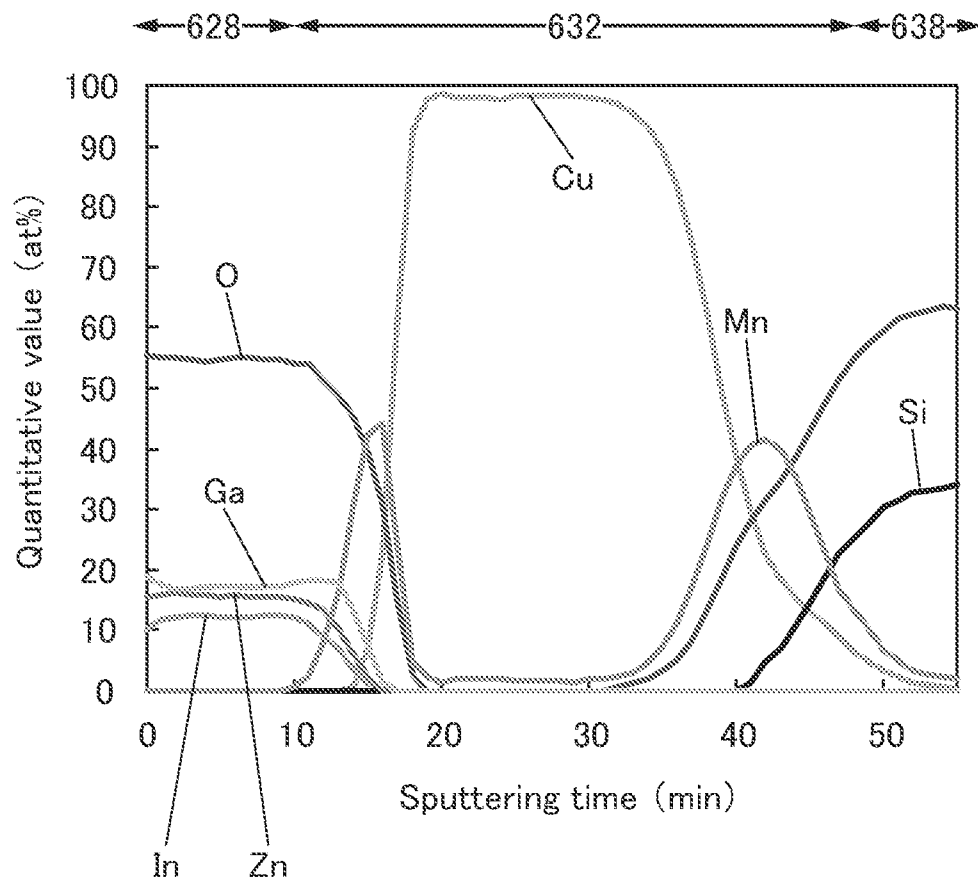


FIG. 61



INTERNATIONAL SEARCH REPORT

International application No.

PCT/IB2014/066146

A. CLASSIFICATION OF SUBJECT MATTER			
Int.Cl. H01L29/786(2006.01)i, H01L21/28(2006.01)i, H01L29/417(2006.01)i, H01L51/50(2006.01)i			
According to International Patent Classification (IPC) or to both national classification and IPC			
B. FIELDS SEARCHED			
Minimum documentation searched (classification system followed by classification symbols)			
Int.Cl. H01L29/786, H01L21/28, H01L29/417, H01L51/50			
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched			
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2015 Registered utility model specifications of Japan 1996-2015 Published registered utility model applications of Japan 1994-2015			
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)			
C. DOCUMENTS CONSIDERED TO BE RELEVANT			
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.	
Y	JP 2013-153093 A (Hitachi Cable, Ltd.) 2013.08.08, pars.0067-0076, figs.5, 6 & CN 103227206 A & KR 10-2013-0086910 A	1-31	
Y	JP 2011-181913 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.09.15, pars.0122-0133, fig.5 & US 2011/0193077 A1 & WO 2011/096263 A1 & TW 201203544 A & KR 10-2012-0117914 A	1-22	
Y	JP 2011-049539 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2011.03.10, fig.3 & US 2011/0024751 A1 & WO 2011/013596 A1 & CN 102473734 A & KR 10-2012-0051720 A & TW 201133858 A	2, 12	
☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.			
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family			
Date of the actual completion of the international search		Date of mailing of the international search report	
04.03.2015		17.03.2015	
Name and mailing address of the ISA/JP		Authorized officer	
Japan Patent Office		IWAMOTO, Tsutomu	
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan		Telephone No. +81-3-3581-1101 Ext. 3516	

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB2014/066146

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2013/168624 A1 (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2013.11.14, pars.0066-0131, figs.2, 3 & JP 2013-254950 A & US 2013/0299819 A1 & TW 201401514 A	11-22, 31
Y	JP 2013-179290 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2013.09.09, par.0116, figs.2, 3 & US 2013/0207111 A1 & KR 10-2013-0092463 A & TW 201338174 A	23-31
Y	WO 2012/017584 A1 (SHARP KABUSHIKI KAISHA) 2012.02.09, pars.0059, 0072-0073, figs.9, 14 & JP 5269254 B & US 2013/0208205 A1 & CN 103053027 A & KR 10-2013-0069731 A	23-31
Y	JP 2008-182055 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2008.08.07, par.0115, fig.3 (No Family)	30