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(71) Applicant: **QUALCOMM MEMS TECHNOLOGIES, INC.** [US/US]; 5775 Morehouse Drive, San Diego, California 92121-1714 (US).

(72) Inventors: **LASITER, Jon Bradley**; 5775 Morehouse Drive, San Diego, California 92121 (US). **SHENOY, Ravindra V.**; 5775 Morehouse Drive, San Diego, Califor-

nia 92121 (US). **BLACK, Justin Phelps**; 5775 Morehouse Drive, San Diego, California 92121 (US). **KIDWELL, Donald William**; P.O. Box 320941, Los Gatos, California 95032 (US).

(74) Agents: **GRIFFITH, John F.** et al.; Weaver Austin Villeneuve & Sampson LLP, P.O. Box 70250, Oakland, California 94612-0250 (US).

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(54) Title: HIGH CAPACITANCE DENSITY METAL-INSULATOR-METAL CAPACITORS

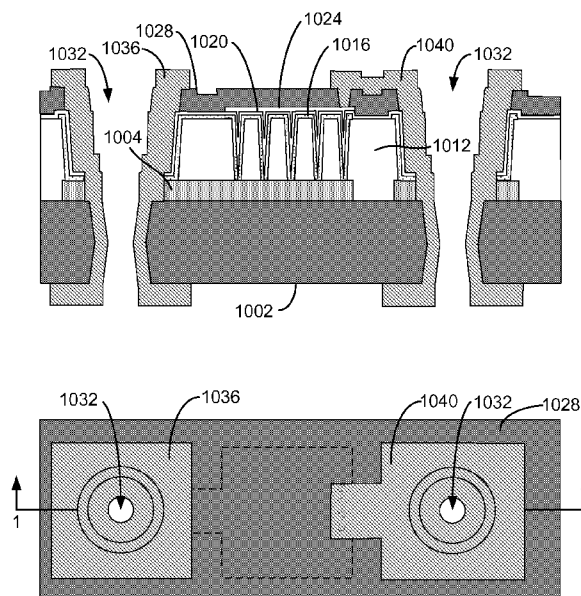


FIGURE 10H

(57) Abstract: This disclosure provides systems, methods and apparatus comprising high capacitance density metal-insulator-metal capacitors. In one aspect, an apparatus includes a first base metal layer (1004) on a first side of a substrate (1002). A first polymer layer (1012) is disposed on the first base metal layer and on the first side of the substrate. The first polymer layer defines a first plurality of vias (1014) through the first polymer layer, the first plurality of vias exposing portions of the first base metal layer. A first electrode layer (1016) is disposed on the first polymer layer. The first electrode layer contacts the portions of the first base metal layer. A first dielectric layer (1020) is disposed on the first electrode layer. A second electrode layer (1024) is disposed on the first dielectric layer. The first dielectric layer electrically isolates the first electrode layer from the second electrode layer.



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HIGH CAPACITANCE DENSITY METAL-INSULATOR-METAL CAPACITORS

CROSS-REFERENCE TO RELATED APPLICATIONS

5 **[0001]** This patent document claims priority to co-pending U.S. Patent Application No. 13/454,949, filed April 24, 2012, entitled “HIGH CAPACITANCE DENSITY METAL-INSULATOR-METAL CAPACITORS,” by Lasiter et al. (Attorney Docket No. QUALP113/111481), which claims priority to U.S. Provisional Patent Application No. 61/611,703, filed March 16, 2012, entitled “HIGH
10 CAPACITANCE DENSITY METAL-INSULATOR-METAL CAPACITORS,” by Lasiter et al. (Attorney Docket No. QUALP113P/111481P1). The disclosures of these prior applications are considered part of, and are hereby incorporated by reference in, this patent document.

15 TECHNICAL FIELD

[0002] This disclosure relates generally to capacitor devices and more particularly to high capacitance density metal-insulator-metal capacitor devices.

DESCRIPTION OF THE RELATED TECHNOLOGY

20 [0003] Electromechanical systems (EMS) include devices having electrical and mechanical elements, actuators, transducers, sensors, optical components (including mirrors) and electronics. Electromechanical systems can be manufactured at a variety of scales including, but not limited to, microscales and nanoscales. For example, microelectromechanical systems (MEMS) devices can include structures having sizes

25 ranging from about a micron to hundreds of microns or more. Nanoelectromechanical systems (NEMS) devices can include structures having sizes smaller than a micron including, for example, sizes smaller than several hundred nanometers.

Electromechanical elements may be created using deposition, etching, lithography, and/or other micromachining processes that etch away parts of substrates and/or

30 deposited material layers, or that add layers to form electrical and electromechanical devices.

[0004] One type of EMS device is called an interferometric modulator (IMOD). As used herein, the term interferometric modulator or interferometric light modulator

refers to a device that selectively absorbs and/or reflects light using the principles of optical interference. In some implementations, an interferometric modulator may include a pair of conductive plates, one or both of which may be transparent and/or reflective, wholly or in part, and capable of relative motion upon application of an appropriate electrical signal. In an implementation, one plate may include a stationary layer deposited on a substrate and the other plate may include a reflective membrane separated from the stationary layer by an air gap. The position of one plate in relation to another can change the optical interference of light incident on the interferometric modulator. Interferometric modulator devices have a wide range of applications, and are anticipated to be used in improving existing products and creating new products, especially those with display capabilities.

[0005] Capacitor devices or capacitors may be used in implementations of EMS devices and/or associated with systems in which EMS devices are implemented. One type of capacitor device, for example, is a metal-insulator-metal (MIM) capacitor. With smaller capacitors, an increase in the capacitance density compared to larger capacitors may be used to supply the same capacitance as a larger capacitor.

SUMMARY

[0006] The systems, methods and devices of the disclosure each have several innovative aspects, no single one of which is solely responsible for the desirable attributes disclosed herein.

[0007] One innovative aspect of the subject matter described in this disclosure can be implemented in an apparatus including a first base metal layer on a first side of a substrate. A first polymer layer may be disposed on the first base metal layer and on the first side of the substrate. The first polymer layer may define a first plurality of vias through the first polymer layer, the vias exposing portions of the first base metal layer. A first electrode layer may be disposed on the first polymer layer. The first electrode layer may contact the portions of the first base metal layer. A first dielectric layer may be disposed on the first electrode layer. A second electrode layer may be disposed on the first dielectric layer. The first dielectric layer may electrically isolate the first electrode layer from the second electrode layer.

[0008] In some implementations, a first via of the first plurality of vias in the first polymer layer may have an aspect ratio of at least about 10 to 1. In some implementations, the apparatus may further include a second base metal layer on a

second side of the substrate. A second polymer layer may be disposed on the second base metal layer and on the second side of the substrate. The second polymer layer may define a second plurality of vias through the second polymer layer, the vias exposing portions of the second base metal layer. A third electrode layer may be disposed on the second polymer layer. The third electrode layer may contact the portions of the second base metal layer. A second dielectric layer may be disposed on the third electrode layer. A fourth electrode layer may be disposed on the second dielectric layer. The second dielectric layer may electrically isolate the third electrode layer from the fourth electrode layer. A first connection may electrically connect the first and the third electrode layers. A second connection may electrically connect the second and the fourth electrode layers.

[0009] Another innovative aspect of the subject matter described in this disclosure can be implemented an apparatus including a base metal layer on a substrate. A polymer layer may be disposed on the base metal layer and on the substrate. A first electrode layer may be disposed on the polymer layer. The apparatus further includes a second electrode layer, a means for exposing portions of the base metal layer, and a means for electrically isolating the first electrode layer from the second electrode layer. The first electrode layer may contact the portions of the base metal layer.

[0010] In some implementations, the means for exposing portions of the base metal layer may increase a surface area between the first electrode layer and the second electrode layer. In some implementations, the base metal layer may reduce the equivalent series resistance of the apparatus.

[0011] Another innovative aspect of the subject matter described in this disclosure can be implemented in a method including depositing a base metal layer on a surface of a substrate. A polymer layer may be formed on the base metal layer and on the surface of the substrate. A process may be used to pattern a design in the polymer layer. A first electrode layer may be deposited on the polymer layer and on exposed portions of the base metal layer. A dielectric layer may be deposited on the first electrode layer. A second electrode layer may be deposited on the dielectric layer.

[0012] In some implementations, the process used to pattern the design in the polymer layer may be a nanoimprinting process. The nanoimprinting process may include heating the polymer layer, pressing a mold into the polymer layer, cooling the polymer layer, and removing the mold from the polymer layer. Alternatively, the nanoimprinting process may include heating the polymer layer, pressing a mold into

the polymer layer, treating the polymer layer with an ultraviolet light, and removing the mold from the polymer layer.

[0013] Details of one or more implementations of the subject matter described in this specification are set forth in the accompanying drawings and the description
5 below. Although the examples provided in this disclosure are primarily described in terms of electromechanical systems (EMS) and microelectromechanical systems (MEMS)-based displays, the concepts provided herein may apply to other types of displays, such as liquid crystal displays, organic light-emitting diode (“OLED”) displays and field emission displays. Other features, aspects, and advantages will
10 become apparent from the description, the drawings and the claims. Note that the relative dimensions of the following figures may not be drawn to scale.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 shows an example of an isometric view depicting two adjacent
15 pixels in a series of pixels of an interferometric modulator (IMOD) display device.

[0015] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display.

[0016] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1.

20 [0017] Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied.

[0018] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2.

[0019] Figure 5B shows an example of a timing diagram for common and
25 segment signals that may be used to write the frame of display data illustrated in Figure 5A.

[0020] Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1.

[0021] Figures 6B–6E show examples of cross-sections of varying
30 implementations of interferometric modulators.

[0022] Figure 7 shows an example of a flow diagram illustrating a manufacturing process for an interferometric modulator.

[0023] Figures 8A–8E show examples of cross-sectional schematic illustrations of various stages in a method of making an interferometric modulator.

- [0024] Figures 9A and 9B show examples of flow diagrams illustrating a manufacturing process for forming a MIM capacitor.
- [0025] Figures 10A–10H show examples of schematic illustrations of a MIM capacitor at various stages in the manufacturing process.
- 5 [0026] Figures 11A–11D show examples of schematic illustrations of vias in a polymer layer and a portion of a mold that may be used to form vias.
- [0027] Figure 12 shows an example of a cross-sectional schematic illustration of an assembly including a MIM capacitor on both sides of a substrate.
- [0028] Figure 13 shows an example of a cross-sectional schematic illustration of a
10 MIM capacitor.
- [0029] Figure 14 shows an example of a cross-sectional schematic illustration of a metal-insulator-metal-insulator-metal (MIMIM) capacitor.
- [0030] Figures 15A and 15B show examples of system block diagrams illustrating a display device that includes a plurality of interferometric modulators.
- 15 [0031] Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

- [0032] The following description is directed to certain implementations for the
20 purposes of describing the innovative aspects of this disclosure. However, a person having ordinary skill in the art will readily recognize that the teachings herein can be applied in a multitude of different ways. The described implementations may be implemented in any device or system that can be configured to display an image, whether in motion (e.g., video) or stationary (e.g., still image), and whether textual,
25 graphical or pictorial. More particularly, it is contemplated that the described implementations may be included in or associated with a variety of electronic devices such as, but not limited to: mobile telephones, multimedia Internet enabled cellular telephones, mobile television receivers, wireless devices, smartphones, Bluetooth® devices, personal data assistants (PDAs), wireless electronic mail receivers, hand-held
30 or portable computers, netbooks, notebooks, smartbooks, tablets, printers, copiers, scanners, facsimile devices, GPS receivers/navigators, cameras, MP3 players, camcorders, game consoles, wrist watches, clocks, calculators, television monitors, flat panel displays, electronic reading devices (i.e., e-readers), computer monitors, auto displays (including odometer and speedometer displays, etc.), cockpit controls

and/or displays, camera view displays (such as the display of a rear view camera in a vehicle), electronic photographs, electronic billboards or signs, projectors, architectural structures, microwaves, refrigerators, stereo systems, cassette recorders or players, DVD players, CD players, VCRs, radios, portable memory chips, washers, 5 dryers, washer/dryers, parking meters, packaging (such as in electromechanical systems (EMS), microelectromechanical systems (MEMS) and non-MEMS applications), aesthetic structures (e.g., display of images on a piece of jewelry) and a variety of EMS devices. The teachings herein also can be used in non-display applications such as, but not limited to, electronic switching devices, radio frequency 10 filters, sensors, accelerometers, gyroscopes, motion-sensing devices, magnetometers, inertial components for consumer electronics, parts of consumer electronics products, varactors, liquid crystal devices, electrophoretic devices, drive schemes, manufacturing processes and electronic test equipment. Thus, the teachings are not intended to be limited to the implementations depicted solely in the Figures, but 15 instead have wide applicability as will be readily apparent to one having ordinary skill in the art.

[0033] Some implementations described herein relate to high capacitance density metal-insulator-metal (MIM) capacitors. For example, a MIM capacitor may include two metal layers separated by a dielectric layer. A base metal layer in electrical 20 contact with one of the two metal layers may serve to decrease the equivalent series resistance (ESR) of the MIM capacitor.

[0034] For example, in some implementations described herein, a MIM capacitor may include a first base metal layer on a first side of a substrate. A first polymer layer may be disposed on the first base metal layer and on the first side of the 25 substrate. The first polymer layer may define a first plurality of vias through the first polymer layer, the first plurality of vias exposing portions of the first base metal layer. A first electrode layer may be disposed on the first polymer layer. The first electrode layer may contact the portions of the first base metal layer. A first dielectric layer may be disposed on the first electrode layer. A second electrode layer may be 30 disposed on the first dielectric layer. The first dielectric layer may electrically isolate the first electrode layer from the second electrode layer.

[0035] Particular implementations of the subject matter described in this disclosure can be implemented to realize one or more of the following potential advantages. In some implementations, a base metal layer may decrease the ESR of a

MIM capacitor. In some implementations, a polymer layer including vias may increase the surface areas of the electrodes, thus increasing the capacitance density of a MIM capacitor. In some implementations, these features may be combined, yielding a MIM capacitor having a high capacitance density with a low ESR. In some implementations, a substrate on which a MIM capacitor is disposed may function as an interposer. With the MIM capacitor disposed on the substrate functioning as an interposer, the distance of the MIM capacitor from electronic components (e.g., an integrated circuit and a printed circuit board) that the interposer is interconnecting may be reduced, which may reduce the signal to noise ratio.

- 10 **[0036]** An example of a suitable EMS or MEMS device, to which the described implementations may apply, is a reflective display device. Reflective display devices can incorporate interferometric modulators (IMODs) to selectively absorb and/or reflect light incident thereon using principles of optical interference. IMODs can include an absorber, a reflector that is movable with respect to the absorber, and an optical resonant cavity defined between the absorber and the reflector. The reflector can be moved to two or more different positions, which can change the size of the optical resonant cavity and thereby affect the reflectance of the interferometric modulator. The reflectance spectrums of IMODs can create fairly broad spectral bands which can be shifted across the visible wavelengths to generate different colors.
- 15 The position of the spectral band can be adjusted by changing the thickness of the optical resonant cavity, i.e., by changing the position of the reflector.

- 20 **[0037]** Figure 1 shows an example of an isometric view depicting two adjacent pixels in a series of pixels of an interferometric modulator (IMOD) display device. The IMOD display device includes one or more interferometric MEMS display elements. In these devices, the pixels of the MEMS display elements can be in either a bright or dark state. In the bright (“relaxed,” “open” or “on”) state, the display element reflects a large portion of incident visible light, e.g., to a user. Conversely, in the dark (“actuated,” “closed” or “off”) state, the display element reflects little incident visible light. In some implementations, the light reflectance properties of the on and off states may be reversed. MEMS pixels can be configured to reflect predominantly at particular wavelengths allowing for a color display in addition to black and white.

- 30 **[0038]** The IMOD display device can include a row/column array of IMODs. Each IMOD can include a pair of reflective layers, i.e., a movable reflective layer and

a fixed partially reflective layer, positioned at a variable and controllable distance from each other to form an air gap (also referred to as an optical gap or cavity). The movable reflective layer may be moved between at least two positions. In a first position, i.e., a relaxed position, the movable reflective layer can be positioned at a relatively large distance from the fixed partially reflective layer. In a second position, i.e., an actuated position, the movable reflective layer can be positioned more closely to the partially reflective layer. Incident light that reflects from the two layers can interfere constructively or destructively depending on the position of the movable reflective layer, producing either an overall reflective or non-reflective state for each pixel. In some implementations, the IMOD may be in a reflective state when unactuated, reflecting light within the visible spectrum, and may be in a dark state when unactuated, reflecting light outside of the visible range (e.g., infrared light). In some other implementations, however, an IMOD may be in a dark state when unactuated, and in a reflective state when actuated. In some implementations, the introduction of an applied voltage can drive the pixels to change states. In some other implementations, an applied charge can drive the pixels to change states.

[0039] The depicted portion of the pixel array in Figure 1 includes two adjacent interferometric modulators 12. In the IMOD 12 on the left (as illustrated), a movable reflective layer 14 is illustrated in a relaxed position at a predetermined distance from an optical stack 16, which includes a partially reflective layer. The voltage V_0 applied across the IMOD 12 on the left is insufficient to cause actuation of the movable reflective layer 14. In the IMOD 12 on the right, the movable reflective layer 14 is illustrated in an actuated position near or adjacent the optical stack 16. The voltage V_{bias} applied across the IMOD 12 on the right is sufficient to maintain the movable reflective layer 14 in the actuated position.

[0040] In Figure 1, the reflective properties of pixels 12 are generally illustrated with arrows 13 indicating light incident upon the pixels 12, and light 15 reflecting from the IMOD 12 on the left. Although not illustrated in detail, it will be understood by one having ordinary skill in the art that most of the light 13 incident upon the pixels 12 will be transmitted through the transparent substrate 20, toward the optical stack 16. A portion of the light incident upon the optical stack 16 will be transmitted through the partially reflective layer of the optical stack 16, and a portion will be reflected back through the transparent substrate 20. The portion of light 13 that is transmitted through the optical stack 16 will be reflected at the movable reflective

layer 14, back toward (and through) the transparent substrate 20. Interference (constructive or destructive) between the light reflected from the partially reflective layer of the optical stack 16 and the light reflected from the movable reflective layer 14 will determine the wavelength(s) of light 15 reflected from the IMOD 12.

5 **[0041]** The optical stack 16 can include a single layer or several layers. The layer(s) can include one or more of an electrode layer, a partially reflective and partially transmissive layer and a transparent dielectric layer. In some implementations, the optical stack 16 is electrically conductive, partially transparent and partially reflective, and may be fabricated, for example, by depositing one or
10 more of the above layers onto a transparent substrate 20. The electrode layer can be formed from a variety of materials, such as various metals, for example indium tin oxide (ITO). The partially reflective layer can be formed from a variety of materials that are partially reflective, such as various metals, e.g., chromium (Cr), semiconductors, and dielectrics. The partially reflective layer can be formed of one or
15 more layers of materials, and each of the layers can be formed of a single material or a combination of materials. In some implementations, the optical stack 16 can include a single semi-transparent thickness of metal or semiconductor which serves as both an optical absorber and conductor, while different, more conductive layers or portions (e.g., of the optical stack 16 or of other structures of the IMOD) can serve to bus
20 signals between IMOD pixels. The optical stack 16 also can include one or more insulating or dielectric layers covering one or more conductive layers or a conductive/absorptive layer.

[0042] In some implementations, the layer(s) of the optical stack 16 can be patterned into parallel strips, and may form row electrodes in a display device as
25 described further below. As will be understood by one having ordinary skill in the art, the term “patterned” is used herein to refer to masking as well as etching processes. In some implementations, a highly conductive and reflective material, such as aluminum (Al), may be used for the movable reflective layer 14, and these strips may form column electrodes in a display device. The movable reflective layer
30 14 may be formed as a series of parallel strips of a deposited metal layer or layers (orthogonal to the row electrodes of the optical stack 16) to form columns deposited on top of posts 18 and an intervening sacrificial material deposited between the posts 18. When the sacrificial material is etched away, a defined gap 19, or optical cavity, can be formed between the movable reflective layer 14 and the optical stack 16. In

some implementations, the spacing between posts 18 may be approximately 1–1000 μm , while the gap 19 may be less than 10,000 Angstroms ($\text{\AA}$).

[0043] In some implementations, each pixel of the IMOD, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers. When no voltage is applied, the movable reflective layer 14 remains in a mechanically relaxed state, as illustrated by the IMOD 12 on the left in Figure 1, with the gap 19 between the movable reflective layer 14 and optical stack 16. However, when a potential difference, e.g., voltage, is applied to at least one of a selected row and column, the capacitor formed at the intersection of the row and column electrodes at the corresponding pixel becomes charged, and electrostatic forces pull the electrodes together. If the applied voltage exceeds a threshold, the movable reflective layer 14 can deform and move near or against the optical stack 16. A dielectric layer (not shown) within the optical stack 16 may prevent shorting and control the separation distance between the layers 14 and 16, as illustrated by the actuated IMOD 12 on the right in Figure 1. The behavior is the same regardless of the polarity of the applied potential difference. Though a series of pixels in an array may be referred to in some instances as “rows” or “columns,” a person having ordinary skill in the art will readily understand that referring to one direction as a “row” and another as a “column” is arbitrary. Restated, in some orientations, the rows can be considered columns, and the columns considered to be rows. Furthermore, the display elements may be evenly arranged in orthogonal rows and columns (an “array”), or arranged in non-linear configurations, for example, having certain positional offsets with respect to one another (a “mosaic”). The terms “array” and “mosaic” may refer to either configuration. Thus, although the display is referred to as including an “array” or “mosaic,” the elements themselves need not be arranged orthogonally to one another, or disposed in an even distribution, in any instance, but may include arrangements having asymmetric shapes and unevenly distributed elements.

[0044] Figure 2 shows an example of a system block diagram illustrating an electronic device incorporating a 3x3 interferometric modulator display. The electronic device includes a processor 21 that may be configured to execute one or more software modules. In addition to executing an operating system, the processor 21 may be configured to execute one or more software applications, including a web browser, a telephone application, an email program, or other software application.

[0045] The processor 21 can be configured to communicate with an array driver

22. The array driver 22 can include a row driver circuit 24 and a column driver circuit 26 that provide signals to, e.g., a display array or panel 30. The cross section of the IMOD display device illustrated in Figure 1 is shown by the lines 1–1 in Figure 2.

Although Figure 2 illustrates a 3x3 array of IMODs for the sake of clarity, the display array 30 may contain a very large number of IMODs, and may have a different number of IMODs in rows than in columns, and vice versa.

[0046] Figure 3 shows an example of a diagram illustrating movable reflective layer position versus applied voltage for the interferometric modulator of Figure 1. For MEMS interferometric modulators, the row/column (i.e., common/segment) write procedure may take advantage of a hysteresis property of these devices as illustrated in Figure 3. An interferometric modulator may require, for example, about a 10-volt potential difference to cause the movable reflective layer, or mirror, to change from the relaxed state to the actuated state. When the voltage is reduced from that value, the movable reflective layer maintains its state as the voltage drops back below, e.g., 10 volts, however, the movable reflective layer does not relax completely until the voltage drops below 2 volts. Thus, a range of voltage, approximately 3 to 7 volts, as shown in Figure 3, exists where there is a window of applied voltage within which the device is stable in either the relaxed or actuated state. This is referred to herein as the “hysteresis window” or “stability window.” For a display array 30 having the hysteresis characteristics of Figure 3, the row/column write procedure can be designed to address one or more rows at a time, such that during the addressing of a given row, pixels in the addressed row that are to be actuated are exposed to a voltage difference of about 10 volts, and pixels that are to be relaxed are exposed to a voltage difference of near zero volts. After addressing, the pixels are exposed to a steady state or bias voltage difference of approximately 5-volts such that they remain in the previous strobing state. In this example, after being addressed, each pixel sees a potential difference within the “stability window” of about 3–7 volts. This hysteresis property feature enables the pixel design, e.g., illustrated in Figure 1, to remain stable in either an actuated or relaxed pre-existing state under the same applied voltage conditions. Since each IMOD pixel, whether in the actuated or relaxed state, is essentially a capacitor formed by the fixed and moving reflective layers, this stable state can be held at a steady voltage within the hysteresis window without substantially consuming or losing power. Moreover, essentially little or no current flows into the IMOD pixel if the applied voltage potential remains substantially fixed.

[0047] In some implementations, a frame of an image may be created by applying data signals in the form of “segment” voltages along the set of column electrodes, in accordance with the desired change (if any) to the state of the pixels in a given row. Each row of the array can be addressed in turn, such that the frame is written one row at a time. To write the desired data to the pixels in a first row, segment voltages corresponding to the desired state of the pixels in the first row can be applied on the column electrodes, and a first row pulse in the form of a specific “common” voltage or signal can be applied to the first row electrode. The set of segment voltages can then be changed to correspond to the desired change (if any) to the state of the pixels in the second row, and a second common voltage can be applied to the second row electrode. In some implementations, the pixels in the first row are unaffected by the change in the segment voltages applied along the column electrodes, and remain in the state they were set to during the first common voltage row pulse. This process may be repeated for the entire series of rows, or alternatively, columns, in a sequential fashion to produce the image frame. The frames can be refreshed and/or updated with new image data by continually repeating this process at some desired number of frames per second.

[0048] The combination of segment and common signals applied across each pixel (that is, the potential difference across each pixel) determines the resulting state of each pixel. Figure 4 shows an example of a table illustrating various states of an interferometric modulator when various common and segment voltages are applied. As will be readily understood by one having ordinary skill in the art, the “segment” voltages can be applied to either the column electrodes or the row electrodes, and the “common” voltages can be applied to the other of the column electrodes or the row electrodes.

[0049] As illustrated in Figure 4 (as well as in the timing diagram shown in Figure 5B), when a release voltage $V_{C_{REL}}$ is applied along a common line, all interferometric modulator elements along the common line will be placed in a relaxed state, alternatively referred to as a released or unactuated state, regardless of the voltage applied along the segment lines, i.e., high segment voltage V_{S_H} and low segment voltage V_{S_L} . In particular, when the release voltage $V_{C_{REL}}$ is applied along a common line, the potential voltage across the modulator (alternatively referred to as a pixel voltage) is within the relaxation window (see Figure 3, also referred to as a release window) both when the high segment voltage V_{S_H} and the low segment

voltage VS_L are applied along the corresponding segment line for that pixel.

[0050] When a hold voltage is applied on a common line, such as a high hold voltage VC_{HOLD_H} or a low hold voltage VC_{HOLD_L} , the state of the interferometric modulator will remain constant. For example, a relaxed IMOD will remain in a relaxed position, and an actuated IMOD will remain in an actuated position. The hold voltages can be selected such that the pixel voltage will remain within a stability window both when the high segment voltage VS_H and the low segment voltage VS_L are applied along the corresponding segment line. Thus, the segment voltage swing, i.e., the difference between the high VS_H and low segment voltage VS_L , is less than the width of either the positive or the negative stability window.

[0051] When an addressing, or actuation, voltage is applied on a common line, such as a high addressing voltage VC_{ADD_H} or a low addressing voltage VC_{ADD_L} , data can be selectively written to the modulators along that line by application of segment voltages along the respective segment lines. The segment voltages may be selected such that actuation is dependent upon the segment voltage applied. When an addressing voltage is applied along a common line, application of one segment voltage will result in a pixel voltage within a stability window, causing the pixel to remain unactuated. In contrast, application of the other segment voltage will result in a pixel voltage beyond the stability window, resulting in actuation of the pixel. The particular segment voltage which causes actuation can vary depending upon which addressing voltage is used. In some implementations, when the high addressing voltage VC_{ADD_H} is applied along the common line, application of the high segment voltage VS_H can cause a modulator to remain in its current position, while application of the low segment voltage VS_L can cause actuation of the modulator. As a corollary, the effect of the segment voltages can be the opposite when a low addressing voltage VC_{ADD_L} is applied, with high segment voltage VS_H causing actuation of the modulator, and low segment voltage VS_L having no effect (i.e., remaining stable) on the state of the modulator.

[0052] In some implementations, hold voltages, address voltages, and segment voltages may be used which always produce the same polarity potential difference across the modulators. In some other implementations, signals can be used which alternate the polarity of the potential difference of the modulators. Alternation of the polarity across the modulators (that is, alternation of the polarity of write procedures) may reduce or inhibit charge accumulation which could occur after repeated write

operations of a single polarity.

[0053] Figure 5A shows an example of a diagram illustrating a frame of display data in the 3x3 interferometric modulator display of Figure 2. Figure 5B shows an example of a timing diagram for common and segment signals that may be used to write the frame of display data illustrated in Figure 5A. The signals can be applied to the, e.g., 3x3 array of Figure 2, which will ultimately result in the line time 60e display arrangement illustrated in Figure 5A. The actuated modulators in Figure 5A are in a dark-state, i.e., where a substantial portion of the reflected light is outside of the visible spectrum so as to result in a dark appearance to, e.g., a viewer. Prior to writing the frame illustrated in Figure 5A, the pixels can be in any state, but the write procedure illustrated in the timing diagram of Figure 5B presumes that each modulator has been released and resides in an unactuated state before the first line time 60a.

[0054] During the first line time 60a, a release voltage 70 is applied on common line 1; the voltage applied on common line 2 begins at a high hold voltage 72 and moves to a release voltage 70; and a low hold voltage 76 is applied along common line 3. Thus, the modulators (common 1, segment 1), (1,2) and (1,3) along common line 1 remain in a relaxed, or unactuated, state for the duration of the first line time 60a, the modulators (2,1), (2,2) and (2,3) along common line 2 will move to a relaxed state, and the modulators (3,1), (3,2) and (3,3) along common line 3 will remain in their previous state. With reference to Figure 4, the segment voltages applied along segment lines 1, 2 and 3 will have no effect on the state of the interferometric modulators, as none of common lines 1, 2 or 3 are being exposed to voltage levels causing actuation during line time 60a (i.e., $V_{C_{REL}}$ – relax and $V_{C_{HOLD_L}}$ – stable).

[0055] During the second line time 60b, the voltage on common line 1 moves to a high hold voltage 72, and all modulators along common line 1 remain in a relaxed state regardless of the segment voltage applied because no addressing, or actuation, voltage was applied on the common line 1. The modulators along common line 2 remain in a relaxed state due to the application of the release voltage 70, and the modulators (3,1), (3,2) and (3,3) along common line 3 will relax when the voltage along common line 3 moves to a release voltage 70.

[0056] During the third line time 60c, common line 1 is addressed by applying a high address voltage 74 on common line 1. Because a low segment voltage 64 is applied along segment lines 1 and 2 during the application of this address voltage, the

pixel voltage across modulators (1,1) and (1,2) is greater than the high end of the positive stability window (i.e., the voltage differential exceeded a predefined threshold) of the modulators, and the modulators (1,1) and (1,2) are actuated.

Conversely, because a high segment voltage 62 is applied along segment line 3, the pixel voltage across modulator (1,3) is less than that of modulators (1,1) and (1,2), and remains within the positive stability window of the modulator; modulator (1,3) thus remains relaxed. Also during line time 60c, the voltage along common line 2 decreases to a low hold voltage 76, and the voltage along common line 3 remains at a release voltage 70, leaving the modulators along common lines 2 and 3 in a relaxed position.

[0057] During the fourth line time 60d, the voltage on common line 1 returns to a high hold voltage 72, leaving the modulators along common line 1 in their respective addressed states. The voltage on common line 2 is decreased to a low address voltage 78. Because a high segment voltage 62 is applied along segment line 2, the pixel voltage across modulator (2,2) is below the lower end of the negative stability window of the modulator, causing the modulator (2,2) to actuate. Conversely, because a low segment voltage 64 is applied along segment lines 1 and 3, the modulators (2,1) and (2,3) remain in a relaxed position. The voltage on common line 3 increases to a high hold voltage 72, leaving the modulators along common line 3 in a relaxed state.

[0058] Finally, during the fifth line time 60e, the voltage on common line 1 remains at high hold voltage 72, and the voltage on common line 2 remains at a low hold voltage 76, leaving the modulators along common lines 1 and 2 in their respective addressed states. The voltage on common line 3 increases to a high address voltage 74 to address the modulators along common line 3. As a low segment voltage 64 is applied on segment lines 2 and 3, the modulators (3,2) and (3,3) actuate, while the high segment voltage 62 applied along segment line 1 causes modulator (3,1) to remain in a relaxed position. Thus, at the end of the fifth line time 60e, the 3x3 pixel array is in the state shown in Figure 5A, and will remain in that state as long as the hold voltages are applied along the common lines, regardless of variations in the segment voltage which may occur when modulators along other common lines (not shown) are being addressed.

[0059] In the timing diagram of Figure 5B, a given write procedure (i.e., line times 60a–60e) can include the use of either high hold and address voltages, or low

hold and address voltages. Once the write procedure has been completed for a given common line (and the common voltage is set to the hold voltage having the same polarity as the actuation voltage), the pixel voltage remains within a given stability window, and does not pass through the relaxation window until a release voltage is applied on that common line. Furthermore, as each modulator is released as part of the write procedure prior to addressing the modulator, the actuation time of a modulator, rather than the release time, may determine the necessary line time. Specifically, in implementations in which the release time of a modulator is greater than the actuation time, the release voltage may be applied for longer than a single line time, as depicted in Figure 5B. In some other implementations, voltages applied along common lines or segment lines may vary to account for variations in the actuation and release voltages of different modulators, such as modulators of different colors.

[0060] The details of the structure of interferometric modulators that operate in accordance with the principles set forth above may vary widely. For example, Figures 6A–6E show examples of cross-sections of varying implementations of interferometric modulators, including the movable reflective layer 14 and its supporting structures. Figure 6A shows an example of a partial cross-section of the interferometric modulator display of Figure 1, where a strip of metal material, i.e., the movable reflective layer 14 is deposited on supports 18 extending orthogonally from the substrate 20. In Figure 6B, the movable reflective layer 14 of each IMOD is generally square or rectangular in shape and attached to supports at or near the corners, on tethers 32. In Figure 6C, the movable reflective layer 14 is generally square or rectangular in shape and suspended from a deformable layer 34, which may include a flexible metal. The deformable layer 34 can connect, directly or indirectly, to the substrate 20 around the perimeter of the movable reflective layer 14. These connections are herein referred to as support posts. The implementation shown in Figure 6C has additional benefits deriving from the decoupling of the optical functions of the movable reflective layer 14 from its mechanical functions, which are carried out by the deformable layer 34. This decoupling allows the structural design and materials used for the reflective layer 14 and those used for the deformable layer 34 to be optimized independently of one another.

[0061] Figure 6D shows another example of an IMOD, where the movable reflective layer 14 includes a reflective sub-layer 14a. The movable reflective layer

14 rests on a support structure, such as support posts 18. The support posts 18 provide separation of the movable reflective layer 14 from the lower stationary electrode (i.e., part of the optical stack 16 in the illustrated IMOD) so that a gap 19 is formed between the movable reflective layer 14 and the optical stack 16, for example when the movable reflective layer 14 is in a relaxed position. The movable reflective layer 14 also can include a conductive layer 14c, which may be configured to serve as an electrode, and a support layer 14b. In this example, the conductive layer 14c is disposed on one side of the support layer 14b, distal from the substrate 20, and the reflective sub-layer 14a is disposed on the other side of the support layer 14b, proximal to the substrate 20. In some implementations, the reflective sub-layer 14a can be conductive and can be disposed between the support layer 14b and the optical stack 16. The support layer 14b can include one or more layers of a dielectric material, for example, silicon oxynitride (SiON) or silicon dioxide (SiO₂). In some implementations, the support layer 14b can be a stack of layers, such as, for example, a SiO₂/SiON/SiO₂ tri-layer stack. Either or both of the reflective sub-layer 14a and the conductive layer 14c can include, e.g., an aluminum (Al) alloy with about 0.5% copper (Cu), or another reflective metallic material. Employing conductive layers 14a, 14c above and below the dielectric support layer 14b can balance stresses and provide enhanced conduction. In some implementations, the reflective sub-layer 14a and the conductive layer 14c can be formed of different materials for a variety of design purposes, such as achieving specific stress profiles within the movable reflective layer 14.

[0062] As illustrated in Figure 6D, some implementations also can include a black mask structure 23. The black mask structure 23 can be formed in optically inactive regions (e.g., between pixels or under posts 18) to absorb ambient or stray light. The black mask structure 23 also can improve the optical properties of a display device by inhibiting light from being reflected from or transmitted through inactive portions of the display, thereby increasing the contrast ratio. Additionally, the black mask structure 23 can be conductive and be configured to function as an electrical bussing layer. In some implementations, the row electrodes can be connected to the black mask structure 23 to reduce the resistance of the connected row electrode. The black mask structure 23 can be formed using a variety of methods, including deposition and patterning techniques. The black mask structure 23 can include one or more layers. For example, in some implementations, the black mask structure 23 includes a

molybdenum-chromium (MoCr) layer that serves as an optical absorber, an SiO₂ layer, and an aluminum alloy that serves as a reflector and a bussing layer, with a thickness in the range of about 30–80 Å, 500–1000 Å, and 500–6000 Å, respectively. The one or more layers can be patterned using a variety of techniques, including
5 photolithography and dry etching, including, for example, carbon tetrafluoromethane (CF₄) and/or oxygen (O₂) for the MoCr and SiO₂ layers and chlorine (Cl₂) and/or boron trichloride (BCl₃) for the aluminum alloy layer. In some implementations, the black mask 23 can be an etalon or interferometric stack structure. In such
10 interferometric stack black mask structures 23, the conductive absorbers can be used to transmit or bus signals between lower, stationary electrodes in the optical stack 16 of each row or column. In some implementations, a spacer layer 35 can serve to generally electrically isolate the absorber layer 16a from the conductive layers in the black mask 23.

[0063] Figure 6E shows another example of an IMOD, where the movable
15 reflective layer 14 is self-supporting. In contrast with Figure 6D, the implementation of Figure 6E does not include support posts 18. Instead, the movable reflective layer 14 contacts the underlying optical stack 16 at multiple locations, and the curvature of the movable reflective layer 14 provides sufficient support that the movable reflective layer 14 returns to the unactuated position of Figure 6E when the voltage across the
20 interferometric modulator is insufficient to cause actuation. The optical stack 16, which may contain a plurality of several different layers, is shown here for clarity including an optical absorber 16a, and a dielectric 16b. In some implementations, the optical absorber 16a may serve both as a fixed electrode and as a partially reflective layer.

[0064] In implementations such as those shown in Figures 6A–6E, the IMODs
25 function as direct-view devices, in which images are viewed from the front side of the transparent substrate 20, i.e., the side opposite to that upon which the modulator is arranged. In these implementations, the back portions of the device (that is, any portion of the display device behind the movable reflective layer 14, including, for
30 example, the deformable layer 34 illustrated in Figure 6C) can be configured and operated upon without impacting or negatively affecting the image quality of the display device, because the reflective layer 14 optically shields those portions of the device. For example, in some implementations a bus structure (not illustrated) can be included behind the movable reflective layer 14 which provides the ability to separate

the optical properties of the modulator from the electromechanical properties of the modulator, such as voltage addressing and the movements that result from such addressing. Additionally, the implementations of Figures 6A–6E can simplify processing, such as, e.g., patterning.

5 **[0065]** Figure 7 shows an example of a flow diagram illustrating a manufacturing process 80 for an interferometric modulator, and Figures 8A–8E show examples of cross-sectional schematic illustrations of corresponding stages of such a manufacturing process 80. In some implementations, the manufacturing process 80 can be implemented to manufacture, e.g., interferometric modulators of the general type illustrated in Figures 1 and 6, in addition to other blocks not shown in Figure 7. With reference to Figures 1, 6 and 7, the process 80 begins at block 82 with the formation of the optical stack 16 over the substrate 20. Figure 8A illustrates such an optical stack 16 formed over the substrate 20. The substrate 20 may be a transparent substrate such as glass or plastic, it may be flexible or relatively stiff and unbending, and may have been subjected to prior preparation processes, e.g., cleaning, to facilitate efficient formation of the optical stack 16. As discussed above, the optical stack 16 can be electrically conductive, partially transparent and partially reflective and may be fabricated, for example, by depositing one or more layers having the desired properties onto the transparent substrate 20. In Figure 8A, the optical stack 16 includes a multilayer structure having sub-layers 16a and 16b, although more or fewer sub-layers may be included in some other implementations. In some implementations, one of the sub-layers 16a, 16b can be configured with both optically absorptive and conductive properties, such as the combined conductor/absorber sub-layer 16a. Additionally, one or more of the sub-layers 16a, 16b can be patterned into parallel strips, and may form row electrodes in a display device. Such patterning can be performed by a masking and etching process or another suitable process known in the art. In some implementations, one of the sub-layers 16a, 16b can be an insulating or dielectric layer, such as sub-layer 16b that is deposited over one or more metal layers (e.g., one or more reflective and/or conductive layers). In addition, the optical stack 16 can be patterned into individual and parallel strips that form the rows of the display.

[0066] The process 80 continues at block 84 with the formation of a sacrificial layer 25 over the optical stack 16. The sacrificial layer 25 is later removed (e.g., at block 90) to form the cavity 19 and thus the sacrificial layer 25 is not shown in the

resulting interferometric modulators 12 illustrated in Figure 1. Figure 8B illustrates a partially fabricated device including a sacrificial layer 25 formed over the optical stack 16. The formation of the sacrificial layer 25 over the optical stack 16 may include deposition of a xenon difluoride (XeF_2)-etchable material such as molybdenum (Mo) or amorphous silicon (Si), in a thickness selected to provide, after subsequent removal, a gap or cavity 19 (see also Figures 1 and 8E) having a desired design size. Deposition of the sacrificial material may be carried out using deposition techniques such as physical vapor deposition (PVD, e.g., sputtering), plasma-enhanced chemical vapor deposition (PECVD), thermal chemical vapor deposition (thermal CVD), or spin-coating.

[0067] The process 80 continues at block 86 with the formation of a support structure e.g., a post 18 as illustrated in Figures 1, 6 and 8C. The formation of the post 18 may include patterning the sacrificial layer 25 to form a support structure aperture, then depositing a material (e.g., a polymer or an inorganic material, e.g., silicon oxide) into the aperture to form the post 18, using a deposition method such as PVD, PECVD, thermal CVD, or spin-coating. In some implementations, the support structure aperture formed in the sacrificial layer can extend through both the sacrificial layer 25 and the optical stack 16 to the underlying substrate 20, so that the lower end of the post 18 contacts the substrate 20 as illustrated in Figure 6A. Alternatively, as depicted in Figure 8C, the aperture formed in the sacrificial layer 25 can extend through the sacrificial layer 25, but not through the optical stack 16. For example, Figure 8E illustrates the lower ends of the support posts 18 in contact with an upper surface of the optical stack 16. The post 18, or other support structures, may be formed by depositing a layer of support structure material over the sacrificial layer 25 and patterning to remove portions of the support structure material located away from apertures in the sacrificial layer 25. The support structures may be located within the apertures, as illustrated in Figure 8C, but also can, at least partially, extend over a portion of the sacrificial layer 25. As noted above, the patterning of the sacrificial layer 25 and/or the support posts 18 can be performed by a patterning and etching process, but also may be performed by alternative etching methods.

[0068] The process 80 continues at block 88 with the formation of a movable reflective layer or membrane such as the movable reflective layer 14 illustrated in Figures 1, 6 and 8D. The movable reflective layer 14 may be formed by employing one or more deposition processes, e.g., reflective layer (e.g., aluminum, aluminum

alloy) deposition, along with one or more patterning, masking, and/or etching processes. The movable reflective layer 14 can be electrically conductive, and referred to as an electrically conductive layer. In some implementations, the movable reflective layer 14 may include a plurality of sub-layers 14a, 14b, 14c as shown in Figure 8D. In some implementations, one or more of the sub-layers, such as sub-layers 14a, 14c, may include highly reflective sub-layers selected for their optical properties, and another sub-layer 14b may include a mechanical sub-layer selected for its mechanical properties. Since the sacrificial layer 25 is still present in the partially fabricated interferometric modulator formed at block 88, the movable reflective layer 14 is typically not movable at this stage. A partially fabricated IMOD that contains a sacrificial layer 25 also may be referred to herein as an “unreleased” IMOD. As described above in connection with Figure 1, the movable reflective layer 14 can be patterned into individual and parallel strips that form the columns of the display.

[0069] The process 80 continues at block 90 with the formation of a cavity, e.g., cavity 19 as illustrated in Figures 1, 6 and 8E. The cavity 19 may be formed by exposing the sacrificial material 25 (deposited at block 84) to an etchant. For example, an etchable sacrificial material such as Mo or amorphous Si may be removed by dry chemical etching, e.g., by exposing the sacrificial layer 25 to a gaseous or vaporous etchant, such as vapors derived from solid XeF_2 for a period of time that is effective to remove the desired amount of material, typically selectively removed relative to the structures surrounding the cavity 19. Other combinations of etchable sacrificial material and etching methods, e.g. wet etching and/or plasma etching, also may be used. Since the sacrificial layer 25 is removed during block 90, the movable reflective layer 14 is typically movable after this stage. After removal of the sacrificial material 25, the resulting fully or partially fabricated IMOD may be referred to herein as a “released” IMOD.

[0070] Electronic devices may incorporate IMODS as part of a display of the electronic device. Such electronic devices also may include other various electronic components, including capacitor devices or capacitors. One type of capacitor is a metal-insulator-metal (MIM) capacitor. Mobile telephones, for example, may incorporate MIM capacitors that are used during the operation of the mobile telephone. With the reduction in the size of some personal electronic devices, including mobile telephones, there also may be a corresponding reduction in the size of the electronic components, including MIM capacitors, which are part of the

personal electronic devices. When the capacitance density is increased, a smaller capacitor may be used to supply substantially the same capacitance as a larger capacitor.

[0071] However, some capacitors are not ideal electronic components because they may exhibit other electronic properties in addition to capacitance. For example, a capacitor can be modeled as an ideal capacitor in series with a resistor. The resistance of such a resistor is defined as the equivalent series resistance (ESR) of the capacitor. To make a capacitor behave more like an ideal capacitor, it is desirable to keep its ESR as low as possible. When fabricating a MIM capacitor on an insulating substrate, it may be difficult to achieve a high capacitance density while maintaining a low ESR for the capacitor.

[0072] For example, a MIM capacitor having a high capacitance density can be formed by creating a capacitor having a number of nanometer-sized features (e.g., submicron-sized features) or larger features (e.g., features having a size of greater than about 1 micron). This may increase the available surface area of electrodes of the capacitor and thus increase the capacitance density. A MIM capacitor having a low ESR, however, may have thick electrode layers that may aid in reducing the ESR. It may be difficult to incorporate thick electrode layers in nanometer-sized or micron-sized features, however.

[0073] As described herein, a MIM capacitor may be fabricated that has a high capacitance density combined with a low ESR. For example, a MIM capacitor having a capacitance density of greater than about 200 nanofarads per millimeter squared (nF/mm^2), an ESR of less than about 50 milliohms ($\text{m}\Omega$), and a breakdown voltage of greater than about 12 volts may be fabricated. A low ESR is important in the performance of RF devices, as the electronic noise in circuit increases exponentially with increases in ESR.

[0074] To aid in the understanding of implementations of MIM capacitors as described herein, a manufacturing process for a MIM capacitor, accompanied by top-down and cross-sectional schematic illustrations of a MIM capacitor at various stages in the manufacturing process, is set forth below. Figures 9A and 9B show examples of flow diagrams illustrating a manufacturing process for forming a MIM capacitor. Figures 10A–10H show examples of schematic illustrations of a MIM capacitor at various stages in the manufacturing process. Each of Figures 10A–10H show

examples of both a top-down schematic illustration of the MIM capacitor and a cross-sectional schematic illustration of the MIM capacitor through line 1–1 in the top-down schematic illustration.

[0075] In the process 900 shown in Figure 9A, patterning techniques, including masking as well as etching processes, may be used to define the shapes of the different components of a MIM capacitor during the manufacturing process. At block 902 of the process 900, a base metal layer is deposited on a surface of a substrate. The substrate may include different substrate materials, including transparent materials, non-transparent materials, flexible materials, rigid materials, or combinations of these. In some implementations, the substrate may include a glass (e.g., a display glass, a borosilicate glass, or a photoimageable glass). In some other implementations, the substrate may include a semiconductor, silicon-on-insulator (SOI), a flexible plastic, or a metal foil. When the substrate is an electrically conductive material, the surface of the substrate may include an insulating layer between the substrate and the base metal layer.

[0076] In some implementations, the base metal layer may be deposited with a physical vapor deposition (PVD) process, a chemical vapor deposition (CVD) process, or an atomic layer deposition (ALD) process. In some implementations, the base metal layer may include aluminum (Al) or an Al alloy. The base metal layer may be about 0.5 microns to 5 microns thick, in some implementations. The base metal layer may be deposited over an area of the substrate of about 1 millimeter by 1 millimeter or about 1 millimeter by 3 millimeters, in some implementations.

[0077] Figure 10A shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 902) in the process 900. The MIM capacitor includes a substrate 1002 and a base metal layer 1004. Dimensions 1008 and 1010 may each be about 250 microns, in some implementations. The dimensions 1008 and 1010 may each be about 1 millimeter, in some other implementations. For example, the dimension 1008 may be about 1050 microns and the dimension 1010 may be about 750 microns.

[0078] Returning to Figure 9A, at block 904 a polymer layer is formed on the base metal layer and on the surface of the substrate. In some implementations, the polymer layer may be formed using a spin-on process, an extrusion process, a lamination process, or an evaporation process. The polymer layer may be about 10 microns to 250 microns thick, about 1 micron to 5 microns thick, or about 2 microns

to 5 microns thick. In some implementations, the polymer of the polymer layer may have a coefficient of thermal expansion of less than about 25 parts per million per degree Celsius ($25 \times 10^{-6}/^{\circ}\text{C}$). In some implementations, the polymer of the polymer layer may have a loss tangent of less than about 0.01 or less than about 0.001. In

5 some implementations, the polymer layer may include a thermoplastic polymer, and in some other implementations, the polymer layer may include a photosetting polymer.

[0079] At block 906, a design is patterned in the polymer layer. In some implementations, the design may be patterned by an embossing type of process.

10 Depending on the scale of the features of the design, the design may be patterned by a nanoimprinting process (features less than about 1 micron in size; i.e., submicron-sized features) or an embossing process (features greater than about 1 micron in size).

[0080] For example, for a nanoimprinting or embossing process, the polymer layer may first be heated. In some implementations, the polymer layer may be heated
15 to about 100°C to 200°C . Then, a mold having the design that is to be patterned into the polymer layer may be pressed into the polymer layer. For example, to form vias in the polymer layer, the mold may include a number of posts. When the polymer layer is a thermoplastic polymer, after pressing the mold into the polymer layer, the polymer layer may be cooled and then the mold may be removed. When the polymer
20 layer is a photosetting polymer, after pressing the mold into the polymer layer, the polymer layer may be cured with ultraviolet (UV) light and then the mold may be removed. When using a photosetting polymer, the mold may be made out of a material that is transparent to ultraviolet light, such as fused silica, for example.

[0081] In some implementations, the design that is patterned in the polymer layer
25 may include a plurality of features, such as a plurality of vias. The vias may be of a depth in the polymer layer such that the base metal layer is exposed at the bottom of each of the individual vias. In some implementations, a via of the plurality of vias may have an aspect ratio of at least about 10 to 1 (i.e., a ratio of the height of a via to the width of a via). For example, when the polymer layer is about 1 micron to 5
30 microns thick, the via may have an opening on a surface of the polymer layer of about 100 nanometers to 500 nanometers. As another example, when the polymer layer is about 10 microns to 250 microns thick, the via may have an opening on a surface of the polymer layer of about 1 micron to 25 microns.

[0082] With some nanoimprinting or embossing processes, polymer may remain at the bottom of the vias after the process is performed. As a result, the base metal layer may not be exposed at the bottoms of the vias. In some implementations, polymer remaining at the bottoms of vias may be removed with a wet or dry etching process to expose the base metal layer at the bottoms of the vias.

[0083] Figures 11A–11D show examples of schematic illustrations of vias in a polymer layer and a portion of a mold that may be used to form vias. Figure 11A shows an example an isometric projection of a portion of a mold, and Figure 11B shows an example of an isometric projection of a design that may be patterned in the polymer layer using the mold. As shown in Figure 11A, a portion of a mold 1100 may include pillars 1102 that may be used to form vias in the polymer layer. The pillars 1102 as shown in Figure 11A have hexagonal cross sections, but other cross sections may be used. For example, in some implementations, the pillars may have circular or square cross sections. As shown in Figure 11B, a portion of a polymer layer 1110 that has been patterned may include vias 1112. The vias 1112 as shown in Figure 11B have hexagonal cross sections, but other cross sections may be used. For example, in some implementations, the vias may have circular or square cross sections. Vias having a hexagonal cross section may be able to be arranged in a pattern in which the vias have a high packing density, which may serve to increase the capacitance density of the MIM capacitor.

[0084] Figure 11C shows an example of a top-down view of a design that may be patterned in the polymer layer using the mold shown in Figure 11A. The vias 1112 shown in Figure 11C have a hexagonal cross section. A hexagonal diameter 1124 of a via or the opening of a via (i.e., a principal dimension of the via on the surface of the polymer layer) may be about 100 nanometers to 500 nanometers or about 1 micron to 25 microns, in some implementations. For example, a hexagonal diameter 1124 of a via or the opening of a via may be about 15 microns, about 20 microns, or about 25 microns. A spacing 1126 between the vias 1112 may be about 60 nanometers to 400 nanometers or about 600 nanometers to 20 microns, in some implementations. For example, a spacing 1126 between the vias 1112 may be about 10 microns, about 15 microns, or about 20 microns.

[0085] Figure 11D shows an example of a top-down view of a design that may be patterned in the polymer layer. As shown in Figure 11D, the design 1150 includes a plurality of vias 1112. The plurality of vias may include any number of vias. In some

implementations, the plurality of vias may include about 300 to 2000 vias. For example, the plurality of vias may include an array of about 30 vias by 40 vias or about 40 vias by 40 vias. In some implementations, the plurality of vias may include about 423 vias, about 649 vias, or about 732 vias. The number of vias may vary with the principal dimension of the vias on the surface of the polymer layer and with the spacing between the vias.

[0086] Figure 10B shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 906) in the process 900. The MIM capacitor includes the substrate 1002, the base metal layer 1004, and a polymer layer 1012 that has been patterned. The polymer layer 1012 may include a plurality of vias 1014. As shown in Figure 10B, the vias 1014 may expose portions of the base metal layer 1004.

[0087] Returning to Figure 9A, at block 908 a first electrode layer is deposited on the polymer layer and on exposed portions of the base metal layer. In some implementations, the first electrode layer may be deposited with an ALD process. An ALD process may allow the first electrode layer to be deposited on substantially the entire surface of each via (i.e., on the bottom of the via and on the interior sidewalls of the via) without the opening of a via becoming filled with the first electrode layer. In some implementations, the first electrode layer may include Al or an Al alloy. In some implementations, the first electrode layer may be less than about 50 nanometers thick. In some implementations, the first electrode layer may contact the exposed base metal layer at the bottom of each via in the polymer layer.

[0088] Figure 10C shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 908) in the process 900. The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, and a first electrode layer 1016. The first electrode layer 1016 may contact the base metal layer 1004 at the bottom of each of the vias 1014. In some implementations, areas of the first electrode layer 1016 are etched to remove the first electrode layer 1016 from regions of the partially fabricated MIM capacitor.

[0089] Returning to Figure 9A, at block 910 a dielectric layer is deposited on the first electrode layer. In some implementations, the dielectric layer may be deposited with an ALD process. In some implementations, the dielectric layer may include zirconium oxide (ZrO_2), aluminum oxide (Al_2O_3), strontium oxide (SrO), strontium

tin oxide (STO), titanium oxide (TiO₂), combinations of layers of these different oxides, or other dielectrics. In some implementations, the dielectric layer may be about 2 nanometers to 35 nanometers thick.

5 [0090] Figure 10D shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 910) in the process 900. The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, the first electrode layer 1016, and a dielectric layer 1020.

10 [0091] Returning to Figure 9A, at block 912 a second electrode layer is deposited on the dielectric layer. In some implementations, the second electrode layer may be deposited with an ALD process. In some implementations, the second electrode layer may include Al or an Al alloy. In some implementations, the second electrode layer may be less than about 50 nanometers thick.

15 [0092] Figure 10E shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 912) in the process 900. The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, the first electrode layer 1016, the dielectric layer 1020, and a second electrode layer 1024. The dielectric layer 1020 may electrically isolate the first electrode layer 1016 from the second electrode layer
20 1024.

[0093] As noted above, in some implementations, the substrate 1002 may include a glass (e.g., a display glass, a borosilicate glass, or a photoimageable glass). In some implementations, the base metal layer 1004 may include Al or an Al alloy and may be about 0.5 microns to 5 microns thick. In some implementations, the polymer layer
25 1012 may include a thermoplastic polymer, and in some other implementations, the polymer layer may include a photosetting polymer. The polymer layer 1012 may be about 10 microns to 250 microns thick, about 1 micron to 5 microns thick, or about 2 microns to 5 microns thick. In some implementations, the first electrode layer 1016 and the second electrode layer 1024 may include Al or an Al alloy and each may be
30 less than about 50 nanometers thick. In some implementations, the dielectric layer 1020 may include ZrO₂, Al₂O₃, SrO, STO, TiO₂, combinations of layers of these different oxides, or other dielectrics, and may be about 2 nanometers to 35 nanometers thick.

[0094] This completes the manufacturing process for a structure that is capable of

yielding a capacitance. For example, a capacitance may be generated between the second electrode layer 1024 and the first electrode layer 1016 in contact with the base metal layer 1004, with the second electrode layer 1024 and the first electrode layer 1016 being electrically isolated from one another by the dielectric layer 1020. Further process operations may be performed to complete the fabrication of the MIM capacitor, however. Examples of these process operations are shown in Figure 9B.

[0095] At block 952 of the process 950 shown in Figure 9B, a passivation layer is formed on the second electrode layer. In some implementations, the passivation layer may be formed with a PVD process, a CVD process, an ALD process, a spin-on process, an extrusion process, or a lamination process. In some implementations, the passivation layer may include a dielectric layer. For example, the passivation layer may include an oxide, such as SiO₂. In some implementations, the passivation layer may be about 0.2 microns to 100 microns thick. In some implementations, regions of the passivation layer may be etched away to allow electrical contact with the second electrode layer.

[0096] Figure 10F shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 952) in the process 950. The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, the first electrode layer 1016, the dielectric layer 1020, the second electrode layer 1024, and a passivation layer 1028. The passivation layer 1028 may protect the second electrode layer 1024 from oxidation or corrosion. A portion 1030 of the second electrode layer 1024 may not be covered with the passivation layer 1028 so that electrical contact may be made with the second electrode layer 1024. The passivation layer 1028 in the portion 1030 may be etched to remove the passivation layer from the portion 1030. As shown in Figure 10F, the passivation layer 1028 also may be formed on portions of the dielectric layer 1020.

[0097] Returning to Figure 9B, at block 954 vias are formed in the substrate. For example, when the substrate is a glass substrate, through glass vias (TGVs) may be formed that pass completely through the glass substrate. In some implementations, the vias may be formed using a sandblasting process. In some other implementations, when the substrate is a photoimageable glass, the substrate may be exposed to ultraviolet light where the vias in the glass will be and then exposed to an elevated temperature. The vias then may be etched in the photoimageable glass substrate. In

some implementations, the vias may be about 100 microns to 750 microns in diameter.

[0098] Figure 10G shows examples of schematic illustrations of the partially fabricated MIM capacitor at this point (e.g., up through block 954) in the process 950.

5 The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, the first electrode layer 1016, the dielectric layer 1020, the second electrode layer 1024, the passivation layer 1028, and vias 1032.

[0099] Returning to Figure 9B, at block 956 metallization is deposited. The
10 metallization may allow the MIM capacitor to be connected to other devices, for example. In some implementations, the metallization may be deposited with a PVD process, a CVD process, or an ALD process. In some implementations, the metallization includes copper (Cu), a Cu alloy, Al, an Al alloy, nickel (Ni), or other metal. In some implementations, the metallization may be about 0.5 microns to 10
15 microns thick.

[00100] Figure 10H shows examples of schematic illustrations of the fabricated MIM capacitor at this point (e.g., up through block 956) in the process 950. The MIM capacitor includes the substrate 1002, the base metal layer 1004, the polymer layer 1012 that has been patterned, the first electrode layer 1016, the dielectric layer 1020,
20 the second electrode layer 1024, the passivation layer 1028, the vias 1032, and metallization 1036 and 1040. In some implementations, the metallization may be deposited in the same operation, and then regions of the metallization may be etched to form the metallization 1036 and 1040. The metallization 1036 may be in electrical contact with the first electrode layer 1016 and the base metal layer 1004. The
25 metallization 1040 may be in electrical contact with the second electrode layer 1024 by the portion of the second electrode layer 1024 not covered with the passivation layer 1028.

[00101] The manufacturing process shown in Figures 9A and 9B is a via-last process; i.e., the vias are formed at or near the end of the manufacturing process. In
30 some implementations, via-last processes may be compatible with flat panel display (FPD) manufacturing equipment. A MIM capacitor also may be fabricated with a via-first process; i.e., the vias may be formed at or near the beginning of the manufacturing process. In a via-first process, the processing operations can be aligned to register with the vias formed in a substrate.

[00102] In some implementations, the apparatus described herein may function as interposers. For example, the process 900 shown in Figure 9 may further include forming at least one through via in the substrate. In some implementations, at block 956, the at least one through via may be filled with the material of the metallization.

5 [00103] An interposer may serve to connect a first electronic component to a second electronic component. In some implementations, the at least one through via in the substrate may include a conductive material and may be configured to electrically connect a first electronic component to a second electronic component. For example, an interposer may connect an integrated circuit to a printed circuit
10 board. When the substrate serves as an interposer, a MIM capacitor on the substrate may function as a decoupling capacitor. A decoupling capacitor may function to decouple one part of an electronic circuit from another. The decoupling capacitor may be configured as a shunt between the two parts of the electronic circuit, and the effect of electronic noise generated by a first part of the electronic circuit on a second
15 part of the electronic circuit may be reduced.

[00104] Figure 12 shows an example of a cross-sectional schematic illustration of an assembly including a MIM capacitor on both sides of a substrate. In some implementations, the two MIM capacitors may have similar configurations, and in some other implementations, the two MIM capacitors may have different
20 configurations. In some implementations, an assembly including a MIM capacitor on both sides of a substrate with the MIM capacitors in electrical contact with one another (e.g., connected in parallel) may have a higher capacitance compared to an assembly having a MIM capacitor on only one side of a substrate, with little effect on the ESR or the breakdown voltage of the MIM capacitors.

25 [00105] For example, assembly 1200 may include a MIM capacitor on each side of a substrate 1002. Each MIM capacitor may similar to the MIM capacitor shown in Figure 10H, for example. Each MIM capacitor may include a base metal layer 1004, a polymer layer 1012 that has been patterned, and a first electrode layer 1016 in electrical contact with the base metal layer 1004. A dielectric layer 1020 may
30 electrically isolate the first electrode layer 1016 from a second electrode layer 1024. A passivation layer 1028 may protect the second electrode layer 1024 from oxidation or corrosion. Metallization 1036 may be in electrical contact with the first electrode layer 1016 and the base metal layer 1004 of each of the MIM capacitors. Metallization 1040 may be in electrical contact with the second electrode layer 1024

of each of the MIM capacitors by a portion of the second electrode layer 1024 not covered with the passivation layer 1028.

[00106] In a manufacturing process for the assembly 1200 shown in Figure 12, the MIM capacitors may be fabricated at the same time or the MIM capacitors may be fabricated separately.

[00107] In some implementations, the substrate 1002 of the assembly 1200 may be an interposer. One or more silicon dies may be attached to the top of assembly 1200 and a substrate or a printed circuit board may be attached to the bottom of the assembly 1200. Thus, the assembly 1200, including a MIM capacitor on each side of a substrate 1002, may be used in microelectronics applications.

[00108] Figure 13 shows an example of a cross-sectional schematic illustration of a MIM capacitor. MIM capacitor 1300 shown in Figure 13 may be similar to the MIM capacitor shown in Figure 10H, but without vias in the substrate on which the MIM capacitor has been fabricated. The MIM capacitor 1300 includes a substrate 1002, a base metal layer 1004, a polymer layer 1012 that has been patterned, a first electrode layer 1016, a dielectric layer 1020, a second electrode layer 1024, a passivation layer 1028, and metallization 1036 and 1040.

[00109] In some implementations, the substrate 1002 may include a glass (e.g., a display glass, a borosilicate glass, or a photoimageable glass). In some implementations, the base metal layer 1004 may include Al or an Al alloy and may be about 0.5 microns to 5 microns thick. In some implementations, the polymer layer 1012 may include a thermoplastic polymer, and in some other implementations, the polymer layer 1012 may include a photosetting polymer. The polymer layer 1012 may be about 10 microns to 250 microns thick, about 1 micron to 5 microns thick, or about 2 microns to 5 microns thick. In some implementations, the first electrode layer 1016 and the second electrode layer 1024 may include Al or an Al alloy and each may be less than about 50 nanometers thick. In some implementations, the dielectric layer 1020 may include ZrO_2 , Al_2O_3 , SrO, STO, TiO_2 , combinations of layers of these different oxides, or other dielectrics, and may be about 2 nanometers to 35 nanometers thick.

[00110] In some implementations, the passivation layer 1028 may include a dielectric layer, such as an oxide (e.g., SiO_2), and may be about 0.2 microns to 100 microns thick. For example, a passivation layer 1028 of SiO_2 may have a thickness of about 1.5 microns. The passivation layer 1028 may protect the second electrode layer

1024 from oxidation or corrosion. In some implementations, the metallization 1036 may be in electrical contact with the first electrode layer 1016 and the base metal layer 1004. The metallization 1040 may be in electrical contact with the second electrode layer 1024 by a portion of the second electrode layer 1024 not covered with the passivation layer 1028. In some implementations, the metallization 1036 and 1040 may include Cu, a Cu alloy, Al, an Al alloy, Ni, or other metal, and may be about 0.5 microns to 10 microns thick.

[00111] Figure 14 shows an example of a cross-sectional schematic illustration of a metal-insulator-metal-insulator-metal (MIMIM) capacitor. A MIMIM capacitor may include an additional dielectric layer and an additional metal layer as compared to a MIM capacitor. Further, a MIMIM capacitor may have a higher capacitance density (e.g., the capacitance density may double) than a MIM capacitor having comparable dimensions. In some implementations, the materials and thicknesses of the different material layers included in a MIMIM capacitor may be similar to the materials and thicknesses of the different material layers included in a MIM capacitor. In some other implementations, the materials and thicknesses of the different material layers included in a MIMIM capacitor may be different than the materials and thicknesses of the different material layers included in a MIM capacitor.

[00112] The MIMIM capacitor 1400 shown in Figure 14 includes a substrate 1002, a base metal layer 1004, a polymer layer 1012 that has been patterned, and a first electrode layer 1016. The first electrode layer 1016 may contact the base metal layer 1004 at the bottom of each of the vias in the polymer layer 1012. A first dielectric layer 1020 may electrically isolate the first electrode layer 1016 from a second electrode layer 1024. A second dielectric layer 1402 may electrically isolate the second electrode layer 1024 from a third electrode layer 1406. A passivation layer 1410 may protect the third electrode layer 1406 from oxidation or corrosion.

[00113] Metallization 1414 may be in electrical contact with the first electrode layer 1016 and the base metal layer 1004. The metallization 1414 also may be in electrical contact with the third electrode layer 1406. Metallization 1418 may be in electrical contact with the second electrode layer 1024 by a portion of the second electrode layer 1024 not covered with the second dielectric layer 1402.

[00114] In some implementations, the second dielectric layer 1402 may include ZrO_2 , Al_2O_3 , SrO , STO , TiO_2 , combinations of layers of these different oxides, or other dielectrics, and may be about 2 nanometers to 35 nanometers thick. In some

implementations, the third electrode layer 1406 may include Al or an Al alloy and may be less than about 50 nanometers thick. In some implementations, the passivation layer 1410 may include a dielectric layer, such as an oxide (e.g., SiO₂), and may be about 0.2 microns to 100 microns thick. For example, a passivation layer 1028 of SiO₂ may have a thickness of about 1.5 microns. In some implementations, the metallization 1414 and 1418 may include Cu, a Cu alloy, Al, an Al alloy, Ni, or other metal, and may be about 0.5 microns to 10 microns thick.

[00115] Additional configurations of the MIM and MIMIM capacitors disclosed herein are possible. For example, an assembly may include a MIMIM capacitor on both sides of a substrate, similar to the assembly 1200 shown in Figure 12. As another example, additional metal layers and dielectric layers may be added to the MIM and MIMIM capacitors disclosed herein to further increase the capacitance density of the capacitor.

[00116] Further, operations of the process 900 shown in Figure 9A and the process 950 shown in Figure 9B may be combined and/or rearranged to form any of the MIM or MIMIM capacitors disclosed herein. For example, to fabricate the MIMIM capacitor 1400 shown in Figure 14, further metal deposition and dielectric deposition operations may be performed to form the additional electrode and dielectric layers in the MIMIM capacitor.

[00117] Figures 15A and 15B show examples of system block diagrams illustrating a display device 40 that includes a plurality of interferometric modulators. The display device 40 can be, for example, a smart phone, a cellular or mobile telephone. However, the same components of the display device 40 or slight variations thereof are also illustrative of various types of display devices such as televisions, tablets, e-readers, hand-held devices and portable media players.

[00118] The display device 40 includes a housing 41, a display 30, an antenna 43, a speaker 45, an input device 48 and a microphone 46. The housing 41 can be formed from any of a variety of manufacturing processes, including injection molding, and vacuum forming. In addition, the housing 41 may be made from any of a variety of materials, including, but not limited to: plastic, metal, glass, rubber and ceramic, or a combination thereof. The housing 41 can include removable portions (not shown) that may be interchanged with other removable portions of different color, or containing different logos, pictures, or symbols.

[00119] The display 30 may be any of a variety of displays, including a bi-stable or

analog display, as described herein. The display 30 also can be configured to include a flat-panel display, such as plasma, EL, OLED, STN LCD, or TFT LCD, or a non-flat-panel display, such as a CRT or other tube device. In addition, the display 30 can include an interferometric modulator display, as described herein.

5 **[00120]** The components of the display device 40 are schematically illustrated in Figure 15B. The display device 40 includes a housing 41 and can include additional components at least partially enclosed therein. For example, the display device 40 includes a network interface 27 that includes an antenna 43 which is coupled to a transceiver 47. The transceiver 47 is connected to a processor 21, which is connected
10 to conditioning hardware 52. The conditioning hardware 52 may be configured to condition a signal (e.g., filter a signal). The conditioning hardware 52 is connected to a speaker 45 and a microphone 46. The processor 21 is also connected to an input device 48 and a driver controller 29. The driver controller 29 is coupled to a frame buffer 28, and to an array driver 22, which in turn is coupled to a display array 30. In
15 some implementations, a power supply 50 can provide power to substantially all components in the particular display device 40 design.

[00121] The network interface 27 includes the antenna 43 and the transceiver 47 so that the display device 40 can communicate with one or more devices over a network. The network interface 27 also may have some processing capabilities to relieve, for
20 example, data processing requirements of the processor 21. The antenna 43 can transmit and receive signals. In some implementations, the antenna 43 transmits and receives RF signals according to the IEEE 16.11 standard, including IEEE 16.11(a), (b), or (g), or the IEEE 802.11 standard, including IEEE 802.11a, b, g, n, and further implementations thereof. In some other implementations, the antenna 43 transmits
25 and receives RF signals according to the BLUETOOTH standard. In the case of a cellular telephone, the antenna 43 is designed to receive code division multiple access (CDMA), frequency division multiple access (FDMA), time division multiple access (TDMA), Global System for Mobile communications (GSM), GSM/General Packet Radio Service (GPRS), Enhanced Data GSM Environment (EDGE), Terrestrial
30 Trunked Radio (TETRA), Wideband-CDMA (W-CDMA), Evolution Data Optimized (EV-DO), 1xEV-DO, EV-DO Rev A, EV-DO Rev B, High Speed Packet Access (HSPA), High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), Evolved High Speed Packet Access (HSPA+), Long Term Evolution (LTE), AMPS, or other known signals that are used to communicate within

a wireless network, such as a system utilizing 3G or 4G technology. The transceiver 47 can pre-process the signals received from the antenna 43 so that they may be received by and further manipulated by the processor 21. The transceiver 47 also can process signals received from the processor 21 so that they may be transmitted from the display device 40 via the antenna 43.

[00122] In some implementations, the transceiver 47 can be replaced by a receiver. In addition, in some implementations, the network interface 27 can be replaced by an image source, which can store or generate image data to be sent to the processor 21. The processor 21 can control the overall operation of the display device 40. The processor 21 receives data, such as compressed image data from the network interface 27 or an image source, and processes the data into raw image data or into a format that is readily processed into raw image data. The processor 21 can send the processed data to the driver controller 29 or to the frame buffer 28 for storage. Raw data typically refers to the information that identifies the image characteristics at each location within an image. For example, such image characteristics can include color, saturation and gray-scale level.

[00123] The processor 21 can include a microcontroller, CPU, or logic unit to control operation of the display device 40. The conditioning hardware 52 may include amplifiers and filters for transmitting signals to the speaker 45, and for receiving signals from the microphone 46. The conditioning hardware 52 may be discrete components within the display device 40, or may be incorporated within the processor 21 or other components.

[00124] The driver controller 29 can take the raw image data generated by the processor 21 either directly from the processor 21 or from the frame buffer 28 and can re-format the raw image data appropriately for high speed transmission to the array driver 22. In some implementations, the driver controller 29 can re-format the raw image data into a data flow having a raster-like format, such that it has a time order suitable for scanning across the display array 30. Then the driver controller 29 sends the formatted information to the array driver 22. Although a driver controller 29, such as an LCD controller, is often associated with the system processor 21 as a stand-alone Integrated Circuit (IC), such controllers may be implemented in many ways. For example, controllers may be embedded in the processor 21 as hardware, embedded in the processor 21 as software, or fully integrated in hardware with the array driver 22.

[00125] The array driver 22 can receive the formatted information from the driver controller 29 and can re-format the video data into a parallel set of waveforms that are applied many times per second to the hundreds, and sometimes thousands (or more), of leads coming from the display's x-y matrix of pixels.

5 [00126] In some implementations, the driver controller 29, the array driver 22, and the display array 30 are appropriate for any of the types of displays described herein. For example, the driver controller 29 can be a conventional display controller or a bi-stable display controller (such as an IMOD controller). Additionally, the array driver 22 can be a conventional driver or a bi-stable display driver (such as an IMOD display
10 driver). Moreover, the display array 30 can be a conventional display array or a bi-stable display array (such as a display including an array of IMODs). In some implementations, the driver controller 29 can be integrated with the array driver 22. Such an implementation can be useful in highly integrated systems, for example, mobile phones, portable-electronic devices, watches or small-area displays.

15 [00127] In some implementations, the input device 48 can be configured to allow, for example, a user to control the operation of the display device 40. The input device 48 can include a keypad, such as a QWERTY keyboard or a telephone keypad, a button, a switch, a rocker, a touch-sensitive screen, a touch-sensitive screen integrated with display array 30, or a pressure- or heat-sensitive membrane. The microphone 46
20 can be configured as an input device for the display device 40. In some implementations, voice commands through the microphone 46 can be used for controlling operations of the display device 40.

[00128] The power supply 50 can include a variety of energy storage devices. For example, the power supply 50 can be a rechargeable battery, such as a nickel-
25 cadmium battery or a lithium-ion battery. In implementations using a rechargeable battery, the rechargeable battery may be chargeable using power coming from, for example, a wall socket or a photovoltaic device or array. Alternatively, the rechargeable battery can be wirelessly chargeable. The power supply 50 also can be a renewable energy source, a capacitor, or a solar cell, including a plastic solar cell or
30 solar-cell paint. The power supply 50 also can be configured to receive power from a wall outlet.

[00129] In some implementations, control programmability resides in the driver controller 29 which can be located in several places in the electronic display system. In some other implementations, control programmability resides in the array driver

22. The above-described optimization may be implemented in any number of hardware and/or software components and in various configurations.

[00130] The various illustrative logics, logical blocks, modules, circuits and algorithm steps described in connection with the implementations disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. The interchangeability of hardware and software has been described generally, in terms of functionality, and illustrated in the various illustrative components, blocks, modules, circuits and steps described above. Whether such functionality is implemented in hardware or software depends upon the particular application and design constraints imposed on the overall system.

[00131] The hardware and data processing apparatus used to implement the various illustrative logics, logical blocks, modules and circuits described in connection with the aspects disclosed herein may be implemented or performed with a general purpose single- or multi-chip processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, or, any conventional processor, controller, microcontroller, or state machine. A processor also may be implemented as a combination of computing devices, such as a combination of a DSP and a microprocessor, a plurality of microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration. In some implementations, particular steps and methods may be performed by circuitry that is specific to a given function.

[00132] In one or more aspects, the functions described may be implemented in hardware, digital electronic circuitry, computer software, firmware, including the structures disclosed in this specification and their structural equivalents thereof, or in any combination thereof. Implementations of the subject matter described in this specification also can be implemented as one or more computer programs, i.e., one or more modules of computer program instructions, encoded on a computer storage media for execution by, or to control the operation of, data processing apparatus.

[00133] Various modifications to the implementations described in this disclosure may be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other implementations without departing from the spirit or

scope of this disclosure. Thus, the claims are not intended to be limited to the implementations shown herein, but are to be accorded the widest scope consistent with this disclosure, the principles and the novel features disclosed herein. The word “exemplary” is used exclusively herein to mean “serving as an example, instance, or illustration.” Any implementation described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other possibilities or implementations. Additionally, a person having ordinary skill in the art will readily appreciate, the terms “upper” and “lower” are sometimes used for ease of describing the figures, and indicate relative positions corresponding to the orientation of the figure on a properly oriented page, and may not reflect the proper orientation of an IMOD as implemented.

[00134] Certain features that are described in this specification in the context of separate implementations also can be implemented in combination in a single implementation. Conversely, various features that are described in the context of a single implementation also can be implemented in multiple implementations separately or in any suitable subcombination. Moreover, although features may be described above as acting in certain combinations and even initially claimed as such, one or more features from a claimed combination can in some cases be excised from the combination, and the claimed combination may be directed to a subcombination or variation of a subcombination.

[00135] Similarly, while operations are depicted in the drawings in a particular order, a person having ordinary skill in the art will readily recognize that such operations need not be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. Further, the drawings may schematically depict one more example processes in the form of a flow diagram. However, other operations that are not depicted can be incorporated in the example processes that are schematically illustrated. For example, one or more additional operations can be performed before, after, simultaneously, or between any of the illustrated operations. In certain circumstances, multitasking and parallel processing may be advantageous. Moreover, the separation of various system components in the implementations described above should not be understood as requiring such separation in all implementations, and it should be understood that the described program components and systems can generally be integrated together in a single software product or packaged into multiple software products. Additionally,

other implementations are within the scope of the following claims. In some cases, the actions recited in the claims can be performed in a different order and still achieve desirable results.

CLAIMS

What is claimed is:

- 5 1. An apparatus comprising:
 a first base metal layer on a first side of a substrate;
 a first polymer layer disposed on the first base metal layer and on the first side
of the substrate, the first polymer layer defining a first plurality of vias through the first
polymer layer exposing portions of the first base metal layer;
10 a first electrode layer disposed on the first polymer layer, the first electrode
layer contacting the portions of the first base metal layer;
 a first dielectric layer disposed on the first electrode layer; and
 a second electrode layer disposed on the first dielectric layer, the first
dielectric layer electrically isolating the first electrode layer from the second electrode
15 layer.
2. The apparatus of claim 1, wherein a first via of the first plurality of vias in the first
polymer layer has an aspect ratio of at least about 10 to 1.
- 20 3. The apparatus of claims 1 or 2, wherein a first via of the first plurality of vias in
the first polymer layer has an opening on a surface of the first polymer layer of about
100 nanometers to 500 nanometers, and wherein the first polymer layer is about 1
micron to 5 microns thick.
- 25 4. The apparatus of claims 1 or 2, wherein a first via of the first plurality of vias in
the first polymer layer has an opening on a surface of the first polymer layer of about
1 micron to 25 microns, and wherein the first polymer layer is about 10 microns to
250 microns thick.
- 30 5. The apparatus of any one of the preceding claims, wherein the first base metal
layer, the first electrode layer, and the second electrode layer include aluminum.
6. The apparatus of any one of the preceding claims, wherein the first base metal
layer reduces the equivalent series resistance of the apparatus.

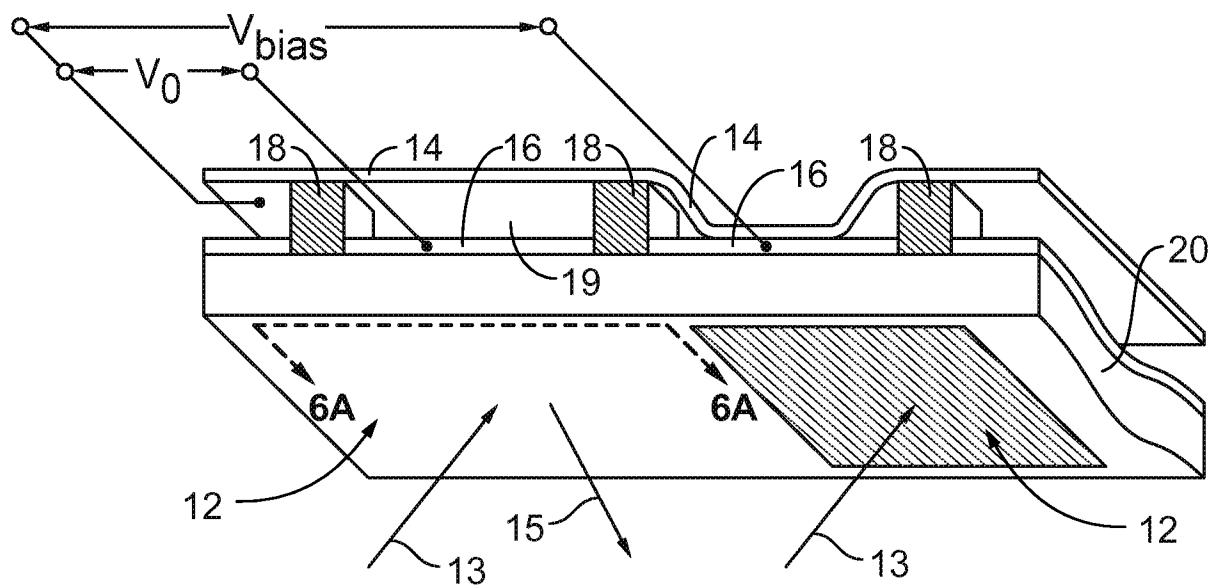
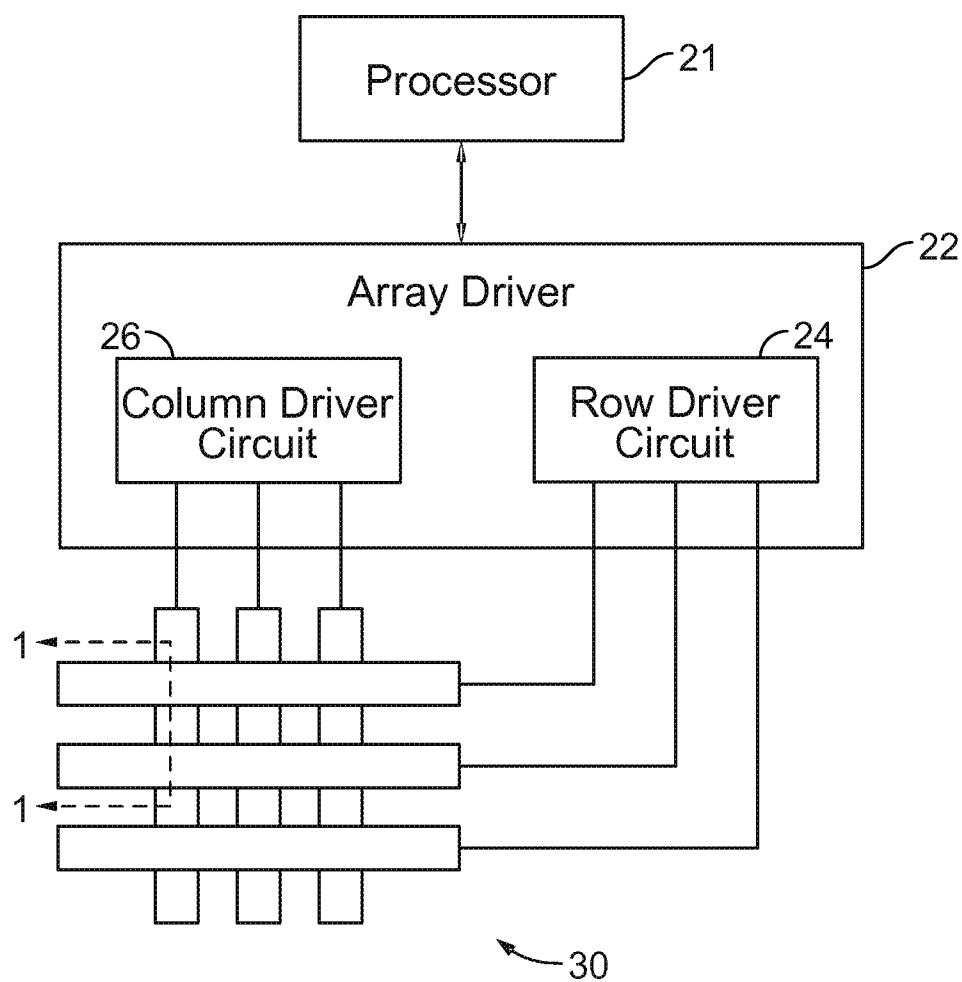
7. The apparatus of any one of the preceding claims, wherein the substrate is a glass substrate.
8. The apparatus of any one of the preceding claims, the substrate defining at least one through via in the substrate.
9. The apparatus of claim 8, wherein the substrate is an interposer, and wherein the through via includes a conductive material configured to electrically connect a first electronic component on the first side of the substrate to a second electronic component on a second side of the substrate opposite to the first side, wherein the second electronic component is disposed on a second substrate or a printed circuit board (PCB).
10. The apparatus of any one of the preceding claims, further comprising:
- a second base metal layer on a second side of the substrate;
 - a second polymer layer disposed on the second base metal layer and on the second side of the substrate, the second polymer layer defining a second plurality of vias through the second polymer layer exposing portions of the second base metal layer;
 - a third electrode layer disposed on the second polymer layer, the third electrode layer contacting the portions of the second base metal layer;
 - a second dielectric layer disposed on the third electrode layer;
 - a fourth electrode layer disposed on the second dielectric layer, the second dielectric layer electrically isolating the third electrode layer from the fourth electrode layer;
 - a first connection electrically connecting the first and the third electrode layers; and
 - a second connection electrically connecting the second and the fourth electrode layers.
11. The apparatus of claim 10, wherein the first connection includes a first via through the substrate, and wherein the second connection includes a second via through the substrate.

12. The apparatus of claims 10 or 11, wherein a first via of the second plurality of vias in the second polymer layer has an aspect ratio of at least about 10 to 1.
13. A system comprising the apparatus of any one of the preceding claims, the
5 system further comprising:
 a display;
 a processor that is configured to communicate with the display, the processor being configured to process image data; and
 a memory device that is configured to communicate with the processor.
- 10 14. The system of claim 13, further comprising:
 a driver circuit configured to send at least one signal to the display; and
 a controller configured to send at least a portion of the image data to the driver circuit.
- 15 15. The system of claims 13 or 14, further comprising:
 an image source module configured to send the image data to the processor.
16. The system of claim 15, wherein the image source module includes at least one of
20 a receiver, transceiver, and transmitter.
17. The system of any one of the preceding claims, further comprising:
 an input device configured to receive input data and to communicate the input data to the processor.
- 25 18. An apparatus comprising:
 a base metal layer on a substrate;
 a polymer layer disposed on the base metal layer and on the substrate;
 a first electrode layer disposed on the polymer layer;
30 a second electrode layer;
 means for exposing portions of the base metal layer, the first electrode layer contacting the portions of the base metal layer; and
 means for electrically isolating the first electrode layer from the second electrode layer.

19. The apparatus of claim 18, wherein the means for exposing portions of the base metal layer increases a surface area between the first electrode layer and the second electrode layer.
- 5
20. The apparatus of claims 18 or 19, wherein the base metal layer reduces the equivalent series resistance of the apparatus.
21. A method comprising:
- 10 depositing a base metal layer on a surface of a substrate;
 forming a polymer layer on the base metal layer and on the surface of the substrate;
 patterning a design in the polymer layer;
 depositing a first electrode layer on the polymer layer and on exposed portions
- 15 of the base metal layer;
 depositing a dielectric layer on the first electrode layer; and
 depositing a second electrode layer on the dielectric layer.
22. The method of claim 21, wherein the patterning includes embossing.
- 20
23. The method of claim 21, wherein the patterning includes a nanoimprinting process.
24. The method of claim 23, wherein the nanoimprinting process includes:
- 25 heating the polymer layer;
 pressing a mold into the polymer layer;
 cooling the polymer layer; and
 removing the mold from the polymer layer.
- 30 25. The method of claim 23, wherein the nanoimprinting process includes:
 heating the polymer layer;
 pressing a mold into the polymer layer;
 treating the polymer layer with an ultraviolet light; and
 removing the mold from the polymer layer.

26. The method of any one of claims 21-25, wherein the design in the polymer layer includes a plurality of vias, a first via of the plurality of vias having an aspect ratio of at least about 10 to 1.

5

**Figure 1****Figure 2**

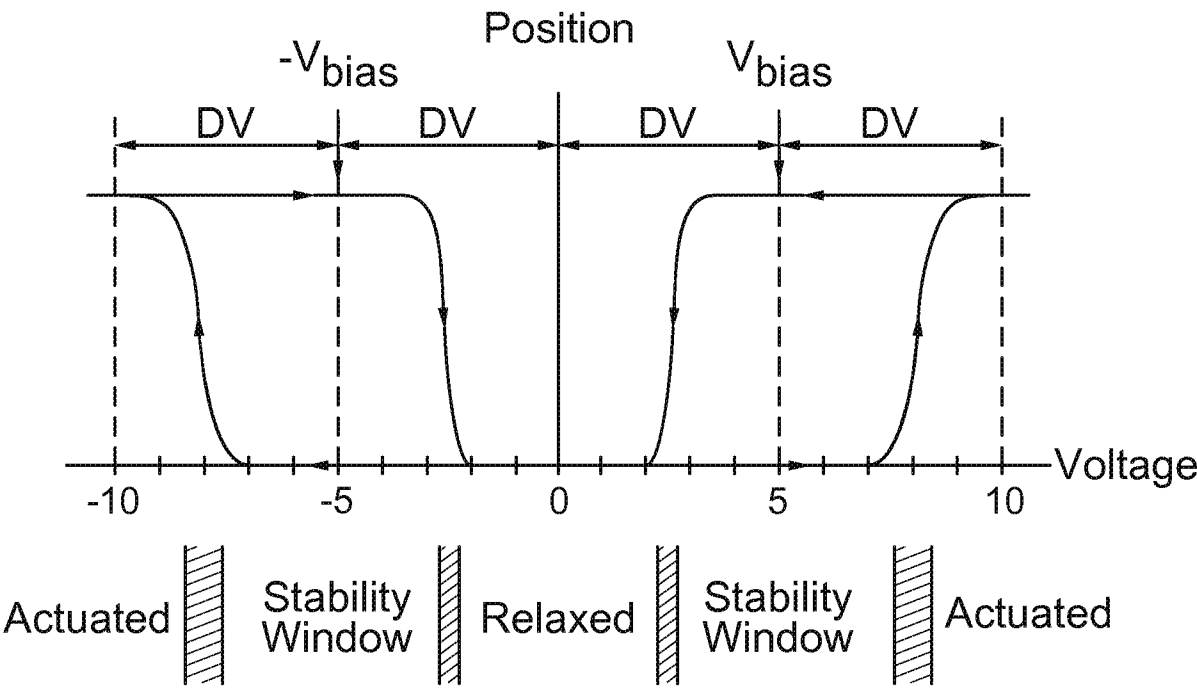


Figure 3

Common Voltages						
Segment Voltages		$V_{C_ADD_H}$	$V_{C_HOLD_H}$	V_{C_REL}	$V_{C_HOLD_L}$	$V_{C_ADD_L}$
	V_{S_H}	Stable	Stable	Relax	Stable	Actuate
	V_{S_L}	Actuate	Stable	Relax	Stable	Stable

Figure 4

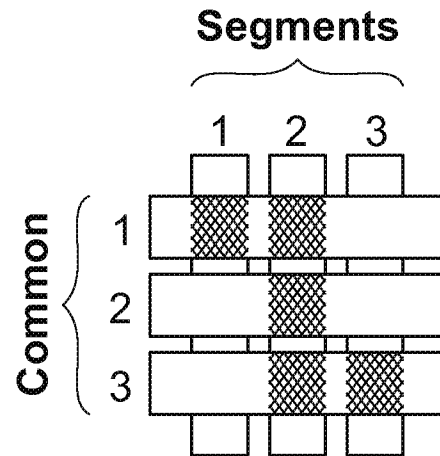


Figure 5A

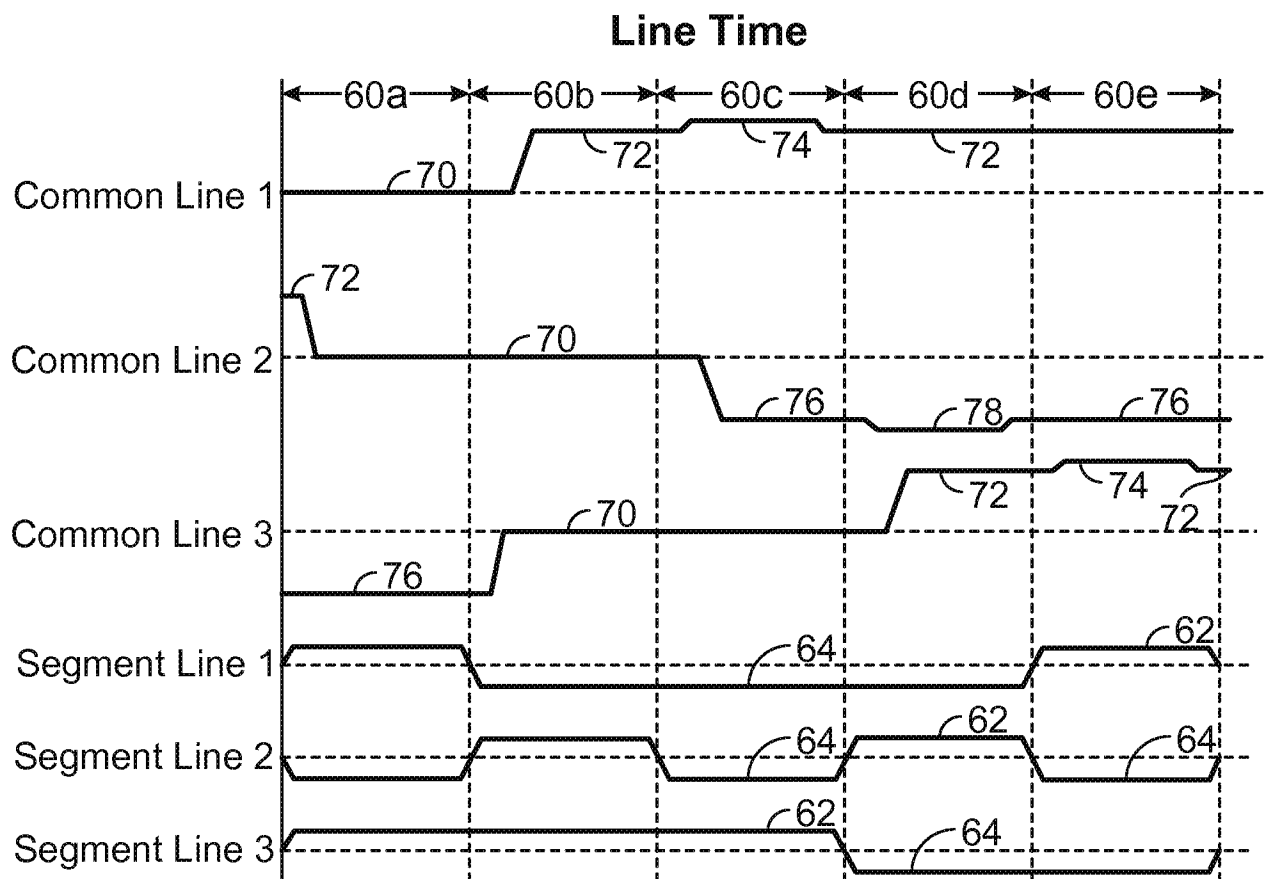


Figure 5B

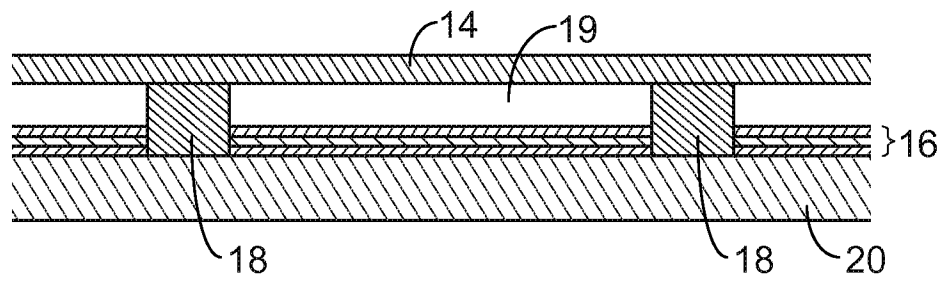


Figure 6A

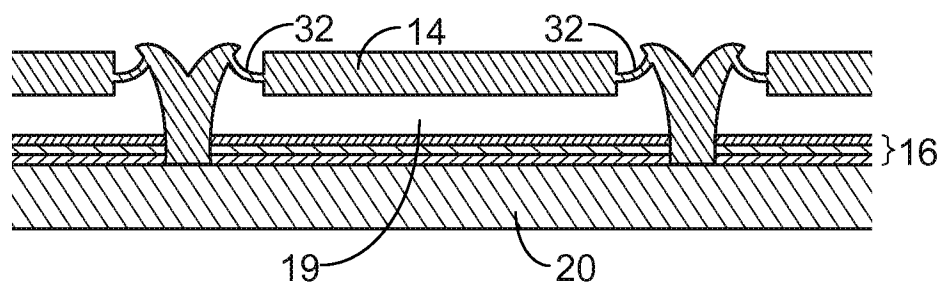


Figure 6B

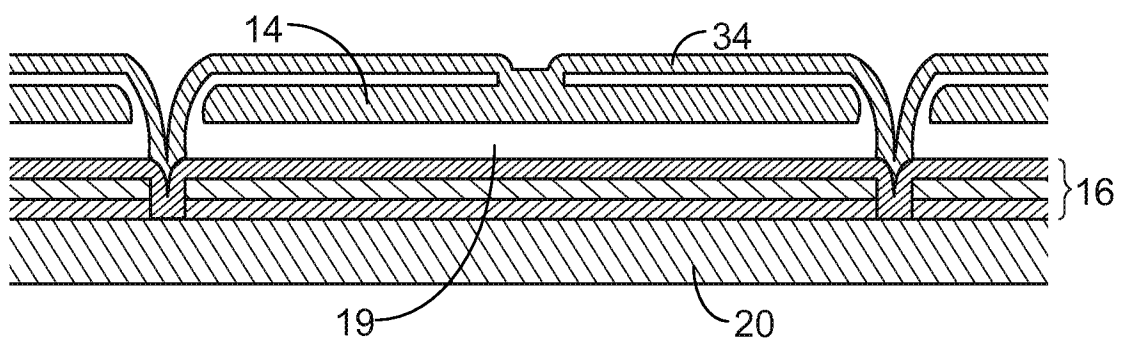


Figure 6C

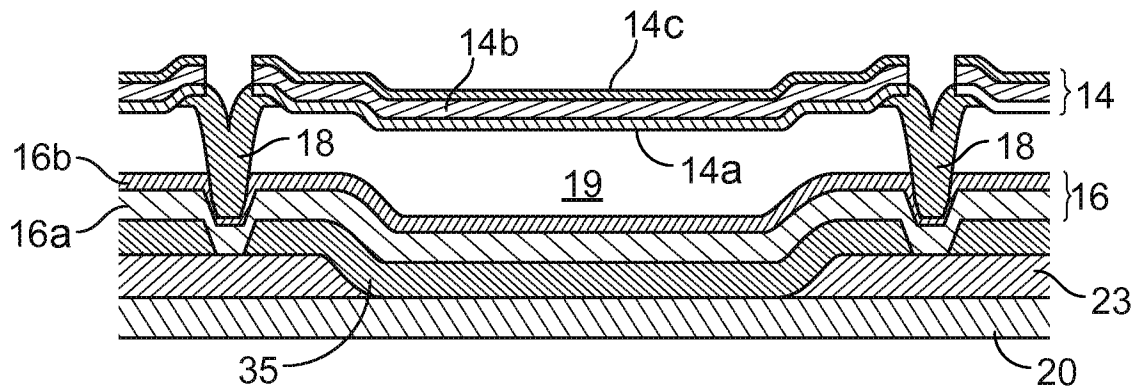


Figure 6D

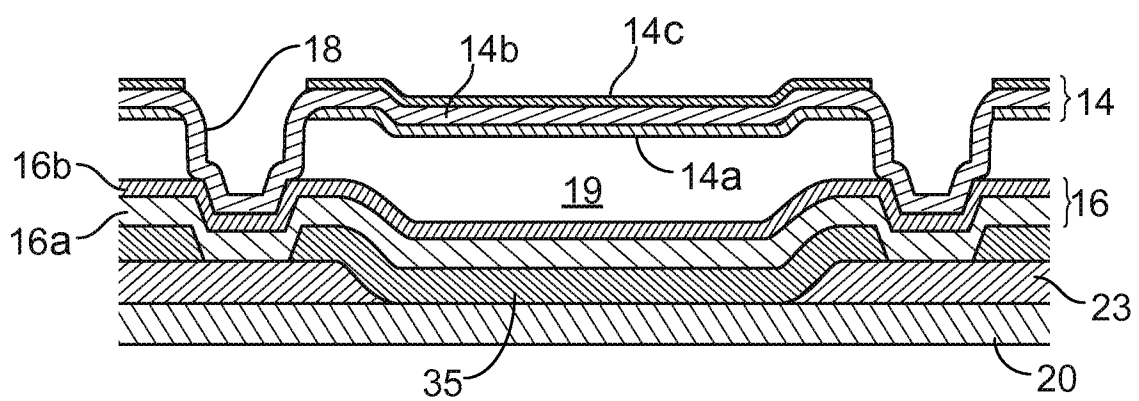
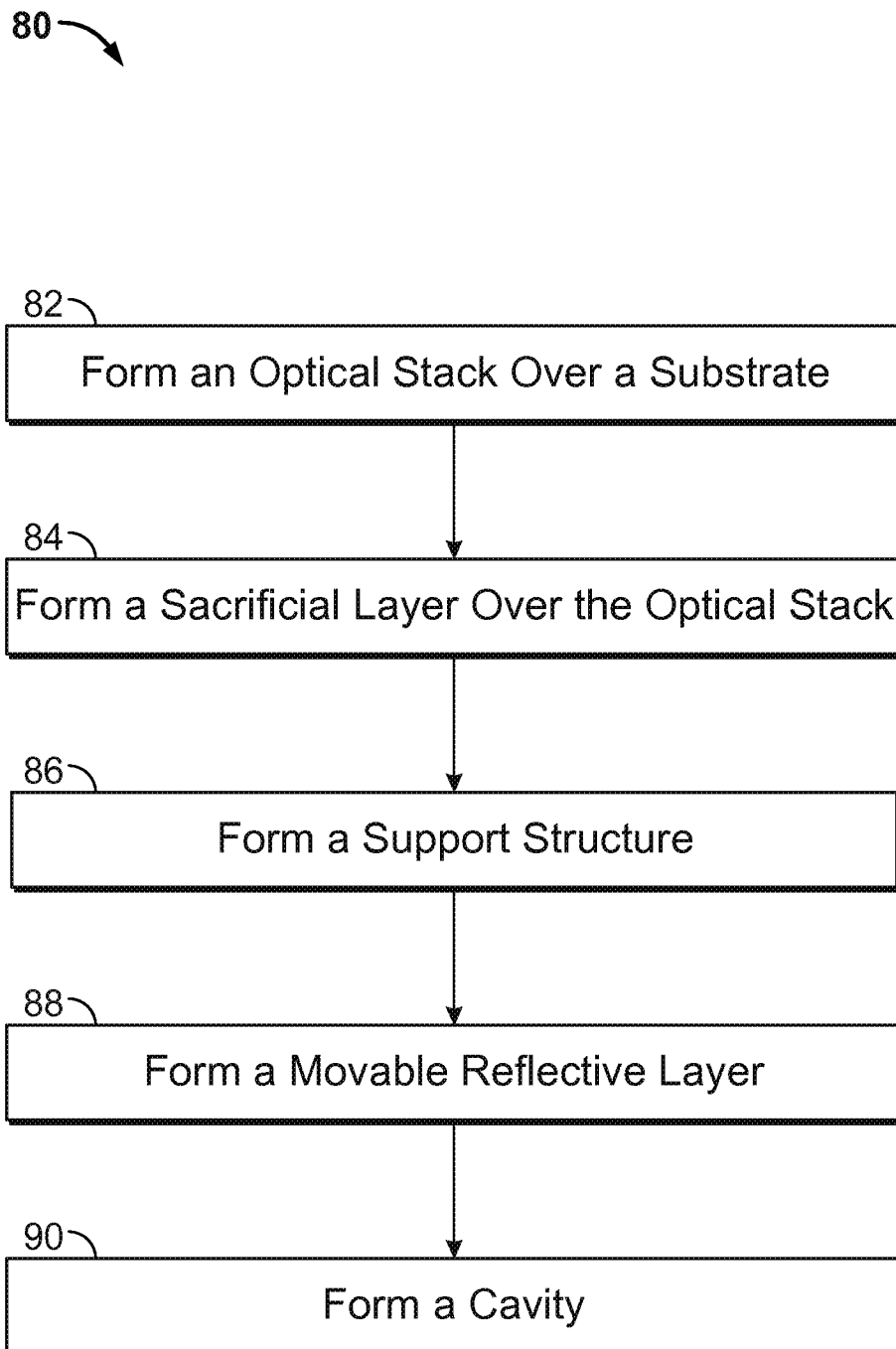


Figure 6E

**Figure 7**

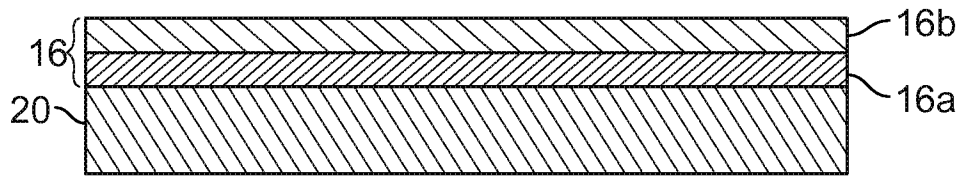


Figure 8A

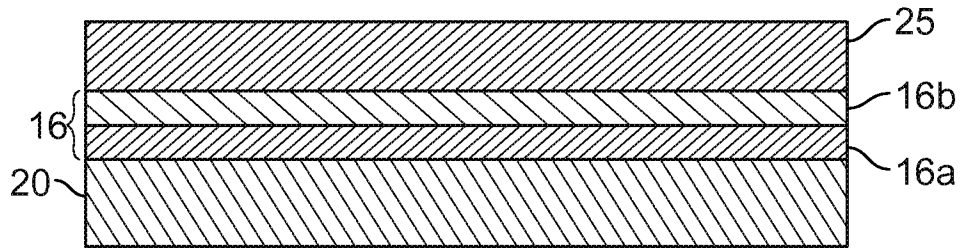


Figure 8B

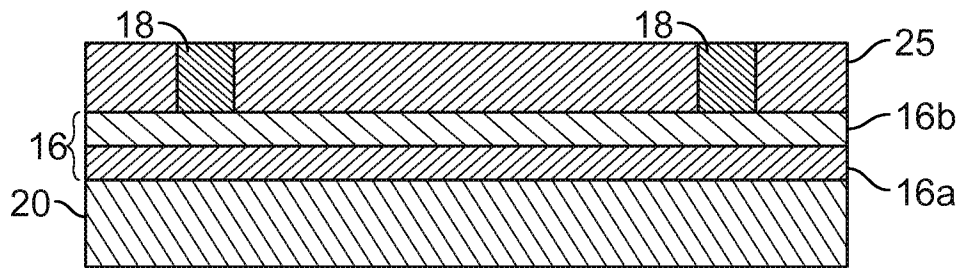


Figure 8C

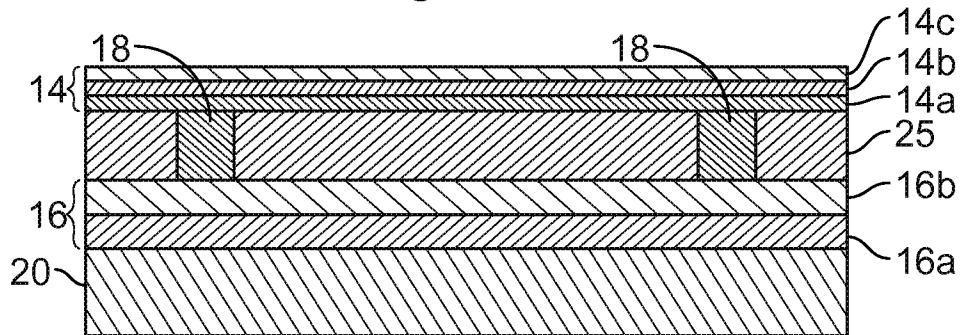


Figure 8D

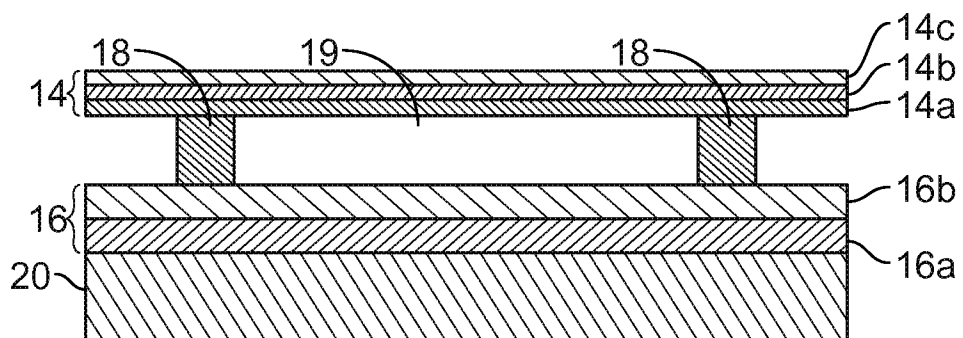
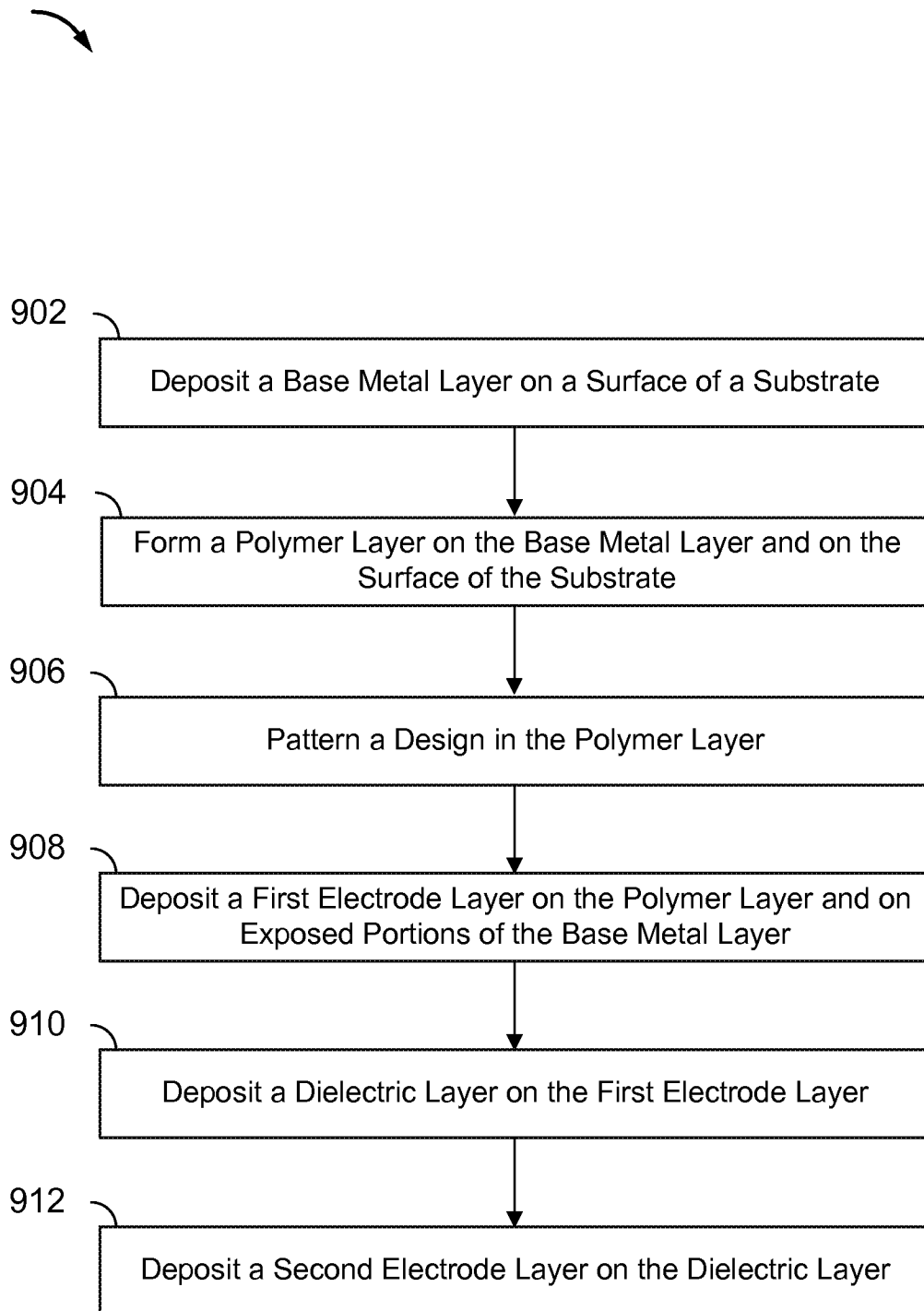
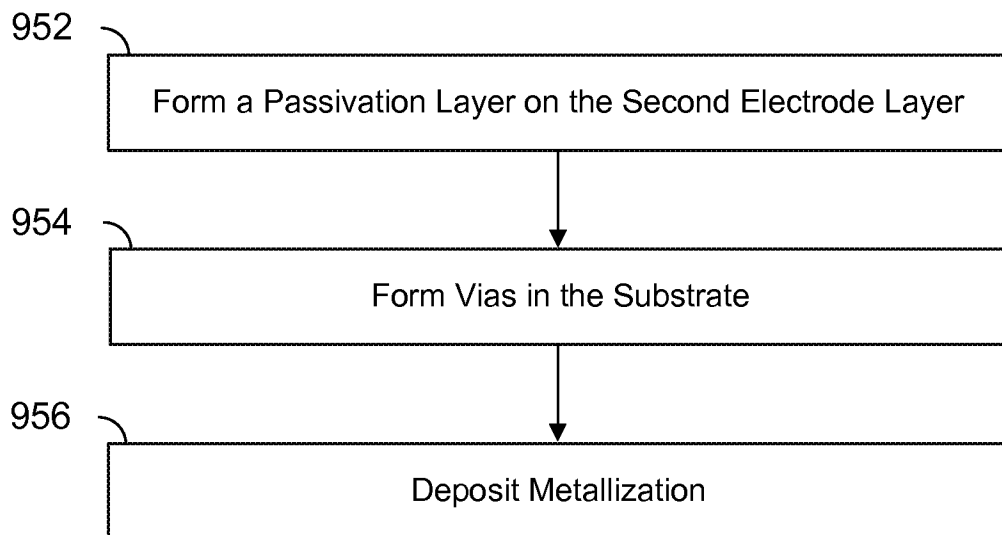


Figure 8E

900

**Figure 9A**

950

**Figure 9B**

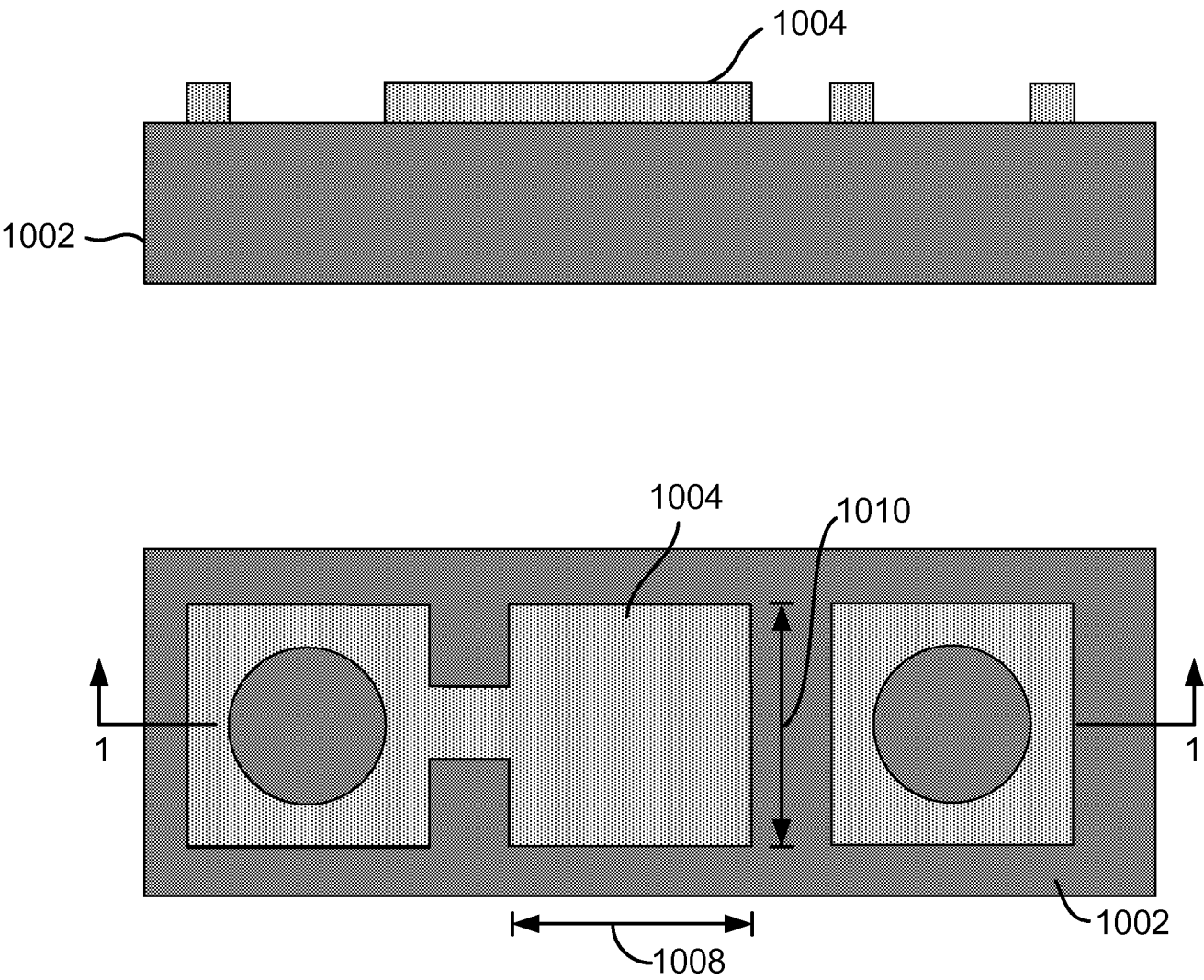


FIGURE 10A

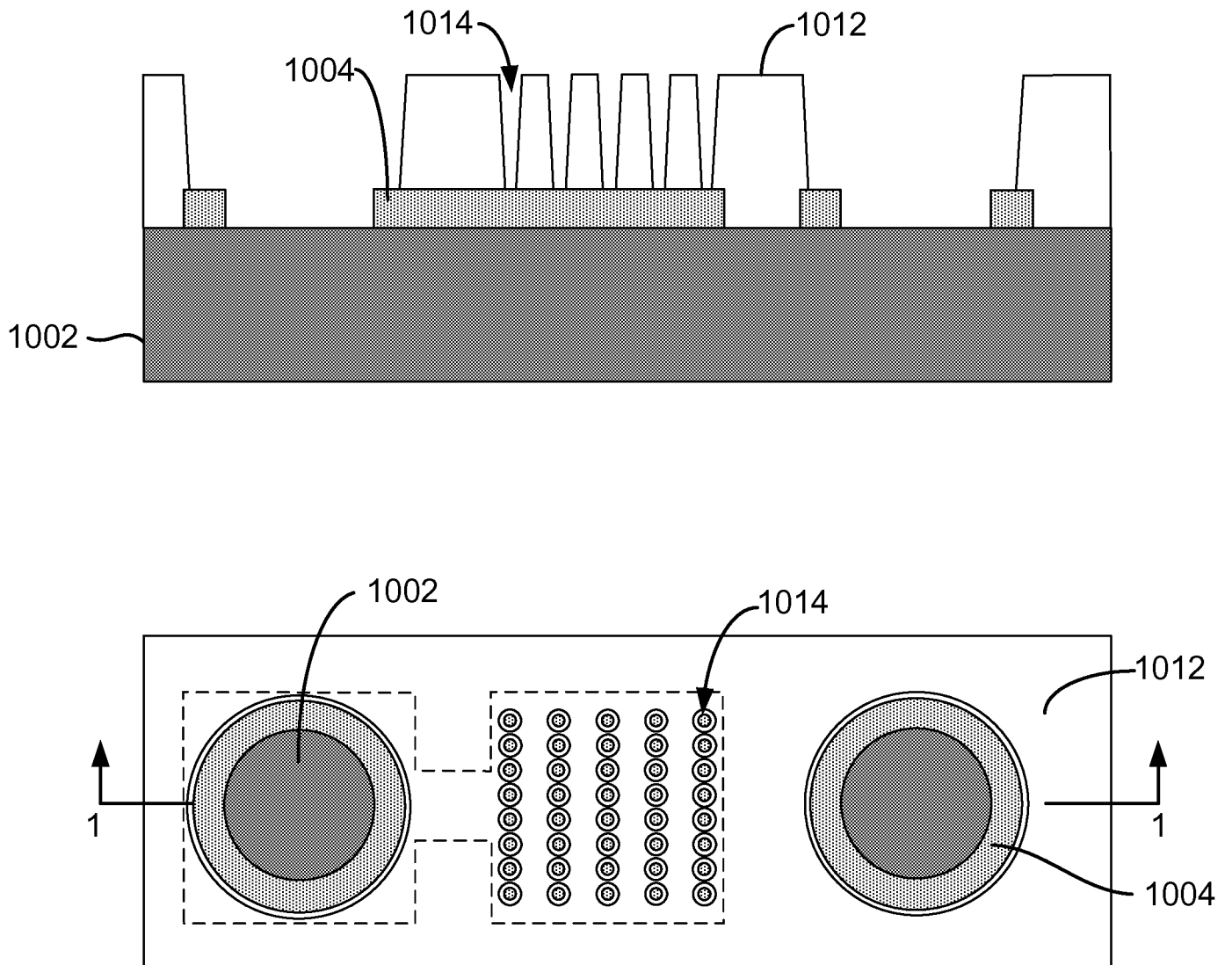


FIGURE 10B

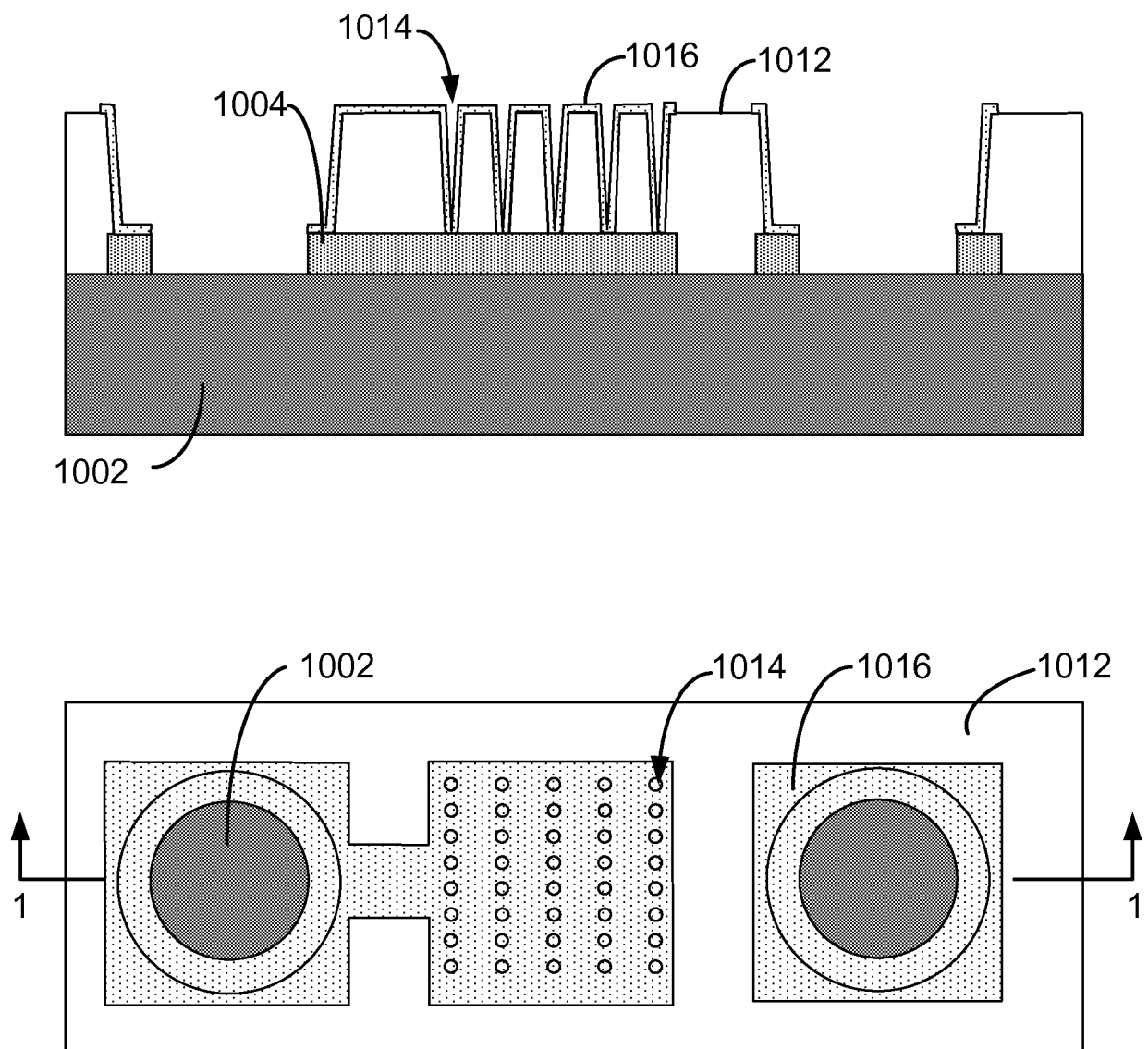


FIGURE 10C

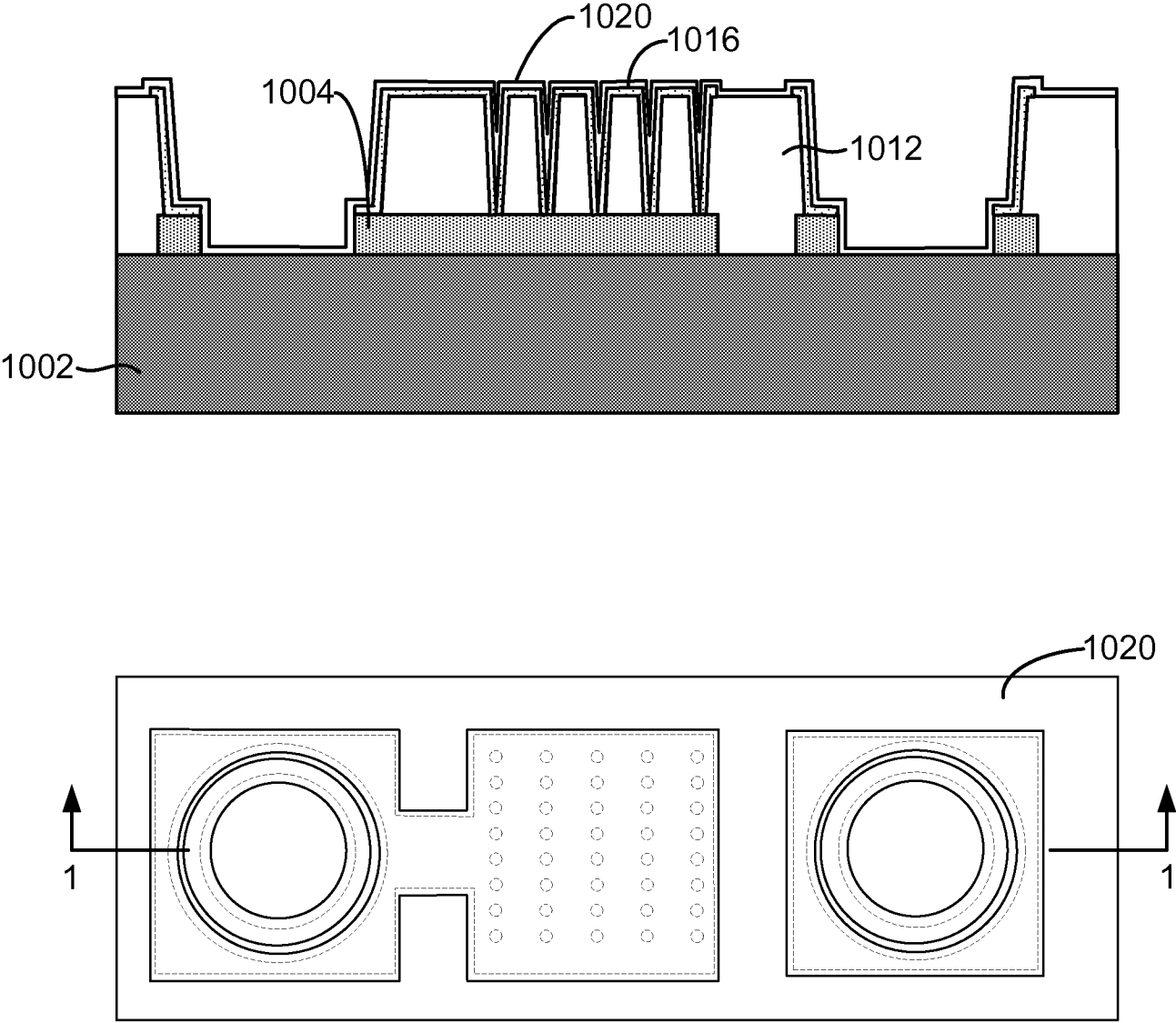


FIGURE 10D

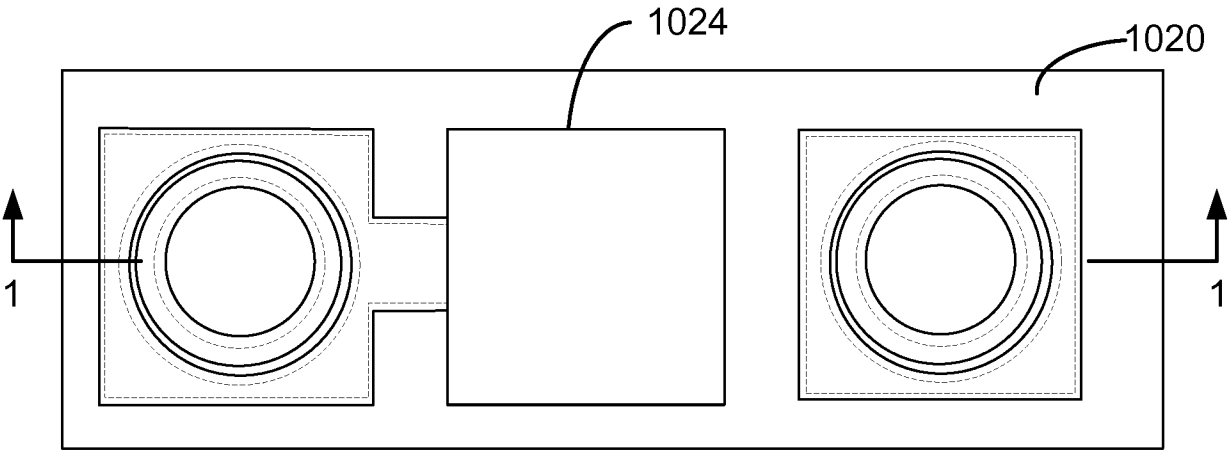
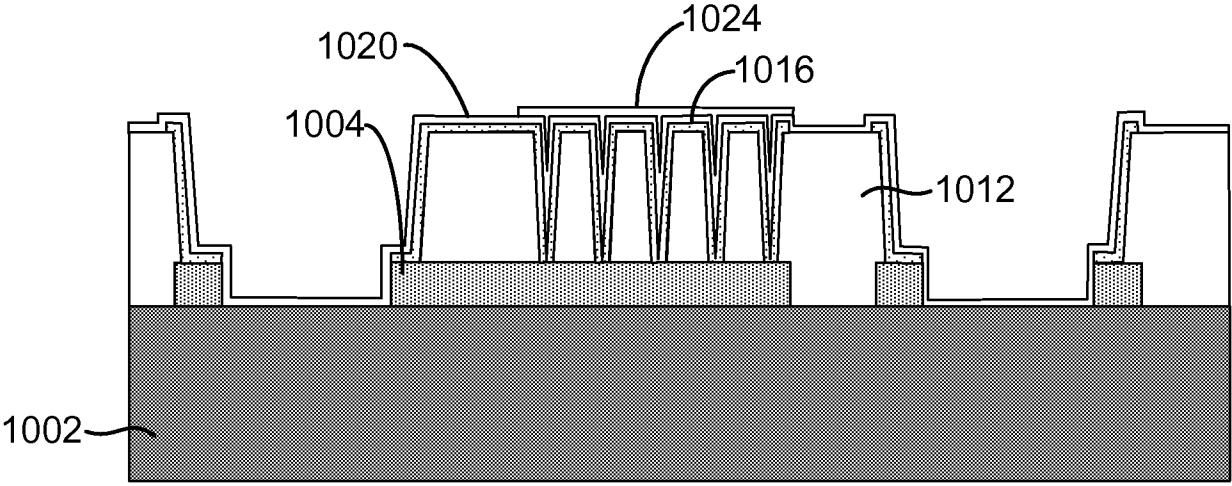


FIGURE 10E

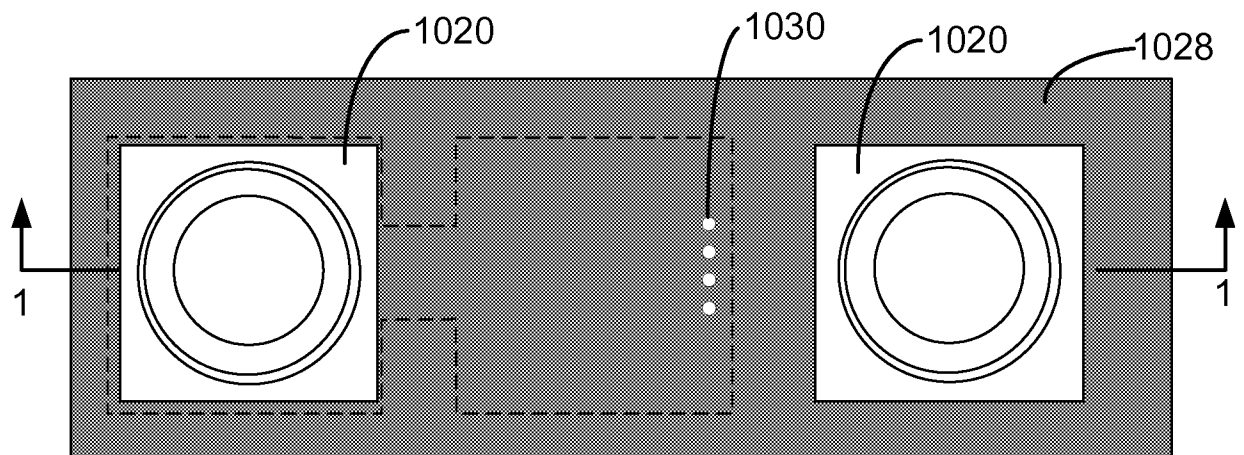
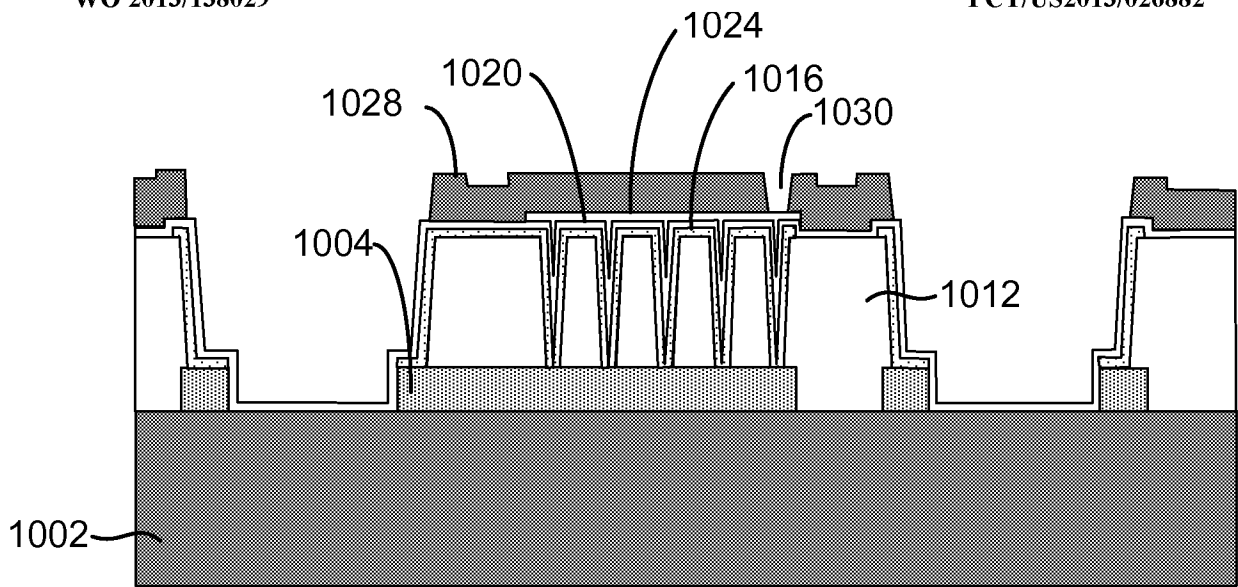


FIGURE 10F

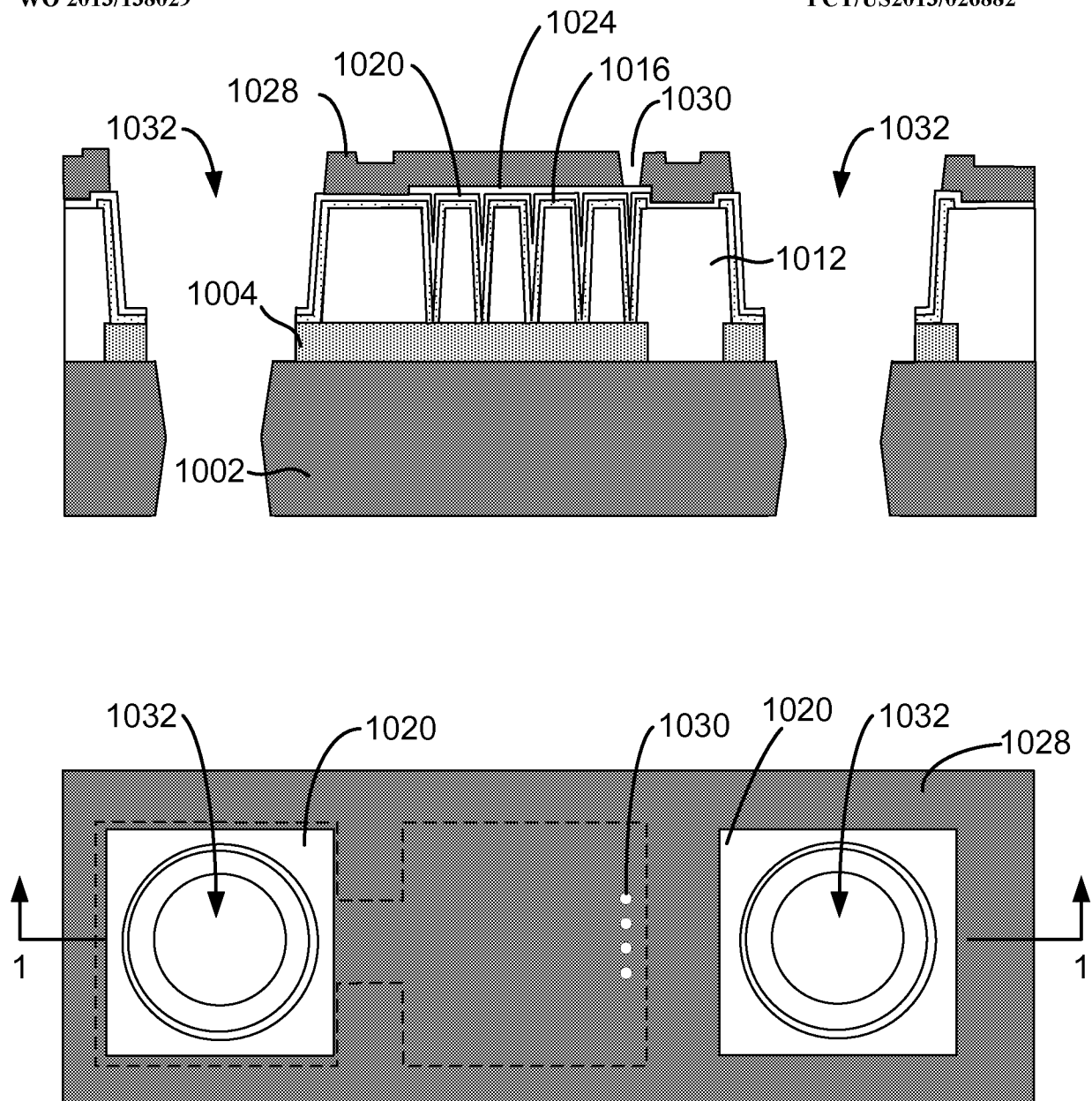


FIGURE 10G

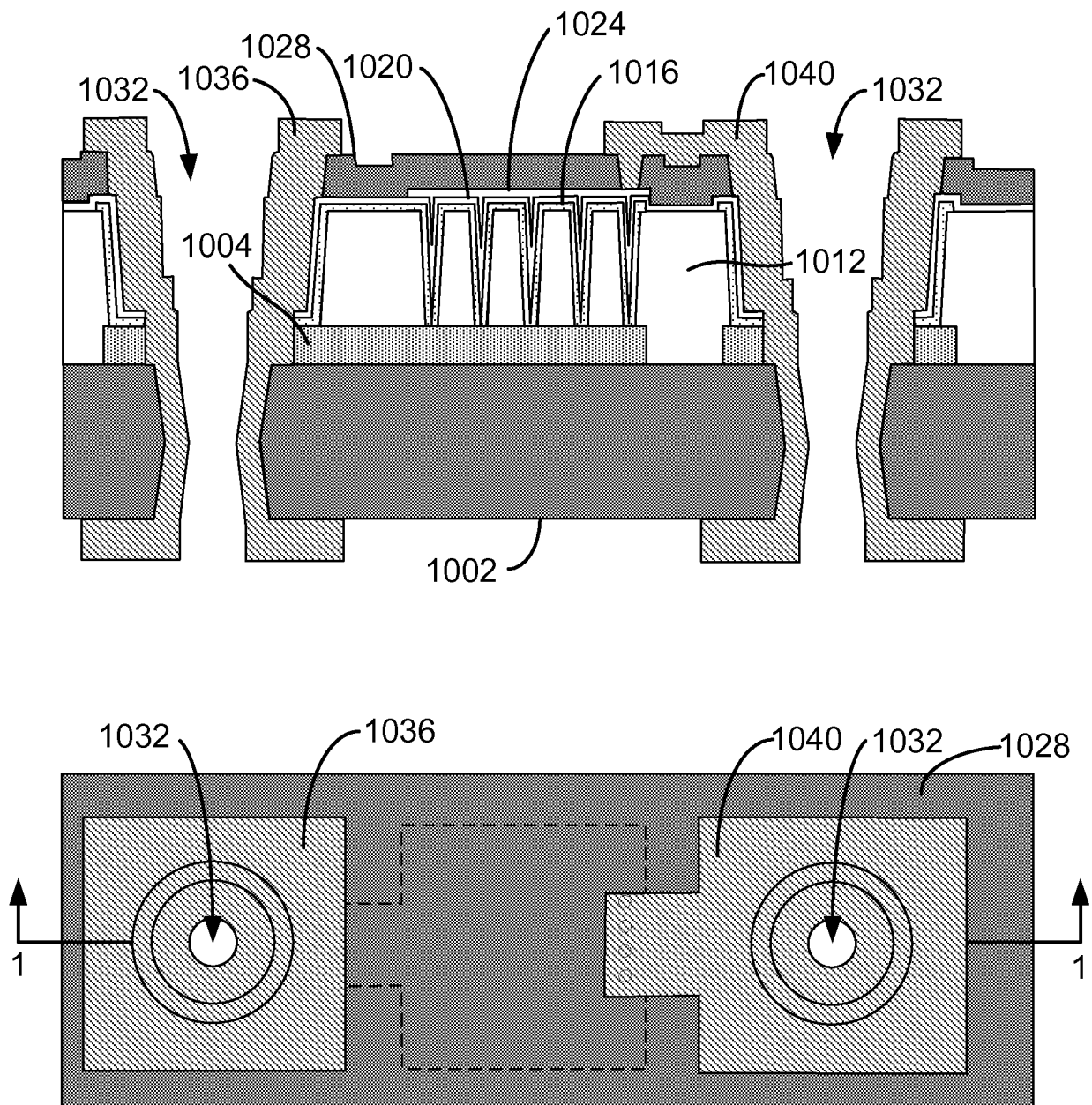


FIGURE 10H

FIGURE 11A

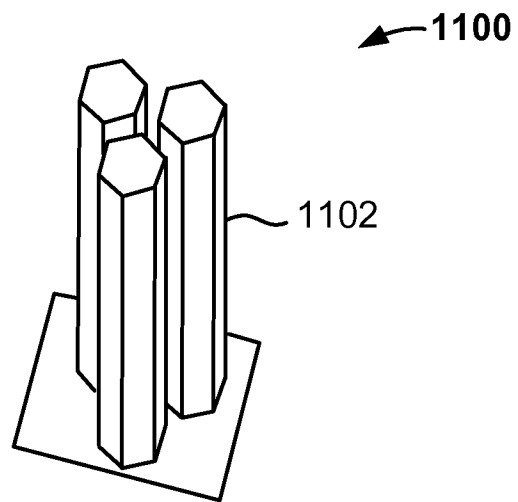


FIGURE 11B

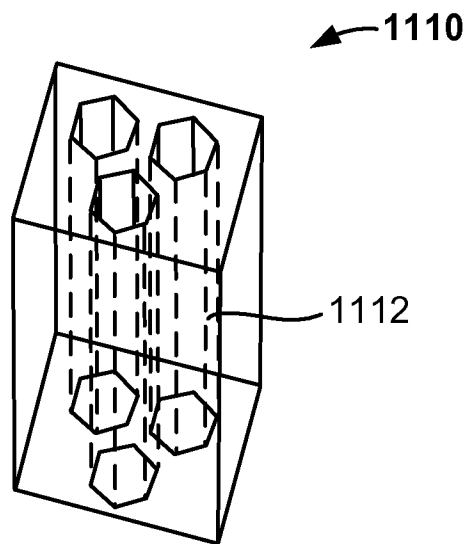
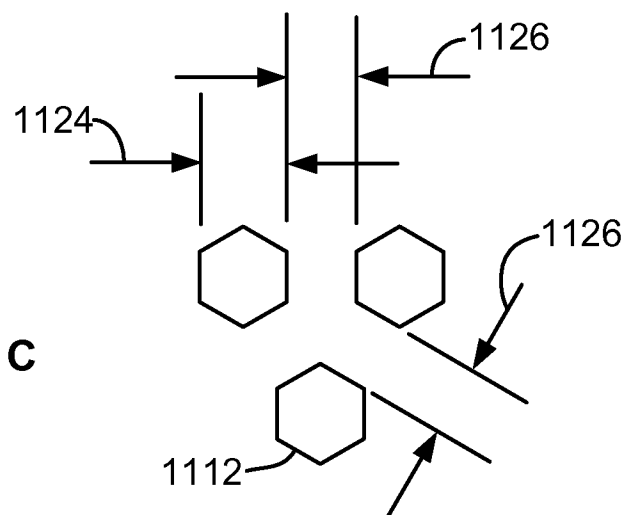
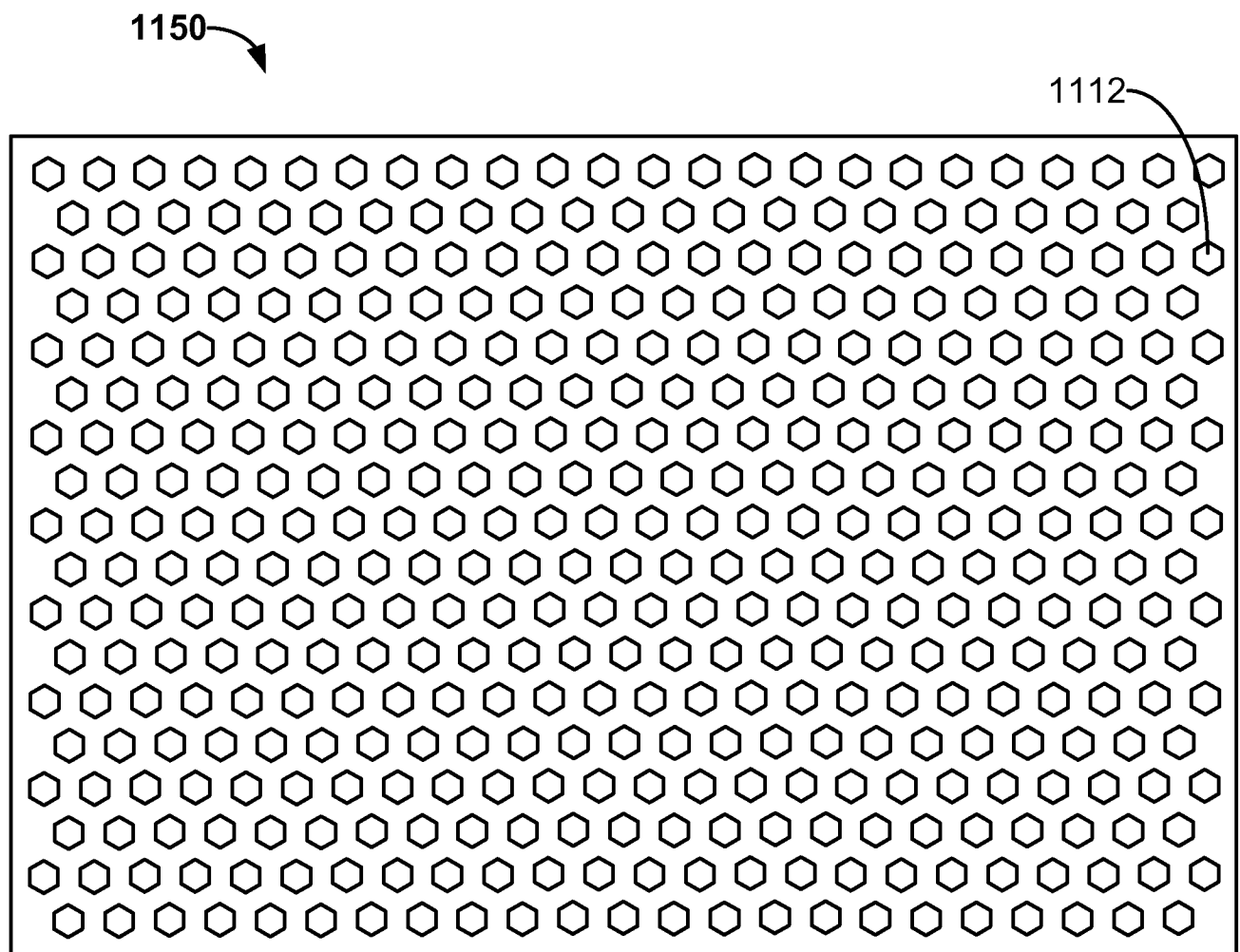


FIGURE 11C



**FIGURE 11D**

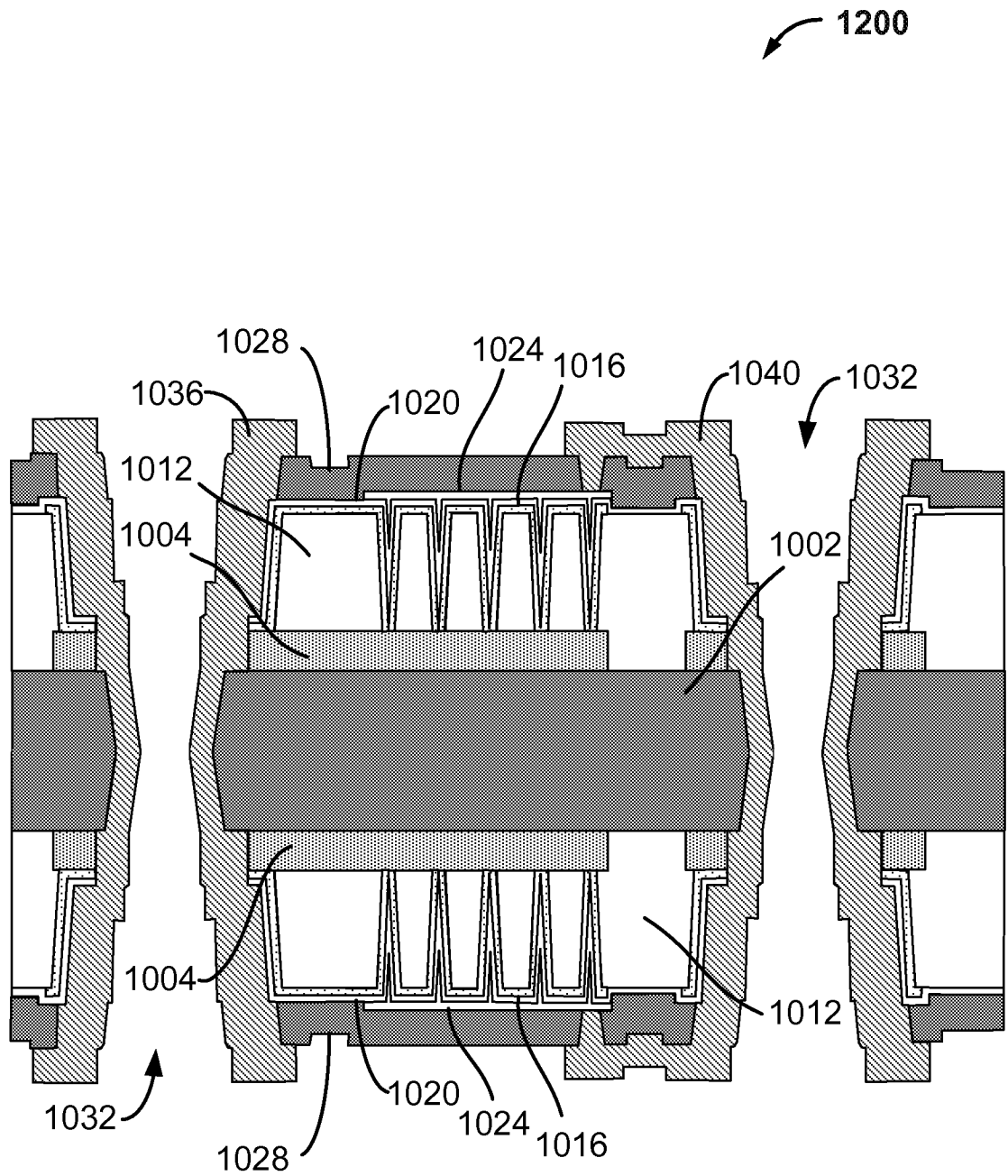


FIGURE 12

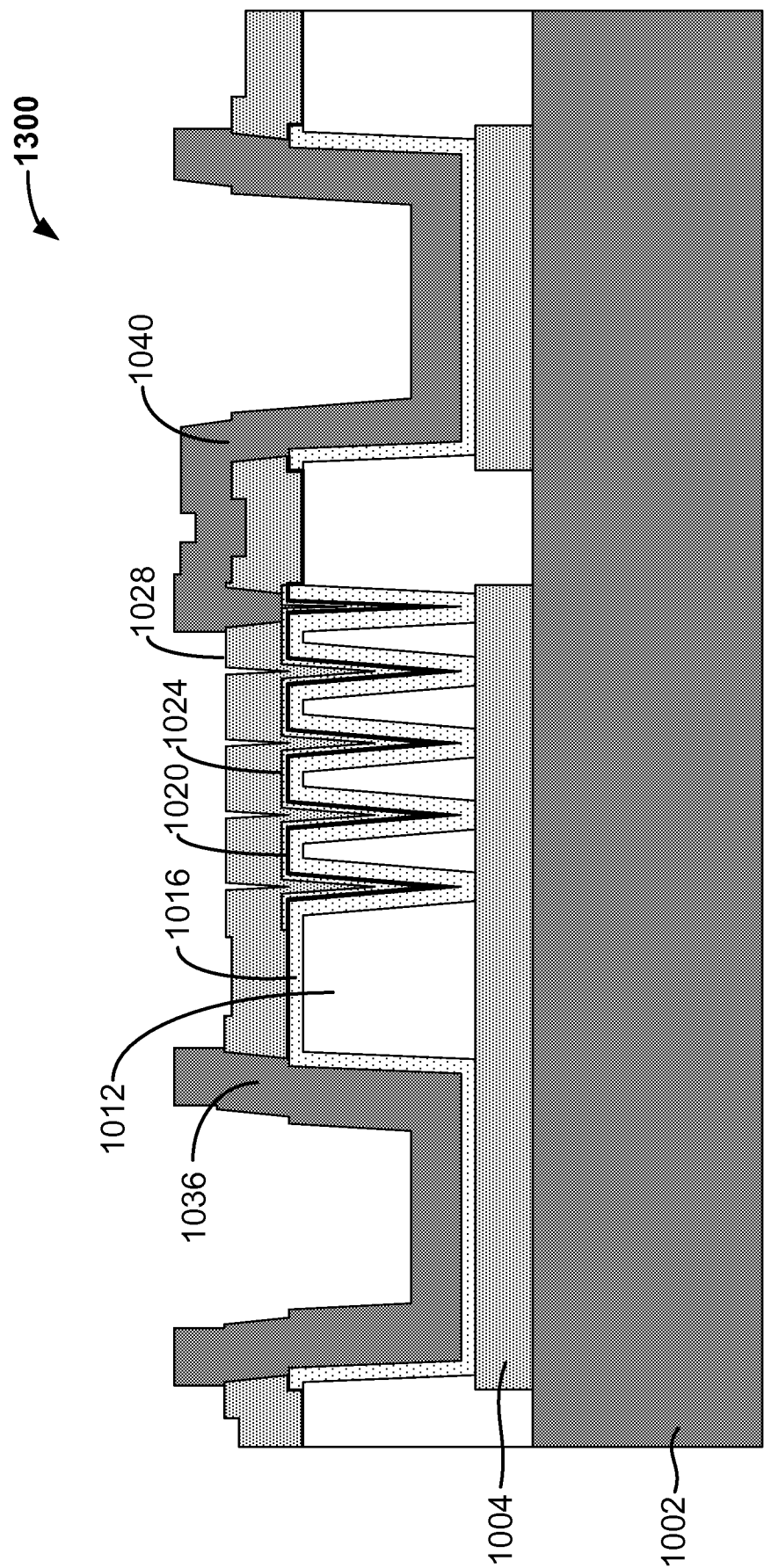


FIGURE 13

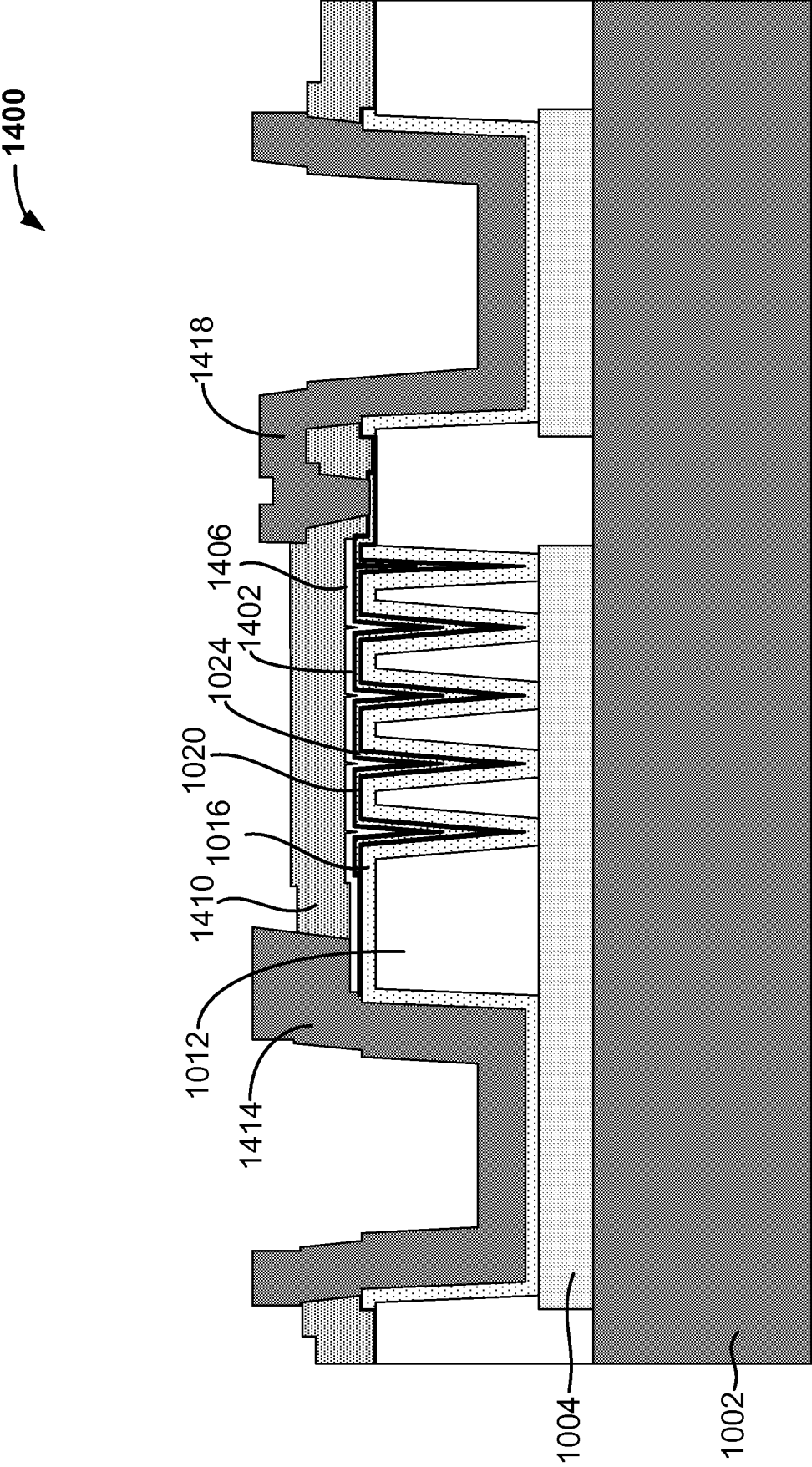


FIGURE 14

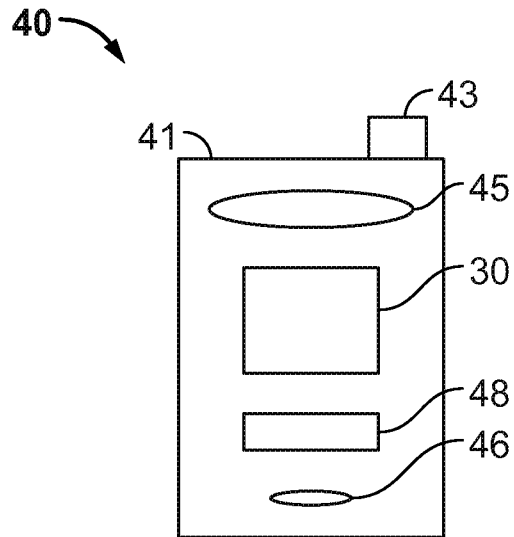


Figure 15A

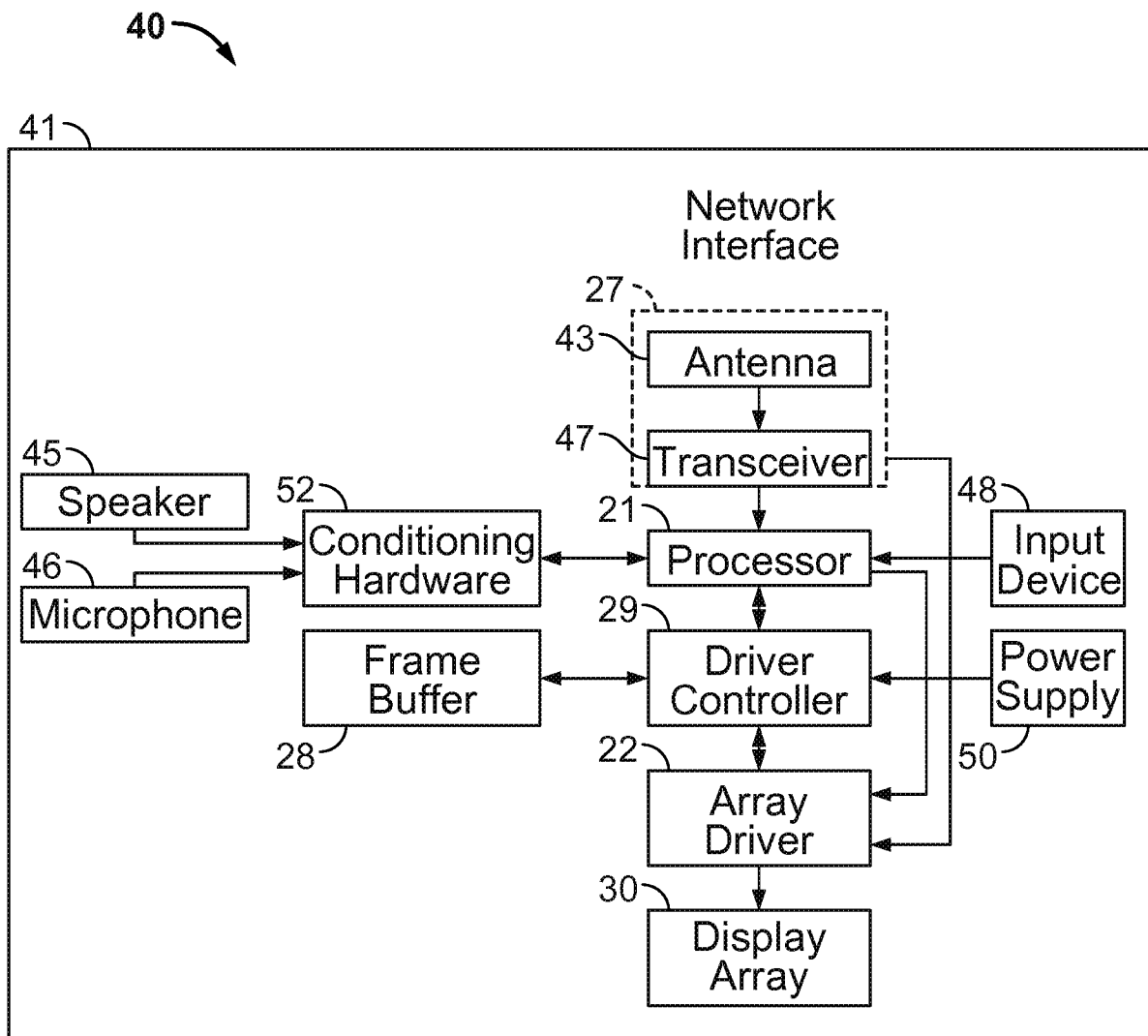


Figure 15B

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/026882

A. CLASSIFICATION OF SUBJECT MATTER

INV. H01L49/02 H01L23/64 H01L23/522
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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X A	US 2006/049524 A1 (LIN MOU-SHIUNG [TW] ET AL) 9 March 2006 (2006-03-09) abstract; figures 17b,c paragraphs [0085] - [0095], [0113] -----	1-6, 18-26 7-17
Y	US 2011/149374 A1 (LAN JE-HSIUNG [US] ET AL) 23 June 2011 (2011-06-23) abstract; figures 1-3E paragraphs [0017] - [0027] ----- -/-	13-17



Further documents are listed in the continuation of Box C.



See patent family annex.

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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Date of the actual completion of the international search

7 May 2013

Date of mailing of the international search report

15/05/2013

Name and mailing address of the ISA/

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040,
Fax: (+31-70) 340-3016

Authorized officer

Mosig, Karsten

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2013/026882

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y	US 2010/025095 A1 (GUO LI HUI [SG] ET AL) 4 February 2010 (2010-02-04) abstract; figure 4 paragraphs [0063] - [0071] -----	8-12

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No

PCT/US2013/026882

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