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Declarations under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

[Continued on next page]

(54) **Title**: LINEAR SYSTEM FOR LINK TRAINING

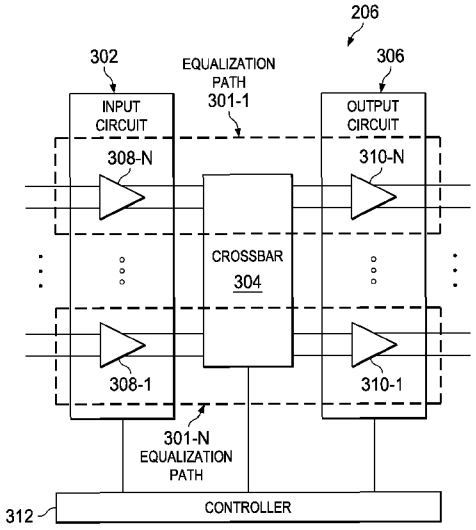

FIG. 3

(57) **Abstract**: An apparatus for equalizing channels is provided, which is generally transparent to link training. The apparatus generally includes equalization paths formed by an input circuit (302), a crossbar (304), an output circuit (306) and a controller (312). Each equalization path is coupled to at least one of the channels, and a controller has a VGA loop, a crossbar loop, and a driver loop. The AGC loop receives a first reference voltage and provides a gain control signal to the input circuit, and the gain control network comprises a replica of at least one of the equalization paths. The crossbar loop receives a second reference voltage and provides a crossbar control signal to the crossbar. The driver loop receives a third reference voltage and provides a driver control signal for the output circuit.

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— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

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LINEAR SYSTEM FOR LINK TRAINING

[0001] This relates generally to signal conditioning system and, more particularly, to linear signal conditioning system with gain control.

BACKGROUND

[0002] FIG. 1 shows an example of a conventional Automatic Gain Control (AGC) circuit 100. While the AGC circuit 100 is generally referred to having the characteristic of "gain control," it is actually an Automatic Level Control (ALC) circuit. In operation, the level detector 104 detects the level of the output signal OUT (usually peak level), and the controller 106 compares the level of the output signal OUT against a fixed (reference) level REF. Based on the results of this comparison, the controller 106 can then adjust, with control signal CNTL, the gain of the Variable Gain Amplifier (VGA) to generally maintain level of the output signal OUT. When the AGC circuit 100 is used in a linear signal conditioning device (such as a linear equalizer), the AGC circuit 100 is non-transparent to link training (i.e., the level of the output signal OUT does not respond to level changes in the input signal IN during link training) and may prevent optimal system configuration in terms of bit error rate, power, and electromagnetic interference (EMI). Additionally, limiting (non-linear) devices can distort the transmitter waveform and make it difficult for the receiver Decision Feedback Equalizer (DFE) to recover the data correctly. Thus, there is a need for an improved AGC circuit.

[0003] Some examples of conventional system are described in: U.S. Patent Nos. 6415003, 6421381 and 7050517; U.S. Patent Publ. No. 2003/0016770; and Hidaka et al., "A 4-Channel 1.25–10.3 Gb/s Backplane Transceiver Macro With 35 dB Equalizer and Sign-Based Zero-Forcing Adaptive Control," IEEE J. Solid-State Circuits, Vol. 44, No. 12, December 2009.

SUMMARY

[0004] An example embodiment provides an apparatus for equalizing a plurality of channels that is generally transparent to link training. The apparatus comprises a plurality of equalization paths formed by an input circuit, a crossbar, and an output circuit, wherein each equalization path is coupled to at least one of the channels; and a controller having: a gain

control loop that receives a first reference voltage and that provides a gain control signal to the input circuit, wherein the gain control loop includes a replica of at least one of the equalization paths; a crossbar loop that receives a second reference voltage and that provides a crossbar control signal to the crossbar; and a driver loop that receives a reference voltage and that provides a driver control signal for the output circuit.

[0005] In an example embodiment, the input circuit further comprises a plurality of variable gain amplifiers (VGAs), wherein each VGA is coupled to at least one of the channels and is coupled to the crossbar.

[0006] In an example embodiment, the output circuit further comprises a plurality of drivers that are each coupled to the crossbar.

[0007] In an example embodiment, the crossbar further comprises a plurality multiplexers wherein each multiplexer is coupled to each VGA and is coupled to at least one of the drivers.

[0008] In an example embodiment, the gain control loop further comprises: a replica VGA that receives the first reference voltage; a replica multiplexer that is couple to the replica VGA; a replica driver that is coupled to the replica multiplexer; and a control network that receives the first reference voltage, that is coupled to the replica driver, and that is coupled to each VGA of the input circuit.

[0009] In an example embodiment, the replica multiplexer further comprises a first replica multiplexer, and wherein the control network further comprises a first control network, and wherein the crossbar loop further comprises: a second replica multiplexer receives the second reference voltage; and a second control network that receives the second reference voltage, that is coupled to the second replica multiplexer, and that is coupled to each multiplexer of the crossbar.

[0010] In an example embodiment, the driver loop further comprises: a second replica driver receives the third reference voltage; and a third control network that receives the third reference voltage, that is coupled to the second replica driver, and that is coupled to each driver of the output circuit.

[0011] In an example embodiment, each of the first, second, and third control networks further comprise: a first voltage divider that receives receive one of the first, second, and third reference voltages; a second voltage divider is coupled to one of the first replica driver, the

second replica multiplexer, and the second replica driver; and a control signal generator that is coupled between the first and second voltage dividers.

[0012] In an example embodiment, the control signal generator further comprises: a difference amplifier that is coupled to each of the first and second voltage dividers; a filter that is coupled to the difference amplifier; a voltage-to-current (V2I) converter that is coupled to the filter; and a current mirror circuit that is coupled to the V2I converter.

[0013] In an example embodiment, an apparatus is provided. The apparatus comprises a transmitter having a plurality of channels; a transmission medium that is coupled to the transmitter; a receiver that is coupled to the transmission medium, wherein the receiver includes a linear equalizer that equalizes the plurality of channels and that is generally transparent to link training, and wherein the linear equalizer includes: a plurality of equalization paths formed by an input circuit, a crossbar, and an output circuit, wherein each equalization path is coupled to at least one of the channels; and a controller having: a gain control network that receives a first reference voltage and that provides a gain control signal to the input circuit, wherein the gain control network includes a replica of at least one of the equalization paths; a crossbar loop that receives a second reference voltage and that provides a crossbar control signal to the crossbar; and a driver loop that receives a this reference voltage and that provides a driver control signal for the output circuit.

[0014] In an example embodiment, the receiver further comprises a decision feedback equalizer (DFE), and wherein the linear equalizer is coupled between the transmission medium and the DFE.

[0015] In an example embodiment, the apparatus is a 10GBase-KR compliant communication system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] FIG. 1 is a diagram of an example of a conventional AGC circuit;

[0017] FIG. 2 is a diagram of an example of a system embodiment;

[0018] FIG. 3 is a diagram of an example of the linear equalizer of FIG. 2;

[0019] FIG. 4 is a diagram of an example of the controller of FIG. 3;

[0020] FIG. 5 is a diagram of an example of control signal generator of FIG. 4; and

[0021] FIG. 6 is a diagram depicting the function of the linear equalizer of FIG. 3.

DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

[0022] FIG. 2 illustrates an example of a communication system 200 embodiment implementing principles of the invention. This communication system 200 can, for example, be an Ethernet system compliant with the standards set forth in Institute of Electrical and Electronics Engineers (IEEE) 802.3ba, dated June 17, 2010, and/or IEEE 802.3ap dated June 25, 2010. Preferably, this system 200 can be compliant with 10GBase-KR (which is associated with these standards). Additionally, each of these standards is incorporated herein by reference for all purposes. This system 200 generally includes a transmitter 202 that can include several channels (i.e., 4 channels), a transmission medium 204 (which can be an Ethernet cable), and a receiver 206. The receiver generally includes a linear equalizer 206 and DFE 208 that can compensate (for example) for EMI and inter-symbol interference (ISI).

[0023] The linear equalizer 206 can be seen in greater detail in FIG. 3. As shown, the equalizer 206 generally includes equalization paths 301-1 to 301-N, where each equalization path 301-1 to 301-N generally corresponds to one of the channels. These paths 301-1 to 301-N are formed by portions of an input circuit 302, crossbar 304, and output circuit 306. Namely, the input circuit includes variable gain amplifiers (VGAs) 308-1 to 308-N (which each generally correspond to at least one of the channels), and the output circuit 306 generally includes drivers 310-1 to 310-N (which, again, each generally corresponds to at least one of the channels). The crossbar 304 generally includes multiplexers that are each coupled to each of the VGAs 308-1 to 308-N and to a driver 310-1 to 310-N so as to be generally associated with one of the channels. For the sake of simplicity of the drawings, the details of the crossbar 304 are not shown, and use of the crossbar 304 allows for dynamically reconfigurable equalization paths.

[0024] Also included within the linear equalizer 206 is a controller 312, which is shown in greater detail in FIG. 4. As shown, the controller 312 is generally comprised of a VGA loop 402, a crossbar loop 404, and a driver loop 406 (as well as other components that have been omitted for the sake of simplicity). Each of these loops 402, 404, and 406 is a replica of at least a portion of at least one of the equalization paths 301-1 to 301-N. This means that the components of these loops 402, 404, and 406 have components that are scaled down to reduce power/area, but and have gains equal or proportional components within the equalization paths 301-1 to 301-N. Specifically, the VGA loop is generally comprised of a replica VGA 410 (which can be a replica of at least one of VGAs 308-1 to 308-N), a replica multiplexer 412-1

(which can be a replica of at least one of the multiplexers of the crossbar 304), and a replica driver 412-1 (which can be a replica of at least one of the drivers 310-1 to 310-N). The crossbar loop 404 includes a replica multiplexer 412-2, and the driver loop generally includes a replica driver 414. Each of these loops 402, 404, and 406 also includes a control network 401-1 to 401-3, respectively, that employ a voltage dividers 416-1 to 416-3 and 420-1 to 420-3 and control signal generators 418-1 to 418-1 to 418-3.

[0025] In operation, these loops 402, 404, and 406 compare the output level to the input level (rather than the reference level) to generally maintain the channel gain (rather than the output level), which allows link training to be transparent. A reference voltage for each of these loops 402, 404, and 406 is generated by reference circuits 408-1 to 408-3 (which are typically bandgap circuits). The VGA loop 402 can then generate a gain control signal to adjust the gains of VGAs 308-1 to 308-N (where there is usually one signal for each VGA 308-1 to 308-N) and generally functions as the main AGC loop to (for example) remove residual errors from the equalization paths 310-1 to 310-N due to the finite loop gain. The crossbar loop 402 can generate a crossbar control signal to adjust the gains of multiplexers within the crossbar 304 (where there is usually one signal for each multiplexer), functioning generally as a nested AGC loop, and the driver loop 406 can generate a driver control signal to adjust the gains of drivers 310-1 to 310-N, (where there is usually one signal for each driver 310-1 to 310-N), functioning generally as a nested AGC loop. By using these three loops 402, 404, and 406, gain control can be maintained over process, supply voltage, and process variation, and, by employing the nested AGC loops, in particular, gain variation of each stage can be controlled while not introducing excessive noise amplification and non-linearity. Additionally, with the nested (localized) control loops, the gains are independent of configuration of equalization paths 301-1 to 301-N.

[0026] In order to generate the control signals from control networks 401-1 to 401-3, control signal generators 418-1 to 418-3 (which can be seen in greater detail in FIG. 5 and which are hereinafter referred to as 418) make comparisons between the input and output levels. Namely, the control signal generator 418 uses a difference amplifier 502 that compares the levels between the input and output signals (after passing through dividers 416-1 to 416-3 and 420-1 to 420-3). This difference is then filtered with filter 504 (which can, for example, be a low pass resistor-capacitor filter and which assists in maintaining loop stability) and converted to a current with voltage-to-current (V2I) converter 506. Using the current (which is proportional to the

difference between the input and output levels), current mirror circuit 508 can generate currents used to control the gains of the VGAs 308-1 to 308-N, multiplexers, or driver 310-1 to 310-N, as appropriate. The control currents are also more immune to local ground fluctuation than control voltages.

[0027] Turning now to FIG. 6, a comparison between the system 200 with and without gain control can be seen. As shown, the ratio between input and output voltage (i.e. gain) for the system 200 with gain control is much less variant than without gain control over a broad range. It should also be noted that the circuits of FIGS. 3-5 depict a differential arrangement, but it is also possible to employs the equalizer 206 in a single ended system.

[0028] Those skilled in the art to which the invention relates will appreciate that modifications may be made to the described embodiments, and also that many other embodiments are possible, within the scope of the claimed invention.

CLAIMS

What is claimed is:

1. An apparatus for equalizing a plurality of channels that is generally transparent to link training, the apparatus comprising:

a plurality of equalization paths formed by an input circuit, a crossbar, and an output circuit, wherein each equalization path is coupled to at least one of the channels; and

a controller having:

a gain control loop that receives a first reference voltage and that provides a gain control signal to the input circuit, wherein the gain control loop includes a replica of at least one of the equalization paths;

a crossbar loop that receives a second reference voltage and that provides a crossbar control signal to the crossbar; and

a driver loop that receives a this reference voltage and that provides a driver control signal for the output circuit.

2. The apparatus of Claim 1, wherein the input circuit further comprises a plurality of variable gain amplifiers (VGAs), wherein each VGA is coupled to at least one of the channels and is coupled to the crossbar.

3. The apparatus of Claim 2, wherein the output circuit further comprises a plurality of drivers that are each coupled to the crossbar.

4. The apparatus of Claim 3, wherein the crossbar further comprises a plurality multiplexers wherein each multiplexer is coupled to each VGA and is coupled to at least one of the drivers.

5. The apparatus of Claim 4, wherein the gain control loop further comprises:

a replica VGA that receives the first reference voltage;

a replica multiplexer that is couple to the replica VGA;

a replica driver that is coupled to the replica multiplexer; and

a control network that receives the first reference voltage, that is coupled to the replica driver, and that is coupled to each VGA of the input circuit.

6. The apparatus of Claim 5, wherein the replica multiplexer further comprises a first replica multiplexer, and wherein the control network further comprises a first control network, and wherein the crossbar loop further comprises:

a second replica multiplexer receives the second reference voltage; and

a second control network that receives the second reference voltage, that is coupled to the second replica multiplexer, and that is coupled to each multiplexer of the crossbar.

7. The apparatus of Claim 6, wherein the driver loop further comprises:

a second replica driver receives the third reference voltage; and

a third control network that receives the third reference voltage, that is coupled to the second replica driver, and that is coupled to each driver of the output circuit.

8. The apparatus of Claim 7, wherein each of the first, second, and third control networks further comprise:

a first voltage divider that receives receive one of the first, second, and third reference voltages;

a second voltage divider is coupled to one of the first replica driver, the second replica multiplexer, and the second replica driver; and

a control signal generator that is coupled between the first and second voltage dividers.

9. The apparatus of Claim 8, wherein the control signal generator further comprises:

a difference amplifier that is coupled to each of the first and second voltage dividers;

a filter that is coupled to the difference amplifier;

a voltage-to-current (V2I) converter that is coupled to the filter; and

a current mirror circuit that is coupled to the V2I converter.

10. An apparatus comprising:

a transmitter having a plurality of channels;

a transmission medium that is coupled to the transmitter;

a receiver that is coupled to the transmission medium, wherein the receiver includes a linear equalizer that equalizes the plurality of channels and that is generally transparent to link training, and wherein the linear equalizer includes:

a plurality of equalization paths formed by an input circuit, a crossbar, and an output circuit, wherein each equalization path is coupled to at least one of the channels; and

a controller having:

a gain control loop that receives a first reference voltage and that provides a gain control signal to the input circuit, wherein the gain control loop includes a replica of at least one of the equalization paths;

a crossbar loop that receives a second reference voltage and that provides a crossbar control signal to the crossbar; and

a driver loop that receives a this reference voltage and that provides a driver control signal for the output circuit.

11. The apparatus of Claim 10, wherein the input circuit further comprises a plurality of VGAs, wherein each VGA is coupled to at least one of the channels and is coupled to the crossbar.

12. The apparatus of Claim 11, wherein the output circuit further comprises a plurality of drivers that are each coupled to the crossbar.

13. The apparatus of Claim 12, wherein the crossbar further comprises a plurality multiplexers wherein each multiplexer is coupled to each VGA and is coupled to at least one of the drivers.

14. The apparatus of Claim 13, wherein the gain control loop further comprises:

a replica VGA that receives the first reference voltage;

a replica multiplexer that is couple to the replica VGA;

a replica driver that is coupled to the replica multiplexer; and

a control network that receives the first reference voltage, that is coupled to the replica driver, and that is coupled to each VGA of the input circuit.

15. The apparatus of Claim 14, wherein the replica multiplexer further comprises a first replica multiplexer, and wherein the control network further comprises a first control network, and wherein the crossbar loop further comprises:

a second replica multiplexer receives the second reference voltage; and

a second control network that receives the second reference voltage, that is coupled to the second replica multiplexer, and that is coupled to each multiplexer of the crossbar.

16. The apparatus of Claim 15, wherein the driver loop further comprises:

a second replica driver receives the third reference voltage; and

a third control network that receives the third reference voltage, that is coupled to the second replica driver, and that is coupled to each driver of the output circuit.

17. The apparatus of Claim 16, wherein each of the first, second, and third control networks further comprise:

a first voltage divider that receives receive one of the first, second, and third reference voltages;

a second voltage divider is coupled to one of the first replica driver, the second replica multiplexer, and the second replica driver; and

a control signal generator that is coupled between the first and second voltage dividers.

18. The apparatus of Claim 17, wherein the control signal generator further comprises:

a difference amplifier that is coupled to each of the first and second voltage dividers;

a filter that is coupled to the difference amplifier;

a voltage-to-current (V2I) converter that is coupled to the filter; and

a current mirror circuit that is coupled to the V2I converter.

19. The apparatus of Claim 18, wherein the transmitter further comprises a decision feedback equalizer (DFE), and wherein the linear equalizer is coupled between the transmission medium and the DFE.

20. The apparatus of Claim 19, wherein the apparatus is a 10GBase-KR compliant communication system.

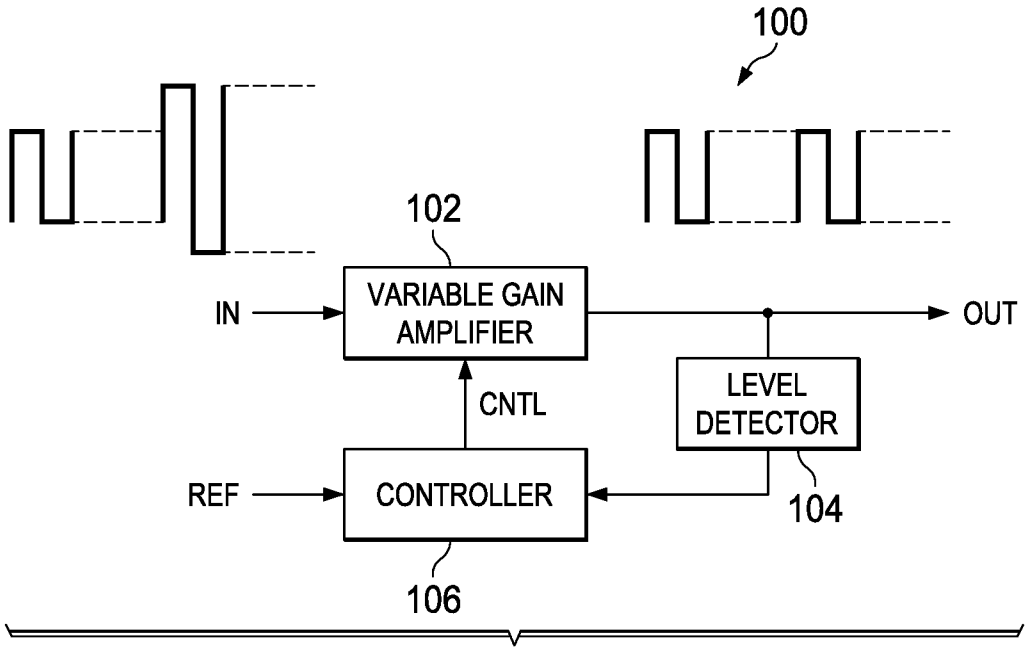


FIG. 1
(PRIOR ART)

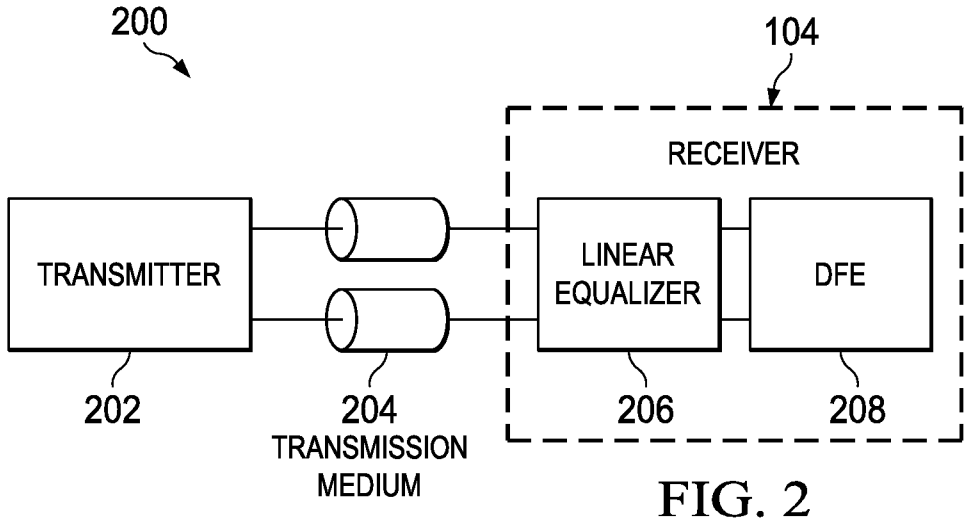


FIG. 2

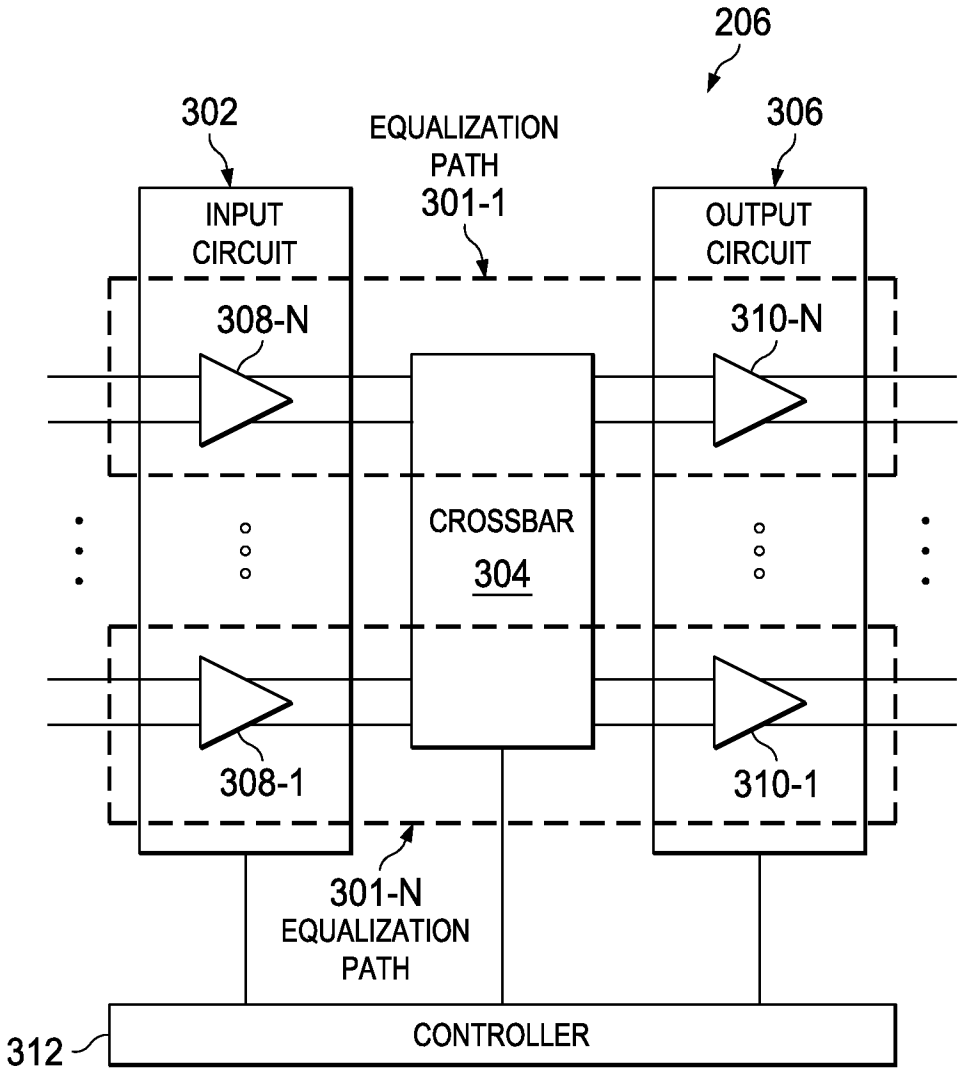

206
302
EQUALIZATION PATH
301-1
306
INPUT CIRCUIT
OUTPUT CIRCUIT
308-N
310-N
CROSSBAR
304
308-1
310-1
301-N
EQUALIZATION PATH
312
CONTROLLER

FIG. 3

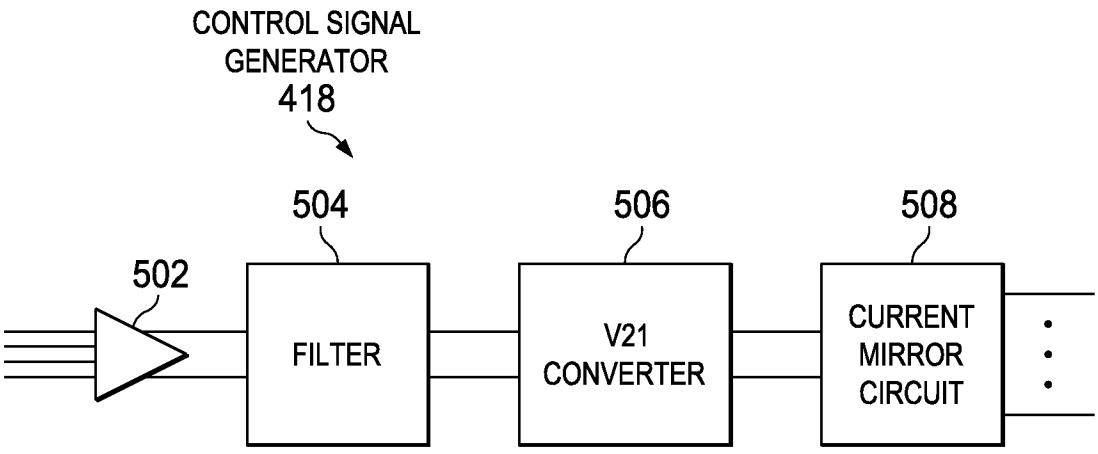
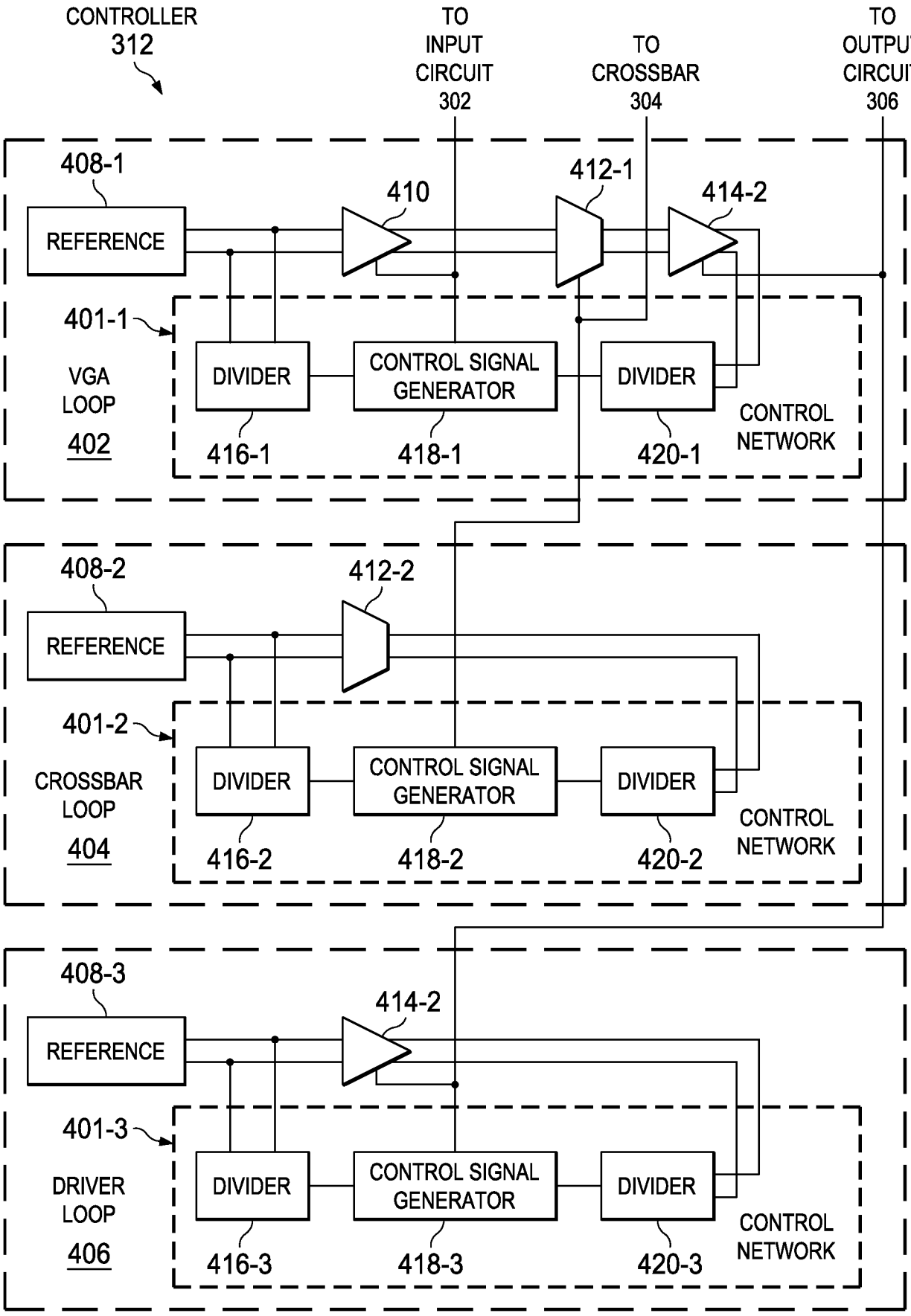

CONTROL SIGNAL GENERATOR
418
504
506
508
502
FILTER
V21 CONVERTER
CURRENT MIRROR CIRCUIT

FIG. 5


CONTROLLER
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TO
INPUT
CIRCUIT
302
TO
CROSSBAR
304
TO
OUTPUT
CIRCUIT
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414-2
401-1
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LOOP
402
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CONTROL SIGNAL
GENERATOR
DIVIDER
CONTROL
NETWORK
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418-1
420-1
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401-2
CROSSBAR
LOOP
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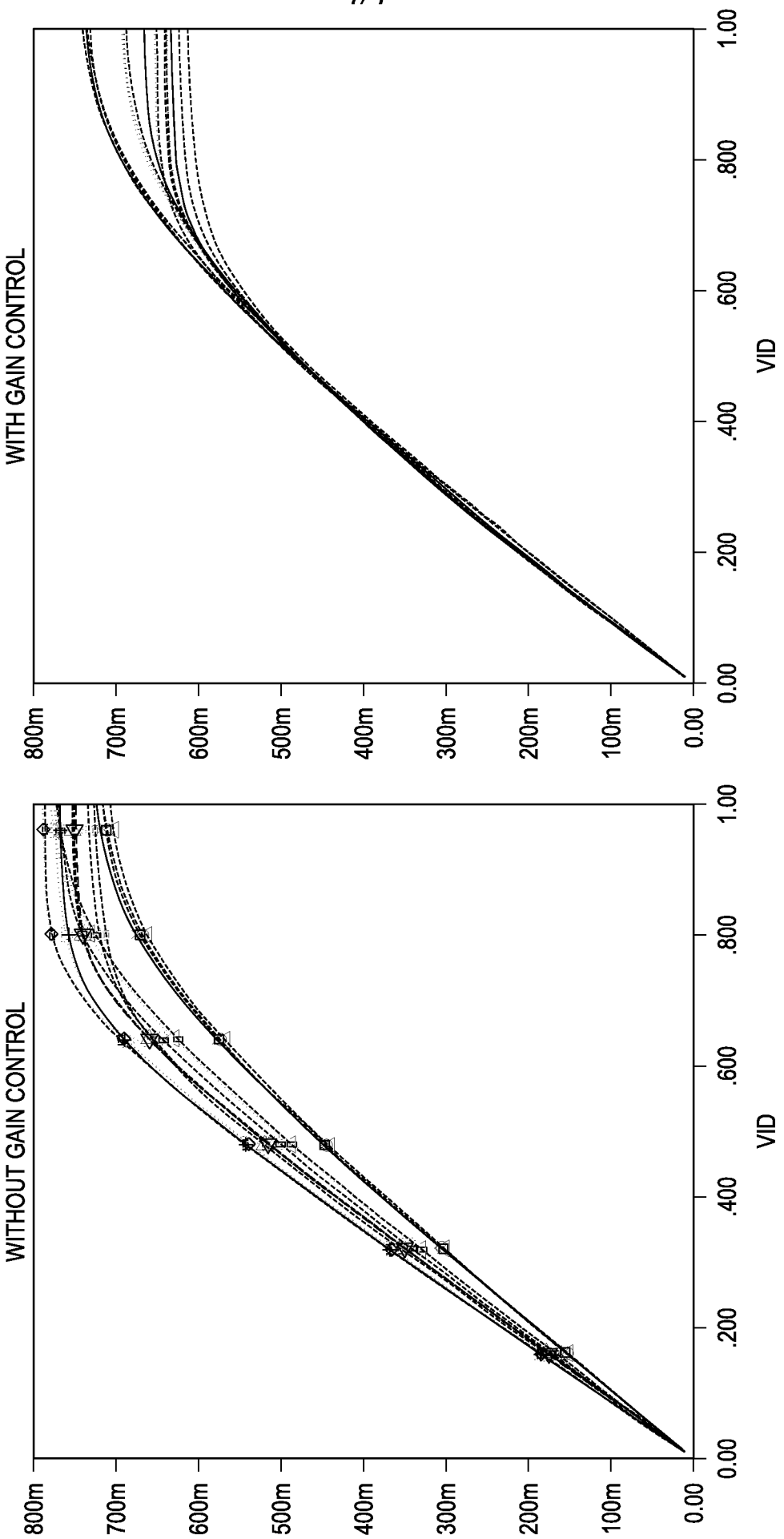
FIG. 4

FIG. 6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VID

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2012/062413

A. CLASSIFICATION OF SUBJECT MATTER

H04L 27/01(2006.01)i, H03G 3/20(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H04L 27/01; H03G 3/30; H03D 1/04; H04L 27/36; H04L 25/03; H03K 5/159; H03H 7/30

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: equalization, path, linear, gain, control, crossbar

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 7180941 B2 (APU SIVADAS et al.) 20 February 2007 See column 4, line 48; column 6, line 30; column 8, line 8; and figures 10-14.	1-20
A	US 2006-0188043 A1 (JARED L. ZERBE et al.) 24 August 2006 See paragraphs 35-41; and figure 1.	1-20
A	US 2010-0194478 A1 (XAVIER MAILLARD) 5 August 2010 See paragraphs 53-65; and figures 1, 2.	1-20
A	US 2011-0170632 A1 (JOEL L. DANZIG et al.) 14 July 2011 See paragraphs 15-24; claims 1, 9; and figures 1, 2.	1-20
A	US 2009-0304066 A1 (ERIK CHMELAR et al.) 10 December 2009 See paragraphs 24-28; claim 1; and figure 2a.	1-20

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
20 MARCH 2013 (20.03.2013)	**22 MARCH 2013 (22.03.2013)**

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