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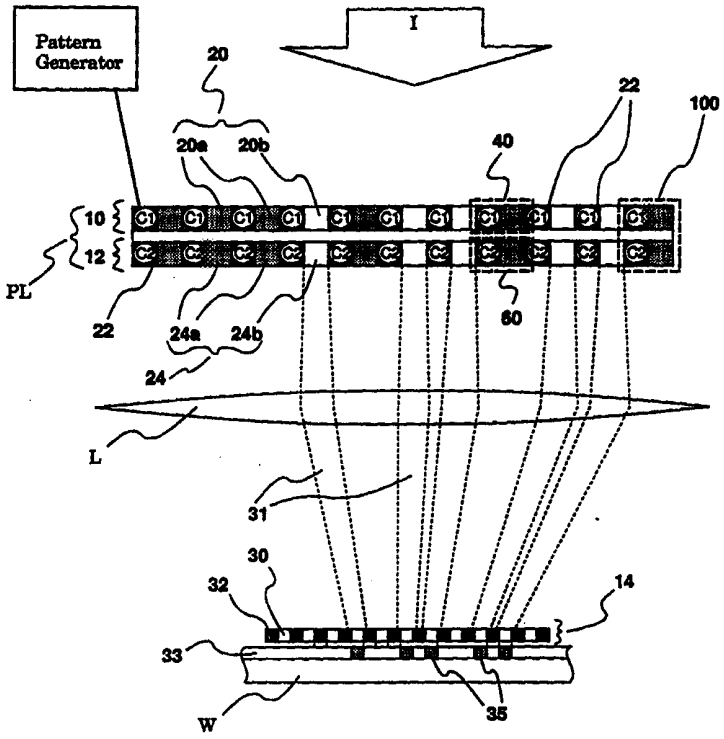
(54) Title: TRANSFERRING A PROGRAMMABLE PATTERN BY PHOTON LITHOGRAPHY

(57) Abstract

A programmable structure for exposing a wafer (W) allows the lithographic pattern to be changed under electronic control. The programmable structure comprises a programmable array of shutters (12) and may include a programmable array of selective amplifiers (10). The shutters and selective amplifiers can work in tandem to form a "programmable layer" (PL). A diffraction limiter (14) can be used to provide projection lithography with certain advantages associated with contact lithography without requiring some of the disadvantages of contact lithography.



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TRANSFERRING A PROGRAMMABLE PATTERN BY PHOTON LITHOGRAPHY

Cross-Reference to Related Applications

This application claims the benefit of U.S. Provisional Application No. 60/051,121 filed 27 June 1997 entitled "A Shutter For a Programmable Photon Lithography Mask"; U.S. Provisional Application No. 60/058,701 filed 12 September 1997 entitled "A Doped Solid-State Lithography Mask"; U.S. Provisional Application No. 60/058,702 filed 12 September 1997 entitled "A Device to Improve Resolution In Lithography Using A Programmable Mask"; and U.S. Provisional Application No. 60/060,254 filed 29 September 1997 entitled "A Selective Amplifier For a Programmable Photon Lithography Mask."

Field of Invention

This invention relates to microfabrication, and more particularly to systems, methods, and techniques for manufacturing integrated circuit chips using photon lithography. Still more particularly, the present invention relates to systems, methods, and techniques in connection with programmable masks for microlithography.

Background and Summary of the Invention

Lithography is used to transfer a specific pattern onto a surface. Lithography can be used to transfer a variety of patterns including, for example, painting, printing, and the like. More recently, lithographic techniques have become widespread for use in "microfabrication" – a

major example of which is the manufacture of integrated circuits such as computer chips.

In a typical microfabrication operation, lithography is used to define patterns for miniature electrical circuits. The lithography defines a pattern specifying the location of metal, insulators, doped regions, and other features of a circuit printed on a silicon wafer or other substrate. The resulting semiconductor circuit can perform any of a number of different functions.

Improvements in lithography have been mainly responsible for the explosive growth of computers in particular and the semiconductor industry in general. The major improvements in lithography can, for the most part, be put into two categories: an increase in chip size, and a decrease in the minimum feature size (improvement in resolution). Both of these improvements allow an increase in the number of transistors on a single chip (and in the speed at which these transistors can operate). For example, the computer circuitry that would have filled an entire room in 1960's technology can now be placed on a silicon "die" the size of your thumbnail. A device the size of a wristwatch can contain more computing power than the largest computers of several decades ago.

One type of lithography that is commonly used in the mass production of computer chips is known as “parallel lithography”. Parallel lithography generally prints an entire pattern at one time. This is usually accomplished by projecting photons through a mask onto a photoresist-coated semiconductor wafer, as shown in Fig 1. A mask

(designated by an "M" in Fig 1) provides a template of the desired circuit. A photoresist coat, which may be a thin layer of material coated on the wafer which changes its chemical properties when impinged upon by light, is used to translate or transfer the mask template onto the semiconductor wafer. In more detail, mask M allows photons (incident light, designated by an "I") to pass through the areas defining the features but not through other areas. An example of a typical mask construction would be deposits of metal on a glass substrate. In a way analogous to the way light coming through a photographic negative exposes photographic paper, light coming through the mask exposes the photoresist. The exposed photoresist bearing the pattern selectively "resists" a further process (e.g., etching with acid, bombardment with various particles, deposition of a metallic or other layer, etc.) Thus, this lithography technique using photoresist can be used to effectively translate the pattern defined by the mask into a structural pattern on the semiconductor wafer. By repeating this technique several times on the same wafer using different masks, it is possible to build multi-layered semiconductor structures (e.g., transistors) and associated interconnecting electrical circuits.

Parallel lithography as described above has the advantage that it is possible to achieve a high throughput since the whole image is formed at once. This makes parallel lithography useful for mass production. However, parallel lithography has the disadvantage that a new mask is required each time one desires to change patterns.

Because masks can have very complex patterns, masks are quite costly and susceptible to damage.

For mass production, parallel lithography is usually done using a machine known as a "stepper." As schematically depicted in Fig 1, a stepper consists of a light source ("I"), a place to hold a mask ("M"), an optical system ("lenses", "L") for projecting and demagnifying the image of the mask onto a photoresist-coated wafer ("W"), and a stage ("S") to move the wafer. The process of exposing a wafer using a stepper is summarized in Fig 2A, and is depicted from a side view in Figs 2B-2E. In each exposure, a stepper only exposes a small part of the wafer, generally the size of one chip. Since there are often many separate chips on each wafer, the wafer must be exposed many times. The stepper exposes the first chip (Fig 2B), then moves ("steps") over (Fig 2C) to expose the next chip (Fig 2D) and repeats this process (Fig 2E) until the entire wafer is exposed. This process is known as "step and repeat" and is the origin of the name "stepper."

A stepper must also be capable of precisely positioning the wafer relative to the mask. This precise positioning (overlay accuracy) is needed because each lithography step must line up with the previous layer of lithography. A stepper spends a significant portion of its time positioning the stage and the rest exposing the photoresist. Despite the great precision necessary, steppers must be capable of high throughput to be useful for mass production. There are steppers that can process one hundred 8-inch wafers per hour.

One way to increase the usefulness of a chip is to increase its size. In the "step and repeat" example described above, the size of the chip is limited to the exposure size of the stepper. The exposure size is small (roughly 20 mm x 40 mm) because of the cost of an optical system that is capable of projecting a high quality image of the mask onto the wafer. It is very expensive to increase the size of a chip by increasing the exposure size of the stepper (for example, this would require a larger lens - which by itself can cost many hundreds of thousands of dollars). Another approach is to modify a stepper so that light only shines on a subsection of the mask at a given time. Then, the mask and wafer can be scanned (moved relative to the fixed light source) simultaneously until the entire mask is imaged onto the wafer, as in Figs 3A-3C. This modified stepper is known as a "scanner" or "scanner/stepper".

Scanners offer increased chip size at the expense of increased complexity and mask costs. Because scanner masks are larger, the masks are more fragile and are more likely to contain a defect. The increased size and fragility of the mask mean that the masks for a scanner will be more expensive than the masks for a stepper. Also, because the image is being demagnified, the mask and wafer must be scanned at different speeds, as depicted by the length of the arrows in Figs 3A-3C. Because of the great precision required, differential scanning increases the cost and complexity of a scanner when compared with a stepper.

Many chip manufacturers are looking toward future improvements in resolution and/or exposure size to help continue the growth that has driven the semiconductor industry for the past thirty years. The improvements in these areas have been partly the result of improvements in the optical systems used to demagnify the mask and of the use of shorter wavelength light. In particular, modern lithography systems used for mass production are "diffraction limited", meaning that the smallest feature size that it is possible to print is determined by the diffraction of light and not by the size of features on the mask. In order to improve the resolution, one must use either a shorter wavelength of light or another technique such as optical proximity correction or phase shifting.

Another option for improving resolution is to put the mask in contact with the wafer, as in Fig 4; the effects of diffraction can be lessened by not giving the light a chance to "spread out" after it passes through the mask. Unfortunately, contact lithography is not suitable for mass production for at least two reasons. First, the mask must now be the same size as the final pattern, making the mask more expensive and more fragile. Second, because the mask is in contact with the wafer, it is easily damaged.

The present invention overcomes many of the disadvantages of prior lithographic microfabrication processes while providing further improvements that can significantly enhance the ability to make more complicated semiconductor chips at lower cost.

One aspect provided by this invention provides a new type of programmable structure for exposing a wafer. The programmable structure allows the lithographic pattern to be changed under electronic control. This provides great flexibility, increasing the throughput and decreasing the cost of chip manufacture and providing numerous other advantages.

The programmable structure provided in accordance with one example embodiment of the invention consists of an array of shutters that can be programmed to either transmit light to the wafer (referred to as its "open" state) or not transmit light to the wafer (referred to as its "closed" state). A simplified example lithography system incorporating such a programmable mask is schematically depicted in Fig 5A exposing an example pattern. In Fig 5B the same programmable mask PPM is shown exposing a different pattern.

The programmable mask shown in Figures 5A and 5B can provide a two-dimensional array of individual shutters each of which can be programmed to either transmit light ("open", "transparent") or block light ("closed", "opaque"). At least one such two-dimensional array of structures can be placed between a wafer and a source of electromagnetic energy. Each of the structures may comprise an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source. The structures can be controlled to selectively modulate, in accordance with a programmable pattern, electromagnetic energy impinging on the wafer.

In accordance with this aspect provided by the invention, a system for exposing a wafer may comprise a source of electromagnetic energy, a collimating lens optically coupled to the electromagnetic energy source, a wafer stage, and a two-dimensional array of structures disposed between the wafer stage and the collimating lens. Each of the structures in the array may comprise an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source. An electrical controller coupled to the two-dimensional array may be used to electrically control the semiconductor structures to selectively modulate, in accordance with a changeable pattern, electromagnetic energy from the source that is directed toward the wafer stage.

In accordance with a further aspect provided by the present invention, the programmable structure can comprise or include an array of selective amplifiers. In accordance with this aspect provided by the invention, a programmable electromagnetic energy modulating structure comprises a two-dimensional array of solid-state selective amplifiers each comprising regions of permanently opaque material and active regions. Control circuitry disposed within the array can be provided to selectively control each of the active regions to toggle between an amplifying state and a non-amplifying state. Thus, each selective amplifier is programmed to either amplify light (somewhat analogous to the "open" or "transparent" state of a shutter) or be "non-amplifying" (its "closed" or "opaque" state). In the non-amplifying state, some portion of the incident light is transmitted through the amplifier material. The portion of incident light that is transmitted

through the amplifier can range from 0 – 100%, depending on the specific design and operating conditions. Selective amplification has all of the advantages of a programmable structure that uses shutters with several added advantages -- including reduction in the time required to expose the resist.

In accordance with a further aspect provided by the invention the shutters and selective amplifiers can work in tandem to form a "programmable layer". When the programmed pattern calls for light to pass (or, not pass) through a particular pixel, both the selective amplifier and shutter corresponding to that pixel would be put into their open (or, closed) state. Figs 6A-6F schematically depicts the operation of an example shutter (labeled as "SH") (Figs 6A-6B), an example selective amplifier (labeled as "AM") (Figs 6C-6D), and an example device (labeled as "X") combining the two (Figs 6E-6F). In each of these figures, "I" represents the intensity of light incident on the shutter/amplifier, and " I′ " represents the light intensity after interacting with the shutter/amplifier. Combining a selective amplifier with a shutter in this manner achieves increased contrast over selective amplification alone.

In accordance with another aspect provided by the present invention, a programmable technique is provided for creating a pattern to be imaged onto a wafer that can be implemented as a viable production technique. Thus, the present invention also provides a technique of making integrated circuits. In accordance with this aspect provided by the invention, a wafer having a surface covered with

photoresist is placed on a movable wafer stage. A source directs electromagnetic energy toward a two-dimensional array of semiconductor structures disposed between the source and the wafer stage. The electron distribution within the structures is electrically controlled to define a desired microfabrication exposure pattern that modulates electromagnetic energy from said source that impinges on the wafer in accordance with a pattern. The modulated energy is used to expose the photoresist with the pattern. The wafer is then etched to selectively remove portions of the photoresist based on the desired microfabrication exposure pattern, and the etched wafer is treated to construct a semiconductor structure layer on the wafer.

In accordance with a further aspect provided by this invention, a diffraction limiter can be used to provide certain advantages associated with contact lithography without requiring some of the disadvantages of contact lithography. In accordance with this aspect of the invention, the diffraction limiter may provide an opaque layer in which there is an array of transparent regions ("holes") distributed in a one-to-one correspondence to the selective amplifiers/shutters. The diffraction limiter is placed in contact with the wafer, and the light that passes through the programmable layer is incident upon it. The diffraction limiter allows the advantages of contact lithography while maintaining the distance between the programmable layer and wafer.

In accordance with a further aspect provided by the present invention, a programmable shutter array, a programmable selective amplifier array, and a diffraction limiter can all be used in a common

system. For example, Fig 7A depicts schematically a lithography setup incorporating the above three components. Fig 7B shows a zoomed-in view of the diffraction limiter (denoted by "D") and wafer section. These three components provide a programmable lithography system that offers high throughput, extremely accurate pattern reproduction, and excellent resolution.

Implementing a diffraction limiter in conjunction with any programmable lithography system should significantly reduce the disadvantages associated with contact lithography. This device is placed in contact with the wafer and thus reduces the effects of diffraction (see Figs 7A and 7B.) Even though the diffraction limiter is close to the wafer and could be damaged, it is inexpensive and is easily replaced. Additionally, one can apply techniques such as phase shifting and/or optical proximity correction on the diffraction limiter itself. Because of the simple, regular shape of the pixels on the diffraction limiter, such corrections should be easily optimized.

Lithography in accordance with the present invention potentially allows a high throughput to be achieved. For example, only a single programmable structure is necessary to print any desired pattern. A non-exhaustive list of some of the many features and advantages provided by the present invention are as follows:

- Programmable lithography offers increased flexibility over conventional parallel lithography. This increased flexibility means that a greater variety of chips can be easily produced. It also opens up ways to improve the manufacture of all types of semiconductor

products. It also simplifies the entire process of designing and manufacturing semiconductor products.

- No need to have different masks to produce different chips. Because a single programmable structure can be programmed with an arbitrary pattern, it is no longer necessary to fabricate (and purchase) new mask sets in order to print new chips. This is extremely cost-effective for producing small quantities of specialized chips because the cost of a mask set can be prohibitively expensive. In producing large quantities of chips the cost of the mask set is less significant because it is a fixed cost amortized over many more chips.

- Electronic alignment. Because it is extremely important to line up the current lithography step with previous steps, steppers spend a significant amount of time mechanically aligning the wafer with the mask. With programmable lithography the pattern can be programmed into the "programmable layer" (i.e. the programmable area within the mask) such that it is aligned with the wafer. This saves time over having to mechanically align as in the case of a conventional mask.

- Disconnecting the size of the chip from the exposure size of the stepper. In conventional parallel lithography, the size of a chip is determined by the exposure size of the stepper. However, with programmable lithography a different pattern can be loaded into the programmable layer at each exposure. Hence, there is no longer any reason that the same pattern needs to be imaged each time the

stepper does an exposure. Consequently, in programmable lithography, the size of the chip is not intrinsically determined by the size of each individual exposure. This "disconnect" between chip and exposure size is a significant advantage of programmable lithography because chip performance and chip size are closely tied together.

- Simplified optical proximity correction. Optical proximity correction is a technique that is used to increase the resolution of the optical system at a given wavelength of light. Because of diffraction, the pattern on the mask is not faithfully reproduced on the wafer. In order to compensate for this, the pattern on the mask can be altered to account for diffraction so that the desired pattern can be imaged onto the wafer. One problem with this technique in a conventional mask is that it is difficult to decide how to alter the shape on the mask such that the desired shape will appear on the wafer. This is mainly due to the size and complexity of the desired pattern. Programmable lithography greatly simplifies this problem because in programmable lithography the same shape (e.g., a square) is always being imaged onto the wafer by each pixel, and the correction can be made on a pixel-by-pixel basis.

- Simplified phase shifting. As with optical proximity correction, phase shifting is also a technique that is used to increase the resolution of the optical system at a given wavelength of light. In this technique, a material that causes a phase shift in light is placed on the mask. The phase shifting material causes destructive

interference at the wafer between light from neighboring features in order to eliminate the diffraction tails. Phase shifting also suffers from the same problem as optical proximity correction; due to the size and complexity of the pattern it is difficult to decide where to place the phase shifting material. As with optical proximity correction, programmable lithography allows this problem to be greatly simplified because the same shape is always being imaged onto the wafer at each pixel. Programmable lithography also allows the possibility of active phase shifting. In active phase shifting, each pixel would contain an additional layer in which there would be a material whose index of refraction changes when a voltage is applied.

- Simplification of the chip making process. One of the big problems facing chip manufacturers is the growing complexity of the chip making process. With each new chip the manufacturer must get a brand new mask set. They must also inspect and repair these masks. With programmable lithography only a single programmable structure is needed to produce an entire chip. In the event that a programmable mask breaks it can simply be replaced with another identical programmable mask. Additionally, programmable lithography will facilitate research and development of new products because of the greater ease of producing prototype devices.

- The shutters and/or selective amplifiers can be fabricated easily. Each individual shutter can be a device similar to devices that are

typically used in chips themselves. This allows the design and fabrication of the shutter to draw on the enormous amount of knowledge associated with production techniques and operation of these devices.

- The shutters and/or selective amplifiers can be small and densely packed. Small shutters mean that the lithography system can produce small features without the need for demagnification, although it could be used in a system that does include demagnification. Densely packed shutters mean high throughput because they reduce the number of exposures necessary to expose the entire wafer.

- The shutters and/or selective amplifiers can work for short wavelength light. Shorter wavelengths provide better resolution, which is important for chip performance.

- The shutters and/or selective amplifiers generally will not break during normal operation. This is important because the mask must be able to flawlessly reproduce the desired image. If even a single pixel is incorrect then the entire chip is likely to be worthless.

- The shutters and/or selective amplifiers can switch states quickly. The speed of the shutters is relevant for throughput and may become significant when many shutters must be addressed.

- Selective amplifiers can be used alone and/or in combination with programmable shutters. An array of selective amplifiers can be used in the place of or in addition to a PPM to project more light

onto the wafer in some areas than in others corresponding to the pattern to be imaged. Or, an array of selective amplifiers can be used in a stand-alone system, e.g., when the non-amplified light is not sufficient to expose the resist and the amplified light is.

- Programmable lithography provides a resolution and throughput comparable to conventional parallel lithography while retaining all of the advantages of programmable lithography.

Brief Description of the Drawings

These and other features and advantages provided by the present invention will be better and more completely understood by referring to the following detailed description of presently preferred example embodiments in conjunction with the drawings, of which:

Fig 1 shows an example prior art technique of parallel lithography using a stepper;

Fig 2A summarizes the operation of an example prior art stepper;

Figs 2B to 2E show the simplified operation of an example prior art stepper;

Figs 3A to 3C show the simplified operation of an example prior art scanner;

Fig 4 shows an example prior art contact lithography technique;

Figs 5A and 5B show a simplified example of technique of lithography in accordance with a preferred embodiment of the present invention using a programmable structure;

Figs 6A and 6B illustrate example operation of shutters provided in accordance with the present invention;

Figs 6C and 6D illustrate example operation of selective amplifiers provided in accordance with the present invention;

Figs 6E and 6F illustrate example operation of a combination shutter/selective amplifier array in accordance with the present invention;

Fig 7A shows an example lithography setup in accordance with a presently preferred example embodiment of the present invention;

Fig 7B shows a zoomed-in view of the diffraction limiter and wafer of Fig 7A;

Fig 8 shows a more detailed example embodiment of the invention and its components in accordance with the present invention;

Fig 9 shows an example single selective amplifier and its components in accordance with the present invention;

Fig 10 shows an example single shutter and its components in accordance with the present invention;

Fig 11 shows an example single programmable pixel and its components in accordance with the present invention;

Figs 12A to 12H show an example technique of programmable lithography for a "4-step programmable layer" in accordance with the present invention;

Fig 13A summarizes an example electronic alignment technique in accordance with the present invention;

Figs 13B to 13G shows an example electronic alignment technique in accordance with the present invention; and

Figs 14A to 14F show an example technique in accordance with the present invention for printing chips that are larger than the exposure size of the mask.

Detailed Description of Example Embodiments

In an example preferred embodiment, the invention consists of three main components: an array of selective amplifiers **10**, an array of solid-state shutters **12**, and a diffraction limiter **14**. Taken together, the array of amplifiers **10** and the array of shutters **12** form what we shall call a "programmable layer", **PL**. Fig 8 shows these three components incorporated into an example setup for performing lithography. In this figure, incident light, **I**, shines on the programmable layer from above. A pattern generator feeds the user-defined pattern into the programmable layer.

The array of selective amplifiers **10** consists of regions of a permanently opaque material **22** (a metal such as aluminum) and active regions **20**. Each active region **20** within the array of selective amplifiers **10** is associated with a single selective amplifier **40**. The active regions **20** can be toggled between a non-amplifying **20a** and amplifying **20b** state via control circuitry (designated by an encircled **C1**).

Following the array of selective amplifiers **10** is an array of solid-state shutters **12**. The array of solid-state shutters **12** consists of regions of a permanently opaque material **22** and active regions **24**. Each active region **24** within the array of shutters **12** is associated with a single shutter **60**. The active regions **24** can be toggled between an opaque **24a** and a transparent **24b** state via control circuitry (designated by an encircled **C2**).

For reference, a given selective amplifier **40** and its corresponding solid-state shutter **60** will be taken as a "programmable pixel" **100**.

A diffraction limiter **14** is placed in contact with a resist-coated wafer. The diffraction limiter **14** is comprised of regions of a transparent material **30** (such as single crystal sapphire) and regions of an opaque material **32** (a metal such as aluminum). In the preferred embodiment, this is accomplished by depositing opaque material such as aluminum onto a transparent substrate such as sapphire. The transparent regions individually correspond to the locations of the active regions of the programmable pixels in the programmable layer.

Fig 9 details a single selective amplifier **40**. Each single selective amplifier **40** consists of a section (**46**, **48**, **50**, **52**) capable of selectively amplifying a beam of light, the circuitry **C1** needed to control the state of the selective amplifier, and a material **22** that blocks the light between adjacent selective amplifiers. In the preferred embodiment, the section capable of selectively amplifying light is a junction **52**

between a p-type semiconductor **48** (such as p-doped GaN) and an n-type semiconductor **50** (such as n-doped GaN) with metal contacts **46** (such as aluminum) that are used to bias the junction **52**. The control circuitry **C1** would be capable of turning the bias on or off. The plane of the p-n junction **52** is oriented such that the normal of the plane is perpendicular to the incoming light. The p-n junction **52** is exposed to the incident light through a hole **44** in the permanently opaque region **22**. The semiconductor materials **48** and **50** must be chosen such that stimulated emission occurs for the wavelength of incident light being used.

Fig 10 details a single solid-state shutter **60**. Each single solid-state shutter **60** consists of a section (**66**, **68**, **70**, **72**) capable of either blocking or transmitting the incident light, the circuitry **C2** needed to control the state of the shutter, and a material **22** that blocks the light between adjacent shutters. In the preferred embodiment, the section capable of either blocking or transmitting light is a MOS structure: an insulator region **68** (such as SiO_2) is sandwiched between metal electrodes **66** (such as aluminum) and a semiconductor region **70** (such as n-doped (n^{++}) GaN). Control circuitry **C2** is used to bias the MOS structure across the electrodes **66**. The active region **72** is exposed to the incident light through a hole **64** in the permanently opaque region **22**.

Fig 11 details a programmable pixel **100**. Each programmable pixel **100** consists of a single selective amplifier **40**, a single shutter **60**, a transparent insulator **102** (such as SiO_2) between the amplifier and

shutter, the control circuitry, represented by an encircled **C1** and **C2**, needed to control the state of the pixel, and a material **22** that blocks the light between adjacent pixels. The active region of the amplifier portion **52** must overlap the active region of the shutter **72** to form the active region of the pixel **104**. The active region of the pixel **104** is exposed to the incident light through a hole **106** in the permanently opaque region **22**.

The combined control circuitry, **C1** and **C2**, needs to be capable of toggling a voltage across each individual pixel **100** depending on the pattern supplied by the user via the pattern generator. This control circuitry is similar to the standard type of addressing used in memory devices or an LCD.

The above-described example embodiment is specified as to be useful in a lithography system utilizing (approximately) 385 nm (and longer) wavelength light. However, there are many other possible embodiments. For instance, the choice of specific materials for the various semiconductors and insulators can render the system useful for other wavelengths of incident light. Specifically, the band gap of the semiconductor in the selective amplifier determines the wavelengths of light that can be amplified. Of course, the materials chosen for the amplifier must be capable of amplifying light. For example, this could be accomplished in the manner described in the ensuing theory of operation section. Likewise, for the shutter, the materials used can be optimized for operation with a selected wavelength of incident light, again described in the theory of operation section.

Also, the specific geometry of electrodes and active materials could be modified while still retaining the usefulness of the invention. For instance, all the electrodes could be placed on the top surface of the device. Or, for example, the orientation of the plane of the junctions does not necessarily need to be completely perpendicular to the incoming light. This could simplify the fabrication process of the pixels.

Furthermore, since shorter wavelengths are desirable in lithography, materials with a large band gap are desirable for use in the pixels. In fact, some materials that may not typically be thought of as semiconductors may be useful for our purposes because they have a large band gap, such as sapphire, diamond, SiO_2, LiF, ZnS, AlN, ZnSe, etc... Additionally, in the amplifier section, our invention uses electric fields to induce a population inversion, but this is not the only possible means of doing so. Other techniques include but are not limited to optical pumping, thermal pumping, etc... Similarly, in the shutter section, our invention uses electric fields to change the density of occupied states, but this is not the only possible means for doing so. Other techniques include but are not limited to changing the temperature of the semiconductor or shining light onto the semiconductor.

There is a large field of research devoted to controlling population densities for the purpose of creating, manipulating, blocking, or amplifying light. One active area of interest in this field is the creation of semiconductor lasers. Many of the structures created

for semiconductor lasers or optical amplifiers could be used for selective amplification (in fact, semiconductor lasers could be used in the place of the selective amplifiers, in which case an external light source would not be necessary.) These other structures would include but would not be limited to heterostructures and vertical cavity surface emitting lasers (VCSELs). Similar structures could also be used for the shutter. While these other structures operate on similar principles to those described in the theory of operation section, they might provide some advantages, like decreasing the amount of voltage or current required to operate the device, or increasing the area of the active region.

There are also many possible alternate embodiments for the diffraction limiter. The materials must merely satisfy the requirement that the transparent regions individually correspond to the locations of the active regions of the programmable pixels in the programmable layer with opaque regions in between. For instance, the transparent regions could be physical holes etched through an opaque substrate, or, the transparent and opaque regions could be semiconductors with varying levels and/or kinds of doping.

Example Operation of Preferred Embodiments

In accordance with the preferred embodiments described above, each individual pixel **100** has the ability to either block or amplify light, **I**, and is able to be toggled between the two settings by means of the

control circuitry **C1** and **C2**. The pattern generator will control the individual pixels **100** in such a way that the control circuitry **C1** and **C2** always act in tandem within a given pixel.

The pattern generator addresses the control circuitry **C1** to control a potential difference across the metal contacts **46**. If the semiconductor **48** is doped n-type and the semiconductor **50** is doped p-type, then a depletion region is created in the active region **52**. When a potential difference is applied across the contacts **46**, a population inversion is formed in the depletion (active) region **52**. Incident light of the appropriate wavelength causes stimulated emission and is thus amplified in the active region **52**. If no potential difference is applied across the contacts **46**, the light passes through the region **52** unaltered. This satisfies our requirement for a selective amplifier.

The pattern generator simultaneously addresses the control circuitry **C2** to control a potential difference across the metal contacts **66**. When a potential difference is applied, this changes both the density of states and the conductivity of the semiconductor **70** in the region **72** adjacent to the semiconductor-insulator **(70-68)** interface. For instance, if the semiconductor **70** is doped n-type and a proper potential difference is applied across the metal contacts **66**, then a depletion region is created in the active region **72**. In the depletion (active) region **72** the conduction band electrons are repelled by the electric field created by the bias. The conductivity is dramatically decreased in the depletion (active) region **72**. The density of occupied states in the depletion (active) region **72** is also changed because the

states at the bottom of the conduction band that were previously filled are no longer filled. Hence, incident light with energy less than the semiconductor **70** band gap is transmitted through the device in the presence of a potential difference, and is absorbed in the absence of a potential difference. (Conversely, as per the theory of operation section, certain wavelengths of light with an energy greater (including x-rays) than the semiconductor **70** band gap are transmitted through the device in the absence of a potential difference, and are absorbed in the presence of a potential difference.) This satisfies our requirement for a shutter.

In order to utilize the programmable layer, **PL**, one must do a series of exposures of the photoresist **33**. Between each exposure two actions can be taken: (a) any or all of the pixels **100** can be toggled to a new state, and/or (b) the substrate can be moved, if necessary. By selecting which pixels **100** to make opaque or transparent the manufacturer can generate any pattern that he or she desires. Figs 12A to 12H depict an example of this process using what we shall call a "4-step programmable layer." The term "4-step" means that in order to create a pattern that fills the entire area of the mask, the substrate must be exposed four times. Each step is shown in a different pair of figures, one representing a perspective view and the other representing a top view. For example, Figs 12A and 12B both depict the first exposure step, from differing views. In the example depicted, the printing of the desired pattern is completed in the last step, shown in Figs 12G and 12H. Another case would be if the programmable layer

were designed such that the desired pattern could be printed without needing to move the substrate at all (similar to the setup in Fig 7A). Lithography using this "1-step programmable layer" would act as a fully parallel process.

A light source, **I**, illuminates the programmable layer, **PL**, from above and the light transmitted **31** by the layer passes through a lens, **L**, and is demagnified. After demagnification, the image of the programmable layer, **PL**, impinges on the diffraction limiter **14** which is held in close proximity with a substrate coated with a photosensitive resist **33** as in Fig 8. Light **31** is only transmitted through the diffraction limiter in transparent regions **30** and not through regions covered by opaque material **32**, and thus exposes the resist in regions **35**. The same setup is depicted in a more schematic way in Fig 7A for purposes of clarity.

One example technique for electronic alignment is summarized in Fig 13A. Fig 13B shows a wafer, **W**, that has been previously processed. Fig 13C shows the pattern that the user intends to add and its position relative to the previously processed features. Fig 13D shows the programmable layer, **PL** , coarsely aligned with the wafer. At this stage, the programmable layer is not yet aligned to with a pixel, and if an exposure were made the resulting pattern would be misaligned with the previously processed features as in Fig 13E. Fig 13F shows the programmable layer after alignment to within a pixel, and the subsequent successful exposure. Given a different coarse alignment, Fig 13G shows the case in which a different individual pixel

in the programmable layer has been aligned with the previously processed features, and the subsequent successful exposure. Figs 13F-13G together demonstrate that the absolute location of the programmable layer relative to the wafer is not important as long as the programmable layer is aligned to within any single pixel. The pattern can be electronically shifted to a new set of pixels in the programmable layer such that they will project the image in the correct location.

An example of how to use an example preferred embodiment provided in accordance with the present invention to disconnect the chip size from the exposure size is summarized in Fig 14A. Fig 14B shows the pattern that the user intends to print on the wafer, **W**. Note that this pattern is about four times the single exposure size of the programmable layer, **PL**. In each of the Figs 14C-14F, the programmable layer is loaded with the proper section of the total pattern, an exposure is made, and the wafer is moved to the left by a fixed amount. In Fig 14F, the desired pattern has been printed.

Theory of Operation

We begin with a discussion of an example shutter in accordance with the present invention, followed by a discussion of an example selective amplifier in accordance with the present invention.

For the preferred embodiment array of shutters to work, it is necessary that the various shutters can be made either "transparent" or "opaque" to the incident light. For a mask, both terms "transparent" and "opaque" describe the ratio of the intensity of incident light to the

intensity of transmitted light. An "opaque" material is different relative to a "transparent" material in that the amount of light attenuated is much greater in the case of the "opaque" material. The amount of attenuation is best measured using the concept of an attenuation coefficient, α, defined by the relation

$$\frac{I}{I_o} = e^{-\alpha z}, \qquad (1.)$$

where I is the transmitted intensity, I_o is the incident intensity, and z is the thickness of material traversed. Using this, if we compare the transmitted intensities through a "transparent" material and an "opaque" material, we get a measure of the contrast in light impinging on the resist, C, as

$$C = \frac{I_{transparent}}{I_{opaque}} = \frac{e^{-\alpha_{transparent} \cdot z}}{e^{-\alpha_{opaque} \cdot z}} = e^{+(\alpha_{opaque} - \alpha_{transparent}) \cdot z} . \qquad (2.)$$

If this contrast is a large number, the resist will only be actively exposed when the shutter is in the "transparent" state. Thus, if we can control the attenuation coefficient in a material, i.e. vary it from $\alpha_{transparent}$ to α_{opaque} so that their difference is appreciable, then the system is a useful candidate for a programmable mask.

The attenuation coefficient, α, arises from all possible mechanisms of absorption of the light combined. For our system, the two mechanisms we are most interested in are (a) absorption by "free" carriers in the conduction band, and (b) atomic/interband photoeffect.

Absorption by "free" carriers in the conduction band

In a simple classical model of conduction, the conductivity of a material is directly proportional to the number of free electrons per unit volume available to interact. These charges are capable of absorbing or reflecting the incident light. If the fields of the light are harmonic as $e^{i(\bar{k}\cdot\bar{x}-\omega t)}$ then we can write the wavevector as

$$k = \beta + i\frac{\alpha}{2}\ , \qquad (3.)$$

where

$$\left.\begin{matrix}\beta\\ \frac{\alpha}{2}\end{matrix}\right\} = \sqrt{\mu\varepsilon}\,\frac{\omega}{c}\left[\frac{\sqrt{1+\left(\frac{4\pi\sigma}{\omega\varepsilon}\right)^2}\pm 1}{2}\right]^{\frac{1}{2}}, \qquad (4.)$$

where μ is the magnetic permeability, ε is the dielectric constant, σ is the conductivity of the material, c is the speed of light, and $\omega = E/\hbar$ is the circular frequency of the light.

Inserting Eq. (4.) into Eq. (3.), and using the $e^{i(\bar{k}\cdot\bar{x}-\omega t)}$ dependency, we see that the amplitude of the light incident in the z direction will drop off exponentially as $e^{-\frac{\alpha z}{2}}$, and hence the intensity will go as $e^{-\alpha z}$, verifying that α is indeed the attenuation coefficient mentioned earlier. Hence, a change in the conductivity, σ, in Eq. (4.) will result in a corresponding change in the attenuation coefficient, α.

Although the above classical treatment is not sufficient to describe the details of the interactions of photons with the conduction

band electrons, the qualitative property of the conductivity affecting the absorption coefficient still holds true. For a more complete description, one must treat the system quantum mechanically. The next section deals with the quantum mechanical interaction of light with a solid.

Absorption via atomic/interband photoeffect

In this case, an electron absorbs an incident photon and is promoted to an excited state. If the energy of the light is insufficient to liberate it from the material completely (photoelectric knockout), then the electron must be promoted into another quantized state in the material. If such a state does not exist, the incident photon is not absorbed because energy cannot be conserved. Furthermore, if the state does exist but is already occupied by another electron (ignoring spin), the transition is also forbidden by the Pauli principle. If the transition is allowed, the probability that such an interband transition will occur can be written

$$P_{if}(E_\gamma) \propto T_{if}\, g_f(E_f)\, g_i(E_i), \quad \text{with } E_f = E_i + E_\gamma \quad (5.)$$

where T_{if} is the transition matrix element, $g_i(E_i)$ is the density of states initially occupied by electrons, and $g_f(E_f)$ is the density of unoccupied final states into which the electron may be promoted. The attenuation coefficient is proportional to this probability, P_{if}. Hence, if one can change either g_i or g_f then one can effectively make the material "transparent" or "opaque".

To illustrate how the absorption can be controlled in a shutter we now look to specific examples.

We will consider a Metal-Oxide-Semiconductor device ("MOS") as an example, but the discussion could also be applied to other structures such as p-n junctions, and even insulators. The region of interest will be in the semiconductor, near the interface with the oxide. The semiconductor has a band gap which we will choose to be 1 eV. In the intrinsic case, light with an energy less than 1 eV incident on the semiconductor is not able to promote electrons from the valence band to the conduction band. Hence, interband transitions will not contribute to the attenuation coefficient. The "free" electrons in the conduction band solely interact with the incident light. With this, if we consider the case where we dope the semiconductor as n-type (i.e. adding more free electrons to the conduction band), more light will be absorbed as we increase the dopant concentration (because there are more electrons interacting). For light energies less than the band gap, we will consider the material to then be "opaque" to the light, as the electrons in the conduction band absorb a significant amount of the incident intensity.

Next, if we apply a voltage to the MOS structure, we create a region near the interface in which the number of conduction band electrons is reduced compared to the non-biased case. Now we have a situation where the amount of light absorbed is less, because we have in effect changed the conductivity of the semiconductor in this depletion region. This situation is "transparent" relative to the aforementioned "opaque" setup. The actual materials used and the technique for creating the depletion region should be chosen in such a

way to maximize the contrast, C, while keeping the actual transmitted intensity, $I_{transparent}$, as large as possible (so that the process takes as little time as possible.)

Another example would be to choose incident light with an energy just larger than the band gap energy. Then, interband transitions are likely to dominate the absorption. In the same n-type doped MOS structure as above, the density of unoccupied states in the conduction band, g_f, into which a valence band electron can be promoted is reduced near the bottom of the conduction band. This is due to the presence of a large concentration of electrons from the dopant atoms. Now, consider the situation in which we apply a voltage across the interface. This creates a depletion region in which there are fewer electrons present in the conduction band, and hence more unoccupied states. Comparing the biased and unbiased situations, one can see that the latter should be more "opaque" than the former, because more valence band electrons can be promoted into the newly vacated conduction band states. Once again, materials and voltages, etc...can be chosen to maximize both contrast and "transparent" intensity. Also, if we had used p-type doping rather than n-type, a corresponding change in g_i would have appeared. Depleting the region of holes would have the same effect of toggling the state of the shutter. One should note that in the previously stated examples, the attenuation coefficient is only appreciably changed for a specific range of light energies, determined by properties such as but not limited to the choice of materials in the MOS structure, the bias supplied, and the dopant

density. It should also be noted that this transition-blocking effect can work for photon energies corresponding to any transition within the material. For example, changing the density of unoccupied states in the conduction band, g_f, can affect the absorption of light (x-rays) on inner shell electrons in a material. Higher energies of light are desirable in lithography because the effects of diffraction are reduced as the light energy is increased.

Next, for the preferred embodiment array of selective amplifiers to work, it is necessary that the various selective amplifiers can be made either "amplifying" or "non-amplifying" to the incident light. For a mask, both terms "amplifying" and "non-amplifying" describe the ratio of the intensity of incident light to the intensity of output light. An "amplifying" state is defined relative to a "non-amplifying" state in that the amount of light at the output is much greater. Using this, if we compare the output intensities through an "amplifying" material and a "non-amplifying" material, we get a measure of the contrast in light impinging on the resist, C, as

$$C = \frac{I_{amplifying}}{I_{non-amplifying}} = \frac{I_{amplifying}}{I_o}, \qquad (6.)$$

where $I_{non\text{-}amplifying}$ is the incident intensity I_o, and $I_{amplifying}$ is the output intensity. The contrast is typically an increasing function of the thickness of the selective amplifier.

If this contrast is a large number, the resist will only be actively exposed when the selective amplifier is in the "amplifying" state. Thus, if we can control the amount of amplification in a material such

that C is large, then the system is a useful candidate for use in a programmable mask.

The amplification occurs by a process known as stimulated emission. If an electron exists in a state that is an energy ΔE above another state, then when the electron drops (makes a transition) from the higher state to the lower state it will emit a photon with energy ΔE. A photon with energy ΔE that passes near the electron in the excited state can cause the electron to drop to the lower state and emit a photon with the same energy, phase, and direction as the first photon. This is the process of stimulated emission. Stimulated emission is a well-known process and is the basis of the laser. In order for stimulated emission to occur, several conditions must be met. One condition is that there must be a population inversion. Ordinarily, electrons are in the lowest state available to them. When there are more electrons in an excited state than in the lower state then a population inversion exists. Another condition for stimulated emission is that there must be initial photons of the proper energy to cause the electrons to drop from the excited state.

In the preferred embodiment of the array of selective amplifiers, biasing the p-n junctions causes population inversions and the incident light provides the initial photons necessary for stimulated emission. The light that is shined on the biased p-n junctions is therefore amplified; the biased situation is the aforementioned "amplifying" state. The light that is incident on the unbiased p-n junctions is transmitted but not amplified. This allows the incident light to be selectively

amplified by controlling which p-n junctions are biased. As long as there is appreciable amplification, and hence appreciable contrast, selective amplifiers can be useful in a lithography system.

Although the preferred embodiment describes a complex device that combines various components, each component in itself represents either a new technology or a great improvement upon existing technology. For example, an array of selective amplifiers or an array of shutters could be used as a stand-alone programmable structure, either with or without a diffraction limiter. Additionally, either type of array or a diffraction limiter could be implemented as part of any programmable lithography scheme.

Therefore, while the invention has been described in connection with what is presently considered to be the most practical and preferred embodiment, it is to be understood that the invention is not to be limited to the disclosed embodiment, but on the contrary, is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WE CLAIM:

1. A method of exposing a wafer comprising:

placing at least one two-dimensional array of structures between a wafer and a source of electromagnetic energy, said structures each comprising an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source; and

controlling the structures to selectively modulate, in accordance with a programmable pattern, electromagnetic energy impinging on the wafer.

2. A method as in claim 1 wherein at least some of the active regions comprise a material having a band gap.

3. A method as in claim 1 wherein at least some of the active regions comprise semiconductor material.

4. A method as in claim 1 wherein the controlling step includes applying at least one of (a) a voltage, and (b) a current, to said structures.

5. A method as in claim 1 wherein the structures each comprise at least one of a PN junction semiconductor structure and a metal-insulating-semiconductor structure.

6. A method as in claim 1 wherein the controlling step (b) comprises:

(b1) controlling said structures to selectively modulate the electromagnetic energy impinging on the wafer in accordance with a first pattern; and

(b2) controlling said structures to selectively modulate the electromagnetic energy impinging on the wafer in accordance with a second pattern different from the first pattern.

7. A method as in claim 6 wherein steps (b1) and (b2) result in exposing, in an overlayed manner, the same part of the wafer.

8. A method as in claim 6 wherein steps (b1) and (b2) result in exposing different, adjacent regions of the wafer to provide an exposure pattern that is larger than the modulated electromagnetic energy pattern impinging on the wafer at any one time.

9. A method as in claim 6 further including moving the wafer between step (b1) and step (b2).

10. A method as in claim 1 wherein each of said structures comprises an electromagnetic energy shutter.

11. A method as in 10 wherein each of said structures further comprises an electromagnetic energy amplifier.

12. A method as in claim 1 wherein each of said structures comprises an electromagnetic energy amplifier.

13. A method as in claim 1 further including:

aligning at least one of structures with a wafer feature;

determining the position of said array relative to said wafer; and

programming said array to offset an exposure pattern within said array such that said exposure pattern is located correctly on said wafer.

14. A method as in claim 1 further including the step of disposing a diffraction limiter between said array and said wafer.

15. A system of exposing a wafer comprising:

at least one two-dimensional array of structures disposed between a wafer and a source of electromagnetic energy, said structures each comprising an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source; and

a controller that controls the structures to selectively modulate, in accordance with a programmable pattern, electromagnetic energy impinging on the wafer.

16. A system as in claim 15 wherein at least some of the active regions comprise a material having a band gap.

17. A system as in claim 15 wherein at least some of the active regions comprise semiconductor material.

18. A system as in claim 15 wherein the controller includes driver circuitry that applies at least one of (a) a voltage, and (b) a current, to said structures.

19. A system as in claim 15 wherein the structures each comprise at least one of a PN junction semiconductor structure and a metal-insulating-semiconductor structure.

20. A system as in claim 15 wherein the controller controls said structures to selectively modulate the electromagnetic energy impinging on the wafer alternatively in accordance with at least (a) a first pattern, and (b) a second pattern different from the first pattern.

21. A system as in claim 20 wherein controller controls the array to overlay said first and second patterns onto the same part of the wafer.

22. A system as in claim 20 wherein the controller controls the array to expose different, adjacent regions of the wafer to provide an exposure pattern that is larger than the modulated electromagnetic energy pattern impinging on the wafer at any one time.

23. A system as in claim 20 further including means for moving the wafer between the first pattern exposure and the second pattern exposure.

24. A system as in claim 15 wherein each of said structures comprises an electromagnetic energy shutter.

25. A system as in 24 wherein each of said structures further comprises an electromagnetic energy amplifier.

26. A system as in claim 15 wherein each of said structures comprises an electromagnetic energy amplifier.

27. A system as in claim 15 further including:

means mechanically coupled to at least one of the array and the wafer, for aligning at least one of structures with a wafer feature; and

means for determining the position of said array relative to said wafer, and

wherein the controller programs said array to offset an exposure pattern within said array such that said exposure pattern is located correctly on said wafer.

28. A system as in claim 15 further including a diffraction limiter disposed between said array and said wafer.

29. Apparatus for exposing a wafer using an illumination source, said apparatus comprising:

means disposed between said wafer and said illumination source for modulating electromagnetic energy passing therethrough to the wafer, said means for modulating comprising at least one two-dimensional array of plural means for supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said illumination source; and

means, coupled to the means for supporting, for controlling the means for supporting to selectively modulate, in accordance with a programmable pattern, electromagnetic energy impinging on the wafer.

30. Apparatus as in claim 20 wherein at least some of the means for supporting at least in part comprise a material having a band gap.

31. Apparatus as in claim 20 wherein at least some of the means for supporting at least in part comprise semiconductor material.

32. Apparatus as in claim 20 wherein the means for controlling includes means for applying at least one of (a) a voltage, and (b) a current, to said means for supporting.

33. Apparatus as in claim 20 wherein the means for supporting each comprise at least one of a PN junction semiconductor structure and a metal-insulating-semiconductor structure.

34. Apparatus as in claim 20 wherein the means for controlling comprises:

means for controlling said means for supporting to selectively modulate the electromagnetic energy impinging on the wafer in accordance with a first pattern; and

means for controlling said means for supporting to selectively modulate the electromagnetic energy impinging on the wafer in accordance with a second pattern different from the first pattern.

35. Apparatus as in claim 34 wherein said means for controlling causes the same part of the wafer to be exposed in an overlayed manner with the first pattern and the second pattern.

36. Apparatus as in claim 34 wherein said means for controlling cause different, adjacent regions of the wafer to be exposed with the first and second patterns, to provide an overall exposure pattern that is larger than the modulated electromagnetic energy pattern impinging on the wafer at any one time.

37. Apparatus as in claim 34 further including means for moving the wafer between exposure with the first pattern and exposure with the second pattern.

38. Apparatus as in claim 20 wherein each of said means for supporting comprises an electromagnetic energy shutter.

39. Apparatus as in 38 wherein each of said means for supporting further comprises an electromagnetic energy amplifier.

40. Apparatus as in claim 20 wherein each of said means for supporting comprises an electromagnetic energy amplifier.

41. Apparatus as in claim 20 further including:

means for aligning at least one of said means for supporting with a wafer feature;

means for determining the position of said array relative to said wafer; and

means for programming said array to offset an exposure pattern within said array such that said exposure pattern is located correctly on said wafer.

42. Apparatus as in claim 20 further including a diffraction limiter disposed between said array and said wafer.

43. A system for exposing a wafer comprising:

a source of electromagnetic energy;

a collimating lens optically coupled to the electromagnetic energy source;

a wafer stage;

a two-dimensional array of structures disposed between the wafer stage and the collimating lens, each said structures in the array comprising an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source; and

an electrical controller coupled to the two-dimensional array, the controller electrically controlling the semiconductor structures to selectively modulate, in accordance with a changeable pattern, electromagnetic energy from the source that is directed toward the wafer stage.

44. A method of making integrated circuits comprising:

providing a wafer having a surface covered with photoresist;

placing the wafer on a movable wafer stage;

directing electromagnetic energy toward a two-dimensional array of semiconductor structures disposed between a source of said electromagnetic energy and said wafer stage;

electrically controlling the electron distribution within the structures to define a desired microfabrication exposure pattern that modulates electromagnetic energy from said source that impinges on the wafer in accordance with a pattern, thereby exposing the photoresist with said pattern;

etching the wafer to selectively remove portions of said photoresist based on said desired microfabrication exposure pattern; and

treating said etched wafer to construct a semiconductor structure layer on said wafer.

45. A system for making integrated circuits from wafers, the system comprising:

a source of electromagnetic energy;

means for providing a wafer having a surface covered with photoresist;

means for placing the wafer on a movable wafer stage;

means for directing electromagnetic energy toward a two-dimensional array of semiconductor structures disposed between the source of said electromagnetic energy and said wafer stage;

means for electrically controlling the electron distribution within the two-dimensional array of semiconductor structures to selectively modulate the electromagnetic energy impinging on the wafer in accordance with a desired microfabrication exposure pattern, thereby exposing the photoresist with said pattern;

means for etching the wafer to selectively remove portions of said photoresist based on said desired microfabrication exposure pattern; and

means for treating said etched wafer to construct a semiconductor structure layer on said wafer.

46. A system as in claim 45 further comprising a diffraction limiter disposed between the wafer stage and the two-dimensional array.

47. In a semiconductor chip fabrication line, a wafer exposing unit comprising:

a movable wafer stage for supporting and positioning a wafer having a surface covered with photoresist;

a controllable source of electromagnetic energy;

a two-dimensional array of semiconductor structures disposed between said source of said electromagnetic energy and said wafer stage, the structures within the array each comprising an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy from said source;

a pattern generator that defines a microfabrication pattern; and

an electrical controller coupled to the two-dimensional array and the pattern generator, the electrical controller electrically changing the electron distributions within each of the semiconductor structure active regions to selectively modulate the electromagnetic energy impinging on the wafer in accordance with said microfabrication exposure pattern, thereby exposing the photoresist with said pattern.

48. A system as in claim 47 further comprising a diffraction limiter disposed between the wafer stage and the two-dimensional array.

49. A programmable structure for use in microfabrication lithography of a wafer, the programmable structure comprising:

a two-dimensional array of semiconductor structures each comprising an active region supporting an electron distribution that can

be changed to affect the modulation of electromagnetic energy from said source; and

electronics coupled to the semiconductor structures, the electronics electrically controlling the semiconductor structures to selectively modulate electromagnetic energy impinging on the wafer in accordance with a microfabrication pattern.

50. A system as in claim 49 wherein the semiconductor structures comprise semiconductor shutters.

51. A system as in claim 49 wherein the semiconductor structures comprise MOS structures.

52. A system as in claim 49 wherein the semiconductor structures comprise PN junctions.

53. A system as in claim 52 wherein the electronics includes means for changing the bias across each of the PN junctions.

54. A system as in claim 49 wherein the semiconductor structures each include an active semiconductor region that can be electrically switched between a state of relatively high optical transmissivity and a state of relatively low optical transmissivity.

55. A system as in claim 49 wherein the semiconductor structures each comprise an active semiconductor region that is selectively, electrically controllable to switch between an amplifying state and a non-amplifying state.

56. A system as in claim 49 wherein the semiconductor structures comprise optical amplifiers.

57. A method of making a programmable mask for use in microfabrication lithography, the method comprising:

incorporating a plurality of semiconductor structures into a two-dimensional array, said structures each comprising an active region supporting an electron distribution that can be changed to affect the modulation of electromagnetic energy;

incorporating into said array, electrical circuitry coupled to the semiconductor structure that electrically controls the semiconductor structures to operate in different electromagnetic modulating states; and

testing said array by operating said electrical circuitry to determine whether the array is capable of selectively modulating electromagnetic energy in accordance with a two-dimensional test pattern.

58. A programmable electromagnetic energy modulating structure comprising:

a two-dimensional array of solid-stage shutters each comprising regions of permanently opaque regions and active regions; and

control circuitry disposed within the array, the control circuitry selectively controlling each of the active regions to toggle between an opaque stage and a transparent state.

59. A programmable electromagnetic energy modulating structure comprising:

a two-dimensional array of solid-state selective amplifiers each comprising regions of permanently opaque material and active regions; and

control circuitry disposed within the array, the control circuitry selectively controlling each of the active regions to toggle between an amplifying state and a non-amplifying state.

60. A diffraction limiter for use in microfabrication, said diffraction limiter comprising a two-dimensional array of transparent regions and opaque regions, said transparent regions having locations individually corresponding to the locations of the active regions of a programmable mask.

61. A method of exposing a wafer comprising:

placing a structure between a wafer and a source of electromagnetic energy;

illuminating said structure with electromagnetic energy from said source;

amplifying, with said structure, a portion of the incident electromagnetic energy corresponding to a pattern; and

outputting, from said structure to said wafer, said amplified electromagnetic energy corresponding to said pattern.

62. A method as in claim 61 wherein said pattern is substantially permanently defined.

63. A method as in claim 61 further including the step of programming the pattern into said structure.

64. A system of exposing a wafer comprising:

means for placing a structure between a wafer and a source of electromagnetic energy;

means for illuminating said structure with electromagnetic energy from said source;

means for amplifying, with said structure, a portion of the incident electromagnetic energy corresponding to a pattern; and

means for outputting, from said structure to said wafer, said amplified electromagnetic energy corresponding to said pattern.

65. A system as in claim 64 wherein said pattern is substantially permanently defined.

66. A system as in claim 64 further including the step of programming the pattern into said structure.

67. A method of exposing a wafer comprising:

placing a structure between a wafer and a source of electromagnetic energy, said structure comprising a first region in which the electron distribution has been altered relative to a second region;

illuminating said structure with electromagnetic energy from said source;

masking, with said structure, a portion of the incident electromagnetic energy corresponding to a pattern; and

outputting, from said structure to said wafer, said masked electromagnetic energy corresponding to said pattern.

68. A method as in claim 67 wherein said first region has a different doping level than the second region.

69. A method as in claim 67 wherein said structure comprises a material with a band gap.

70. A method as in claim 67 wherein said structure comprises a semiconductor material.

71. A method as in claim 67 wherein said electromagnetic transmissivity of said first region and said second region are substantially permanently defined.

72. In a step and repeat lithography system, a method for electronically aligning an exposure pattern with a wafer having at least one feature, during a microfabrication process, the method comprising:

providing a programmable two-dimensional array defining plural picture elements;

aligning at least one of said picture elements with said wafer feature;

measure the position of said array relative to said wafer; and

programming said array to offset an exposure pattern within said array such that said exposure pattern is located correctly on said wafer.

73. A programmable structure for use in microfabrication lithography of a wafer, the programmable structure comprising:

a two-dimensional array of light sources; and electronics coupled to the light sources, the electronics electrically controlling the light sources to selectively emit electromagnetic energy impinging on the wafer in accordance with a microfabrication pattern.

74. A structure as in claim 73 wherein the light sources comprise semiconductor lasers.

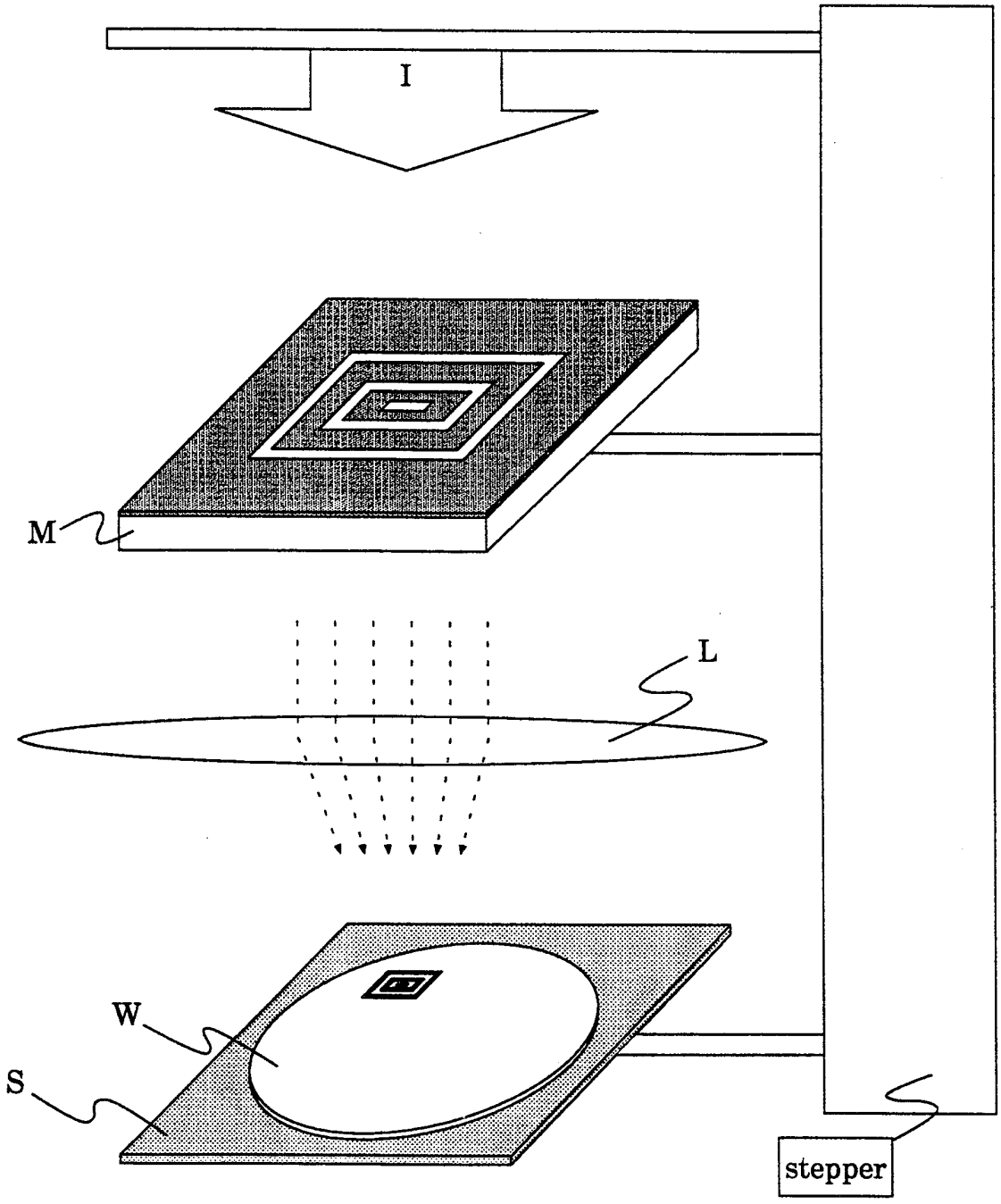


Fig. 1 (prior art)

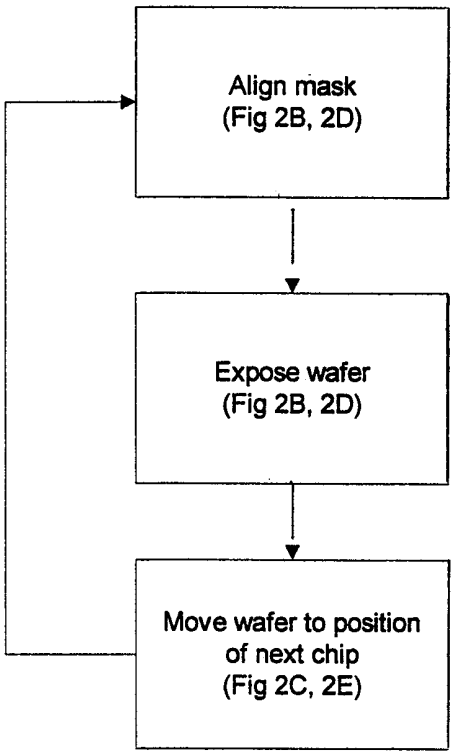


Fig. 2A (prior art)

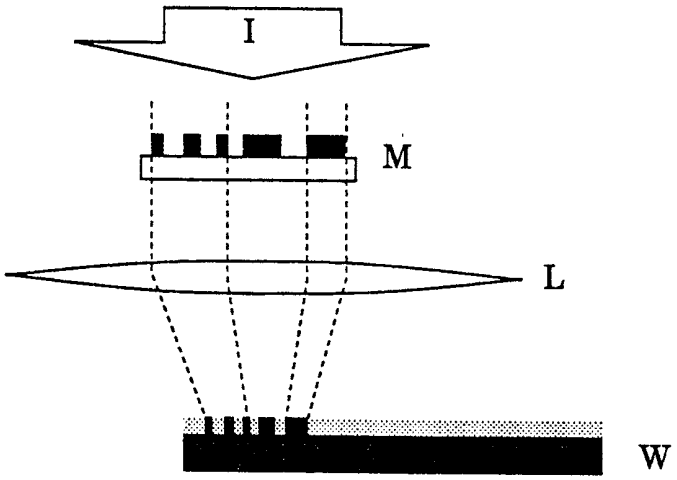


Fig. 2B (prior art)

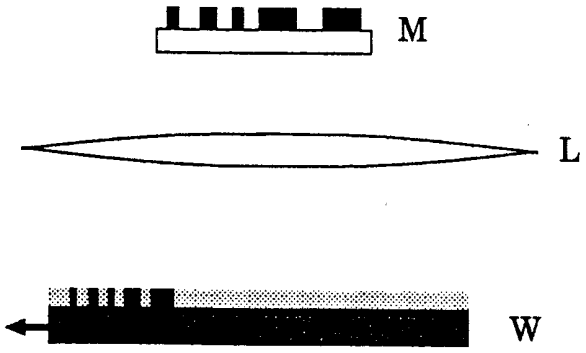


Fig. 2C (prior art)

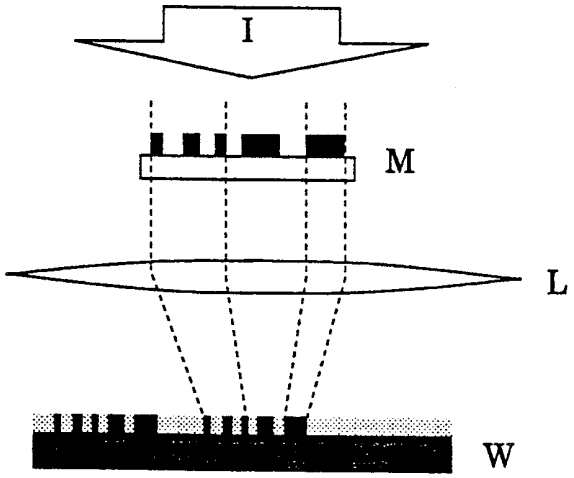


Fig. 2D (prior art)

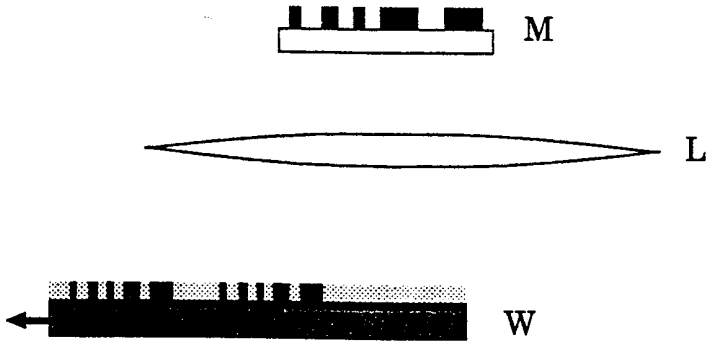


Fig. 2E (prior art)

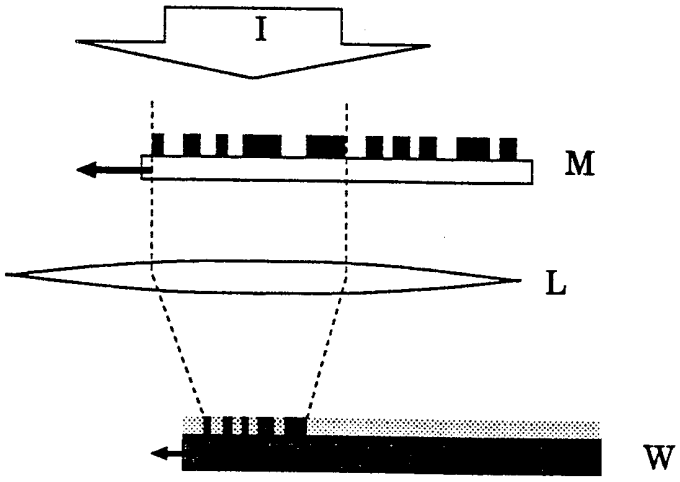


Fig. 3A (prior art)

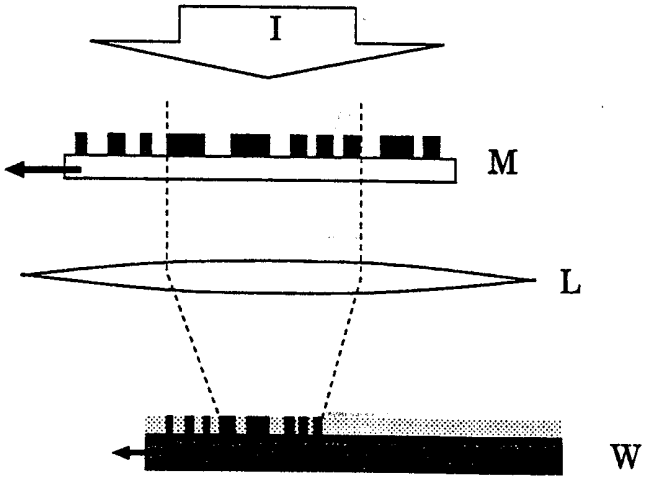


Fig. 3B (prior art)

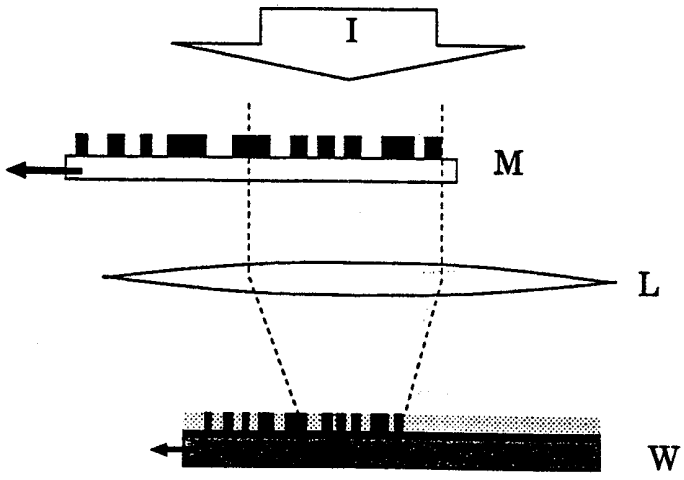


Fig. 3C (prior art)

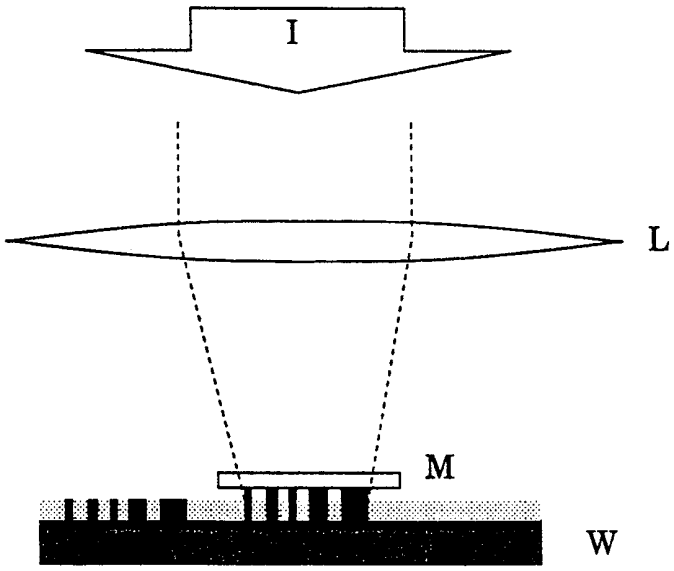


Fig. 4 (prior art)

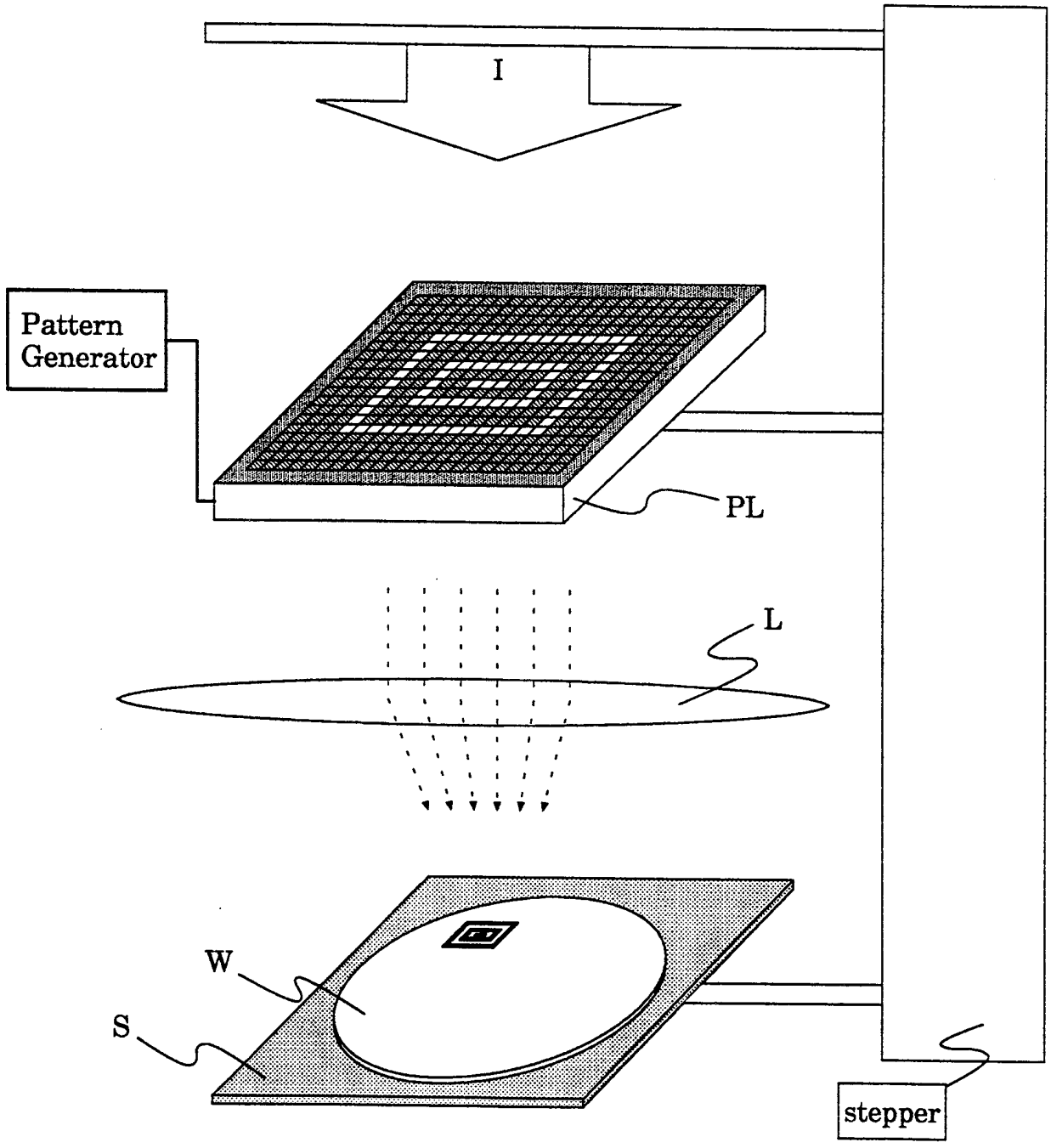


Fig. 5A

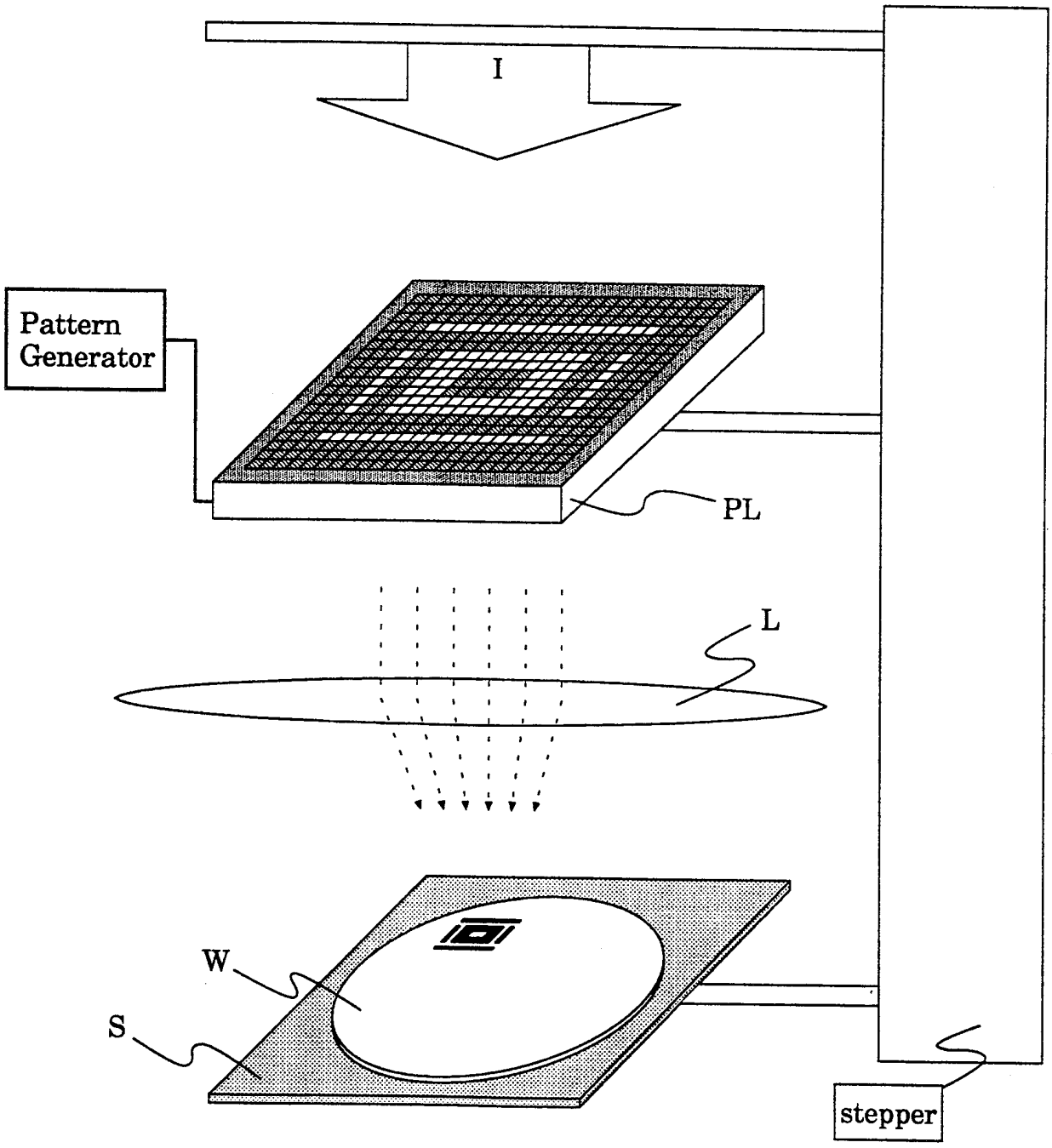


Fig. 5B

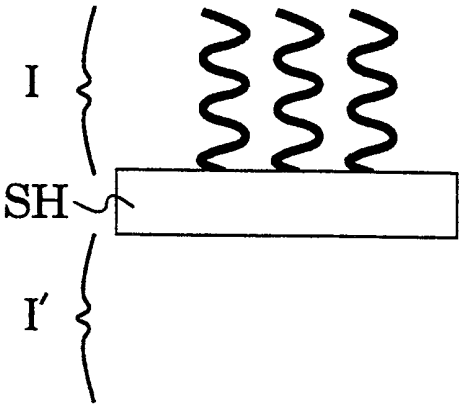


Fig. 6A

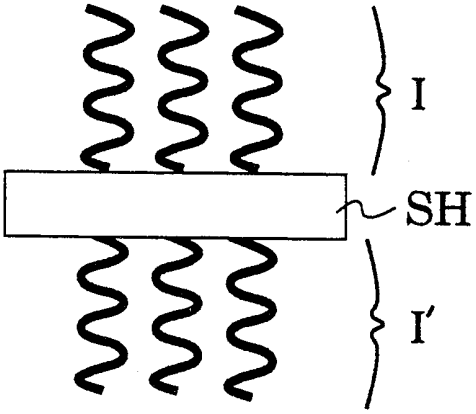


Fig. 6B

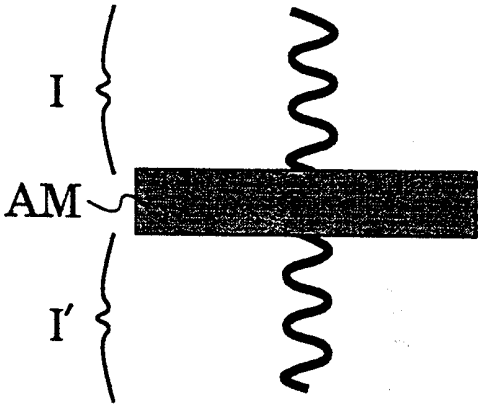


Fig. 6C

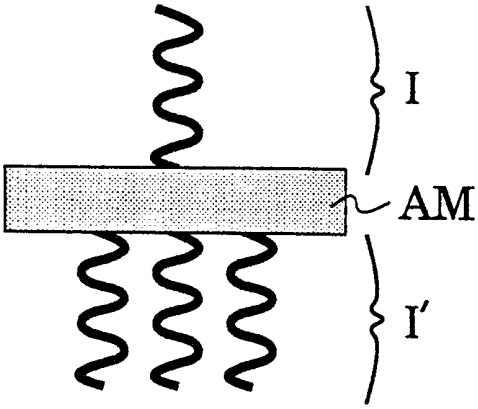


Fig. 6D

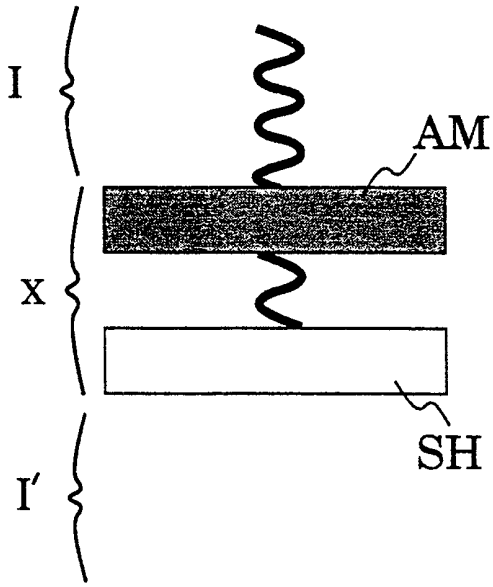


Fig. 6E

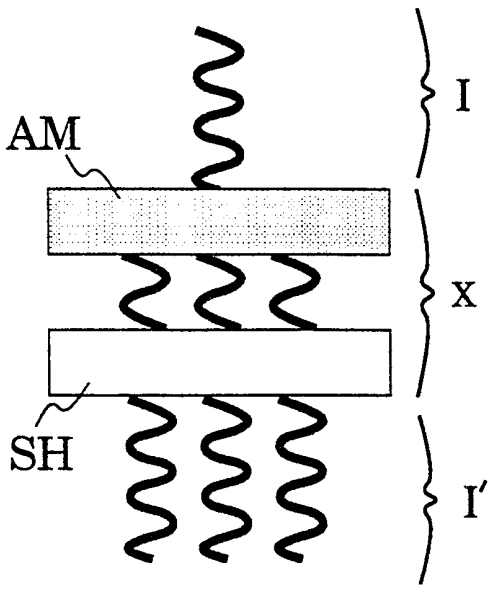


Fig. 6F

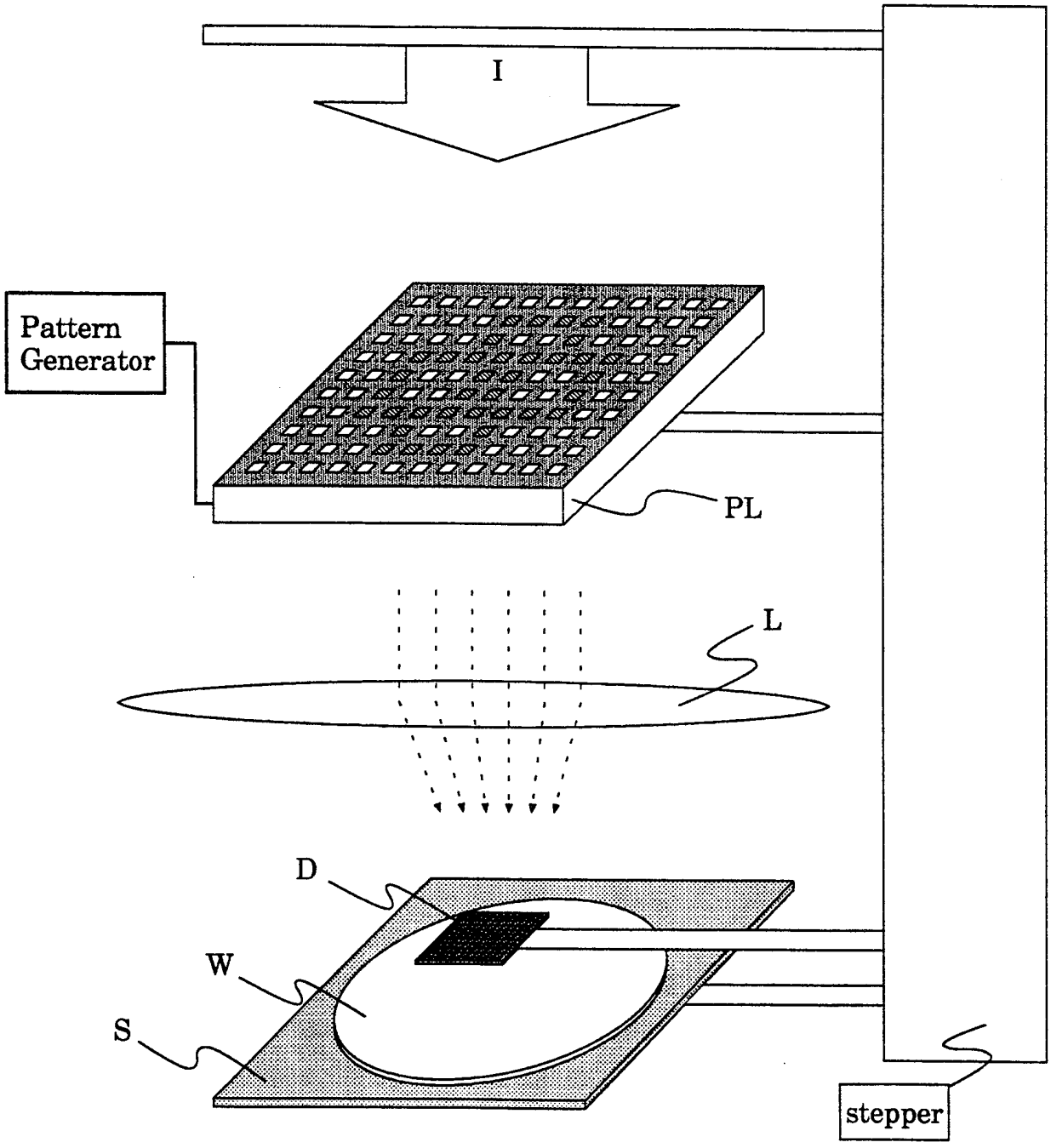


Fig. 7A

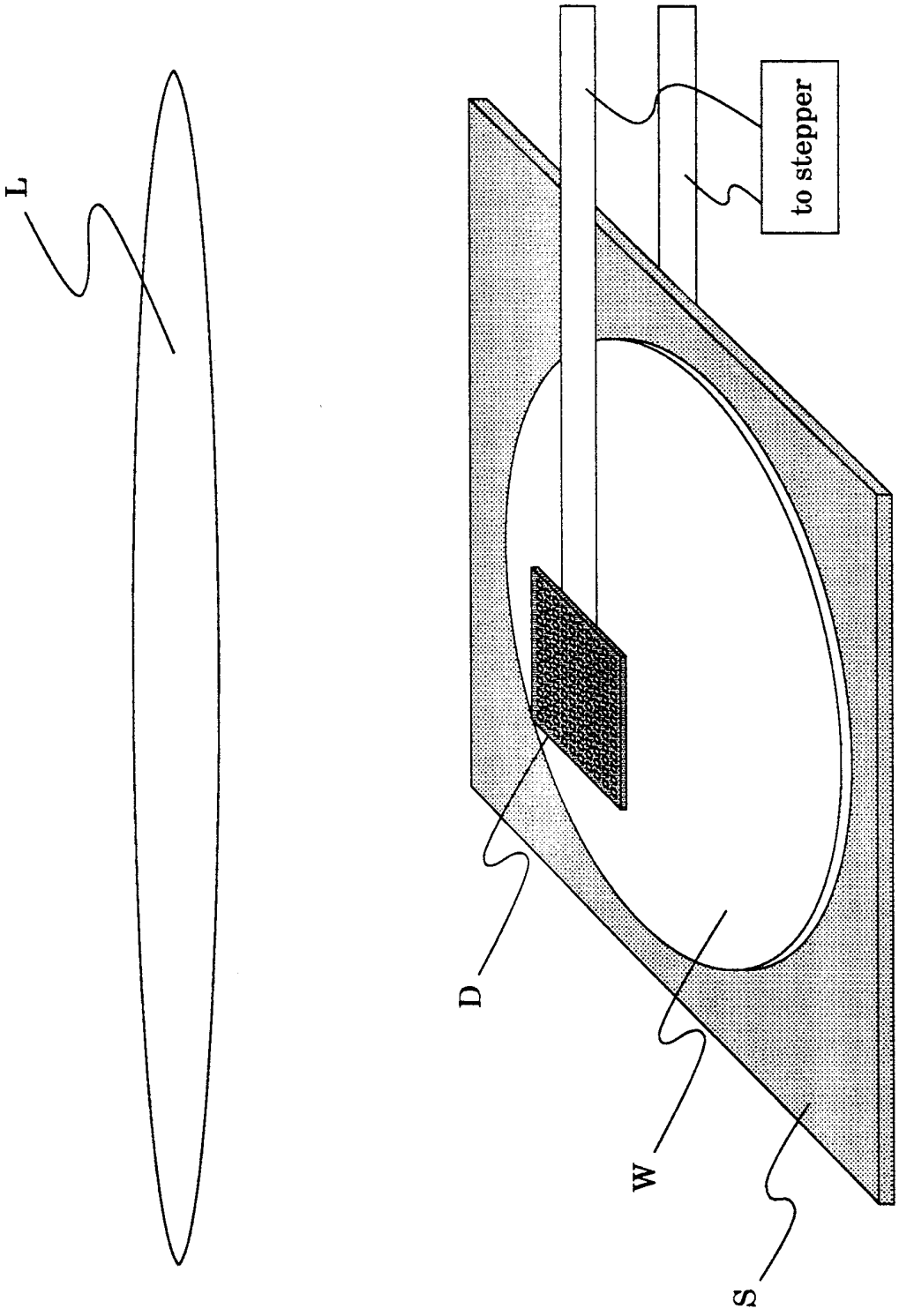
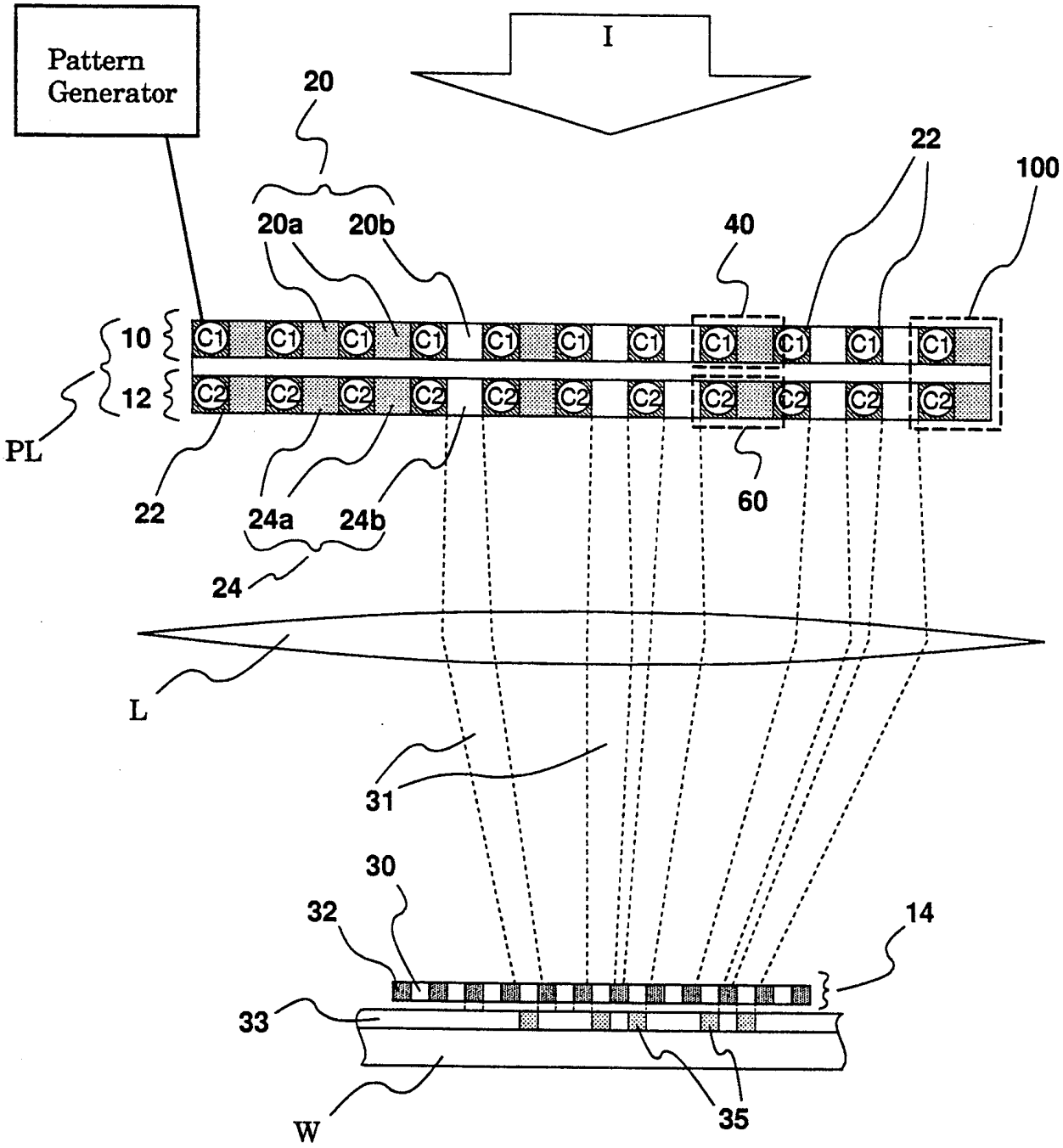


Fig. 7B


Pattern Generator
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20a
20b
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100
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10
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C1
C2
PL
22
24a
24b
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L
31
30
32
14
33
W
35

Fig. 8

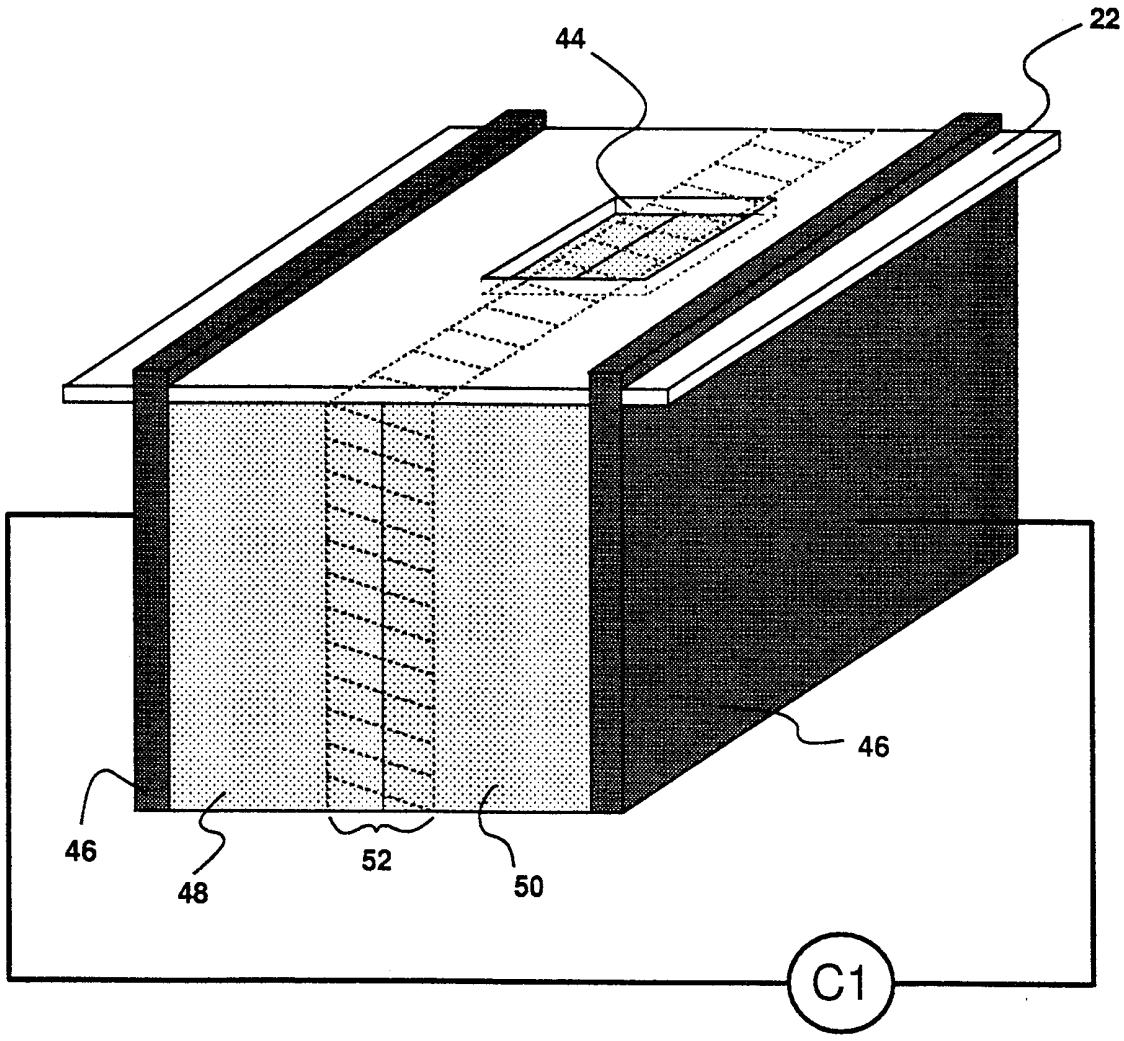


Fig. 9

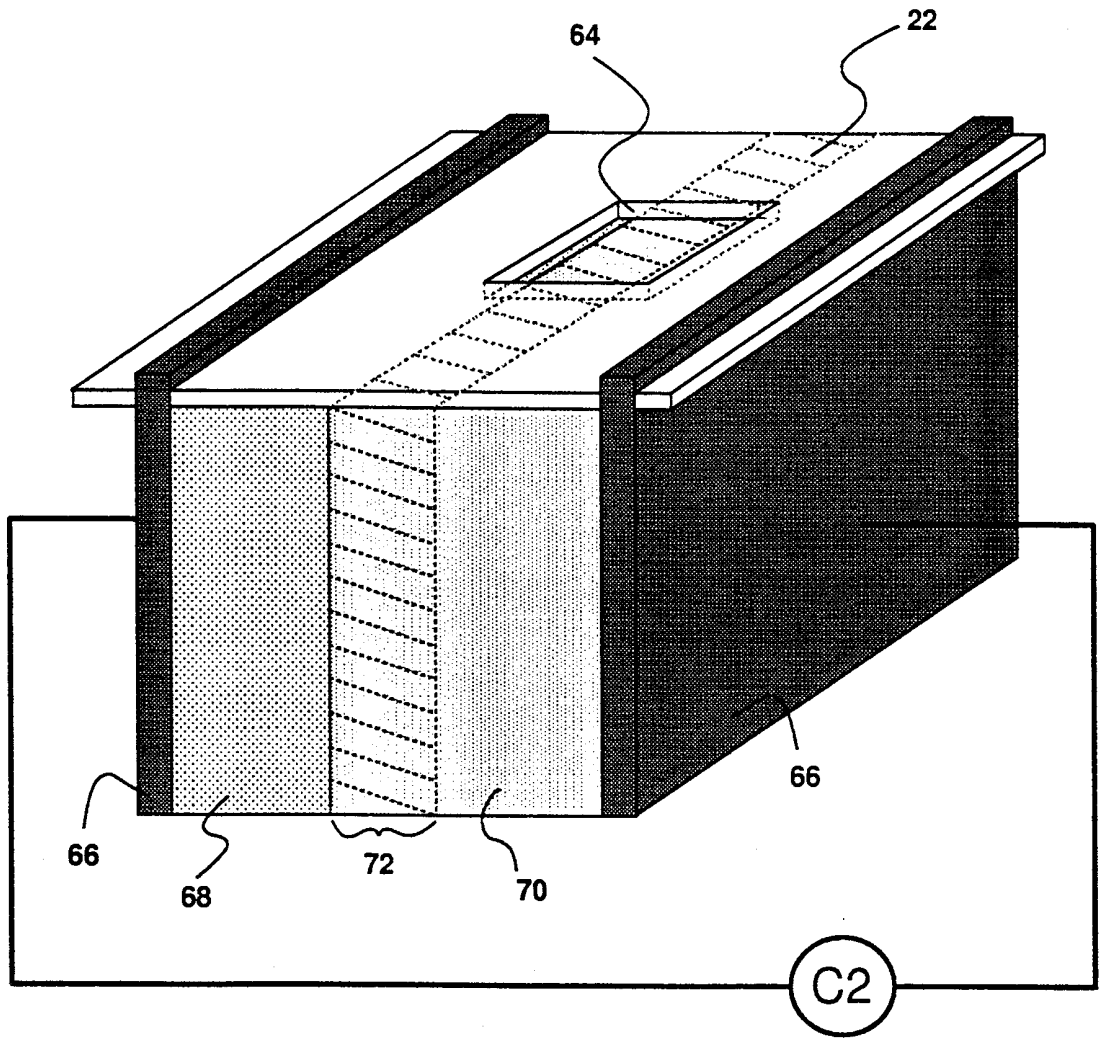
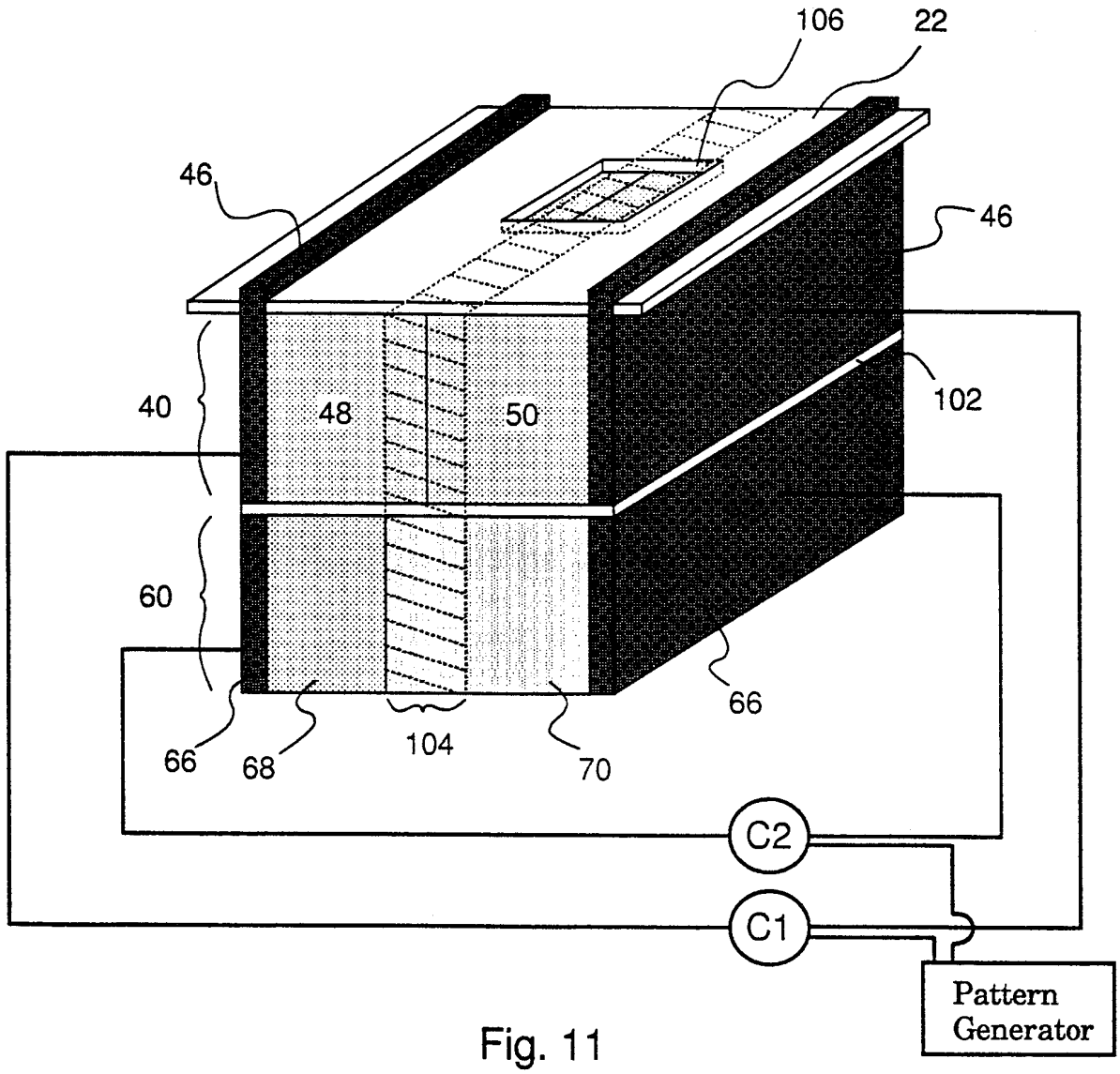


Fig. 10


106
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C2
C1
Pattern Generator

Fig. 11

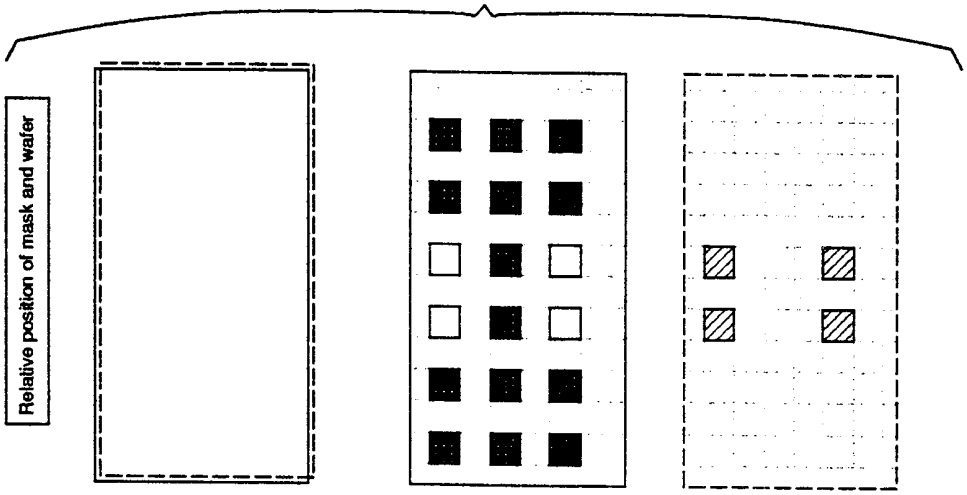

Fig. 12B

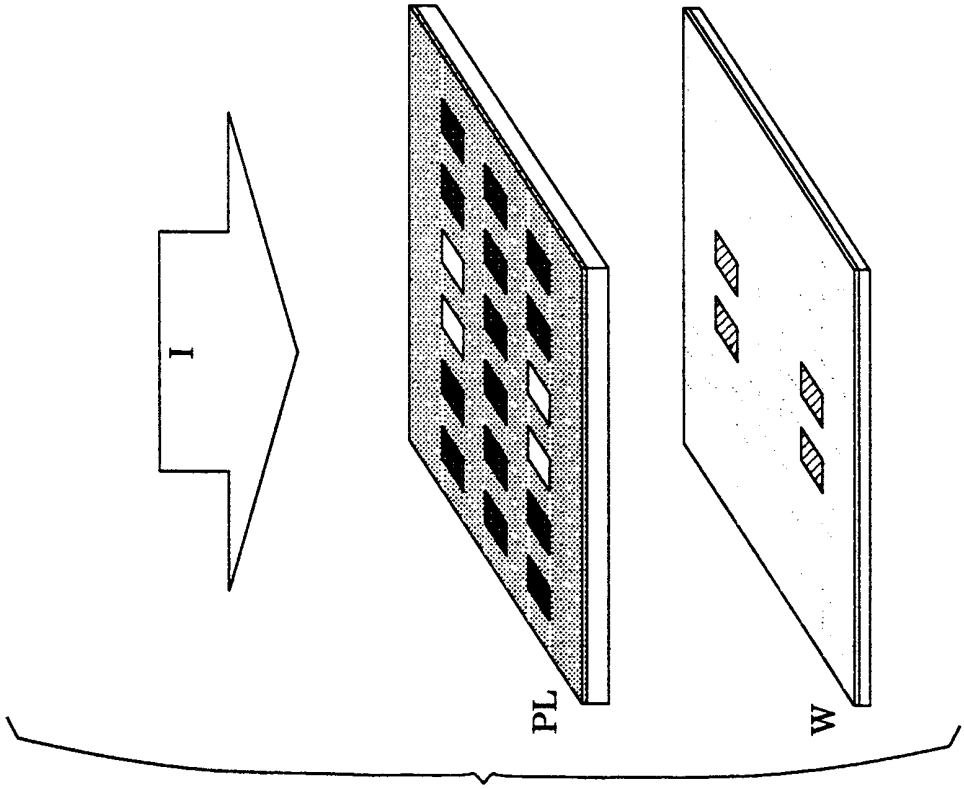

Fig. 12A

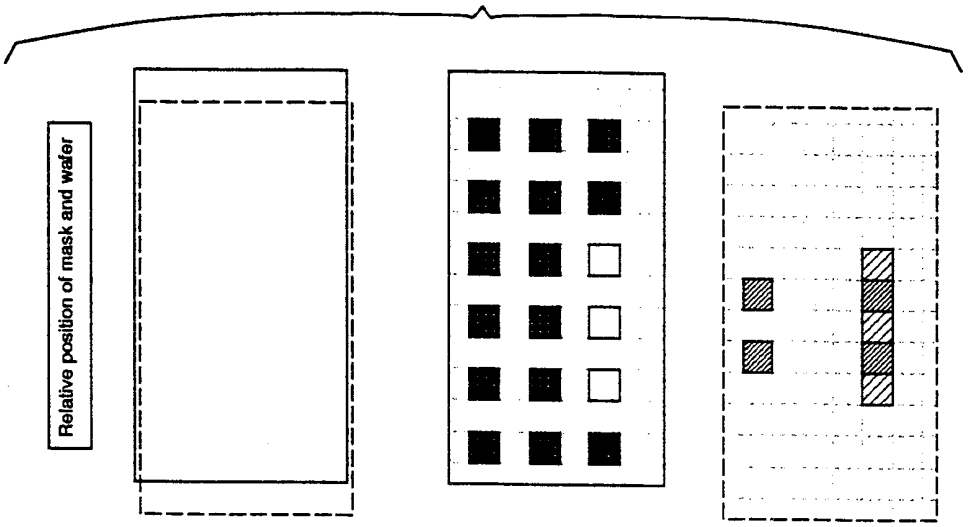

Fig. 12D

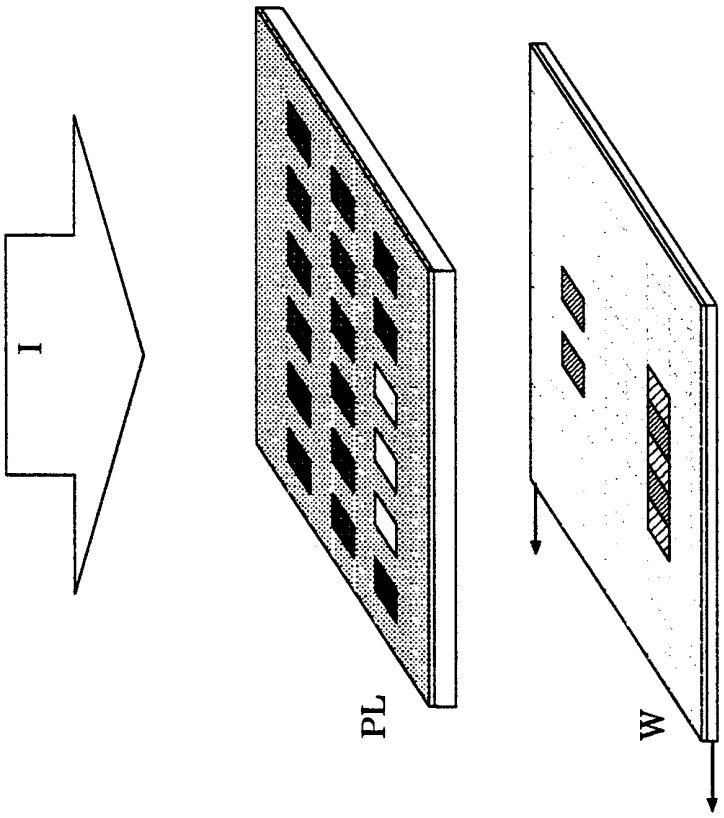

Fig. 12C

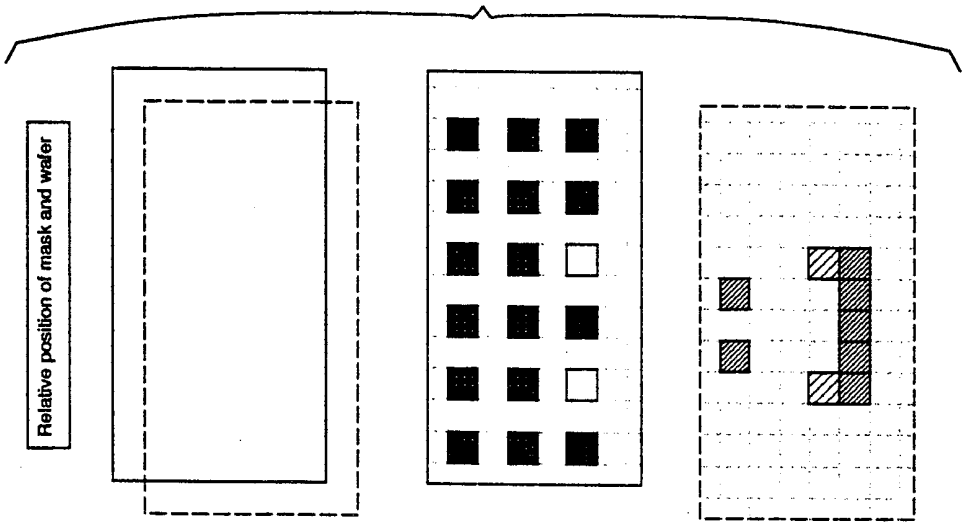

Fig. 12F

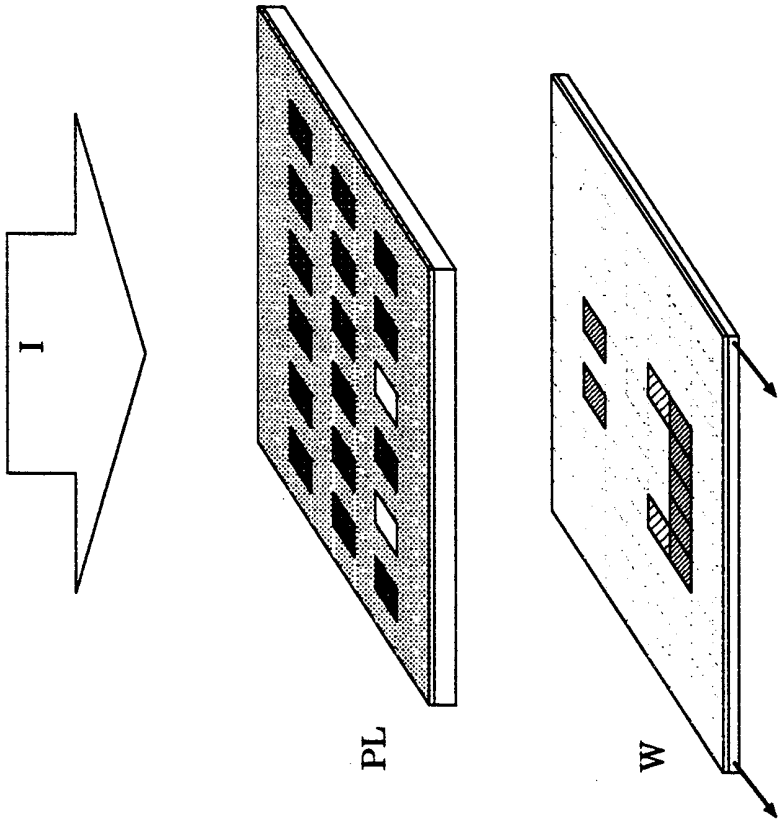

Fig. 12E

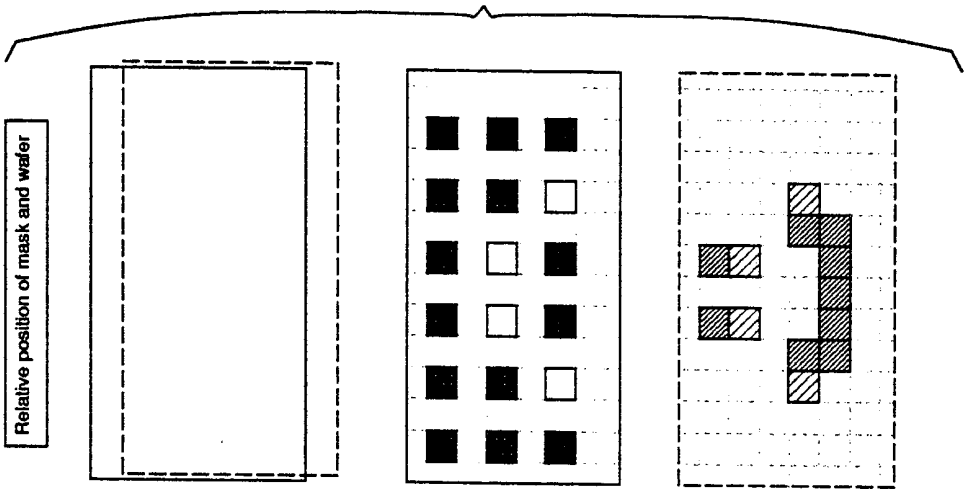

Fig. 12H

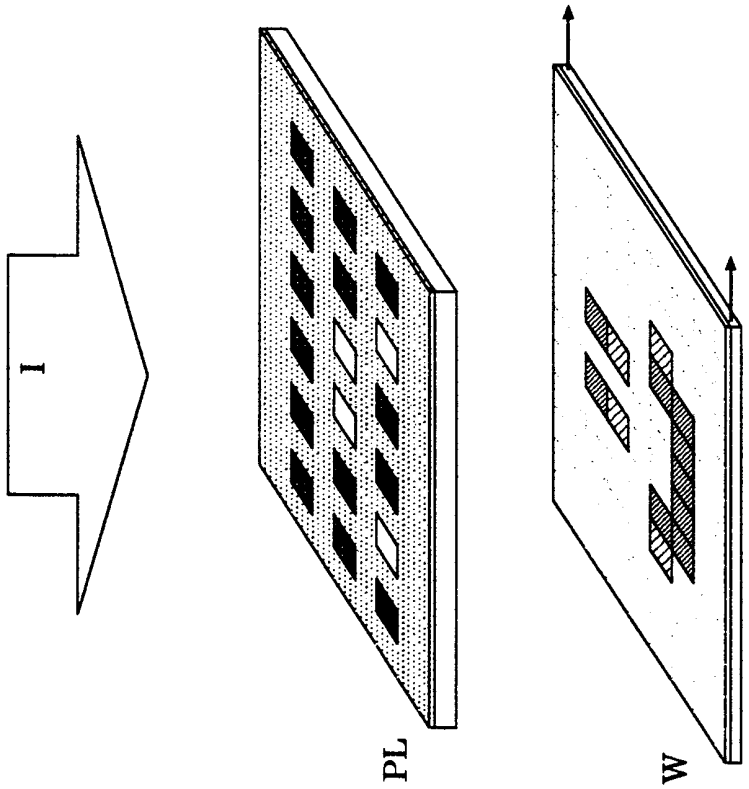

Fig. 12G

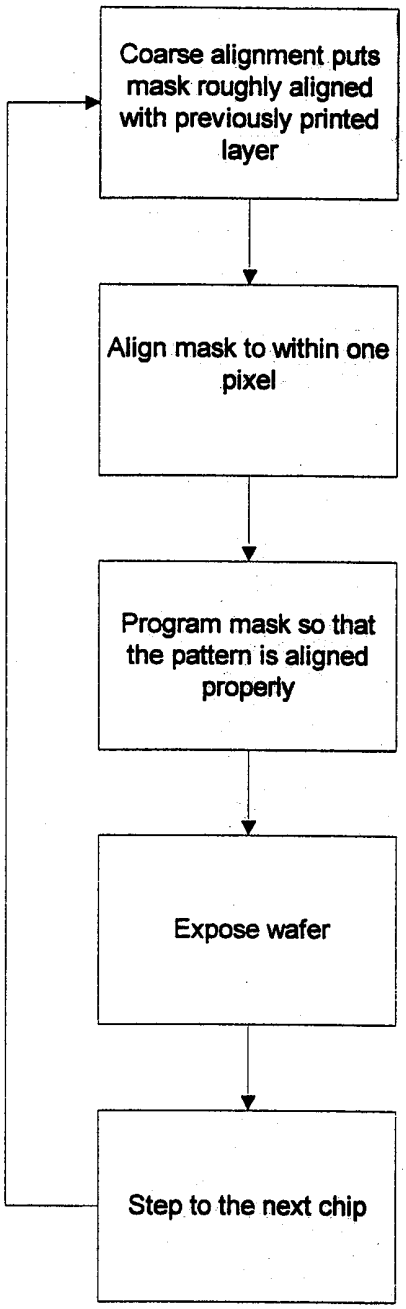
Coarse alignment puts mask roughly aligned with previously printed layer
Align mask to within one pixel
Program mask so that the pattern is aligned properly
Expose wafer
Step to the next chip

Fig. 13A

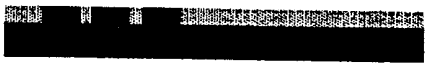

Fig. 13B

Fig. 13C

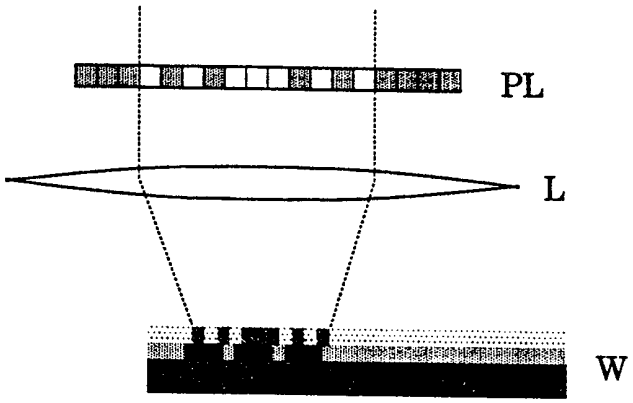

Fig. 13D

Fig. 13E

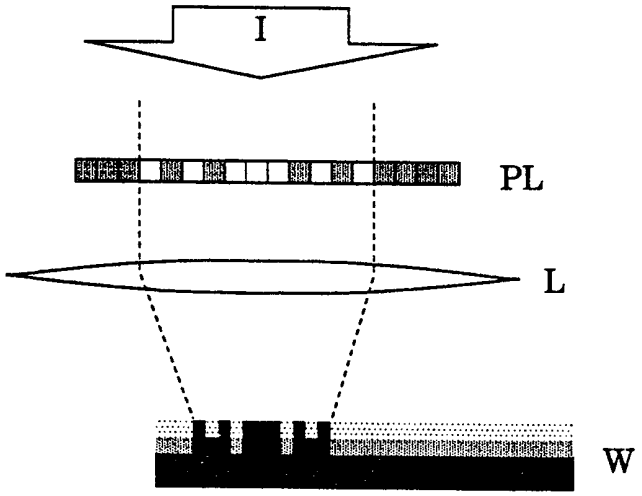

Fig. 13F

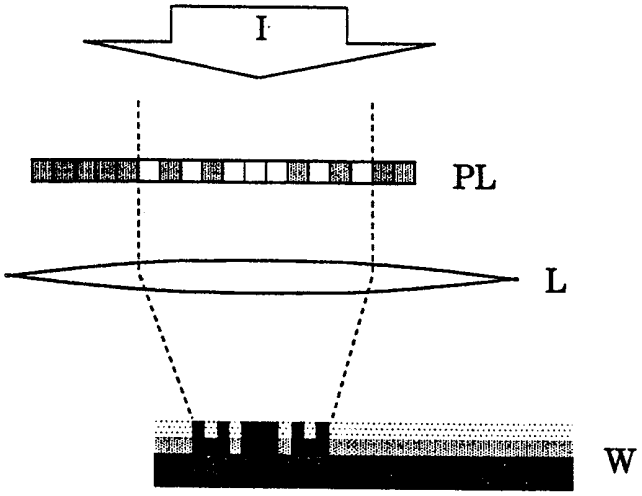

Fig. 13G

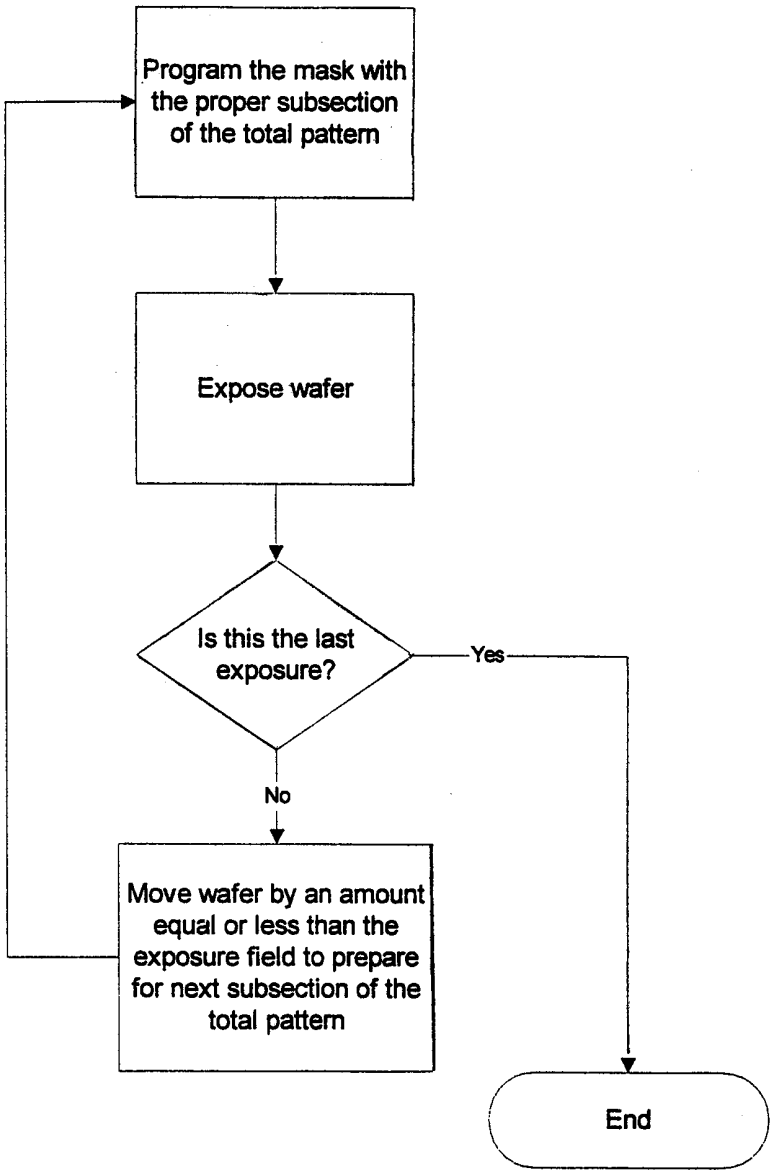
Program the mask with the proper subsection of the total pattern
Expose wafer
Is this the last exposure?
Yes
No
Move wafer by an amount equal or less than the exposure field to prepare for next subsection of the total pattern
End

Fig. 14A

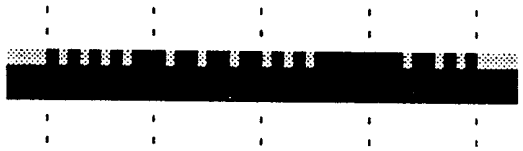

Fig. 14B

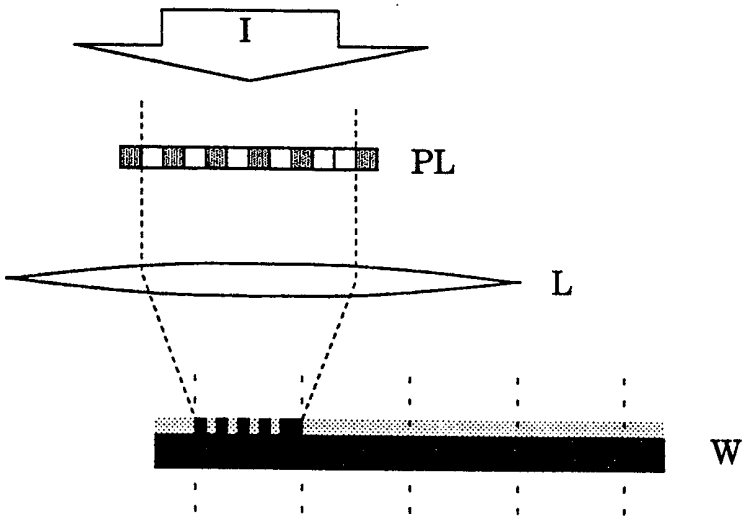

Fig. 14C

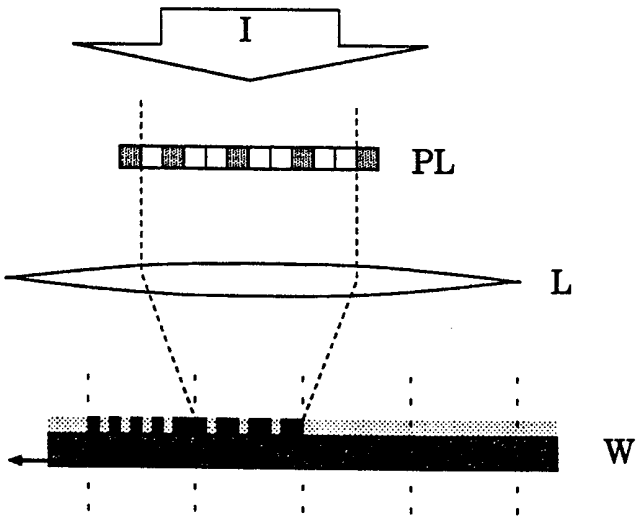

Fig. 14D

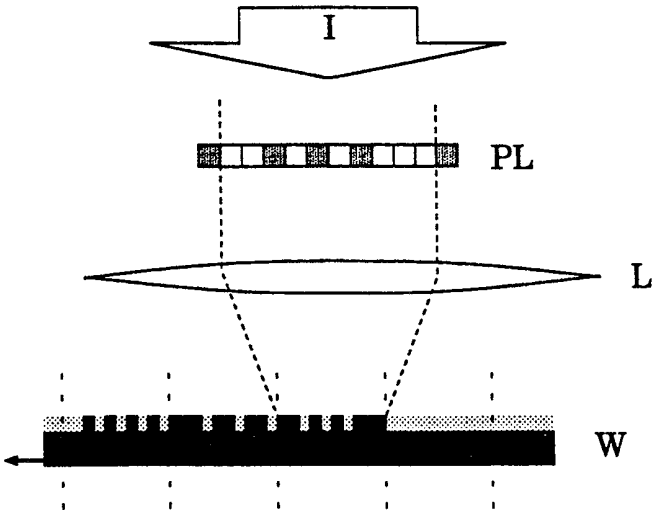

Fig. 14E

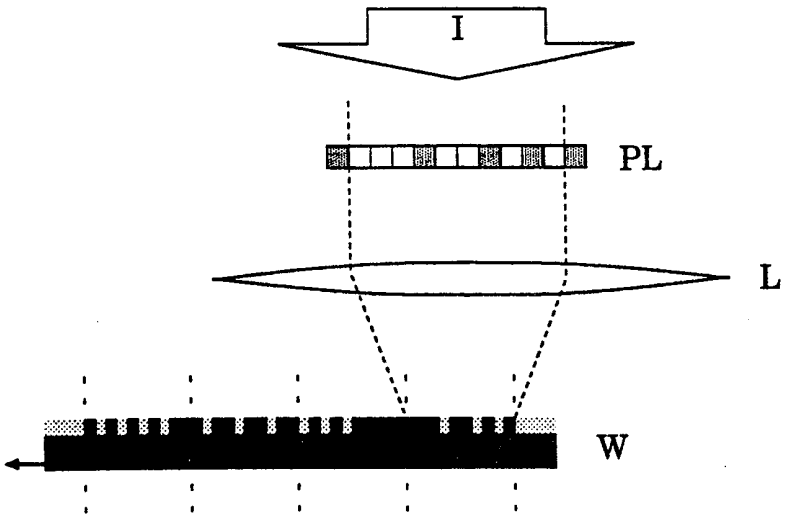

Fig. 14F

INTERNATIONAL SEARCH REPORT

National Application No
PCT/US 98/13068

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G03F7/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 91 10170 A (MANUFACTURING SCIENCES INC) 11 July 1991	1-10, 15-24, 29-38, 43-45, 47, 49-54, 57-59, 67-71
	see page 31, line 11 - page 32, line 22 see page 11, line 19 - page 14, line 12	
Y		13,14, 27,28, 41,42, 46,48
	see figures 1-5,18	
A		11,12, 25,26, 39,40, 55,56
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 September 1998	29/09/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Heryet, C

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

national Application No
PCT/US 98/13068

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	"ULTRA-RESOLUTION IMAGE TRANSFER" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 34, no. 10A, 1 March 1992, pages 158-162, XP000302260 see page 158 - page 160, paragraph 1 see page 161, paragraph 2 - page 163 see figure	60
Y		14,28, 42,46,48
X	EP 0 552 953 A (HUGHES AIRCRAFT CO) 28 July 1993 see column 1, line 45 - column 3, line 22 see figure	72
Y		13,27,41
X	GB 2 133 618 A (GEN ELECTRIC CO PLC) 25 July 1984 see page 1, line 86 - line 107 see figure	61,62, 64,65
X	US 4 586 053 A (HUGHES JOHN L) 29 April 1986 see column 3, line 20 - line 31; figure 3	61,63, 64,66
X	US 5 343 271 A (MORISHIGE YUKIO) 30 August 1994 see abstract; figure 11	73,74

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 98/13068

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		IL 104469 A	31-12-1995
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		GB 2140246 A,B	21-11-1984
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