SEMICONDUCTOR DEVICE INCLUDING DETECTOR CIRCUIT CAPABLE OF PERFORMING HIGH-SPEED OPERATION

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Abstract
A detector circuit and a negative voltage generating circuit capable of performing a high-speed operation are provided. A negative voltage generating circuit includes a charge pump circuit, a first voltage divider circuit that makes a voltage division between an output of the charge pump circuit and a power supply to output a detect potential, a reference voltage generating circuit that generates a reference potential, and a comparator circuit that compares the detect potential and the reference potential. The charge pump circuit is driven by an output signal of the comparator circuit and generates the negative voltage. In the first voltage divider circuit, NMOS transistors make the voltage division between the negative voltage and the power supply to obtain the detect potential.
FIG. 6

FIRST VOLTAGE DIVIDER CIRCUIT

REFERENCE VOLTAGE GENERATING CIRCUIT

LEVEL SHIFT CIRCUIT

LEVEL SHIFT CIRCUIT

V_DIV

V_REF

V_SDIV

V_SREF

COMPARATOR CIRCUIT

S_DET

FIG. 7

LEVEL SHIFT CIRCUIT

V_DIN

V_SVIN

LEVEL SHIFT CIRCUIT

V_REF

V_SREF

C2

C1

N12

N13

N14

N15

P18

P19

P4

N5

I1

V_C

VCON

CP

S_DET
**FIG. 8**

REFERENCE - - - - - - - - - - - - - - WOLTAGE GENERATING CIRCUIT

VREF

R3 C3

DETECTOR CIRCUIT

VNEG

SDET

**FIG. 9**

REFERENCE - - - - - - - - - - - - - - WOLTAGE GENERATING CIRCUIT

VREF

R4 C4

DETECTOR CIRCUIT

VNEG

SDET
SEMICONDUCTOR DEVICE INCLUDING DETECTOR CIRCUIT CAPABLE OF PERFORMING HIGH-SPEED OPERATION

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention
[0002] The present invention relates to a semiconductor device, and especially to a negative voltage generating circuit and a detector circuit provided therein.
[0003] 2. Description of the Background Art
[0004] Usually, a semiconductor device including a DRAM (Dynamic Random Access Memory) is provided with negative voltage generating circuitry for generating a voltage that is negative and lower than the ground (GND) potential (hereinafter referred to as a negative voltage). The negative voltage is used as a substrate bias potential and controls the transistor substrate effect. For example, in a DRAM that uses a PMOS transistor as a memory cell transfer gate, the negative voltage is used as a voltage for driving the transistor (activation voltage). It is necessary to set the transistor driving voltage sufficiently low, in order to write a ground-level signal to the memory cell during write and to extract a signal voltage with a sufficient amplitude from the memory cell during read.
[0005] In general, when a negative voltage generated by a negative voltage generating circuit is used, the negative voltage, potential variations are suppressed by large capacitance of the substrate, and the negative voltage generating circuit is not required to provide high-speed response. However, when the semiconductor device using the negative voltage as a transistor driving voltage is operated at high speed, the current consumption related to the negative voltage is large and therefore high-speed response of the negative voltage generating circuit is needed. Steadily supplying the negative voltage even when the current consumption related to the negative voltage is large requires quickly detecting potential variations of the negative voltage and feeding power (supplying charge).
[0006] Conventional negative voltage generating circuits are disclosed in Japanese Patent Application Laid-Open Nos. 10-239357 (1998) and 11-312392 (1999), for example. The negative voltage generating circuit described in Japanese Patent Application Laid-Open No. 10-239357, for example, includes a charge pump circuit for generating a negative voltage and a detector circuit for detecting the potential of the negative voltage (which is referred to also as “a negative voltage sensing circuit” or “a level detecting circuit”). When detecting the negative voltage becoming higher than a desired value because of current consumption, the detector circuit activates the charge pump circuit to supply charge to the negative voltage output so that the negative voltage keeps the desired value.
[0007] In conventional negative voltage generating circuits, the detector circuits do not have high-speed response. Accordingly, when the semiconductor device using the negative voltage as a transistor driving voltage is operated at high speed, the detector circuit may fail to sufficiently follow instantaneous variations of the negative voltage, which leads to unstable supply of the negative voltage.
[0008] Also, breakdown voltages of semiconductor devices are becoming lower because of recent downsizing of LSIs, i.e., miniaturization of transistors, which unavoidably leads to lower operating voltages (power-supply voltages). Moreover, battery-driven portable devices, for example, demand reduction of power consumption through reduction of operating voltage and reduction of consumption current. However, lower operating voltage further deteriorates the detector circuit response and reduces the stability of the negative voltage generating circuit. This hinders reduction of power consumption of the semiconductor devices.

SUMMARY OF THE INVENTION

[0009] An object of the present invention is to provide a semiconductor device including a detector circuit that is capable of performing stable high-speed operation and a negative voltage generating circuit having the detector circuit.
[0010] In an aspect of the invention, a semiconductor device includes a detector circuit that detects a level of a negative voltage. The detector circuit includes: a first voltage divider circuit that outputs a detect potential generated by a voltage division made by a plurality of MOS transistors connected in series between a potential of the negative voltage and a positive power-supply potential; and a comparator circuit that compares the detect potential and a predetermined reference potential.
[0011] The first voltage divider circuit included in the detector circuit is composed of a plurality of MOS transistors. Accordingly, the detect potential quickly varies following a variation of the negative voltage because of the effect of capacitive coupling by the gate capacitance and parasitic capacitance of the MOS transistors. This enables the comparator circuit to detect the variation of the negative voltage quickly, thus offering high-speed response.
[0012] These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] FIG. 1 is a diagram illustrating the configuration of a negative voltage generating circuit according to a first preferred embodiment;
[0014] FIGS. 2A, 2B and 3 are diagrams used to describe a negative voltage generating circuit according to a third preferred embodiment;
[0015] FIG. 4 is a diagram illustrating the configuration of a comparator circuit of a negative voltage generating circuit according to a fourth preferred embodiment;
[0016] FIG. 5 is a diagram illustrating the configuration of a comparator circuit of a negative voltage generating circuit according to a fifth preferred embodiment;
[0017] FIG. 6 is a diagram illustrating the configuration of a negative voltage generating circuit according to a sixth preferred embodiment;
[0018] FIG. 7 is a diagram showing a modification of the comparator circuit of the negative voltage generating circuit according to the sixth preferred embodiment;
[0019] FIG. 8 is a diagram illustrating the configuration of a negative voltage generating circuit according to a seventh preferred embodiment;
[0020] FIG. 9 is a diagram illustrating the configuration of a negative voltage generating circuit according to an eighth preferred embodiment;
[0021] FIGS. 10 to 12 are diagrams showing examples of the configuration of a first voltage divider circuit according to a ninth preferred embodiment;
Fig. 13 is a circuit diagram of conventional word line driver and DRAM cell;

Fig. 14 is a cross-sectional view of the conventional word line driver and DRAM cell;

Fig. 15 is a circuit diagram of a word line driver and a DRAM cell according to a tenth preferred embodiment;

Fig. 16 is a cross-sectional view of the word line driver and the DRAM cell according to the tenth preferred embodiment;

Fig. 17 is a circuit diagram of a first voltage divider circuit according to the tenth preferred embodiment; and

Fig. 18 is a cross-sectional view of the first voltage divider circuit according to the tenth preferred embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will now be described. In this specification, for the sake of simplicity of description, when the potential of a negative voltage is low (i.e., when the absolute value of the negative voltage is large), it may be expressed as "the negative voltage is deep". On the other hand, when the potential of the negative voltage is high (i.e., when the absolute value of the negative voltage is small), it may be expressed as "the negative voltage is shallow".

First Preferred Embodiment

Fig. 1 is a diagram illustrating the configuration of a negative voltage generating circuit included in a semiconductor device according to a first preferred embodiment of the present invention. As shown in Fig. 1, the negative voltage generating circuit includes a charge pump circuit 1, a detector circuit 2, and a reference voltage generating circuit 3.

The charge pump circuit 1 is driven by an output signal of the detector circuit 2 ("detect signal S_DET described later) and generates and outputs a predetermined negative voltage V_NEG.

The detector circuit 2 includes a first voltage divider circuit 21 and a comparator circuit 22. The first voltage divider circuit 21 includes two diode-connected NMOS transistors N1 and N2, where the NMOS transistors N1 and N2 make a voltage division between the output of the charge pump circuit 1 (the negative voltage V_NEG) and a power supply V_DD as a positive potential, and the first voltage divider circuit 21 outputs the obtained potential V_DD with the potential at a node connecting the NMOS transistor N1 and the NMOS transistor N2, which is hereinafter referred to as "detect potential V_DET".

In this preferred embodiment, the channel width sizes of the NMOS transistors N1 and N2 are set equal to each other. That is, the voltage division ratio of the first voltage divider circuit 21 is ½ and the detect potential V_DET is given as V_DET = (V_DD + V_NEG)/2. The detect potential V_DET is inputted to the comparator circuit 22.

The comparator circuit 22 compares the detect potential V_DET outputted from the first voltage divider circuit 21 and a predetermined reference potential V_REF outputted from the reference voltage generating circuit 3 to detect the level of the negative voltage V_NEG. That is, when the negative voltage V_NEG is deeper than a given value, the detect potential V_DET is smaller than the reference potential V_REF and the detect signal S_DET outputted from the comparator circuit 22 is kept at an L (Low) level. When the negative voltage V_NEG becomes shallower than a given value, the detect signal S_DET varies to an H (High) level.

As shown in Fig. 1, the comparator circuit 22 includes a comparator CP and inverters I1 to I3 provided in its output stage. The inverters I1 to I3 wave-shape an output voltage V_c from the comparator CP to convert it into the detect signal S_DET as a logical signal.

The comparator CP includes PMOS transistors P1 and P2 forming a differential pair, NMOS transistors N3 and N4 forming a current mirror circuit as a load, and a PMOS transistor P3 functioning as a constant-current source. That is, the comparator CP is a so-called "current mirror type differential amplifier".

Also, a PMOS transistor P5 is provided to give a constant current to the inverter I1 (a PMOS transistor P4 and an NMOS transistor N5) that receives the output voltage V_c from the comparator CP. A constant voltage V_CON is applied to the gates of both of the PMOS transistor P3 and the PMOS transistor P5.

In this circuit configuration, the response speeds of the comparator CP and the inverter I1 are determined by the magnitudes of the currents supplied through the PMOS transistors P3 and P5. That is, by keeping the output voltage V_CON constant, the response speeds of the comparator CP and the inverter I1 are kept constant without depending on the voltage of the power supply V_DD.

The PMOS transistors P3 and P5 function also to restrict to given values the through currents flowing from the power supply V_DD to the ground GND through the comparator CP and the inverter I1, thereby suppressing the current consumption of the comparator CP and the inverter I1. The current values supplied from the PMOS transistors P3 and P5 can be adjusted by adjusting the magnitude of the voltage V_CON applied to their gates or by adjusting the channel width sizes.

As mentioned earlier, the charge pump circuit 1 is driven by the detect signal S_DET. That is, the charge pump circuit 1 is activated when the detect signal S_DET attains the H level and then supplies charge to the output node to deepen the negative voltage V_NEG. When the negative voltage V_NEG becomes deeper than a particular value, the detect signal S_DET goes to the L level and then the charge pump circuit 1 is inactivated and stops the supply of charge. The charge pump circuit 1 thus operates according to the detect signal S_DET so as to keep the negative voltage V_NEG at a value based on the level of the reference potential V_REF.

The reference voltage generating circuit 3, for generating the reference potential V_REF, includes a second voltage divider circuit 31 and a buffer circuit 32. The second voltage divider circuit 31 includes two resistors R1 and R2, where the resistors R1 and R2 make a voltage division between the ground GND and the power supply V_DD and the second voltage divider circuit 31 outputs the obtained predetermined potential V_REFO (the potential of a node connecting the resistor R1 and the resistor R2).

In this preferred embodiment, the resistance values n [Ω] and m [Ω] of the resistors R1 and R2 in the second voltage divider circuit 31 are set equal to each other. That is, the voltage division ratio is 1/2 as in the first voltage divider circuit 21, and V_REFO = V_DD/2. The potential V_REFO outputted from the second voltage divider circuit 31 is inputted to the buffer circuit 32 (adjustment circuit). The buffer circuit 32...
makes the magnitude of the potential $V_{REFO}$ smaller by a predetermined adjustment value and outputs it as the reference potential $V_{REF}$.

[0042] As shown in FIG. 1, the buffer circuit 32 includes PMOS transistors P6 to P11 and NMOS transistors N6 to N9. The transistors P10 and P11, both receiving a constant voltage $V_{CON}$ at their gates, pass constant current to the buffer circuit 32 and restrict the through current flowing through the buffer circuit 32 to suppress current consumption. The current values supplied from the PMOS transistors P10 and P11 can be adjusted by adjusting the magnitude of the voltage $V_{CON}$ applied to their gates or by adjusting the channel width sizes.

[0043] When the channel width sizes of the PMOS transistors P6, P7, P8 and P9 and the NMOS transistors N6, N7, N8 and N9 are defined as $W_{P6}W_{P7}W_{P8}W_{P9}$, $W_{N6}W_{N7}W_{N8}W_{N9}$ and $W_{P6}$, $W_{P7}$, $W_{P8}$, $W_{P9}$, $W_{N6}$, $W_{N7}$, $W_{N8}$, and $W_{N9}$, and the gradient of the transistors’ $I_{DS}$-$V_{GS}$ characteristic ($I_{DS}$-gated voltage current, $V_{T1}$-gate voltage in the sub-threshold region, with the logarithm of $I_{DS}$ is defined as $S$ (the quantity of variation of the gate voltage required for a one-digit variation of the current (the so-called S factor)), then the reference potential $V_{REF}$ outputted from the buffer circuit 32 is given as:

$$V_{REF} = \frac{1}{2}\left(1 + 2^S\right)\frac{W_{P6}W_{P7}W_{P8}W_{P9}W_{N6}W_{N7}W_{N8}W_{N9}}{W_{P6}W_{P7}W_{P8}W_{P9}}\cdot V_{CON}$$

[0044] Where, when the channel width sizes of the PMOS transistors P6 to P9 and the NMOS transistors N6 to N9 are set as:

$$(W_{P6}W_{P7}W_{P8}W_{P9})(W_{N6}W_{N7}W_{N8}W_{N9})$$

then the reference potential $V_{REF}$ is lower than the output potential $V_{REFO}$ of the second voltage divider circuit 31. Then, when a definition is given as:

$$\Delta V = \frac{1}{2}\left(1 + 2^S\right)\frac{W_{P6}W_{P7}W_{P8}W_{P9}W_{N6}W_{N7}W_{N8}W_{N9}}{W_{P6}W_{P7}W_{P8}W_{P9}} \cdot V_{CON}$$

the expression of the reference potential $V_{REF}$ is given as:

$$V_{REF} = V_{REFO} - \Delta V$$

That is, $\Delta V$ corresponds to the “adjustment value” mentioned above.

[0045] The reference potential $V_{REF}$ outputted from the buffer circuit 32 is inputted to the comparator circuit 22 (the comparator CP). The capacitor CI is provided to stabilize the reference potential $V_{REF}$.

[0046] The operation of the negative voltage generating circuit according to the preferred embodiment will be described below. In this preferred embodiment, $V_{DD}=V_{DD}+V_{NNEG}/2$ and $V_{REF}=V_{REFO}-\Delta V=V_{DD}/2-\Delta V$, so that the detector circuit 2 outputs the detect signal $S_{DET}$ at the L level when $V_{NNEG}/2>\Delta V$, and outputs the detect signal $S_{DET}$ at the L level when $V_{NNEG}/2<\Delta V$. That is, the detector circuit 2 operates to detect the negative voltage $V_{NNEG}$ so that $V_{NNEG}=-\Delta V/2$.

[0047] The detect signal $S_{DET}$ outputted from the detector circuit 2 is inputted to the charge pump circuit 1, and the charge pump circuit 1 is driven by the detect signal $S_{DET}$. When the negative voltage $V_{NNEG}$ is shallower than $-\Delta V/2$, the detect signal $S_{DET}$ is at the H level and the charge pump circuit 1 is activated to deepen the negative voltage $V_{NNEG}$. When the negative voltage $V_{NNEG}$ reaches $-\Delta V/2$ and the detect signal $S_{DET}$ goes to the L level, the charge pump circuit 1 is then inactivated and stops the supply of charge to the negative voltage $V_{NNEG}$ output node. The negative voltage generating circuit thus keeps the output of the negative voltage $V_{NEG}$ at $-\Delta V/2$.

[0048] As is known from the description above, the value of the negative voltage $V_{NEG}$ outputted from the negative voltage generating circuit of the preferred embodiment can be adjusted by varying the value of $\Delta V$ by adjusting the channel width sizes of the PMOS transistors P6 to P9 and the NMOS transistors N6 to N9 of the buffer circuit 32.

[0049] When the negative voltage $V_{NEG}$ instantly varies because of, e.g., current consumption of the device that uses the negative voltage $V_{NEG}$ as a driving voltage, the detect potential $V_{DET} = (V_{DD}+V_{NEG})/2$ varies. According to the present invention, since the first voltage divider circuit 21 is composed of the NMOS transistors N1 and N2, the detect potential $V_{DET}$ quickly varies following the variation of the negative voltage $V_{NEG}$ because of the effect of capacitive coupling by the gate capacitance and parasitic capacitance of the NMOS transistors N1 and N2. This offers high-speed response superior to those of conventional detector circuits.

[0050] Also, as described earlier, the response speeds of the comparator CP and the inverter I1 are determined by the magnitudes of the currents supplied through the PMOS transistors P3 and P5, and are hardly affected by the power-supply voltage $V_{DD}$. For example, increasing the current flowing to the comparator CP shortens the charging/discharging time of the input gate of the next-stage inverter I1, which enhances the high-speed response of the comparator CP. Also, the high-speed response of the inverter I1 can be enhanced by increasing the current flowing to the inverter I1. Thus, the negative voltage generating circuit of the preferred embodiment is capable of performing high-speed operation even when the power-supply voltage is low.

[0051] However, as mentioned earlier, the PMOS transistors P3 and P5 have a function of suppressing the current consumption by restricting the currents flowing in the comparator CP and the inverter I1 to given values, and therefore it is not preferred that the PMOS transistors P3 and P5 supply excessively large current values. Accordingly, it is desirable to properly set the current values in accordance with the purpose of use of the negative voltage generating circuit. The current values supplied from the PMOS transistors P3 and P5 can be controlled by adjusting the magnitude of the voltage $V_{CON}$ applied to the gates of the PMOS transistors P3 and P5 or by adjusting the channel width sizes of the PMOS transistors P3 and P5.

[0052] As described so far, according to this preferred embodiment, the NMOS transistors N1 and N2 in the first voltage divider circuit 21 make a voltage division between the power supply $V_{DD}$ and the negative voltage $V_{NEG}$ to obtain the detect potential $V_{DET}$ so that the detect potential $V_{DET}$ quickly responds to variations of the negative voltage $V_{NEG}$. Also, the response speeds of the comparator CP and the inverter I1 are independent of the voltage of the power supply $V_{DD}$ and are determined by the current values supplied from the PMOS transistors P3 and P5. Therefore, the detector circuit 2 and the negative voltage generating circuit including the detector circuit 2 are capable of performing high-speed operation even when the power-supply voltage is low. This contributes to achievement of higher-speed operation of the semiconductor device and reduction of power consumption.

Second Preferred Embodiment

[0053] In the first preferred embodiment, the voltage division ratio of the first voltage divider circuit 21 and the voltage
division ratio of the second voltage divider circuit 31 are set equal to each other. In this case, the value of the negative voltage $V_{NEG}$ outputted from the negative voltage generating circuit does not depend on the potential of the power supply $V_{DD}$. In the first preferred embodiment, for example, the voltage division ratio of the first voltage divider circuit 21 and the voltage division ratio of the second voltage divider circuit 31 are both 1/2, and therefore $V_{NEG} = -\Delta V \times 2$, which shows that the negative voltage $V_{NEG}$ does not depend on the potential of the power supply $V_{DD}$.

[0054] On the other hand, in a second preferred embodiment, the resistance value of the resistor R1 of the second voltage divider circuit 31 and the resistance value of the resistor R2 are set at different values so that the negative voltage $V_{NEG}$ varies depending on the potential of the power supply $V_{DD}$.

[0055] That is, in this preferred embodiment, the voltage division ratio of the second voltage divider circuit 31 is adjusted to be different from the voltage division ratio (1/2) of the first voltage divider circuit 21. Herein, for the sake of simplicity, the voltage division ratio of the first voltage divider circuit 21 is left at 1/2, but the value of the voltage division ratio of the first voltage divider circuit 21 may be adjusted. However, adjusting the voltage division ratio of the second voltage divider circuit 31 is easier because changing the voltage division ratio of the first voltage divider circuit 21 requires changing the channel width sizes of the NMOS transistors N1 and N2.

[0056] When the resistance values of the resistors R1 and R2 of the second voltage divider circuit 31 are represented respectively as $n \Omega$ and $m \Omega$ ($m = n$), the output potential $V_{REFO}$ of the second voltage divider circuit 31 is given as:

$$V_{REFO} = V_{DD}(-m/n) - V_{DD}(-n/m)(1 + 2m).$$

From the relation $V_{REF} = V_{REFO} - \Delta V$, the detect potential of the detector circuit 2, i.e., the negative voltage $V_{NEG}$ outputted from the negative voltage generating circuit, is given as:

$$V_{NEG} = V_{DD}(-m/n) + V_{DD}(-n/m)(1 + 2m).$$

As is known from the expression, the negative voltage $V_{NEG}$ has dependence on the power-supply potential $V_{DD}$ when $m = n$.

[0057] Now, when $m > n$, the negative voltage $V_{NEG}$ varies to become deeper in proportion to the power-supply potential $V_{DD}$. This is effective when the negative voltage $V_{NEG}$ is used as the well potential of an NMOS transistor, for example. That is, when the NMOS transistor turns off and the drain voltage attains the power-supply potential $V_{DD}$, leakage current increases when the power-supply potential $V_{DD}$ is high. However, the leakage current is reduced when the well potential (the negative voltage $V_{NEG}$) varies to be deeper in proportion to the power-supply potential $V_{DD}$.

[0058] On the other hand, when $m < n$, the negative voltage $V_{NEG}$ varies to become shallower in proportion to the power-supply potential $V_{DD}$. For example, when the power-supply potential $V_{DD}$ and the potential of the negative voltage $V_{NEG}$ are applied between the source and drain of a transistor, the electric field is alleviated even when the power-supply potential $V_{DD}$ is high, which improves the reliability of the breakdown voltage of the transistor.

[0059] As described in this preferred embodiment, the negative voltage $V_{NEG}$ outputted from the negative voltage generating circuit has dependence on the power-supply potential $V_{DD}$ when the voltage division ratio of the first voltage divider circuit 21 and the voltage division ratio of the second voltage divider circuit 31 are set at different values. This enables the negative voltage generating circuit to be suitably used according to the purpose of use.

Third Preferred Embodiment

[0060] In this preferred embodiment, the negative voltage generating circuit of the first preferred embodiment is provided with a current cut (shutdown) function for preventing unnecessary current consumption. That is, when the operation of the detector circuit 2 is not needed, a "current cut mode" is selected to cut off the current flowing in the detector circuit, and the detector circuit 2 is placed in an idle state to reduce the power consumption.

[0061] FIGS. 2A, 2B, and 3 are diagrams used to describe the negative voltage generating circuit according to a third preferred embodiment. FIGS. 2A and 2B are circuit diagrams showing examples of the first voltage divider circuit 21 of the negative voltage generating circuit, and FIG. 3 is a circuit diagram of the comparator circuit 22 of the negative voltage generating circuit. Except for the first voltage divider circuit 21 and the comparator circuit 22, the configuration of the negative voltage generating circuit of this preferred embodiment is the same as that shown in FIG. 1. Therefore, only the first voltage divider circuit 21 and the comparator circuit 22 will be described below and the remaining components are not described here again.

[0062] When the first voltage divider circuit 21 is formed of two NMOS transistors (NMOS transistors N1 and N2) as shown in FIG. 1, the current cut function can be given to the first voltage divider circuit 21 with the configuration shown in FIG. 2A, for example. That is, a PMOS transistor P12 is connected in series with the NMOS transistors N1 and N2 to serve as a switching element for cutting off the current flowing to the NMOS transistors N1 and N2.

[0063] The gate of the PMOS transistor P12 receives a current cut signal $S_{CUT}$ as a control signal for placing the detector circuit 2 in the current cut mode. When the current cut signal $S_{CUT}$ goes to an H level, the PMOS transistor P12 turns off and cuts off the current flowing from the power supply $V_{DD}$ to the negative voltage $V_{NEG}$ (the output terminal of the charge pump circuit 1) through the first voltage divider circuit 21 (the NMOS transistors N1 and N2).

[0064] However, when the first voltage divider circuit 21 is formed of NMOS transistors, there is a need to give dedicated P well potentials, which requires isolation of the P wells. In this case, the formation requires a relatively large area to surround the bottoms of the P wells with an N well.

[0065] Accordingly, the first voltage divider circuit 21 may be formed of PMOS transistors. When the first voltage divider circuit 21 is formed of PMOS transistors, there is no need to surround the bottoms of the dedicated N wells with a P well, which contributes to reduction of the formation area. The first voltage divider circuit 21 formed of PMOS transistors can be given the current cut function with the configuration as shown in FIG. 2B, for example.

[0066] That is, the first voltage divider circuit 21, for making a voltage division between the power supply $V_{DD}$ and the negative voltage $V_{NEG}$, is formed of PMOS transistors P13 and P14, and an NMOS transistor N10 is provided between them as a switching element for cutting off the current flowing thereto. Also, in order to prevent floating of the well potential of the PMOS transistor P14 connected on the negative voltage $V_{NEG}$ side, a PMOS transistor P15 is provided to fix the detect potential $V_{DIV}$ at the power supply $V_{DD}$. 
The gates of the NMOS transistor \( N_{10} \) and the PMOS transistor \( P_{15} \) receive an inversion of the current cut signal \( \delta_{cut} \) that is inverted by an inverter \( I_4 \). The inverted signal goes to an \( L \) level when the current cut signal \( \delta_{cut} \) goes to an \( H \) level, and then the NMOS transistor \( N_{10} \) turns off to cut off the current flowing from the power supply \( V_{DD} \) to the negative voltage \( V_{NCG} \) node (the output terminal of the charge pump circuit \( I \)). At the same time, the PMOS transistor \( P_{15} \) turns on and fixes the well potential of the NMOS transistor \( P_{14} \) at the detect potential \( V_{DD} \).

[0062] Thus, in the negative voltage generating circuit, giving a current cut function as shown in FIG. 2A or 2B to the first voltage divider circuit \( D_1 \) reduces the current consumption when the operation of the detector circuit \( I_2 \) is not needed. This is effective when removal of the current flowing between \( V_{DD} \) and negative voltage \( V_{NCG} \) is desired, such as when the device uses the negative voltage generating circuit has a low power consumption mode or when an evaluation of the device is made.

[0069] FIG. 3 shows a circuit configuration in which the comparator circuit \( C_2 \) has a current cut function. That is, a PMOS transistor \( P_{16} \) is provided in series with the PMOS transistor \( P_3 \) that supplies a constant current to the comparator \( C_1 \); so that the through current flowing from the power supply \( V_{DD} \) to the negative voltage \( V_{NCG} \) through the comparator \( C_1 \) can be cut off in the current cut mode. Also, an NMOS transistor \( N_{11} \) is provided in parallel with the NMOS transistors \( N_3 \) and \( N_4 \), forming a current mirror circuit, can be fixed at the ground GND level in the current cut mode. Furthermore, a PMOS transistor \( P_{17} \) is connected between the input end of the inverter \( I_1 \) and the power supply \( V_{DD} \), so that the input to the inverter \( I_1 \) (i.e., the output node of the comparator \( C_1 \)) can be fixed at the \( H \) level in the current cut mode.

[0070] The PMOS transistor \( P_{16} \) and the NMOS transistor \( N_{11} \) receive the above-mentioned current cut signal \( \delta_{cut} \), and the PMOS transistor \( P_{17} \) receives an inversion of the current cut signal \( \delta_{cut} \) through an inverter \( I_5 \).

[0071] When the current cut signal \( \delta_{cut} \) goes to the \( H \) level, the PMOS transistor \( P_{16} \) turns off and cuts off the current of the comparator \( C_1 \). At the same time, the PMOS transistor \( P_{17} \) turns on and the input of the inverter \( I_1 \) at the \( H \) level to prevent the through current flowing in the inverter \( I_1 \) (the detect signal \( \delta_{DP} \) goes to the \( L \) level at this time and the charge pump circuit \( I \) is inactivated). Also, the NMOS transistor \( N_{11} \) turns on and turns off the NMOS transistors \( N_3 \) and \( N_4 \), thus preventing generation of through current flowing through the PMOS transistor \( P_{17} \) and the NMOS transistor \( N_4 \). That is, the NMOS transistor \( N_{11} \), the PMOS transistors \( P_{16}, P_{17} \), and the inverter \( I_5 \) form a through current cutting off circuit that cuts off the current flowing in the comparator circuit \( C_2 \).

[0072] When the first voltage divider circuit \( D_1 \) of FIG. 2A or 2B is combined with the comparator circuit \( C_2 \) of FIG. 3 to form a detector circuit \( C_2 \), it is possible to cut the consumption current of the entire detector circuit \( C_2 \) in the current cut mode.

Fourth Preferred Embodiment

[0073] In the configuration of the negative voltage generating circuit shown in FIG. 1, when the potential of the power Supply \( V_{DD} \) is not sufficiently high in a transition state at the time of turning-on of the power supply, the reference potential \( V_{REF} \) stays close to the potential of the ground GND. At this time, current flows to the PMOS transistors \( P_1 \) and \( P_2 \) of the comparator \( C_2 \) but current does not flow to the NMOS transistors \( N_3 \) and \( N_4 \), and the output of the comparator \( C_1 \) exhibits an \( H \) level. During this period, the detector circuit \( I_2 \) outputs the detect signal \( \delta_{DP} \) at the \( L \) level and so the charge pump circuit \( I \) stays inactive. As a result, the start of the operation of the charge pump circuit \( I \) is delayed, which lengthens the activation time of the negative voltage generating circuit.

[0074] Accordingly, in a fourth preferred embodiment, the detector circuit \( I_2 \) is configured to output the detect signal \( \delta_{DP} \) that activates the charge pump circuit \( I \) (i.e., the detect signal \( \delta_{DP} \) at the \( H \) level) during a transition at the turning-on of the power supply.

[0075] FIG. 4 is a diagram illustrating the configuration of the comparator circuit \( C_2 \) of the negative voltage generating circuit of this preferred embodiment. Except for the comparator circuit \( C_2 \), the circuit configuration is the same as that shown in FIG. 1, and therefore only the configuration of the comparator circuit \( C_2 \) will be described below and the remaining components are not described again.

[0076] In this preferred embodiment, as shown in FIG. 4, the polarities (\( H \) level/\( L \) level) of the output voltage \( V_C \) of the comparator \( C_1 \) are reversed as compared with those of FIG. 1. An inverter \( I_6 \) is added so that the detect signal \( \delta_{DP} \) outputted from the detector circuit \( I_2 \) presents the same logical value as that of FIG. 1.

[0077] In the comparator circuit \( C_2 \) of FIG. 4, when the power-supply voltage is not sufficiently high, the logical value of the detect signal \( \delta_{DP} \) is different from that of the configuration of FIG. 1. That is, as mentioned above, when the potential of the power supply \( V_{DD} \) is not sufficiently high during a transition at a turning-on of the power supply, current flows to the PMOS transistors \( P_1 \) and \( P_2 \) of the comparator \( C_1 \) but current does not flow to the NMOS transistors \( N_3 \) and \( N_4 \). The output voltage \( V_C \) of the comparator \( C_1 \) of FIG. 4 is then at the \( H \) level. Then, the detector circuit \( I_2 \) (the inverter \( I_6 \)) outputs the detect signal \( \delta_{DP} \) at the \( H \) level and the charge pump circuit \( I \) is activated. That is, the charge pump circuit \( I \) is activated immediately after the power supply is turned on, which shortens the activation time of the negative voltage generating circuit.

[0078] When the power supply \( V_{DD} \) attains a sufficiently high value, the detector circuit \( I_2 \) performs ordinary level detecting operation. At this time, the polarity of the output voltage \( V_C \) of the comparator \( C_1 \) of FIG. 4 is opposite to that of FIG. 1, but the detector circuit \( I_2 \) performs the same operation as that of FIG. 1 because of the presence of the inverter \( I_6 \) in the output stage of the detector circuit \( I_2 \).

[0079] According to this preferred embodiment, the charge pump circuit \( I \) is activated immediately after the power supply is turned on, which shortens the activation time of the negative voltage generating circuit. However, with the configuration of the comparator \( C_1 \) of FIG. 4, a large electric field is produced in each transistor immediately after the power supply is turned on, which might deteriorate the reliability of the breakdown voltage. Accordingly, the configuration of FIG. 1, where the charge pump circuit \( I \) is kept inactive until the power supply \( V_{DD} \) becomes sufficiently high, is preferable when the application requires ensuring the breakdown voltage reliability.

Fifth Preferred Embodiment

[0080] In a fifth preferred embodiment, the threshold of the inverter \( I_1 \) receiving the output voltage \( V_C \) of the comparator
CP is set around the middle between the H level potential and the L level potential of the voltage $V_C$.

**[0081]** FIG. 5 is a diagram illustrating the configuration of the comparator circuit 22 of the negative voltage generating circuit of this preferred embodiment. As shown in FIG. 5, the PMOS transistor P5 provided on the power supply $V_{DD}$ side of the inverter 11 is diode-connected. The configuration is the same as that of FIG. 1 except for the configuration of the comparator circuit 22, and therefore only the configuration of the comparator circuit 22 will be described below and the remaining components are not described here again.

**[0082]** The potential of the output voltage $V_c$ of the comparator CP varies in the range from the ground GND to the source potential of the PMOS transistor P2. That is, when the detect potential $V_{DFP}$ is less than the reference potential $V_{REF}$, the potential of the voltage $V_c$ is approximately equal to the ground GND. On the other hand, when the detect potential $V_{DFP}$ is greater than the reference potential $V_{REF}$, the potential of the voltage $V_c$ is approximately equal to the source potential of the PMOS transistor P2.

**[0083]** Accordingly, in the preferred embodiment, the PMOS transistor P5 is disposed on the power supply $V_{DD}$ side of the inverter 11, and the channel width size of the PMOS transistor P5 is set so that the threshold of the inverter 11 is around the middle between the source potential of the PMOS transistor P2 and the potential GND of the ground GND.

**[0084]** Thus, in this preferred embodiment, the threshold of the inverter 11 receiving the output voltage $V_c$ from the comparator CP is set around the middle between the H level potential and the L level potential of the voltage $V_c$, which enlarges the margin of the amplitude of the output voltage $V_c$ of the comparator CP and enhances the reliability of the operation of the detector circuit 2.

**Sixth Preferred Embodiment**

**[0085]** In the negative voltage generating circuit shown in FIG. 1, the detect potential $V_{DFP}$ is low when the power supply $V_{DD}$ is low or when the negative voltage $V_{NEG}$ detected by the detector circuit 2 is deep. When the detect potential $V_{DFP}$ is excessively low, the operation of the comparator CP becomes unstable. Accordingly, this preferred embodiment suggests a negative voltage generating circuit that is capable of performing stable operation even when the detect potential $V_{DFP}$ is low.

**[0086]** FIG. 6 is a diagram illustrating the configuration of the negative voltage generating circuit of this preferred embodiment. In FIG. 6, the components corresponding to those of FIG. 1 are shown at the same reference characters (FIG. 6 does not show the charge pump circuit 1). As shown in FIG. 6, a level shift circuit 23 is interposed between the first voltage divider circuit 21 and the comparator circuit 22, and a level shift circuit 33 is interposed between the reference voltage generating circuit 3 and the comparator circuit 22. In other respects, the configuration is the same as that of the negative voltage generating circuit shown in FIG. 1.

**[0087]** The level shift circuit 23 and the level shift circuit 33 raise the detect potential $V_{DFP}$ and the reference potential $V_{REF}$ to particular levels, respectively. That is, in the negative voltage generating circuit of FIG. 6, the comparator circuit 22 receives a potential $V_{DFP}$ obtained by raising the level of the detect potential $V_{DFP}$ and a potential $V_{REF}$ obtained by raising the level of the reference potential $V_{REF}$.

**[0088]** Accordingly, even when the power supply $V_{DD}$ is low or when the negative voltage $V_{NEG}$ detected by the detector circuit 2 is deep, the comparator CP receives relatively large signals and so operates stably. This enhances the response of the comparator circuit 22 (the detector circuit 2).

**[0089]** When the level shift circuits 23 and 33 precede the comparator circuit 22 as shown in FIG. 6, the comparator circuit 22 may be configured as shown in FIG. 7. That is, the level shift circuit 23 and 33 may be configured so that the detector circuit 22 may be configured as shown in FIG. 6, which is configured so that the differential pair as the input stage of the comparator CP is formed of NMOS transistors N12 and N13, the current mirror circuit as a load is formed of PMOS transistors P18 and P19, and the constant-current source for restricting the current flowing to the comparator CP is formed of a constant-current source for passing a constant current to the inverter 11 (the PMOS transistor P4 and the NMOS transistor N5) that receives the input voltage $V_c$ of the comparator CP is formed of an NMOS transistor N15. This allows application of a common voltage $V_{CON}$ to the gates of the NMOS transistor N14 and the NMOS transistor N15.

**Seventh Preferred Embodiment**

**[0090]** Also, as shown in FIG. 7, the constant-current source for passing a constant current to the inverter 11 (the PMOS transistor P4 and the NMOS transistor N5) that receives the output voltage $V_c$ of the comparator CP is formed of an NMOS transistor N15. This allows application of a common voltage $V_{CON}$ to the gates of the NMOS transistor N14 and the NMOS transistor N15.

**[0091]** In the present invention, the reference potential $V_{REF}$ outputted from the reference voltage generating circuit 3 is susceptible to noise because it is generated using small current. Accordingly, in this preferred embodiment, as shown in FIG. 8, a noise filter circuit 4, composed of a resistor R3 and a capacitor C3, is provided at the node of the reference potential $V_{REF}$ (between the reference voltage generating circuit 3 and the detector circuit 2). In other respects, the configuration of the negative voltage generating circuit is the same as that shown in FIG. 1.

**[0092]** In this preferred embodiment, the comparator CP in the detector circuit 2 receives the reference potential $V_{REF}$ from which noise has been removed by the noise filter circuit 4. This prevents the malfunction that the detect signal $S_{DET}$ outputted by the detector circuit 2 unnecessarily varies due to noise, thus enabling stable operation of the detector circuit 2. This is especially effective when the detector circuit 2 is highly sensitive.

**Eighth Preferred Embodiment**

**[0093]** In the negative voltage generating circuit of the invention, noise may occur in the potential of the negative voltage $V_{NEG}$ at the time of power-feeding (activation) by the charge pump circuit 1 or at the time of current consumption by the semiconductor device. Accordingly, in this preferred embodiment, as shown in FIG. 9, a noise filter circuit 5, composed of a resistor R4 and a capacitor C4, is provided at the node of the negative voltage $V_{NEG}$ (between the charge pump circuit 1 (not shown) and the detector circuit 2). In other respects, the configuration of the negative voltage generating circuit is the same as that of FIG. 1.

**[0094]** In this preferred embodiment, the first voltage divider circuit 21 in the detector circuit 2 receives the negative voltage $V_{NEG}$ from which noise has been removed by the noise filter circuit 5. This reduces noise in the detect potential $V_{DFP}$ outputted from the first voltage divider circuit 21. This prevents the malfunction that the detect signal $S_{DET}$ outputted from the detector circuit 2 unnecessarily varies because of
noise, thus enabling stable operation of the detector circuit 2. This is especially effective when the detector circuit 2 is highly sensitive.

This preferred embodiment may be combined with the seventh preferred embodiment. That is, the generative voltage generating circuit of the invention may include both of the noise filter circuit 4 for removing noise from the reference potential \( V_{REF} \) as shown in FIG. 8 and the noise filter circuit 5 for removing noise from the negative voltage \( V_{NEG} \) as shown in FIG. 9. Removing noise from both of the reference potential \( V_{REF} \) and the negative voltage \( V_{NEG} \) inputted to the detector circuit 2 enables more stable operation of the detector circuit 2.

Ninth Preferred Embodiment

In the preferred embodiments described so far, the generation of the detect potential \( V_{DET} \) in the first voltage divider circuit 21 is achieved by a voltage division between the power supply \( V_{DD} \) and the negative voltage \( V_{NEG} \) that is done by the NMOS transistors N1 and N2. A ninth preferred embodiment shows modifications in which the generation of the detect potential \( V_{DET} \) is achieved by using elements other than MOS transistors.

For example, FIG. 10 is a diagram showing an example in which the first voltage divider circuit 21 is formed of capacitors C11 and C12. That is, in this first voltage divider circuit 21, the capacitor C11 and the capacitor C12 make a voltage division between the power supply \( V_{DD} \) and the negative voltage \( V_{NEG} \) to generate the detect potential \( V_{DET} \). In this case, too, the effect of capacitive coupling by the capacitors C11 and C12 allows the detect potential \( V_{DET} \) to quickly follow variation of the negative voltage \( V_{NEG} \). This offers the effect described in the first preferred embodiment, i.e., high-speed response superior to those of conventional detector circuits.

Also, FIG. 11 shows an example in which the first voltage divider circuit 21 is formed of resistors R11 and R12. That is, in this first voltage divider circuit 21, the resistor R11 and the resistor R12 make a voltage division between the power supply \( V_{DD} \) and the negative voltage \( V_{NEG} \) to generate the detect potential \( V_{DET} \). In this case, the effect of coupling is not obtained, and so high-speed response as described in the first preferred embodiment is not achieved. However, the through current flowing in the first voltage divider circuit 21 is reduced to achieve reduction of power consumption.

Researchers including the inventors of the present invention conducted simulations using SPICE (Simulation Program With Integrated Circuit Emphasis), and the results showed that the first voltage divider circuit 21 using the NMOS transistors N1 and N2 as shown in FIG. 1 exhibited through current variation of about 400 to 500% including those caused by variation in the manufacturing process (e.g., a variation in the range of 1 \( \mu \)A to 5 \( \mu \)A). On the other hand, the first voltage divider circuit 21 shown in FIG. 11, using the same polysilicon as the gate electrode material as the resistors R11 and R12, reduced the variation to about 20% (e.g., a variation in the range of 1 \( \mu \)A to 1.2 \( \mu \)A). That is, the first voltage divider circuit 21 of FIG. 11 realizes steady operation with reduced power consumption, though high-speed response as shown in the first preferred embodiment is not obtained.

As shown in FIG. 12, the resistors R11 and R12 may be connected in parallel respectively with the capacitors C11 and C12 to form a first voltage divider circuit 21. In this case, the capacitors C11 and C12 offer the effect of coupling and the resistors R11 and R12 suppress variation of through current. That is, the first voltage divider circuit 21 of FIG. 12 offers both of the superior high-speed response and the stable operation with reduced power consumption. However, it should be noted that, when the area of the formation of the polysilicon resistance used for the resistors R11 and R12 is large, its parasitic capacitance is not negligible, and it may hinder full achievement of the effect of coupling by the capacitors C11 and C12.

That is to say, as for the elements for forming the first voltage divider circuit 21, MOS transistors, capacitors, resistors, and combinations thereof can be suitably selected according to which factors are important for the application, among high-speed response, the magnitude of consumed current, stability, and area of formation. Particularly, the configuration such as the first voltage divider circuit 21 shown in FIG. 1, using MOS transistors, will be the most effective on the whole, because it is superior in all respects, including high-speed response, the magnitude of consumed current, stability, and area of formation.

In the negative voltage generating circuit shown in FIG. 1, the second voltage divider circuit 31, for generating the potential \( V_{REFO} \) by making a voltage division between the power supply \( V_{DD} \) and ground \( GND \), is formed of the resistors R1 and R1. However, the second voltage divider circuit 31, too, may be formed of MOS transistors, resistors, or capacitors, like the first voltage divider circuit 21. However, in the negative voltage generating circuit of FIG. 1, it is not very important to cause the potential \( V_{REFO} \) to quickly vary, and therefore it is desirable to form the second voltage divider circuit 31 with the resistors R1 and R2 as shown in FIG. 1 to achieve reduction of power consumption.

Tenth Preferred Embodiment

As mentioned earlier, the applications of the negative voltage generating circuit include semiconductor devices using a PMOS transistor as a DRAM cell transfer gate. This preferred embodiment describes a semiconductor device (DRAM device) including the negative voltage generating circuit and DRAM cell according to the invention, particularly a driving circuit for driving a word line to which the control electrode of the transfer gate of a DRAM cell is connected (a word line driver).

FIG. 13 is a circuit diagram of a DRAM cell using a PMOS transistor as a transfer gate, and a conventional common word line driver for driving the DRAM cell. As shown in FIG. 13, the word line driver is an inverter circuit formed of a PMOS transistor P21 and an NMOS transistor N21. The PMOS transistor P21 is connected between a word line WL and a power supply \( V_{CP} \) and the NMOS transistor N21 is connected between the word line WL and a node of the negative voltage \( V_{NEG} \). The gate electrodes of both of the PMOS transistor P21 and the NMOS transistor N21 receive a predetermined control signal CS.

As shown in FIG. 13, the word line WL is connected to the control electrode (gate electrode) of a transfer gate TG (PMOS transistor) in a DRAM cell MC. In the DRAM cell MC, one of the source/drain electrodes of the transfer gate TG is connected to a bit line BL, while the other is connected to a capacitor C holding a voltage corresponding to data. The capacitor C has the other end connected to a predetermined power supply \( V_{CP} \). With the potential of the power supply \( V_{CP} \) being defined as \( "V_{CP}" \) and the potential of the common
power supply $V_{DD}$ (main power supply) shown above being defined as $V_{north}$, those potentials are commonly set such that $0 \leq V_{CI} \leq V_{DD}$.

[0106] On the basis of the control signal $CS$, when turning on the transfer gate $TG$ of the DRAM cell MC, the word line driver in FIG. 13 supplies the word line $WL$ with the potential of the negative voltage $V_{neg}$ (a potential capable of extracting an L (Low) level signal with a sufficiently large amplitude from the DRAM cell MC). When turning off the transfer gate, the word line driver supplies the word line $WL$ with the potential of the power supply $V_{PP}$ (a potential for preventing leakage of data of the DRAM cell MC). Usually, the power supply $V_{PP}$ is equal to the common power supply $V_{DD}$ (main power supply) shown above, or is of a higher voltage than that.

[0107] As shown in FIG. 13, in the conventional word line driver, the back gate of the PMOS transistor $P_{21}$ is connected to the power supply $V_{PP}$ and the back gate of the NMOS transistor $N_{21}$ is connected to the ground GND. FIG. 14 shows a cross-sectional view of the word line driver and the DRAM cell MC.

[0108] As shown in FIG. 14, the word line driver is formed in a P-type semiconductor substrate (P-type substrate) 40. In the P-type substrate 40, a P-type substrate contact region 41 is connected to the ground GND, and so the potential of the P-type substrate 40 is fixed at the potential of ground GND.

[0109] The PMOS transistor $P_{21}$ is formed in an N well 51 and includes a gate electrode 52 formed on the N well 51 and a P-type source region 53 and a P-type drain region 54 formed on the sides of the gate electrode 52. The source region 53 is connected to the power supply $V_{PP}$ and the drain region 54 is connected to the word line $WL$. In the N well 51, an N-type well contact region 55 is connected to the power supply $V_{PP}$ and so the N well 51 (i.e., the back gate of the PMOS transistor $P_{21}$) is electrically connected to the power supply $V_{PP}$.

[0110] The NMOS transistor $N_{21}$ includes a gate electrode 62 formed on the P-type substrate 40 and an N-type source region 63 and an N-type drain region 64 formed on the sides of the gate electrode 62. The source region 63 is supplied with the negative voltage $V_{neg}$ and the drain region 64 is connected to the word line $WL$. As mentioned above, the P-type substrate 40 (i.e., the back gate of the NMOS transistor $N_{21}$) is connected to the ground GND.

[0111] As shown in FIG. 14, the DRAM cell MC is also formed in the P-type substrate 40. The transfer gate $TG$ of the DRAM cell MC is formed in an N well 81, and includes a control electrode (gate electrode) 82 formed on the N well 81 and P-type source/drain regions 83 and 84 formed on the sides of the control electrode 82. The capacitor $C$ has a P-type impurity region 85 connected to the source/drain region 84 as a lower electrode, and is composed of this impurity region 85 and an upper electrode 86 formed on the surface of the impurity region 85 via a dielectric film. In the N well 81, an N-type well contact region 87 connected to the power supply $V_{DD}$ is formed, and so the N well 81 (i.e., the back gate of the transfer gate $TG$) is electrically connected to the power supply $V_{DD}$. In the FIG. 14 example, part of the upper electrode 86 enters the upper part of trench isolation provided with an isolation insulating film 88, thus increasing an effective area of the capacitor $C$ for capacity increase.

[0112] When the negative voltage $V_{neg}$ is deep in the conventional word line driver as shown in FIG. 14, current flows from the ground GND to the node of the negative voltage $V_{neg}$ through the substrate contact region 41, the P-type substrate 40, and the source region 63. Then, the potential of the negative voltage $V_{neg}$ is fixed at the built-in potential (typically 0.5 V) and does not become deeper than that. Accordingly, in this case, it is not necessary to provide the detector circuit in the negative voltage generating circuit that generates the negative voltage $V_{neg}$. However, the power consumption of the word line driver is large because of the current flowing from the ground GND to the node of the negative voltage $V_{neg}$.

[0113] Recently, the widespread use of mobile devices is increasingly demanding reduction of power consumption of DRAM devices used in mobile devices. FIG. 15 is a circuit diagram of a word line driver and the DRAM cell according to this preferred embodiment, and FIG. 16 is its cross-sectional view. In FIGS. 15 and 16, the components having the same functions as those of FIGS. 13 and 14 are shown at the same reference characters.

[0114] As shown in FIG. 15, in the word line driver of the preferred embodiment, the back gate of the NMOS transistor $N_{21}$ is connected to the negative voltage $V_{neg}$. In other respects, the circuit configuration is the same as that shown in FIG. 13. The operation is also the same as that of the word line driver of FIG. 13, and the word line driver operates on the basis of the control signal $CS$ to supply the potential of the negative voltage $V_{neg}$ to the word line $WL$ when turning on the transfer gate $TG$ of the DRAM cell MC, and supplies the potential of the power supply $V_{PP}$ to the word line $WL$ when turning off the transfer gate.

[0115] As shown in FIG. 16, the word line driver of the preferred embodiment is also formed in a P-type substrate 40. In the P-type substrate 40, a P-type substrate contact region 41 is connected to the ground GND and so the potential of the P-type substrate 40 is fixed at the potential of the ground GND.

[0116] The PMOS transistor $P_{21}$ is constructed as shown in FIG. 14. That is, the PMOS transistor $P_{21}$ includes a gate electrode 52 on the N well 51 and a source region 53 and a drain region 54 on the sides of the gate electrode 52. The source region 53 is connected to the power supply $V_{PP}$ and the drain region 54 is connected to the word line $WL$. The N well 51 (i.e., the back gate of the PMOS transistor $P_{21}$) is connected to the power supply $V_{PP}$ through the well contact region 55.

[0117] On the other hand, the NMOS transistor $N_{21}$, unlike that shown in FIG. 14, is formed in a P well 61 in an N-type bottom N well 60, and has a so-called "triple well" structure. In this preferred embodiment, the bottom N well 60 and the N well 51 are formed integrally. Therefore, as well as the potential of the N well 51, the potential of the bottom N well 60 is equal to the potential of the power supply $V_{PP}$.

[0118] The NMOS transistor $N_{21}$ includes a gate electrode 62 on the P well 61 and a source region 63 and a drain region 64 on the sides of the gate electrode 62. The source region 63 is supplied with the negative voltage $V_{neg}$ and the drain region 64 is connected to the word line $WL$. The P well 61 (the back gate of the transistor $N_{21}$) is supplied with the negative voltage $V_{neg}$ through a P-type well contact region 65.

[0119] In the structure of FIG. 16, the bottom N well 60 electrically separates the P-type substrate 40 at the ground GND potential and the P well 61 (negative voltage $V_{neg}$) at the negative voltage $V_{neg}$ potential. Therefore, current does not flow between the ground GND and the node of the negative voltage $V_{neg}$, and the consumed current is smaller than that of the word line driver of FIG. 14, which contributes to
reduction of power consumption of the DRAM device. However, it should be noted that the triple well structure may involve a larger area for formation.

[0120] In this case, the potential of the negative voltage $V_{\text{NEG}}$ can become deeper than the built-in potential, so that it is effective to suppress the variation of the negative voltage $V_{\text{NEG}}$ by using the negative voltage generating circuit having the detector circuit 2 of the invention. The adoption of the negative voltage generating circuit having the detector circuit 2 allows arbitrary setting of the level of the negative voltage $V_{\text{NEG}}$ and quick detection of its variation, thereby allowing stable supply of the negative voltage $V_{\text{NEG}}$. Particularly, an application combined with the detector circuit 2 having the current cut function shown in the third preferred embodiment further reduces the power consumption of the DRAM device.

[0121] When the NMOS transistor N21 of the word line driver has a triple well structure as shown in FIG. 16, it is effective to form the NMOS transistors N1 and N2 with a triple well structure in the first voltage divider circuit 21 (FIG. 17) of the negative voltage generating circuit that supplies the negative voltage $V_{\text{NEG}}$ thereinto.

[0122] FIG. 18 shows a cross-sectional view of the first voltage divider circuit 21 which adopts the triple well structure. As shown in FIG. 18, the NMOS transistors N1 and N2 are formed respectively in P wells 171 and 271 in a bottom N well 70 formed in the P-type substrate 40. The bottom N well 70 is connected to the power supply $V_{DD}$ through a well contact region 71.

[0123] The NMOS transistor N1 includes a gate electrode 172 on the P well 171 and a source region 173 and a drain region 174 on the sides of the gate electrode 172; and the NMOS transistor N2 includes a gate electrode 272 on the P well 271 and a source region 273 and a drain region 274 on the sides of the gate electrode 272. The P wells 171 and 271 respectively have well contact regions 175 and 275 formed therein as the back gate terminals of the NMOS transistors N1 and N2, respectively.

[0124] When the NMOS transistors N1 and N2 of the first voltage divider circuit 21 and the NMOS transistor N21 of the word line driver are formed with a triple well structure as shown in FIGS. 16 and 18, they can be fabricated in parallel in the same manufacturing process, which minimizes the complexity of the DRAM device manufacturing process caused by the adoption of the triple well structure.

[0125] Also, while this preferred embodiment has shown an example in which the first voltage divider circuit 21 is formed of MOS transistors, the first voltage divider circuit 21 may be formed of capacitors or resistors as shown in FIGS. 10 to 12.

[0126] With respect to the relationship between the absolute value of the potential of the positive power supply $V_{DD}$ and the absolute value of the potential of the negative voltage $V_{\text{NEG}}$, it is desirable that the absolute value of the potential of the positive power supply $V_{DD}$ be the larger. In that case, the first voltage divider circuit 21 of the detector circuit 2 shown in FIG. 1 outputs the detect potential $V_{\text{DP}}$ as a positive potential. When the potential of the power supply $V_{DD}$ is from 1.0 to 1.5 V; for example, the potential of the negative voltage $V_{\text{NEG}}$ should be set from approximately -0.3 to -0.8.

[0127] While the invention has been described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is understood that numerous other modifications and variations can be devised without departing from the scope of the invention.

1-(canceled)

12. A semiconductor device comprising a reference potential generating circuit that generates a reference potential, wherein said reference potential generating circuit includes a first divider circuit generating said reference potential by obtaining an intermediate reference potential from a voltage division between a first voltage potential and a second voltage potential; and wherein said reference potential generating circuit further includes an adjustment circuit decreasing said reference potential by a predetermined adjustment value to obtain said reference potential.

13. A semiconductor device comprising a detector circuit that detects a level of a first voltage, and a reference potential generating circuit that generates a reference potential, wherein said detector circuit includes a first divider circuit including a plurality of MOS transistors connected in series between a potential of said first voltage and a potential of said voltage potential, said plurality of MOS transistors being configured to cause a voltage division between said first voltage potential and said voltage potential, and said first divider circuit being configured to output a detect potential generated by the voltage division between said first voltage potential and said second voltage potential;

wherein said reference potential generating circuit includes a second divider circuit generating said reference potential by obtaining an intermediate reference potential from a voltage division between said second voltage potential and a third voltage potential;

wherein said reference potential generating circuit further includes an adjustment circuit decreasing said reference potential by a predetermined adjustment value to obtain said reference potential;

wherein said detector circuit further includes first and second level shift circuits that respectively shift said detect potential and said reference potential to predetermined potential levels;

wherein said detector circuit further includes a comparator circuit compares said level-shifted detect potential and said level-shifted reference potential respectively outputted by said first and second level shift circuits; and

wherein said semiconductor device further comprises a charge pump circuit being driven by an output signal from said comparator circuit to generate said first voltage in accordance with said reference potential.

14. The semiconductor device according to claim 2, further comprising:

a DRAM (Dynamic Random Access Memory) cell; and

a word line driver that drives a word line of said DRAM cell,

said word line driver comprising an NMOS transistor having its drain connected to said word line and its source supplied with said first voltage.