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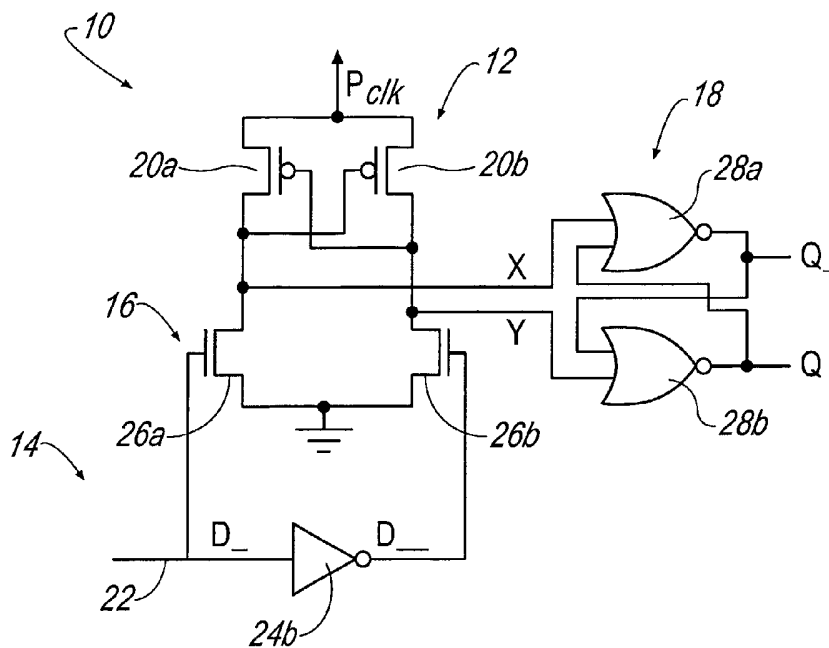
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(54) Title: CLOCK SIGNAL GENERATING CIRCUIT



(57) Abstract: A clock signal generating circuit (40) includes an oscillator portion (302) that sustains a ramped oscillating clock signal in a memory storage device (10) electrically connected to the oscillator portion (302), a switch portion (304) that supplements electrical energy to the oscillator portion (302), and a cycle controller (306) connected to the oscillator portion (302) and the switch portion (304) to supplement energy to the oscillator portion (302) when a peak voltage or current level of the clock signal (PC) falls below a predetermined value.



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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CLOCK SIGNAL GENERATING CIRCUIT

FIELD OF THE INVENTION

[0001] The present invention generally relates to a clock signal generating circuit for a computing device, and more particularly, the present invention relates to a clock signal generating circuit for generating a ramped clock signal.

BACKGROUND OF THE INVENTION

[0002] Conventional computing systems utilize a clock signal generating circuit to provide timing information to a plurality of flip-flops. The flip-flops store binary states, such as 1's and 0's contingent on the absence or presence of a voltage or charge in the flip-flop. The binary states, read or written in the flip-flops, are then used for combinational boolean logic for operation and calculation procedures in the computing system. When writing a logic state in the flip flop by a device external to the flip flop is desired, an oscillating voltage or clock signal operates the flip flop to cause a voltage value representative of the stored state to be stored to be written to the latching circuit in the flip-flop, latch the voltage value and hold it available for reading devices external to the flip-flop. The clock signal is commonly a square wave that drives a gate of a transistor of the flip-flop. The clock signal generating circuit, external to the flip-flops, generates the signal to effectuate read, write and timing processes in the computing device. The square or abrupt signal drives the gates of transistors in the flip-flop to turn them ON and OFF in a relatively quick manner.

[0003] While this structure effectively allows a computing system to effectuate reading of stored logic states contained within the flip-flops, drawback exists. Specifically, only a portion of a computing system's flip-flops are actually read during any given read request. The remainder, however, still receive the clock signal. Commonly, the energy of the clock signal driving the unread flip-flops is dissipated therein, thereby creating energy inefficiencies and increased heat dissipation. When this dissipation effect is multiplied with the numerous flip-flops contained within a computing device, the overall efficiency of that computing device is compromised. The present invention was developed in light of these and other drawbacks.

SUMMARY OF THE INVENTION

[0004] A clock signal generating circuit includes an oscillator portion that sustains a ramped oscillating clock signal in a memory storage device electrically connected to the oscillator portion, a switch portion that supplements electrical energy to the oscillator portion, and a cycle controller connected to the oscillator portion and the switch portion to supplement energy to the oscillator portion when a peak voltage or current level of the clock signal falls below a predetermined value.

[0005] Other aspects of the invention will be apparent to those skilled in the art after reviewing the drawings and the detailed description below.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

[0007] FIG. 1 is a schematic view of a memory storage circuit according to an embodiment of the invention;

[0008] FIG. 2 is a schematic view of a memory storage circuit and clock generator according to an embodiment of the invention;

[0009] FIG. 3 is a schematic view of a memory storage circuit according to an embodiment of the invention;

[0010] FIG. 4 is a schematic view of a clock generator circuit according to an embodiment of the invention; and

[0011] FIG. 5 is a schematic view of a clock generator circuit according to an embodiment of the invention.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0012] It is to be understood that the present invention may be embodied in other specific forms without departing from its essential characteristics. The illustrated and described embodiments are to be considered in all respects only as illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes that come within the meaning and range of equivalency of the claims are to be embraced within their scope.

[0013] Referring now to FIG. 1, the present invention is shown and described. In FIG. 1, a flip-flop 10 includes clock signal receiving circuit 12, input value 14, reading element 16,

and latching element 18. In an embodiment of the invention, clock signal receiving circuit 12 includes two cross-coupled PMOS transistors 20a and 20b. Input value 14 includes a binary value 22, which by absence or presence of a voltage “1” or “0” indicates a Boolean state. Inverter 24b provides an inverted version of binary value 22 to opposite sides of flip-flop 10. An additional inverter can also be added between the inverter 24b and the binary value 22 to, again, invert the binary value supplied to opposite sides of flip-flop 10.

[0014] Reading element 16 includes NMOS transistors 26a and 26b that cooperate with input value 14 and inverter 24b to allow binary value 22 to be read in response to a clock signal. Finally, latching element 18 includes cross-coupled NOR gates 28A and 28B to latch binary value 22 and allow it to be read by an external device.

[0015] With continued reference to FIG. 1, the operation of the present invention will be shown and described. In operation, clock signal receiving circuit 12 is driven by a preferably sinusoidal or other ramped signal Pclk such as a blip clock or other angled wave form. Pclk preferably drives the source of the PMOS transistors 20a and 20b, and not the gates. As the gates of PMOS transistors 20a and 20b are low, these elements allow the clock signal to pass therethrough. The sinusoidal clock signal assists in ensuring that the energy is not dissipated in the transistors, and is instead passed across the transistors. During both high clock values during read operations and during charge recycling, as will be discussed in greater detail, the sinusoidal signal reduces energy loss by limiting the amount of energy dissipated in the element. Of course, other slower ramped signals may be used instead of a sinusoidal clock signal, such as saw tooth or other angled waves, and the present invention is not limited to sinusoidal waves.

[0016] Binary value 22 is inverted by inverter 24b. This inversion process provides opposite charges to different sides of flip-flop 10. As such, when reading of the state of binary value 22 is effectuated, inverter 24b ensures that one NMOS transistor of transistors 26a and 26b conducts while the other does not. By way of a non-limiting example, if binary value 22 is stored as a zero voltage, then a zero voltage to the gate of NMOS transistor 26a while inverter 24b inverts the inverted voltage to supply a voltage to the gate of NMOS transistor 26b. Accordingly, NMOS transistor 26b conducts while NMOS transistor 26a does not conduct. Accordingly, terminal X is not grounded and therefore is at a Pclk voltage while terminal Y is grounded through NMOS transistor 26b and therefore is at ground potential.

[0017] Latching element 18 uses cross-coupled NOR gates 28A and 28B as a set/reset latch to latch these opposite and inverted potentials to output them as $Q_{\bar{}}$ and Q respectively. The high potential of X maintains PMOS transistor 20b in an OFF state while PMOS transistor 20a is allowed to conduct by virtue of low potential of terminal Y . Accordingly, while binary value 22 maintains its current logic state, the charge on terminal X is allowed to oscillate back and forth across PMOS transistor 20a with an external inductor or other energy oscillating circuit in an energy recovering state.

[0018] As such, based on the above non-limiting example, the operation of flip-flop 10 begins with the data input binary value 22 changing at a suitable time before the rising edge of P_{clk} . Inverter 24b derives the complemented input, which is applied to the gate of NMOS transistors 26a and 26b. When the rising edge of the sinusoidal P_{clk} arrives, the cross-coupled PMOS transistors 20a and 20b sense and latch the appropriate value of binary value 22 onto the nodes X and Y . The cross-coupled NOR gates 28A and 28B form a set/reset latch. Therefore, positive pulses on either node X or Y will cause this latch to set or reset, respectively.

[0019] When binary value 22 does not change and remains the same, either node X or Y will remain low, with the other node oscillating in phase of P_{clk} in an energy recovering manner. Specifically, in the example of FIG. 1, node Y remains low while node X oscillates between a high and low state. This is accomplished by transferring charge from the node X across PMOS transistor 20a and back to the oscillating circuit external to the flip-flop 10. This is in contrast to conventional flip-flops which dissipate the unused clock signal in the flip-flop as heat. This feature allows the flip-flop 10 to operate in an energy efficient manner, contrary to devices which merely absorb the stored charge on the respective terminal during each clock cycle, an overall improvement of efficiency and thermal dissipation is achieved.

[0020] When binary value 22 does change state, the above-described operation acts to reset the latching element 18. Specifically, in the example of FIG. 1, when the logic state of binary value 22 changes, the inverted charge to the gate of NMOS transistor 26a causes it to conduct while transistor 26b remains OFF. When P_{clk} goes high, node Y also goes high, while node X goes low. This causes latching element 18 to switch the charge between $Q_{\bar{}}$ and Q and reset the latching element 18. However, once again, the charge Y is not

dissipated in the flip-flop and instead is ultimately recycled back through PMOS transistor 20b to the external clock structure.

[0021] In a most preferred embodiment, the external clock structure, external to the flip-flop, generates a sinusoidal clock wave to achieve maximum efficiency in the flip-flop 10. However, it is understood that other ramp clock signals may be used such as a blip clock, saw tooth configuration, or any other clock signal having a ramp increase and decrease. It is also understood that by external, the clock structure is outside the flip-flop. It may, however, be on-chip or off-chip with the flip-flop.

[0022] Referring now to FIG. 2, a clock tree 100 is shown including a plurality of flip-flops 10. Here, clock signal generator 40 generates a sinusoidal clock wave Pclk that is transmitted to and received from the clock tree 100. In a non-limiting example of an embodiment of the invention, in a .25 micrometer process, the clock tree 100 operates in a frequency range between 200 and 500 MHz. When the binary value 22 is not switching, energy consumption per cycle is under 5fJ at 200MHz and under 25fJ at 500MHz with a switching activity of .25, per cycle energy consumption is under 40fj at 200 MHz and 90fj at 500MHz.

[0023] With reference to FIG. 3, a second embodiment of the present invention is shown and described. In FIG. 3, flip-flop 200 is shown having a different configuration from that of FIG. 1. Specifically, inverter 224b of input value 222 connects to gates 226a and 226b of reading element 116. Pclk drives NMOS transistors 220a and 220b of clock signal receiving circuit 12. Latching element 118 includes cross coupled NAND gates 228A and 228B instead of the NOR gates of FIG. 1. Voltage supply Vdd provides a voltage to the source of PMOS transistors 226a and 226b.

[0024] With continued reference to FIG. 3, the operation of the present invention is shown and described. In FIG. 3, reading element 116 senses the logic state of binary value 222 and latches it with the cross-coupled NAND gates 228A and 228B of latching element 118. As before, one terminal X or Y remains high while the other terminal oscillates in conjunction with the sinusoidal Pclk signal from an external clock signal generator. Accordingly, as before, the high-charge in either X or Y is recycled back through a respective NMOS transistor 220a or 220b and back to the clock signal generating circuit. Therefore, the overall efficiency of the flip-flop is enhanced.

[0025] It should be noted that the sinusoidal or ramped clock signal, provided to the flip flop of the present embodiment, provides energy recovering aspects. Driving both flip-flops 10 and 200 with the clock signal at their sources or drains allows the circuits to operate in their energy recovering state. Specifically, the sinusoidal clock signal driving flip-flops 10 and 200 not only provide timing information, but also provide the voltage required to set and latch the respective logic states in the latching elements 18 and 118 respectively. By driving transistors at their sources or drains as does FIGS. 1 and 3, the present invention uses the clock signal not only for the timing information, but also for operating voltage to read logic states. Accordingly, this energy is able to be recycled back through their respective transistors and to the clock signal generating circuit.

[0026] Referring now to FIG. 4, clock signal generator 40 is shown and described. The clock signal generator according to the present invention provides a clock signal other than an abrupt square wave to allow the energy to be passed through respective transistors, instead of being absorbed by the transistors. Additionally, the clock signal generator 40 also preferably includes features to allow recycling of the clock signal as well as components that monitor when additional energy needs to be added to the recycling system.

[0027] Accordingly, clock signal generator 40 according to an embodiment of the invention includes oscillator portion 302, switch portion 304, cycle controller 306, and reference clock 400. Oscillator portion 302 provides the oscillating recovery features of the preferred system by allowing read voltage from the flip-flops to be recycled. Clock signal generator 40 includes Pclk output node 308 and ground connection 310. Further, oscillator portion 302 includes voltage sources 312A and 312B and inductor 314. As can be seen with reference to FIG. 2, Pclk output node 308, in conjunction with ground connection 310, provides the sinusoidal clock signal to the flip-flops 10.

[0028] Reference clock 400 provides a reference clock signal to delay lines d1, d2 and d3, which will be described in greater detail. Switching portion 304 includes main transistor 320 and secondary transistors 322 and 324. Switching portion 304 provides the additional energy needed when the oscillator portion 302 is depleted of energy. To accomplish this function, an embodiment includes main transistor 320 which connects a voltage source at the cycle controller 306 with ground connection 326. Secondary transistors 322 and 324 are PMOS and NMOS transistors, respectively, which connect a voltage source Vdd with

ground connection 326. Secondary transistors 322 and 324 are connected to cycle controller 306 through a plurality of invertors 338A, 338B and 338C.

[0029] In operation, oscillator portion 302 creates a driven oscillator circuit with the parasitic capacitance of each of the flip-flops 10. As such, the inductor 314 stores energy which is transferred back and forth from the flip-flop 10 and inductor 314. When the read charge sent to the flip-flops 10 by the clock signal generator is recycled, it is recycled back to the inductor 314. Cycle controller 306 monitors the voltage peak level of Pclk and determines when Pclk needs to be replenished. When the cycle controller 306 determines Pclk must be replenished, then cycle controller 306 switches secondary transistor 322 ON and secondary transistor 324 OFF. Therefore, the gate voltage of main transistor 320 is switched ON to provide current flow from cycle controller 306, through main transistor 320 and to ground connection 326. Accordingly, the inductor 314 in parallel with main transistor 314 is replenished.

[0030] Referring now to FIG. 5, cycle controller 306 is described in greater detail. In FIG. 5, cycle controller 306 generally includes reference branch 330 and Pclk branch 332. Delay d3 operates the gates of PMOS transistors 337 to amplify the Pclk and reference voltage ref entered into transistors 329 and 327 respectively at a time dictated by delay d3. The reference voltage ref, different from the reference clock, is a set DC voltage supplied to the cycle controller 306 from which to base the decision of whether oscillator portion 302 needs to be replenished or not. The difference between the peak Pclk voltage and the reference voltage is amplified by transistors 329 and 327. Cross coupled inverters 107 compare the peak Pclk voltage and the reference voltage. Transistors 337 isolate the result of the comparison from the amplifier transistors 329 and 327. Latch circuit 334, comprising cross coupled NAND gates, latches the comparison result between Pclk and ref and feeds it to NAND gate 336. If Pclk is less than ref, then the latched output from latch comparison circuit 334 drives NAND gate 336 with a sufficient ON voltage.

[0031] Additionally, d1 and d2 provide required delay times to ensure that output 338 is turned ON in proper timing sequence with the clock frequency of the circuit. The difference in delay signals, d1-d2, controls the ON time of switch 320. The sum of d1, d2 plus intrinsic delay in the system equals d3. By combining d1 and d2 to create one delay feeding the system, greater accuracy is achieved in the delay. These delays are externally settable, and can be adjusted for the application. As such, when the combined effect of d1

and d2 peak, the NAND gate 335 outputs a voltage, providing an input to NAND gate 336. NAND gate 336, in turn, is turned ON when this input is provided at the same time that latch comparison circuit 334 provides an input, thereby turning the output 338 ON.

[0032] While the present invention has been particularly shown and described with reference to the foregoing preferred and alternative embodiments, it should be understood by those skilled in the art that various alternatives to the embodiments of the invention described herein may be employed in practicing the invention without departing from the spirit and scope of the invention as defined in the following claims. It is intended that the following claims define the scope of the invention and that the method and apparatus within the scope of these claims and their equivalents be covered thereby. This description of the invention should be understood to include all novel and non-obvious combinations of elements described herein, and claims may be presented in this or a later application to any novel and non-obvious combination of these elements. The foregoing embodiments are illustrative, and no single feature or element is essential to all possible combinations that may be claimed in this or a later application. Where the claims recite “a” or “a first” element of the equivalent thereof, such claims should be understood to include incorporation of one or more such elements, neither requiring nor excluding two or more such elements.

CLAIMS

What is claimed is:

1. A clock signal generating circuit, comprising:
 - an oscillator portion adapted to sustain a ramped oscillating clock signal in at least one memory storage device electrically connected to the oscillator portion;
 - a switch portion adapted to supplement electrical energy to the oscillator portion; and
 - a cycle controller connected to the oscillator portion and the switch portion to supplement energy to the oscillator portion when a peak voltage or current level of the clock signal falls below a predetermined value.

2. The clock signal generating circuit according to Claim 1, wherein:
 - the oscillator includes an inductor that is connected to a voltage source at a first end and adapted to connect to the at least one memory storage device at a second end.

3. The clock signal generating circuit according to Claim 2, wherein the switch portion is a switch in parallel with the inductor.

4. The clock signal generating circuit according to Claim 3, wherein the cycle controller connects to the switch to turn the switch ON when energy is to be added to the oscillator portion.

5. The clock signal generating circuit according to Claim 1, wherein the switch portion further comprises:
 - a first alternate switch having a source connected to a power source and a drain connected to a gate of the switch; and
 - a second alternate switch having a source connected to the gate of the switch and a drain connected to ground;wherein the cycle controller turns the first alternate switch ON and the second alternate switch OFF to supplement energy to the oscillator portion.

6. The clock signal generating circuit according to Claim 5, wherein:
the first alternate switch is a PMOS transistor; and
the second alternate switch is a NMOS transistor;
wherein the cycle controller supplies a substantially zero voltage to gates of the first transistor and the second transistor to supplement energy to the oscillator portion.

7. The clock signal generating circuit according to Claim 1, further comprising a flip-flop comprising:

an input value that provides a logic voltage indicating a logic state of the flip-flop;

at least a first transistor connected to a clock signal generating circuit at a source or drain of the first transistor;

at least a second transistor connected to a clock signal generating circuit at a source or drain of the second transistor;

a clock signal generated by the clock signal generating circuit that is ramped or sinusoidal; and

a latching circuit that latches a latch voltage value based on a first clock voltage at a first connection point and a second connection point, wherein the latch voltage is representative of the input value;

wherein the first connection point is a source or drain of the first transistor that is opposite to the clock signal generating circuit; and

wherein the second connection point is a source or drain of the second transistor that is opposite the clock signal generating circuit.

8. The clock signal generating circuit according to Claim 7, wherein the latching circuit is a pair of cross coupled NOR gates that forms a set/reset latch.

9. The clock signal generating circuit according to Claim 7, further comprising:

a third transistor having a source or drain connected to the first connection point, wherein the third transistor has a third gate for setting the third transistor in an ON/OFF condition; and

a fourth transistor having a source or drain connected to the second connection point, wherein the fourth transistor has a fourth gate for setting the fourth transistor in an ON/OFF condition;

wherein the input value is connected to the third gate and the fourth gate to set the third gate and the fourth gate in opposite ON/OFF conditions representative of the input value.

10. The clock signal generating circuit according to 9, further comprising an inverter positioned between the input value and the fourth gate to invert the input value supplied to the fourth gate to set the fourth gate in the opposite ON/OFF condition from the third gate.

11. The flip-flop according to Claim 9, wherein the source of the first transistor and the source of the second transistor are connected to the clock signal generator.

12. The clock signal generating circuit according to Claim 1, wherein the cycle controller further comprises:

a reference signal input adapted to receive a reference DC level signal;

a clock signal input adapted to receive the clock signal;

a comparator circuit adapted to compare the reference signal with a peak value of the clock signal; and

an output circuit turns the switch portion ON to supplement the oscillator portion.

13. The clock signal generating circuit according to Claim 12, wherein the comparator circuit further comprises:

at least a first cascaded amplifier transistor pair driven by a voltage source and having a gate connected to a third delay input;

a clock signal transistor having a gate that communicates with the clock signal, the clock signal transistor being in series with the first cascaded amplifier transistor pair;

a second cascaded amplifier transistor pair driven by a voltage source and having a gate connected to the third delay;

a reference signal transistor having a gate connected to the reference signal input, wherein the reference signal transistor is in series with the second cascaded amplifier transistor pair;

a cross-coupled inverter pair that senses the difference between the clock signal and the reference signal input while the third delay turns the first amplifier transistor pair OFF and the second amplifier transistor pair OFF; and

a cross-coupled latch that latches a turn ON value from the cross coupled inverter pair.

14. The clock signal generating circuit according to Claim 13, further comprising:

a first logic gate that receives an alternate delay input and the turn ON value, an output of the first logic gate connected to the switch portion to turn the switch portion ON or OFF;

wherein the first logic gate turns ON the switch portion ON based on the alternate delay input and the turn ON value.

15. The clock signal generating circuit according to Claim 13, wherein the alternate delay input comprises:

a second delay signal that is cyclical;

a first delay signal that is cyclical; and

a logic gate that generates the alternate delay input when the first delay and second delay simultaneously reach peak values.

16. A method for operating a low power flip-flop, comprising:
generating a single phase ramped clock signal with a clock signal generator;
dispatching the ramped clock signal to a flip-flop;
receiving clock signal energy from the flip-flop;
storing the clock signal energy in a storage area in the clock signal generator; and

supplementing energy to the clock signal when the clock signal falls below a predetermined value.

17. The method according to Claim 16, wherein the step of generating comprises:

providing an oscillator portion that includes an energy storage device;
connecting the energy storage device to the memory storage device to form an oscillator circuit with the memory storage device and the energy storage device; and
providing a current through the energy storage device to force an oscillation during the supplementing step.

18. The method according to Claim 17, wherein the supplementing step further comprises:

comparing a peak value of the clock signal with a reference signal based on a third delay; and
supplementing the clock signal when the reference signal is greater than the clock signal.

19. The method according to Claim 18, wherein the supplementing step further comprises:

providing a first cyclical delay and a second cyclical delay; and
supplementing the clock signal when the first cyclical delay and the second cyclical delay reach simultaneous peak values.

20. The method according to Claim 17, wherein the energy storage device is an inductor and the flip-flop has inherent capacitance to form the oscillator portion.

21. A clock signal generating circuit, comprising:
oscillator means for sustaining a ramped oscillating clock signal in at least one memory storage device electrically connected to the oscillator portion;
switch means for supplementing electrical energy to the oscillator portion;
and

cycle controller means for determining when to supplement energy to the oscillator portion when a peak voltage or current level of the clock signal falls below a predetermined value.

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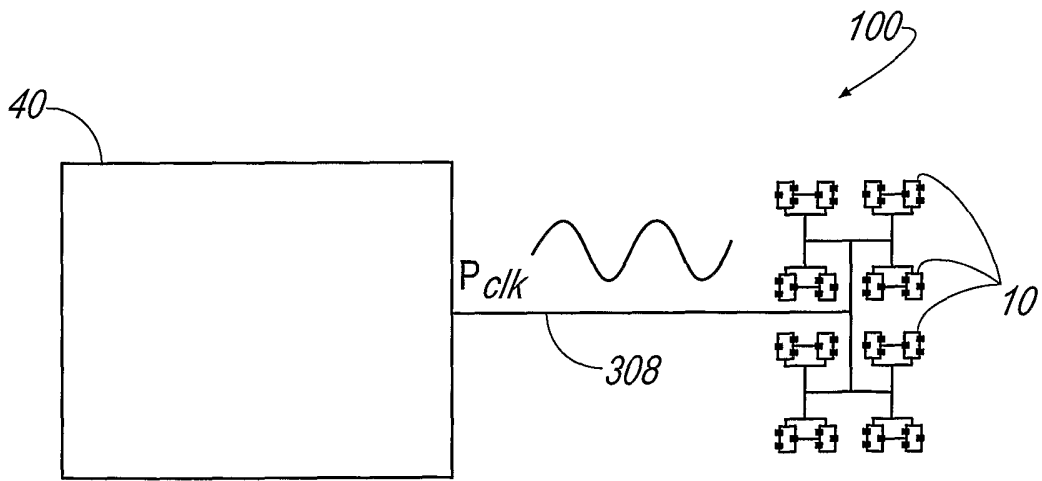
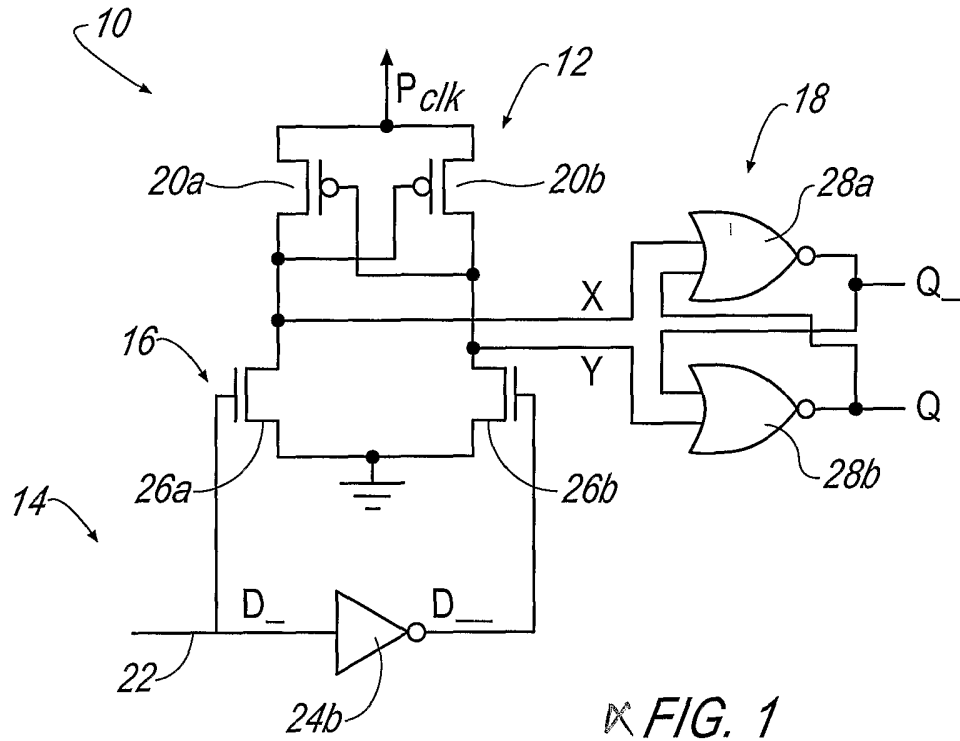
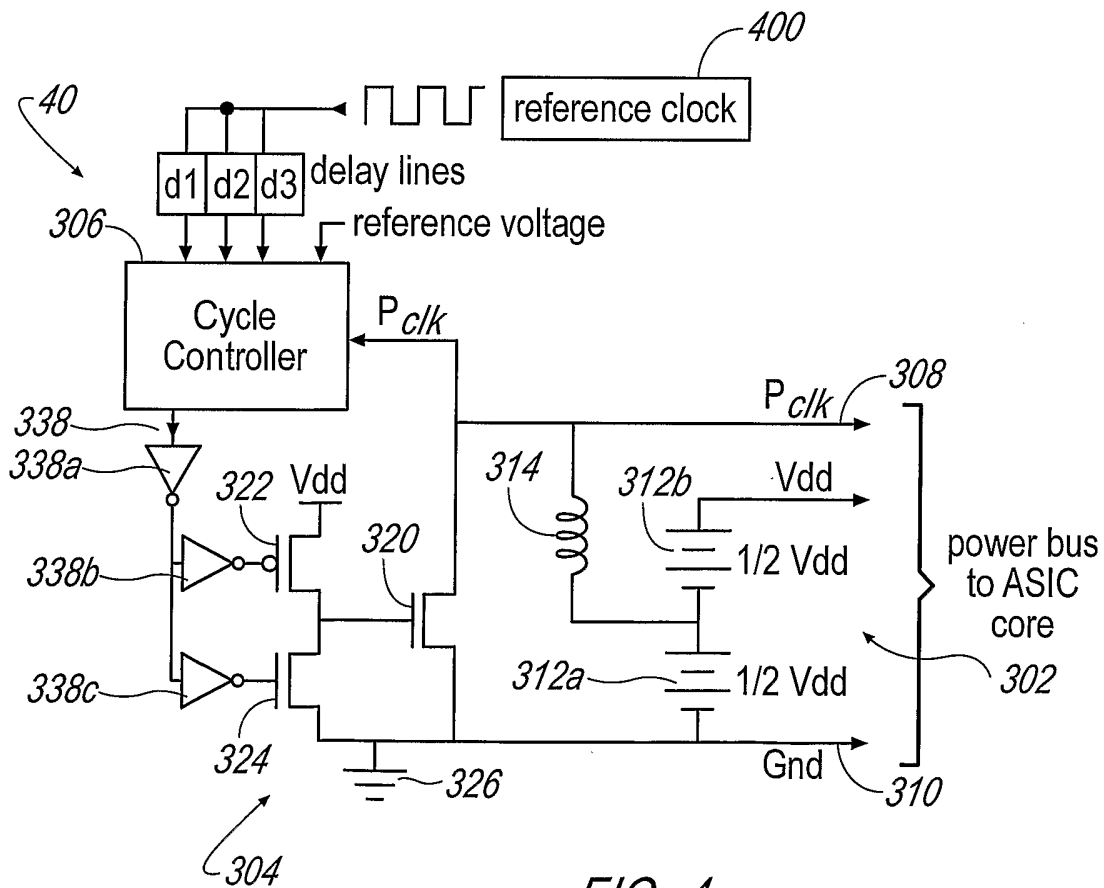
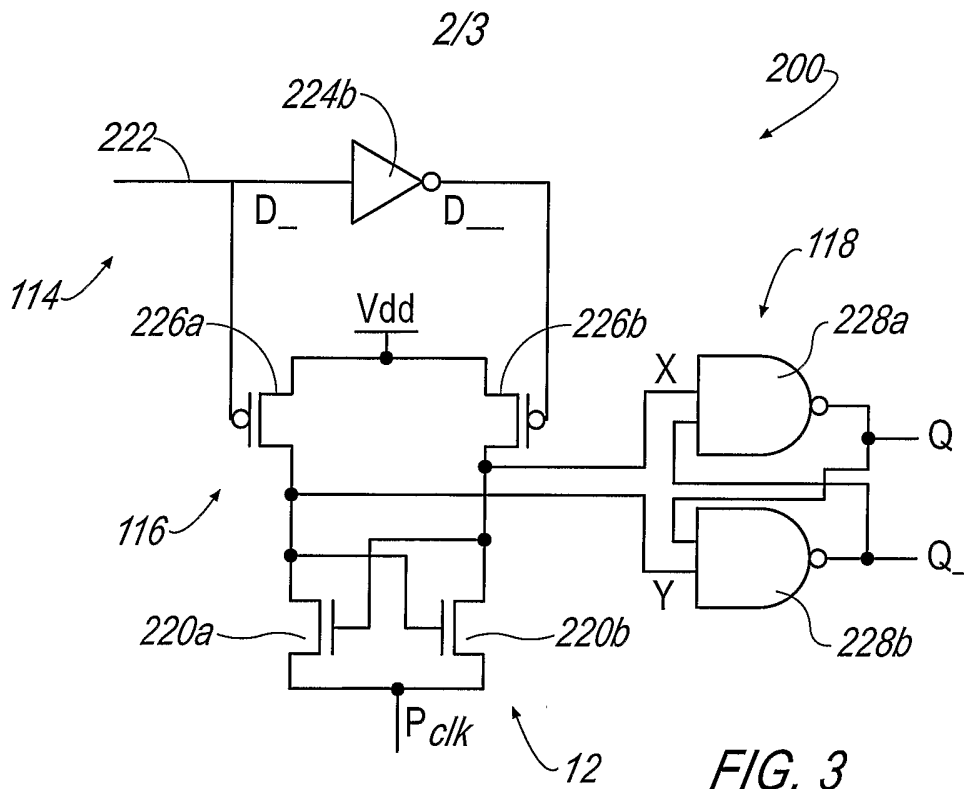


FIG. 2



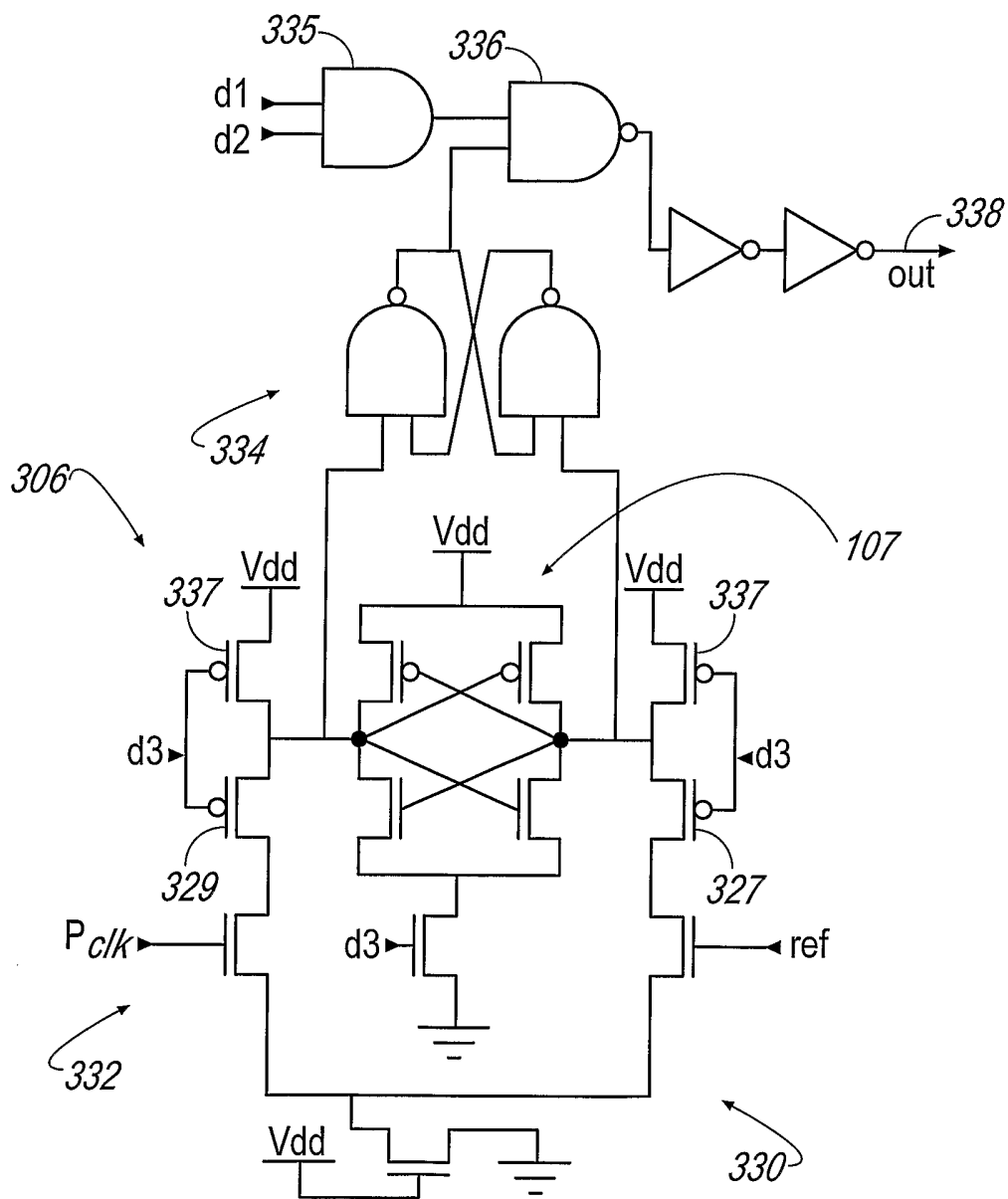


FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/10465

A. CLASSIFICATION OF SUBJECT MATTER		
IPC(7) : G06F 1/04, 1/26 US CL : 713/500, 713/300		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols) U.S. : 713/500, 713/300		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y,P	US 6,477,658 B1 (PANG) 5 November 2002 (05.11.2002), column 4, lines 4-33	1-5, 12, 16-18, 21
Y	US 5,970,074 A (EHIRO) 19 October 1999 (19.10.1999), column 9, lines 18-67	1-5, 12, 16-18, 21
Y	US 5,517,399 A (YAMAUCHI et al) 14 May 1996 (14.5.1996), column 4 line 26 through column 5 line 5.	1-5, 12, 16-18, 21
A	US 5,526,319 A (DENNARD et al) 11 June 1996 (11.06.1996)	1-21
A	US 5,838,203 A (STAMOULIS et al) 17 November 1998 (17.11.1998)	1-21
<input type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents:		
"A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family	
Date of the actual completion of the international search	Date of mailing of the international search report	
18 June 2003 (18.06.2003)	24 JUL 2003	
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703)305-3230	Authorized officer Thomas Lee <i>Peggy Harrod</i> Telephone No. (703) 305-3900	