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L. BESS

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WIDE GATE GENERATOR

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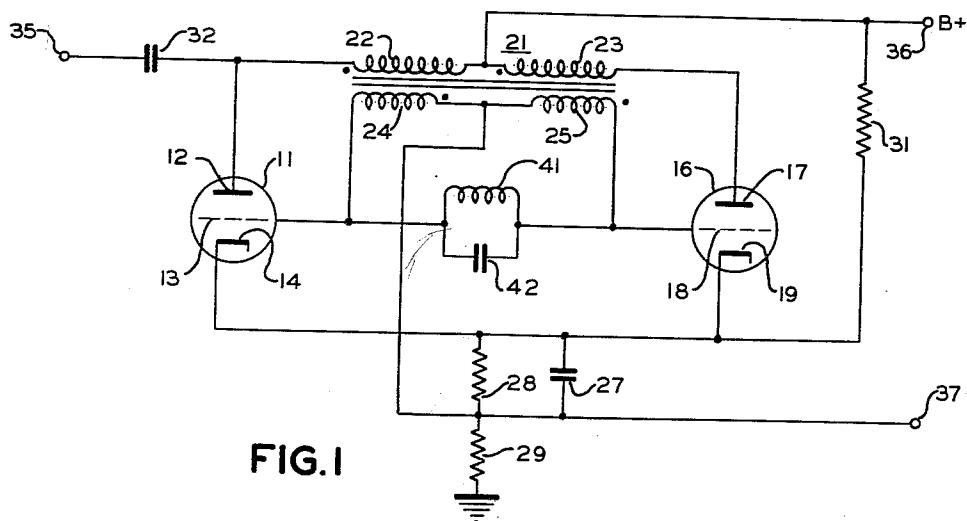


FIG. 1

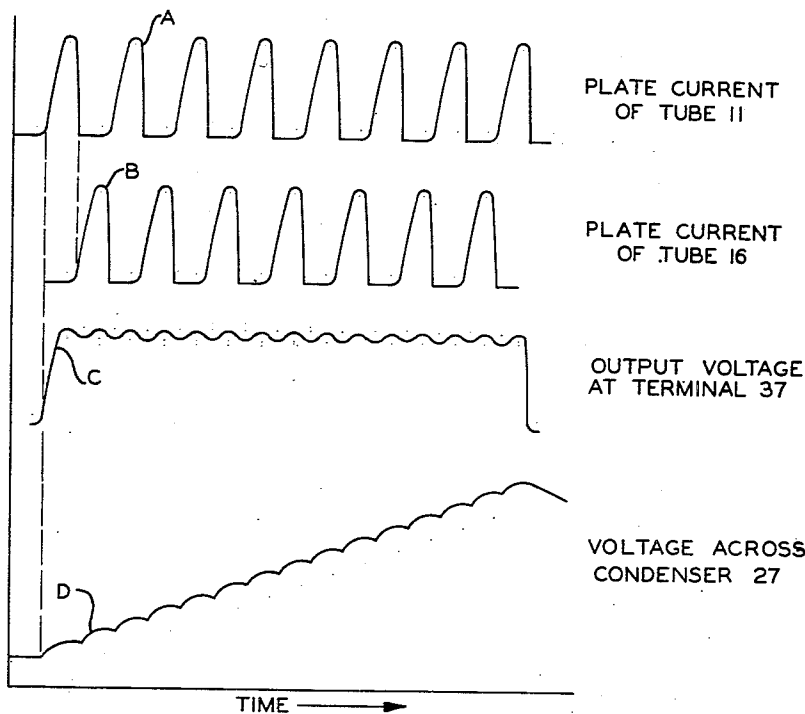


FIG. 2

INVENTOR
LEON BESS

BY

M. A. Hayes

ATTORNEY

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2,708,241

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Leon Bess, Urbana, Ill., assignor, by mesne assignments, to the United States of America as represented by the Secretary of the Navy

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5 Claims. (Cl. 250—27)

This invention relates to electrical trigger circuits and more particularly to comparatively long time or wide gate generating circuits using blocking oscillators.

Heretofore, wide gate generating circuits such as a multivibrator were undesirable since they had a relatively high current drain and failed to generate sufficiently steep leading and trailing edges for the gate.

The general object of the present invention is to overcome the foregoing difficulties.

Another object of the present invention is to provide a wide gate generating circuit using blocking oscillators.

A further object is to provide a wide gate generating circuit having low current drain and generating a wide gate having steep leading and trailing edges.

In accordance with the general principles of the present invention, two blocking oscillators are operated in push-pull and have a common self-biasing circuit. Their outputs are taken from a common cathode resistor to provide a wide gate having steep leading and trailing edges and whose time duration is dependent on the circuit constants of the self-biasing circuit. Further, by biasing the two tubes of the blocking oscillators below cutoff between gates, conduction will take place only during the gate interval thus keeping current drain very low.

The above and other objects of this invention will be apparent from the following specification when taken with the accompanying drawing, in which:

Fig. 1 is a schematic diagram of one form of the invention; and,

Fig. 2 depicts graphs useful in explaining the invention.

Referring to the drawing, and more particularly to Fig. 1, two thermionic tubes 11 and 16 having plates 12 and 17, grids 13 and 18, and cathodes 14 and 19, respectively, are connected to transformer 21 having two primary windings 22 and 23 and two secondary windings 24 and 25, such as to comprise two blocking oscillators operating in push-pull. The parallel combination of resistor 28 and condenser 27 comprises a self-biasing circuit to determine the time duration of the gate and is connected from cathodes 14 and 19, which are connected together, to secondary windings 24 and 25, which are connected together and to grids 13 and 18, respectively. Plates 12 and 17 are connected to a source of positive potential at 36 through primary windings 22 and 23, respectively. A cathode load resistor 29 is connected to ground from output terminal 37, which is common to the junction of condenser 27, resistor 28, and secondary windings 24 and 25. A resistor 31 is connected from positive potential source at 36 to the junction of resistor 28 and cathodes 14 and 19 and has a size such that it will establish a bleeder voltage across resistor 28 to bias tubes 11 and 16 below cutoff during their quiescent interval.

The transformer 21 is connected so that primary windings 22 and 23 are connected together and to a source of positive potential at 36 and secondary windings 24 and 25 are connected together and to the self-biasing circuit. Also, primary windings 22 and 23 are oppositely

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poled with respect to each other (shown by the phasing dots of Fig. 1) such that plates 12 and 17 are of opposite polarity. Likewise, secondary windings 24 and 25 are oppositely poled with respect to each other and to their respective primary windings 22 and 23 such that plate 12 and grid 13 or plate 17 and grid 18 are of opposite polarity. The above polarities of plates and grids of tubes 11 and 16 are the same as found in many push-pull oscillators.

In the quiescent condition of the circuit shown in Fig. 1 neither tube 11 nor 16 is conducting due to the bias voltage across resistor 28 and, therefore, there is no current drain through tubes 11 and 16 from positive potential source at 36. If a negative trigger is now applied to plate 12 through coupling condenser 32 from trigger input terminal 35, tube 11 will begin to conduct since primary winding 22 and secondary winding 24 are oppositely poled causing the input trigger to be positive at grid 13. Tube 16 will remain cutoff since the input trigger will be negative at its grid 18. The flow of plate current in primary winding 22 generates in secondary winding 24 a positive potential for grid 13 causing more plate current to flow through tube 11 and primary winding 22. Thus a regenerative action is set up which continues until plate current becomes essentially constant due to plate saturation. The potential at grid 13 then decreases causing plate current to decrease and setting up a regenerative action in the opposite direction which continues until tube 11 is cut off. Due to distributed capacities associated with the windings of transformer 21 damped oscillations take place in its windings. The first cycle of such oscillation or overshoot produces a positive trigger at grid 18 causing tube 16 to conduct. Tube 16 goes through a cycle similar to that for tube 11 and its overshoot in turn retriggers tube 11.

The plate current of tube 11 is shown as curve A of Fig. 2 and the plate current of tube 16 is shown as curve B of Fig. 2. From the drawing it is obvious that these plate currents flow through resistor 29 and the two together generate an output voltage at terminal 37 such as curve C of Fig. 2.

During each cycle of operation the grid of the conducting tube goes above the cathode potential causing grid current to flow which, along with the plate current, charges up condenser 27. This charging process continues in steps, as shown by curve D of Fig. 2. The above mentioned retrIGGERING likewise continues until some particular overshoot or trigger is insufficient to overcome the bias built up on condenser 27. Then both tubes stop conducting, the gate ends, and condenser 27 discharges through resistor 28 during the quiescent interval before the introduction of the next trigger at terminal 35.

Since the number of retrIGGERINGS is dependent on the time necessary to build up blocking bias on condenser 27, the time duration of the output gate can be determined by the size of resistor 28 and condenser 27. If a variable gate width is desired condenser 27, resistor 28, or both, can be made variable since the time to build up blocking bias is essentially proportional to the size of condenser 27, and resistor 28 determines the initial bias and hence, the amount of additional bias which must be built up during the gate.

It is noticed from curve C of Fig. 2 that some ripple is present in the output gate at terminal 37. This ripple can be reduced by designing the circuit so that each individual pulse is of short time duration. The output gate would then be made up of more pulses from tubes 11 and 16 and the ripple would be less and at a higher frequency such as to be more easily filtered by stray circuit capacitance. Such design has the added advantage that the gate width can be varied in smaller increments of

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time since the output gate at terminal 37 must be made up of a whole number of pulses.

The above mentioned ripple in the output gate may be further reduced by connecting a high frequency resonant circuit, comprising inductor 41 and condenser 42, between grids 13 and 18 as shown in Fig. 1. This produces a still higher frequency ripple which is filtered by stray circuit capacitance.

This invention has the advantage that it provides a wide gate of any desired time duration. Another advantage is that the output gate has steep leading and trailing edges. A further advantage is that there is a very low current drain since tubes 11 and 16 conduct only during the generation of the gate.

The invention described in the foregoing specification need not be limited to the details shown, which are considered to be illustrative of one form the invention may take. Although the invention has been disclosed as using a negative trigger input it is to be understood that a positive trigger connected to either plate or either grid would work equally as well. It is to be further understood that the circuit could be designed so as to be free-running and not require a trigger. It is to be still further understood that the gate width of the output voltage at terminal 37 need not be limited to the number of cycles shown in Fig. 2.

What is claimed is:

1. Apparatus for producing a voltage wave of predetermined time duration comprising, two blocking oscillators, each of said oscillators including a pulse transformer having an input circuit winding, each transformer being inductively coupled to the other transformer, each said oscillator being adapted to induce an oscillatory overshoot in the input circuit winding of the other oscillator to initiate therein a cycle of oscillator operation, and a common biasing circuit for said oscillators having a timing means adapted to be step-charged by successive cycles of operation to a predetermined voltage to bias said oscillators to nonconduction.

2. A wide gate generator comprising, two blocking oscillators having common plate, grid, and cathode connections, each of said blocking oscillators including a pulse transformer, the pulse transformers being inductively cross-coupled, a resistor connected between said common grid connection and a point of reference potential, timing means connected between said common cathode connection and said resistor, said timing means being adapted to be step charged by successive cycles of operation to a potential biasing said oscillators to nonconduction, and means for applying a trigger voltage pulse to one of said oscillators, whereby a voltage wave of predetermined time duration will be developed across said resistor upon the application of said trigger voltage pulse.

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3. Apparatus for producing a voltage wave of predetermined time duration comprising, two push-pull connected blocking oscillators biased to nonconduction by a common self-biasing circuit, a source of voltage pulses, means applying a voltage pulse from said source to one of said oscillators to bias said oscillator to conduction, means coupling the output of each oscillator to the input of the other to induce successive cycles of oscillation, a capacitor connected to shunt said self-biasing circuit thereby to bias said oscillators to nonconduction by step-charging from successive cycles to a predetermined potential value, and a high frequency resonant circuit connected between the inputs of said oscillators to cause high frequency cycling of said oscillators.

4. A wide gate generating circuit comprising, two thermionic tubes each having at least a plate, a grid, and a cathode, a transformer having two primary windings and two secondary windings, a source of trigger voltage input for one of said thermionic tubes, a source of positive voltage, and a cathode circuit including a condenser and a pair of series connected resistors; the plates of said thermionic tubes being connected to said source of positive potential through said primary windings of said transformer, the cathodes of said thermionic tubes being connected together and to ground through said cathode circuit, said condenser being connected between said common cathode connection and the common connection of said resistors to furnish a source of bias for the grids of said thermionic tubes, the output being taken between ground and the common connection of said cathode resistors, and the grids of said thermionic tubes being connected to the aforesaid source of bias through said secondary windings of said transformer; said thermionic tubes acting as blocking oscillators and retriggering one another for a time determined by the constants of said biasing source and providing at said output a wide gate having steep leading and trailing edges.

5. The wide gate generating circuit of claim 4 having in addition a high frequency resonant circuit connected between the grids of said thermionic tubes.

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