(54) Title: CONTENT ADDRESSABLE MEMORY AUGMENTED MEMORY

100
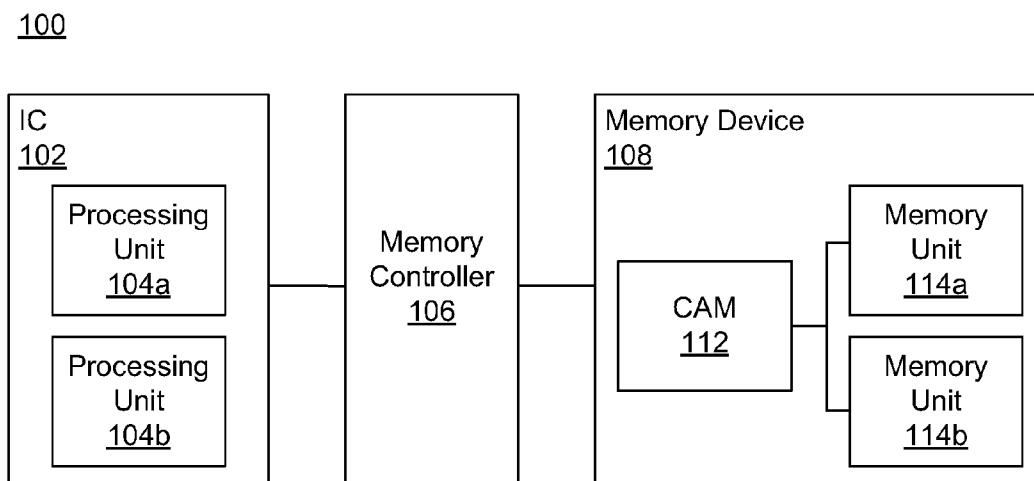
Fig. 1

(57) Abstract: Embodiments of the present disclosure provide methods, apparatuses, and systems including a memory device and content addressable memory configured to store an address associated with one or more memory cells while an access operation is performed on the one or more memory cells. Preferred embodiments show the issuance of a busy signal in case of an address being stored in the CAM and being accessed; or the return of data from the CAM. The use of the CAM and memory in the advanced memory buffer (AMB) of a fully-buffered DIMM (TB-DIMM) is also contemplated

CONTENT ADDRESSABLE MEMORY AUGMENTED MEMORY

TECHNICAL FIELD

[0001]   Embodiments of the present disclosure relate to the field of integrated circuits, and, more specifically, to digital memory apparatuses and systems including content addressable memory.

BACKGROUND

[0001]   Semiconductor memories play a vital role in many electronic systems. Their functions for data storage, code (instruction) storage, and data retrieval/access continue to span a wide variety of applications. Usage of these memories in both stand alone/discrete memory product forms, as well as embedded forms such as, for example, memory integrated with other functions like logic, in a module or monolithic integrated circuit, continues to grow. Cost, operating power, bandwidth, latency, ease of use, the ability to support broad applications, and nonvolatility are all desirable attributes in a wide range of applications.

[0002]   In page architecture memory systems, opening a page of memory may prevent access to another page of the memory bank. This may effectively increase access and cycle times. In multi-processor or multi-core systems, attempts to access memory in parallel while running different applications may compound the delays due to locked up memory banks.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003]   Embodiments of the present disclosure will be readily understood by the following detailed description in conjunction with the accompanying drawings. Embodiments of the disclosure are illustrated by way of example and not by way of limitation in the figures of the accompanying drawings.

[0004]   **Fig. 1** illustrates a functional system block diagram including an exemplary digital memory device including a content addressable memory in accordance with various embodiments of the present disclosure.

[0005]   **Fig. 2** illustrates an exemplary computing system including a memory device including a content addressable memory suitable for practicing the disclosure, in accordance with various embodiments.

[0006]   **Fig. 3** illustrates a flow chart of a method implementing a memory device including a content addressable memory in accordance with various embodiments of the present disclosure.

[0007]   **Fig. 4** illustrates a flow chart of another method implementing a memory device including a content addressable memory in accordance with various embodiments of the present disclosure.

[0008]   **Fig. 5** illustrates a block diagram of a hardware design specification being compiled into GDS or GDSII data format in accordance with various embodiments.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE DISCLOSURE

[0009]   In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which are shown by way of

illustration embodiments in which the disclosure may be practiced. It is to be understood that other embodiments may be utilized and structural or logical changes may be made without departing from the scope of the present disclosure. Therefore, the following detailed description is not to be taken in a limiting sense, and the scope of embodiments in accordance with the present disclosure is defined by the appended claims and their equivalents.

[0010]   Various operations may be described as multiple discrete operations in turn, in a manner that may be helpful in understanding embodiments of the present disclosure; however, the order of description should not be construed to imply that these operations are order dependent.

[0011]   The description may use the phrases "in an embodiment," or "in embodiments," which may each refer to one or more of the same or different embodiments. Furthermore, the terms "comprising," "including," "having," and the like, as used with respect to embodiments of the present disclosure, are synonymous.

[0012]   The term "access operation" may be used throughout the specification and claims and may refer to read, write, or other access operations to one or more memory devices.

[0013]   Various embodiments of the present disclosure may include a digital memory device, such as, but not limited to, random access memory (RAM) device including content addressable memory configured to store at least an address associated with one or more memory cells of a subset of a plurality of memory cells while an access operation is performed on the one or more memory cells. The stored address may indicate, to a processor, for example, that the one or more memory cells associated with the stored address are busy or otherwise inaccessible

at that particular time. Such an indication may reduce the number of cycles wasted due to stalling if the requested address is unavailable.

[0014]   In further embodiments, the content addressable memory may be configured to copy and store data corresponding to at least the address when the access operation is initiated, and to selectively output the stored data to satisfy the access operation. Copying and storing the data may allow memory cells of the subset to freed up or otherwise made available for some subsequent access operation.

[0015]   Referring now to **Fig. 1**, illustrated is a functional block diagram of a system **100** comprising an exemplary digital memory device **108** including one or more memory units **114a**, **114b** and a content addressable memory (CAM) device **112** in accordance with various embodiments of the present disclosure. System **100** may include one or more processors **104a**, **104b**, and may include a memory controller **106** operatively coupled to memory device **108** for selectively routing signals between memory device **108** and processors **104a**, **104b** to control access operations to memory device **108**. Processors **104a**, **104b** may be stand-alone processors or core processors disposed on a single integrated circuit **102**.

[0016]   CAM **112** may be configured to store at least one address associated with one or more memory cells of memory units **114a**, **114b** being accessed. Each of memory units **114a**, **114b** may comprise some subset of memory such as, for example, a memory bank and/or a memory page, and each subset may comprise a plurality of memory cells. Although the illustrated embodiment depicts memory device **108** as including two memory units **114a**, **114b**, memory device **108** may include more or less memory units according to various embodiments within the scope of the disclosure.

4

[0017]　　　　In various embodiments, CAM **112** may be configured to store at least one address of one or more memory cells of one or more of memory units **114a**, **114ba** while an access operation is performed on the one or more memory cells. In various embodiments, the stored address may indicate to one or more of processors **104a**, **104b** that the one or more memory cells associated with the stored address are busy or otherwise inaccessible at that particular time. In embodiments wherein a memory unit **114a** or **114b** comprises a memory page, a stored address may be employed to indicate a busy state of the memory page. Similarly, in embodiments wherein a memory unit **114a** or **114b** comprises a memory bank, a stored address may be employed to indicate a busy state of the memory bank.

[0018]　　　　In various embodiments, one or more of processors **104a**, **104b** may present an address for an access operation to memory device **108**, and CAM **112** may determine whether the address is already stored in CAM **112**. CAM **112** may determine whether the address is already stored by comparing the presented address to those addresses stored in CAM **112** in, for example, an address lookup table. If the address is already stored in CAM **112**, CAM **112** may indicate to processors **104a**, **104b** that the one or more memory cells associated with the stored address are busy. Such an indication may include, for example, a signal on an output pin of memory device **108**.

[0019]　　　　If, on the other hand, the address is not already stored in CAM **112**, CAM **112** may indicate to processors **104a**, **104b** that the one or more memory cells associated with the stored address are available. Such an indication may include a signal, in particular, a "no hit" or "no match" signal, on an output pin of memory device **108**. CAM **112** may, in various embodiments, present the address to the plurality of memory cells of memory device **108** to output data associated with the

address (e.g., during a read operation). CAM **112** may store the address, at least momentarily, for indicating to one or more of processors **104a**, **104b** that the one or more memory cells associated with the newly stored address are busy or otherwise inaccessible at that particular time. In various ones of these embodiments, CAM **112** may store the address during substantially the entire access operation and remove the address after the access operation is completed, which may advantageously allow for a substantially real-time indication of memory availability. As used herein, references to "removing" an address may include, but is not limited to, deleting and/or modifying the address (by, e.g., overwriting with a default address or another address) or marking the stored address invalid (by, e.g., setting an appropriate associated bit).

[0020]   In further embodiments, CAM **112** may be configured to copy and store data corresponding to at least an address associated with one or more memory cells of memory unit **114a** or **114b** when an access operation is initiated. Copying and storing the data may allow memory cells of the memory unit to be freed up or otherwise made available for some subsequent access operation. The cached data may be, in embodiments, selectively output to satisfy the access operation and/or a subsequent access operation.

[0021]   CAM **112** may be configured to store a plurality of addresses or a plurality of addresses and data associated thereto. For example, in various embodiments, CAM **112** may be configured to store a first address and data associated with a first one or more memory cells of a plurality of memory cells, and also to store a second address and data associated with a second one or more memory cells of the plurality of memory cells. In various ones of these embodiments, a first access operation may be satisfied by the first address/data

6

copied and stored in CAM **112** concurrently with a second access operation being performed on the second address/data.

[0022]   In various embodiments, the first one or more memory cells of the plurality of memory cells and the second one or more memory cells of the plurality of memory cells may be disjoint subsets or may be intersecting/non-disjoint subsets. In embodiments wherein the first a one or more memory cells and the second one or more memory cells are intersecting/non-disjoint subsets, the first access operation and the second access operation usually will be read operations to avoid conflicts such as, for example, data incoherence. On the other hand, in embodiments wherein the first one or more memory cells and the second one or more memory cells are disjoint subsets, various parallel access operations may be performed on the first one or more memory cells and the second one or more memory cells. For example, a read or a write operation may be performed on the first one or more memory cells while a read or a write operation is performed on the second one or more memory cells.

[0023]   The memory cells of memory units **114a**, **114b** may be memory cells of any type. For example, the memory cells may be volatile dynamic random access memory (DRAM) cells or static random access memory (SRAM) cells, or nonvolatile memories like flash memory, depending on the application. Further, while not illustrated, memory device **108** may include sense amplifier circuits, decoders, and/or logic circuitry, depending on the application.

[0024]   Memory device **108** may comprise a discrete device or may comprise a system of elements, depending on the application. For example, in various embodiments, CAM **112** and memory units **114a**, **114b** of memory device **108** may comprise a memory module such as, for example, a dual in-line memory module

(DIMM). A DIMM may comprise an advanced memory buffer (AMB), and in various ones of these embodiments, the AMB may include CAM **112**. In various other embodiments, CAM **112** and memory units **114a**, **114b** may be co-located on a single integrated circuit.

[0025]   In various embodiments, the memory controller **106** may be operatively coupled (by, e.g., a bus) to at least one of processors **104a**, **104b** and a memory device **108** and its included elements, or may be incorporated into memory device **108**. CAM **112** may include, for example, memory controller **106**.

[0026]   Memory device **108** may be accessed by one or more of processors **104a**, **104b**. In the illustrated embodiment, two processors **104a**, **104b** are coupled to memory device **108**. In various embodiments, however, more or fewer processors may be coupled to memory device **108**. In various embodiments, processors **104a**, **104b** may comprise processing units or processor cores. For example, processors **104a**, **104b** may comprise dual-core or multi-core processors. Additionally, the processing units may be disposed remotely from each other, or they may be implemented as processing cores commonly disposed on a single integrated circuit **102**. Processors **104a**, **104b** may be coupled to memory device **108** via various elements and may access and precharge various memory units in parallel.

[0027]   Fig. 2 illustrates an exemplary computing system **200** incorporating embodiments of the present disclosure. As illustrated, system **200** may include one or more processors **216**, and system memory **218**, such as, for example, memory device **108** of **Fig 1**.

[0028]   In various embodiments, system memory **218** may include a CAM **219**, such as for example, CAM **112** of **Fig. 1**. CAM **219** may be configured to store at least an address associated with one or more memory cells of memory **218** while an

access operation is performed on the one or more memory cells. The stored

address may indicate, to one or more of processors **216**, for example, that the one or

more memory cells associated with the stored address are busy or otherwise

inaccessible at that particular time. In further embodiments, CAM **219** may be

configured to copy and store data corresponding to at least the address when the

access operation is initiated, and to selectively output the stored data to satisfy the

access operation. Copying and storing the data may allow memory cells to be freed

up or otherwise made available for some subsequent access operation.

[0029]   Additionally, computing system **200** may include mass storage devices

220 (such as, e.g., diskette, hard drive, CDROM, and the like), input/output devices

222 (such as, e.g., keyboard, cursor control, and the like), and communication

interfaces **224** (such as, e.g., network interface cards, modems, and the like). The

elements may be coupled to each other via system bus **226**, which may represent

one or more buses. In the case of multiple buses, they may be bridged by one or

more bus bridges (not illustrated).

[0030]   System **200** may include at least one memory controller **226** embodied

with some or all of the teachings of the present disclosure. Memory controller **226**

may be configured to operate system memory **218**. In embodiments, memory

controller **226** may be configured, for example, to issue read and write access

commands to system memory **218**. In alternative embodiments, system memory

218 may include a controller (not illustrated) to perform some or all of the functions of

memory controller **226**. In embodiments, some or all of the functions of controller

226 could be effectively implemented within system memory **218**. In embodiments,

such functions may be performed by use of a mode register within system memory

218.

[0031]   Other than the teachings of the various embodiments of the present

disclosure, each of the elements of computer system **200** may perform its

conventional functions known in the art. In particular, system memory **218** and mass

storage **220** may be employed to store a working copy and a permanent copy of

programming instructions implementing one or more software applications.

[0032]   Although **Fig. 2** depicts a computer system, one of ordinary skill in the

art will recognize that embodiments of the present disclosure may be practiced using

other devices that utilize DRAM or other types of digital memory such as, but not

limited to, mobile telephones, Personal Data Assistants (PDAs), gaming devices,

high-definition television (HDTV) devices, appliances, networking devices, digital

music players, laptop computers, portable electronic devices, telephones, as well as

other devices known in the art.

[0033]   Referring now to **Fig. 3** and **Fig. 4**, flow charts of exemplary methods

of operation of a memory device are illustrated. With respect to **Fig. 3,** at block **328**,

an access command, such as, for example, a read or write command, may be

received by a memory device including a CAM. The received access command may

include an address or identifier corresponding to one or more memory cells of a

memory unit to be accessed. The received address may be compared at block **330**

to addresses stored in the CAM. If it is determined at query block **332** that an

address matching the requested address is already stored in the CAM, a busy state

may be indicated at block **334**.

[0034]   If, on the other hand, it is determined at query block **332** that a

matching address is not already stored in the CAM, an indication of availability of the

memory cells corresponding to the requested address may be provided at block **336**.

In various embodiments, the requested address may be stored at block **338** for

indicating a busy state in response to subsequent access commands to that

address. At query block **340**, a determination is made as to whether the access

operation is complete. The CAM may continue storing the address at block **342** if

the access operation is not yet complete, whereas the address may be removed

from the CAM at block **344** after the access operation is completed.

[0035]   In further embodiments and as illustrated in **Fig. 4**, the CAM may be

configured to copy and store data corresponding to an address of a one or more

memory cells of a memory unit when an access operation is initiated, and to

selectively output the stored data to satisfy the access operation or another access

operation.

[0036]   At block **446**, an access command, such as, for example, a read or

write command, may be received by a memory device including a CAM. The

received access command may include an address or identifier corresponding to one

or more memory cells of a memory unit to be accessed. The received address may

be compared at block **448** to addresses stored in the CAM. If it is determined at

query block **450** that an address matching the requested address is already stored in

the CAM, the data associated with the address (and already stored in the CAM) is

provided at block **452** in response to the access command.

[0037]   If, on the other hand, it is determined that an address matching the

requested address is not already stored in the CAM, the memory unit may be

accessed at block **454** for the data. The data corresponding to the requested

address may be copied out at block **456** and may be provided at block **458** in

response to the access command.

[0038]   As noted herein, in various embodiments, memory cells as described

herein may be embodied in an integrated circuit. The integrated circuit may be

described using any one of a number of hardware design language, such as but not limited to VHDL or Verilog. The complied design may be stored in any one of a number of data format such as, but not limited to, GDS or GDS II. The source and/or compiled design may be stored on any one of a number of media such as but not limited to DVD. **Fig. 5** illustrates a block diagram depicting the compilation of a hardware design specification **560**, which may be run through a compiler **562** to produce GDS or GDS II data format **564** describing an integrated circuit in accordance with various embodiments.

[0039]   Although certain embodiments have been illustrated and described herein for purposes of description of a preferred embodiment, it will be appreciated by those of ordinary skill in the art that a wide variety of alternate and/or equivalent embodiments or implementations calculated to achieve the same purposes may be substituted for the embodiments shown and described without departing from the scope of the present disclosure. Those with skill in the art will readily appreciate that embodiments in accordance with the present disclosure may be implemented in a very wide variety of ways. This application is intended to cover any adaptations or variations of the embodiments discussed herein. Therefore, it is manifestly intended that embodiments in accordance with the present disclosure be limited only by the claims and the equivalents thereof.

CLAIMS

What is claimed is:

1.   An apparatus comprising:

a memory device including a plurality of memory cells; and

content-addressable memory configured to store a first address associated

with one or more memory cells from a first subset of the plurality of memory cells

while a first access operation is performed on the one or more memory cells.

2.   The apparatus of claim 1, wherein the first subset corresponds to a memory

page, and wherein the content-addressable memory is further configured to use the

stored first address to indicate a busy state of the memory page.

3.   The apparatus of claim 1, wherein the content-addressable memory is further

configured to remove the stored first address after the first access operation is

completed.

4.   The apparatus of claim 1, wherein the content-addressable memory is further

configured to copy and store data corresponding to the first address when the first

access operation is initiated and to selectively output the stored data to satisfy the

first access operation, and wherein the first access operation is a read operation.

5.   The apparatus of claim 4, wherein the content-addressable memory is further

configured to store a second address associated with another one or more memory

cells from the first subset of the plurality of memory cells while a second access

operation is performed on the other one or more memory cells from the first subset, wherein the second access operation is performed at least partially concurrently with the first access operation, and wherein the second access operation is also a read operation.

6.   The apparatus of claim 1, wherein the content-addressable memory is further configured to store a third address associated with one or more memory cells from a second subset of the plurality of memory cells while a third access operation is performed on the one or more memory cells from the second subset, and wherein the first and second subsets have no memory cells in common.

7.   The apparatus of claim 1, further comprising a dual inline memory module (DIMM) including the memory device and the content-addressable memory.

8.   The apparatus of claim 7, wherein the DIMM comprises an advanced memory buffer (AMB) including the content-addressable memory.

9.   The apparatus of claim 1, further comprising a memory controller including the content-addressable memory.

10.   The apparatus of claim 1, wherein the memory device and the content-addressable memory are co-located on one integrated circuit.

11.   The apparatus of claim 1, wherein the first access operation is a selected one of a read operation or a write operation.

12.   A system, comprising:

at least one processor;

a memory subsystem including:

a memory device having a plurality of memory cells; and

content-addressable memory configured to store a first address
associated with one or more memory cells from a first subset of the
plurality of memory cells during performance of a first access operation
on the one or more memory cells; and

a controller coupled to the at least one processor and to the memory
subsystem and configured to selectively route signals between the memory device
and the at least one processor to control access operations to the memory device.

13.   The system of claim 12, wherein the first subset corresponds to a memory
page, and wherein the content-addressible memory is further configured to use the
stored first address to indicate a busy state of the memory page.

14.   The system of claim 12, wherein the content-addressable memory is further
configured to remove the stored first address after completion of the first access
operation .

15.   The system of claim 12, wherein the content-addressable memory is further
configured to copy and store data corresponding to the first address upon initiation of
the first access operation.

16.   The system of claim 15, wherein the content-addressable memory is further configured to store a second address associated with another one or more memory cells from the first subset of the plurality of memory cells during performance of a second access operation on the other one or more memory cells from the first subset, wherein the second access operation is performed at least partially concurrently with the first access operation, and wherein the second access operation is also a read operation.

17.   The system of claim 12, wherein the controller comprises the content-addressable memory.

18.   The system of claim 12, wherein the memory subsystem comprises a dual inline memory module (DIMM) including the memory device and the content-addressable memory.

19.   A method, comprising:

storing a first address associated with a first access operation being performed on a memory unit in a content-addressable memory while the first access operation is being performed, wherein the first address corresponds to one or more memory cells from a first subset of a plurality of memory cells for a memory unit being accessed by the first access operation; and

removing the stored first address from the content-addressable memory after the first access operation has been completed.

20.   The method of claim 19, further comprising accessing the memory unit for data.

21.   The method of claim 20, further comprising:

copying the data out; and

providing the data from the copied data.

22.   The method of claim 19, further comprising:

storing a second address corresponding to another one or more memory cells from the first subset of the plurality of memory cells for the memory unit; and

accessing the memory unit for other one or more memory cells of the first subset.

23.   The method of claim 19, further comprising storing a third address associated with one or more memory cells from a second subset of the plurality of memory cells while a third access operation is performed on the one or more memory cells from the second subset, wherein the first and second subsets have no memory cells in common.
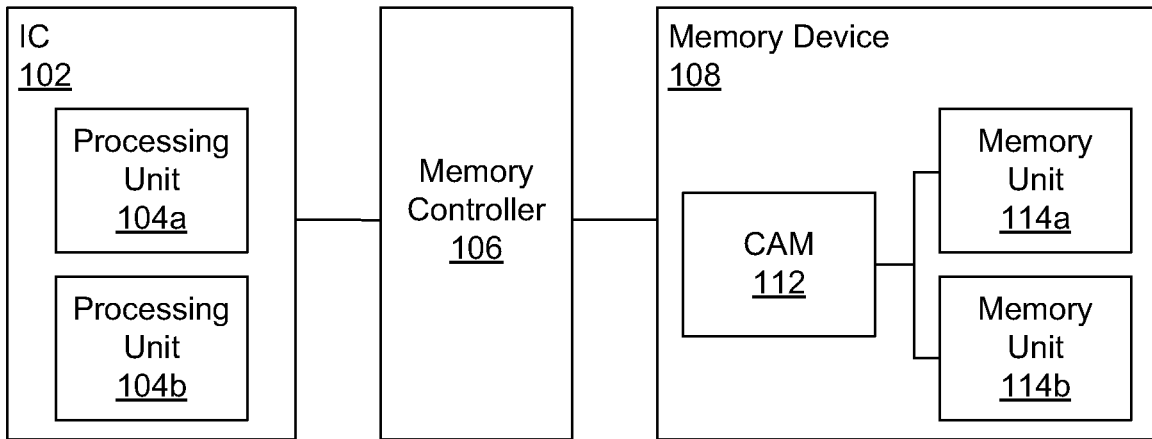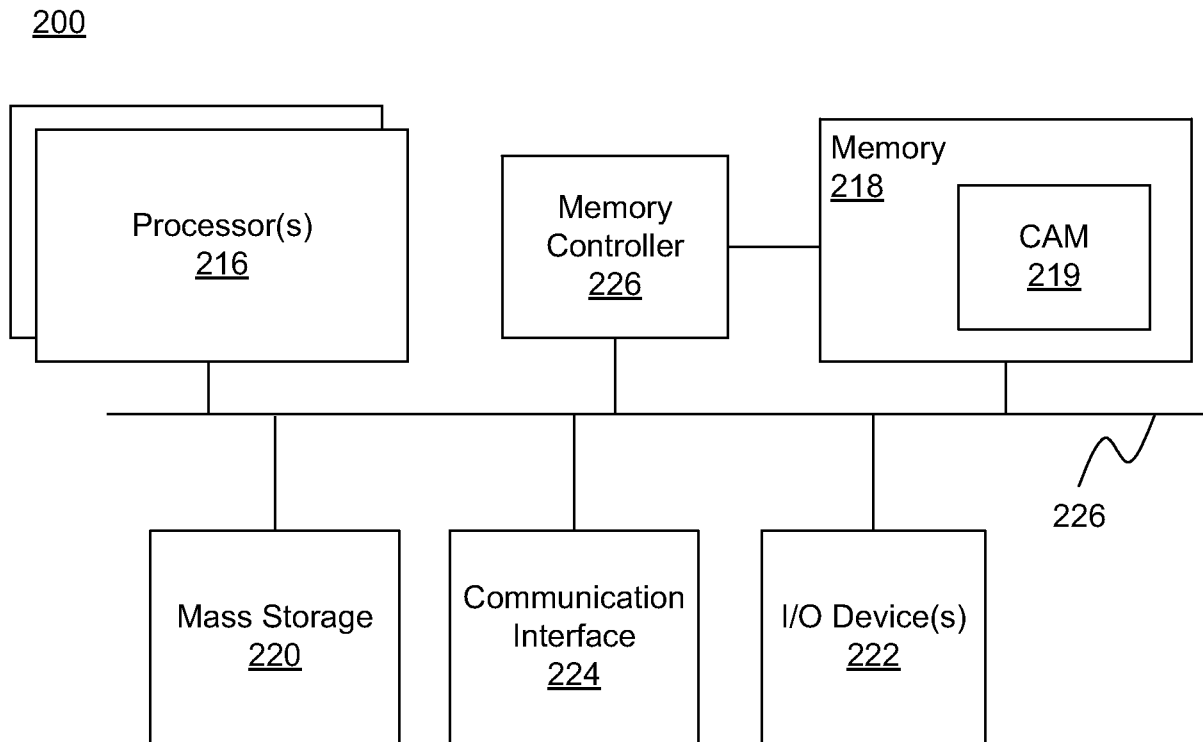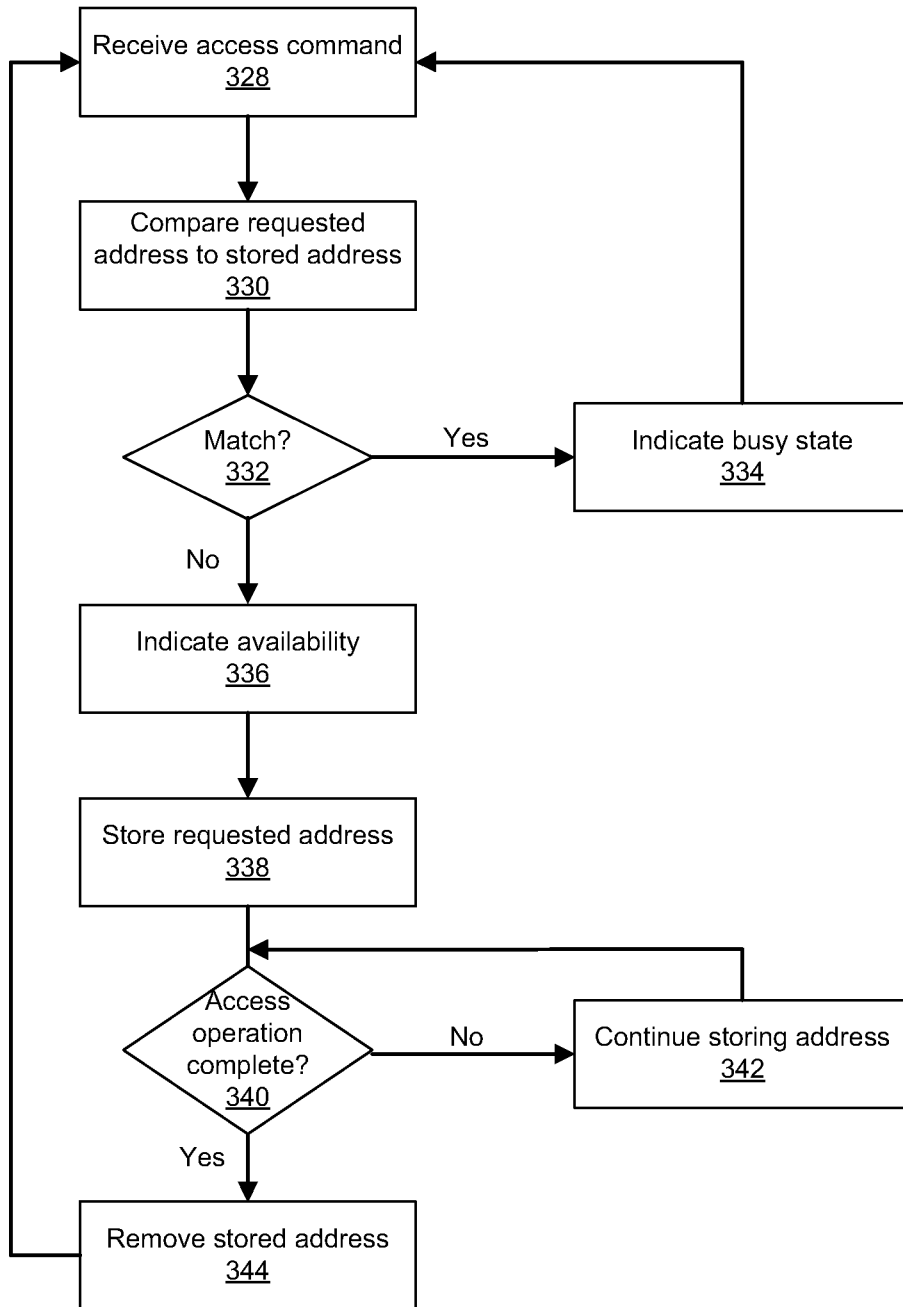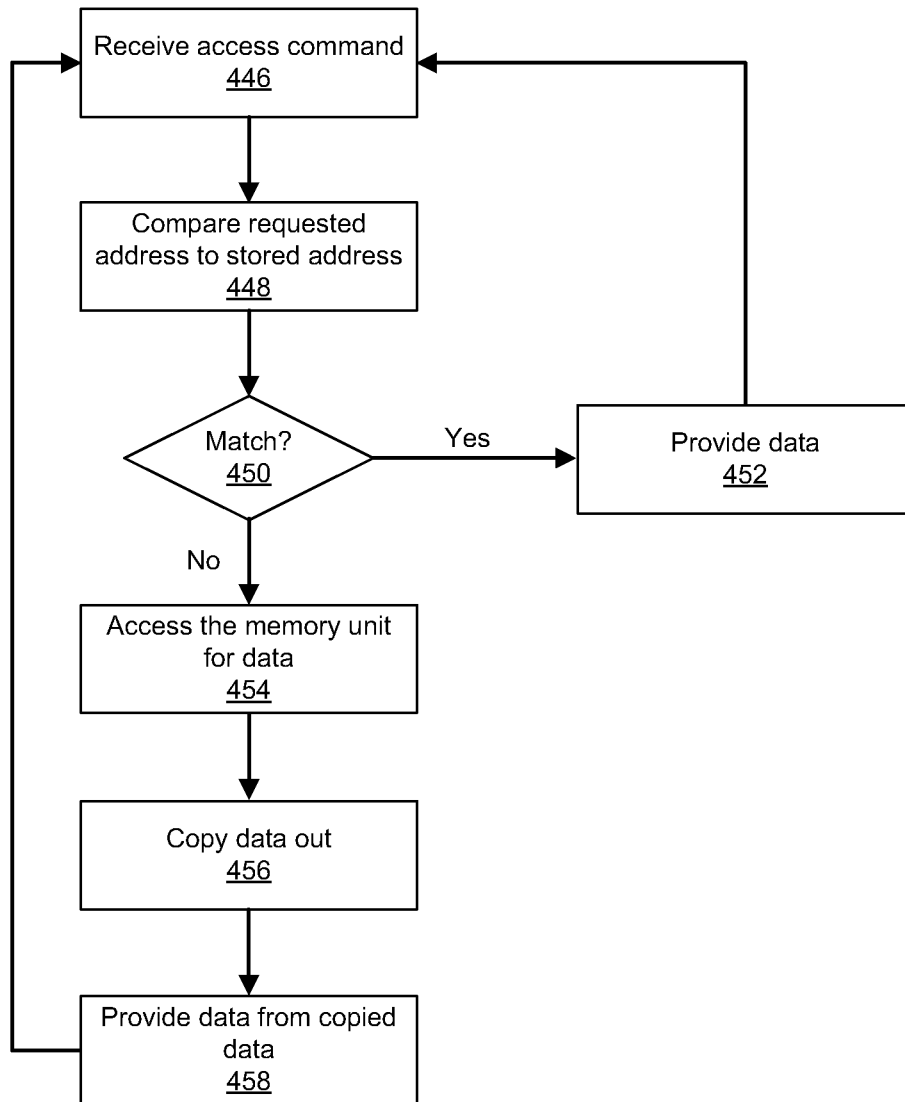
100

Fig. 1
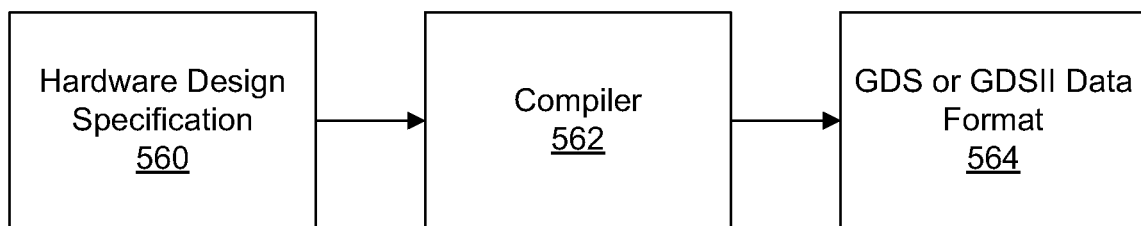
200

Fig. 2

Fig. 3

```
                    ┌──────────────────────┐
              ┌────▶│ Receive access command│◀────┐
              │     │         446            │     │
              │     └──────────┬─────────────┘     │
              │                │                   │
              │                ▼                   │
              │     ┌──────────────────────┐       │
              │     │  Compare requested    │       │
              │     │ address to stored addr│       │
              │     │         448            │       │
              │     └──────────┬─────────────┘       │
              │                │                     │
              │                ▼                     │
              │            ╱────────╲      Yes   ┌──────────────────┐
              │           ╱  Match?  ╲──────────▶│  Provide data    │
              │           ╲   450    ╱           │      452         │
              │            ╲────────╱            └──────────────────┘
              │                │
              │               No
              │                ▼
              │     ┌──────────────────────┐
              │     │  Access the memory unit│
              │     │       for data         │
              │     │         454            │
              │     └──────────┬─────────────┘
              │                │
              │                ▼
              │     ┌──────────────────────┐
              │     │    Copy data out       │
              │     │         456            │
              │     └──────────┬─────────────┘
              │                │
              │                ▼
              │     ┌──────────────────────┐
              └─────│ Provide data from copied│
                    │         data            │
                    │         458            │
                    └──────────────────────┘
```

Fig. 4

5/5

Hardware Design
Specification
560
→
Compiler
562
→
GDS or GDSII Data
Format
564

Fig. 5

INTERNATIONAL SEARCH REPORT

A. CLASSIFICATION OF SUBJECT MATTER
INV. G11C15/00   G06F12/08

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G06F G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 749 087 A (HOOVER RUSSELL D [US] ET AL) 5 May 1998 (1998-05-05) column 2, line 21 - column 5, line 29; figures 1a,2,3,5	1,2,4-6, 9,11-13, 15-17
X	US 5 887 146 A (BAXTER WILLIAM F [US] ET AL) 23 March 1999 (1999-03-23) figures 2,3,9,10,32,38 column 8, lines 40-55 column 12, lines 26-44 column 23, line 45 - column 28, line 13 column 29, line 64 - column 32, line 14	1,12
X	WO 99/26139 A (UNITED TECHNOLOGIES CORP [US]) 27 May 1999 (1999-05-27) page 10, line 8 - page 12, line 16; figures 1,2	1,12

-/--

| X | Further documents are listed in the continuation of Box C. | | X | See patent family annex. |

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 April 2009	27/04/2009

| Name and mailing address of the ISA/
European Patent Office, P.B. 5818 Patentlaan 2
NL – 2280 HV Rijswijk
Tel. (+31–70) 340–2040,
Fax: (+31–70) 340–3016 | Authorized officer

Stocken, Christian |

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 696 937 A (WHITE THEODORE CURT [US] ET AL) 9 December 1997 (1997-12-09) figures 1-3,5,13 column 4, lines 25-43 column 6, line 29 - column 9, line 55	1,12
X	US 4 750 154 A (LEFSKY BRIAN [US] ET AL) 7 June 1988 (1988-06-07) column 1, line 63 - column 5, line 46; figures 1,2	1,12

Patent document cited in search report		Publication date	Patent family member(s)		Publication date
US 5749087	A	05-05-1998	NONE		
US 5887146	A	23-03-1999	US	6026461 A	15-02-2000
WO 9926139	A	27-05-1999	CA	2309820 A1	27-05-1999
			EP	1029277 A1	23-08-2000
			US	6353873 B1	05-03-2002
			US	6473846 B1	29-10-2002
			US	6226710 B1	01-05-2001
US 5696937	A	09-12-1997	NONE		
US 4750154	A	07-06-1988	NONE		