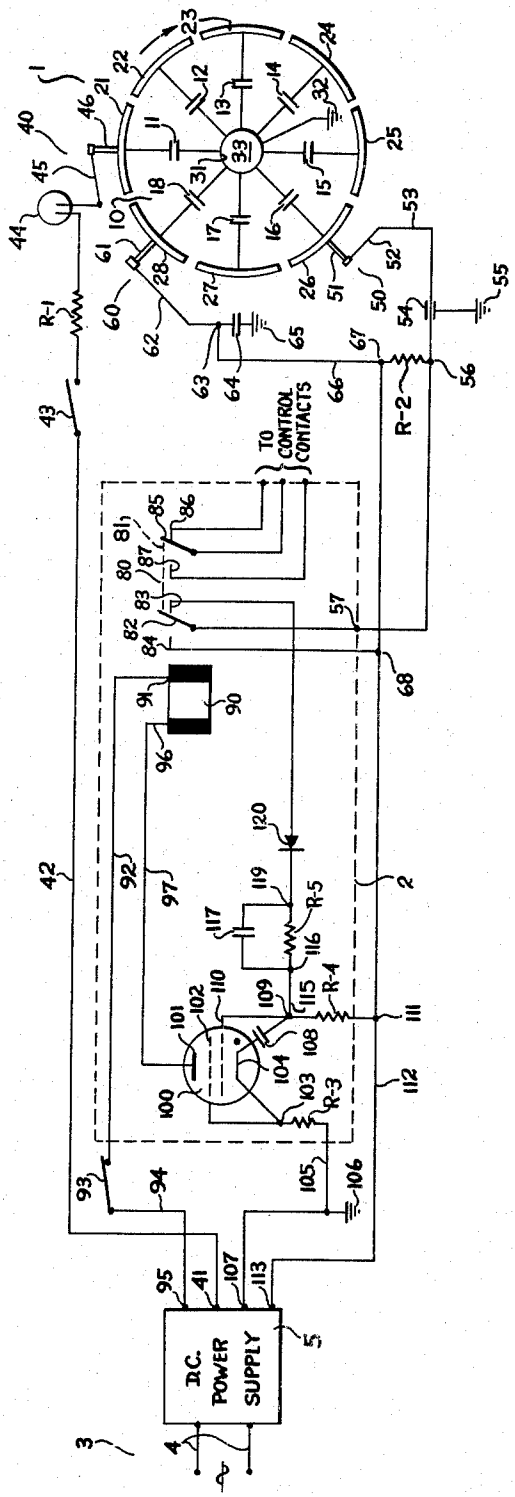
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CAPACITOR MEMORY DEVICE

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CAPACITOR MEMORY DEVICE

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This invention relates to a control apparatus and particularly to a means for receiving a control order at one time and delaying that order until the apparatus being controlled is in the proper condition for execution of the control order.

In a manufacturing process there may be a need for inspection of a product at one point in that process which, as a result of the inspection, will be later acted upon in a particular manner. For example, the product may be graded at one point and, as a result of the grade given, be rejected or sorted at another point in the process. A control system for receiving a grade or other information is required that will hold this information for a period of time which corresponds with the movement of the product and transmits the control information to actuate the necessary elements to continue the processing of the product.

In the operation of a lumber mill such a control is used to receive a grading signal given by a grader and hold this signal until the board which has been graded is in a position to be conveyed to a bin or other storage area for receiving lumber of that grade.

In the past a mechanical memory wheel, such as that disclosed in the U.S. Patent to Farrow No. 2,309,343 issued January 26, 1943, has been used to receive a signal at one time by actuating a pin in the memory wheel, rotating the wheel at a speed to correspond with the movement of the work piece and then actuating a control switch by the actuating pin and thus transmitting the signal to the apparatus controlling the work piece. This and other similar mechanical memory devices have the inherent disadvantages of unreliability due to dirt, wear, and destruction of parts.

It is an object of this invention to provide a simple, reliable, electrical memory control apparatus that is not adversely affected by dirt, moisture, and wear and is economical to construct and is effective in operation.

A further object of this invention is to provide a memory control apparatus which utilizes capacitors to receive a control order at one point in time and to discharge that control order at a later point in time to actuate a control system.

A further object of this invention is to provide a control means which, when it is actuated by the discharge of a memory capacitor, provides a reverse polarity electrical charge to the memory capacitor to restore it to its normal condition.

A still further object of this invention is to provide a capacitor memory control system which has means to prevent erroneous control charges from being placed on the capacitors and also prevents leakage discharge from correctly charged capacitors.

These and other features, objects, and advantages of the invention will become more fully evident from the following description thereof by reference to the accompanying drawing. Various changes may be made, however, in the construction and arrangement of parts in the apparatus and certain features may be used without the use of other features. All such modifications are intended to be within the scope of the appended claims.

The figure is a schematic diagram of the electric circuit, including the memory apparatus and the control means which it operates.

The figure discloses a typical utilization for the memory apparatus which includes a memory unit **1**, a control unit **2** shown by the dash lines, a power supply **3**, which consists of alternating current power leads **4** and a direct current power supply **5**. The memory unit **1** consists of a memory disk element **10**, which is divided into several segments, each segment including a capacitor. As shown there are eight segments in the memory disk containing capacitors **11** through **18**, which at one side make contact with segment contact areas **21** through **28** and at the other side make contact with interior ring **31**. Each segment is electrically insulated from the adjacent segments and the interior ring is grounded by means of ground **32**. The disk element **10** is supported by means of axle **33** and rotated in the direction shown by the arrow by means of a drive means (not shown), which drives the disk element at a speed to correspond with the apparatus being controlled by the memory unit.

As shown in the figure, a write or command element **40** is mounted so that it makes contact with the memory disk segment contact areas individually as the disk is rotated. The write or command circuit begins at the direct current power supply memory disk terminal **41**, is continued by write lead **42** to command or write switch **43**, which is a normally open switch, and from it through resistor R–1 to neon bulb **44**. The purpose for providing neon bulb **44** is to prevent low voltage transient current surges from placing an erroneous positive command charge on the memory capacitors and also to prevent the discharge back through the write circuit of a correctly charged capacitor. Since the neon bulb requires a minimum voltage across it to conduct current, it acts as a block against transient current flow through the write circuit which is below the neon bulb's conducting voltage. The same feature prevents discharge of a charged capacitor through the write circuit due to a faulty command switch, poor insulation, or dampness, since none of these conditions would impose a sufficiently high voltage across the neon bulb to cause it to conduct. The write circuit continues from the neon bulb **44** to the write brush support spring **45**, which supports the write brush contact **46** in order to insure contact between the memory disk element segment contact areas and the write brush contact **46**.

The read element **50** consists of a read brush **51**, which is supported by a read brush support **52**. The read circuit includes read brush **51** and read lead **53**, which lead is shielded to minimize the interference from transient current surges and the shielding material is connected with a shield connection **54** to shield ground **55**. The read circuit continues from the shield connection **54** past bias junction **56** to control unit read junction **57**.

A third element, the erase element **60**, is also in contact with the memory disk contact areas **21** through **28**. The erase element comprises an erase brush **61** which is supported by an erase brush support **62**. The erase element circuit begins at the erase brush **61**, continues to junction **63** to one contact of erase capacitor **64**, which by means of the other contact is connected to erase ground **65**. Continuing from junction **63** on erase lead **66**, the erase circuit includes junction **67** which connects stabilizing resistor R–2 to the read lead **53** at junction **56**. Continuing from junction **67** the erase circuit is connected at control unit erase junction **68** to the control unit **2**.

The control unit is represented by the area within the dashed lines **2** and comprises a control relay element **80** and a thyratron element **100**. The control relay element **80** consists of a control switch arm yoke **81**, which is connected mechanically to the disk switch arm **82**, which in the normal position makes contact with normal disk con-

tact 83 and when the control relay element 80 is energized, the disk switch arm 82 is shifted to the lefthand position making contact with the energized disk contact 84. Also connected to the control switch arm yoke 81 is control switch arm 85 which, in the normal position—the righthand position, makes contact with normal control contact 86 and in the lefthand position, or energized position, makes contact with the energized control contact 87. The control relay element 80 becomes energized when the relay coil 90 has a completed circuit through relay coil terminal 91 through coil lead 92 through normally closed cancel switch 93 to the power lead 94, which is connected to the D.C. power supply terminal 95. The other side of the relay coil 90 completes the circuit through the relay coil 90 through relay coil terminal 96 to anode lead 97.

The thyratron element 100 is a gas-filled tube comprising an anode 101 which is connected to the control relay coil 95 through anode lead 97, a shield grid 102 which through junction 103 is connected with cathode 104. The cathode 104 is also connected through cathode resistor R–3 to cathode lead 105 to a cathode ground 106 and in turn to a D.C. cathode terminal 107. The other end of cathode 104 is connected to cathode capacitor 108, which capacitor is connected through junction 109 to the final element making up the thyratron element 100, the thyratron control grid 110. The control grid 110 is connected through control grid bias resistor R–4 to junction 111 to bias lead 112 to the D.C. bias terminal 113. At the control grid junction 109 control grid lead 115 continues through junction 116 to a control grid capacitor 117 and through a control grid resistor R–5 to the junction 119, which is connected to the control grid rectifier 120, which in turn is connected to the control relay normal disk contact 83.

Having described the individual connections and individual circuits of the units which make up each element in the memory apparatus, the function and interrelation between the various elements will now be disclosed. As a beginning point the memory disk segment contact areas 21 through 28 have normal negative charge such that the capacitors 11 through 18 are charged negatively between the segment contact areas 21 to 28 and the ring ground 32. When an operator closes the command or write switch 43 completing the circuit between the positively charged power supply terminal 41 to the write in brush contact 46, the segment contact area loses its negative charge and becomes positively charged. For example, in the figure, the contact area 21 is in register with write in brush contact 46, putting a positive charge on capacitor 11. Through the disk axle 33 the memory disk element is rotated in the direction of the arrow at a speed in relation to the apparatus which is being controlled by the control unit 2 such that when the segment contact area 21 is in the position to make contact with the read brush 51, the apparatus being controlled by the control unit 2 will be in the position desired for the next step in the controlled operation. Once the segment contact area 21 makes contact with the read brush 51, the capacitor 11 is discharged through the read brush 51 through the read lead 53 to the control unit read contact junction 57 up through the control unit relay disk switch arm 82 connecting with normal disk contact 83, completing the circuit through rectifier 120 and control grid lead 115 to the thyratron control grid 110, which causes the ionization of the control thyratron 100. Once ionized, the control thyratron 100 completes the circuit from the cathode 104 to the anode 101 to energize the control relay coil 90, which pulls the control switch arm yoke 81 from the righthand position to the lefthand position so that switch arm 82 breaks contact with normal disk contact 83 making contact with energized disk contact 84 which, in turn, is connected at junction 68 with the bias lead 112. The read brush 51 now completes the circuit through the control relay 80 to the bias terminal 113 of the D.C. power supply, which places a negative charge upon the capacitor 11. Thus, the memory disk element 10 is back in the starting condition with a negatively charged capacitor ready to receive another write in charge.

To insure that the memory disk element retains a negative charge on the capacitors 11 through 18 when they have not been positively charged by means of the read in circuit there is provided an erase element 60, which continuously connects the D.C. power supply bias terminal 113 through the bias lead 112 to the erase brush 61, making contact with the segment contact areas 21 through 28 prior to the contact areas making contact with the write or command circuit 40.

The control unit 2 becomes de-energized when the cancel switch 93 is opened, which would generally occur when the apparatus being controlled by means of control contacts 86 and 87 has completed its cycle of operation. Once de-energized, the control relay coil 91 permits the control switch arm yoke 81 to resume the normal righthand position, which permits discharging memory disk capacitors to discharge through the control unit 2.

Thus, with the circuit and elements herein disclosed it is possible for a capacitor memory device to carry an operating signal until the apparatus being controlled is in the desired position and such a charged capacitor can discharge through a control unit to initiate the desired control operation to the apparatus being controlled. By incorporating the capacitor read element circuit into the control relay it is possible to insure that the memory capacitors are restored to a negatively charged condition and in this way prevent the possibility of false positive surges from being transmitted from the memory disk to the control unit.

Although there is shown only one memory disk of eight segments, it is possible to increase the number of disks and the number of segments per disk can be varied as desired to increase or decrease the number of possible control orders which can be handled.

Having now described my invention and in what manner the same may be used, what I claim as new and desire to protect by Letters Patent is:

1. A memory apparatus comprising in combination:
write means,
read means,
capacitor means mounted on positioning means for bringing said capacitor means into contact with said read means and said write means in succession,
said write means adapted to place an electrical charge upon said capacitor means when said capacitor means is in contact with said write means,
said capacitor means adapted to discharge said electrical charge through said read means when said read means is in contact with said capacitor means,
control means including relay means,
said control means responsive to said discharge of said capacitor means through said read means to energize said relay means,
said relay means responsive to said energization of said relay means to impress a second electrical charge on said capacitor means.

2. The memory apparatus of claim 1 wherein:
said second electrical charge is of a reverse polarity from said electrical charge placed on said capacitor by said write means.

3. The memory apparatus of claim 1 wherein:
said positioning means operates at a speed in relation to the speed of a means being controlled by said control means.

4. The memory apparatus of claim 1 wherein:
said write means is in series with a conductive means adapted to be conductive responsive to the voltage across said conductive means of a predetermined maximum and to be nonconductive responsive to

said voltage of below said predetermined maximum.

5. The memory apparatus of claim 1 including:

an erase means positioned to contact said capacitor means after said capacitor means has contacted said read means but before said capacitor means contacts said write means with an electrical charge opposite in polarity to said charge placed on said capacitor means by said write means.

6. A memory apparatus comprising in combination:

write means,

read means,

capacitor means mounted on positioning means for bringing said capacitor means into contact with said write means and said read means in succession,

said write means adapted to place a first electrical charge on said capacitor means when said capacitor means is in contact with said write means,

said capacitor means adapted to discharge said first charge through said read means when said read means is in contact with said capacitor means,

control means including relay means,

said control means responsive to said discharge of said capacitor means through said read means to energize said relay means,

said relay means responsive to said energization of said relay means to impress a second electrical charge on said capacitor means,

said positioning means operating at a speed in relation to the speed of a means being controlled by said control means.

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IRVING L. SRAGOW, *Primary Examiner.*