EP.0032154

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 3: H03K 23/30, 3/286	A1	(11) International Publication Number: WO 81/00332
		(43) International Publication Date: 5 February 1981 (05.02.81)

(21) International Application Number: PCT/US80/00895

(22) International Filing Date: 7 July 1980 (07.07.80)

(31) Priority Application Number: 059,008

(32) Priority Date: 19 July 1979 (19.07.79)

(33) Priority Country: US

(71) Applicant: MOTOROLA, INC. [US/US]; 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

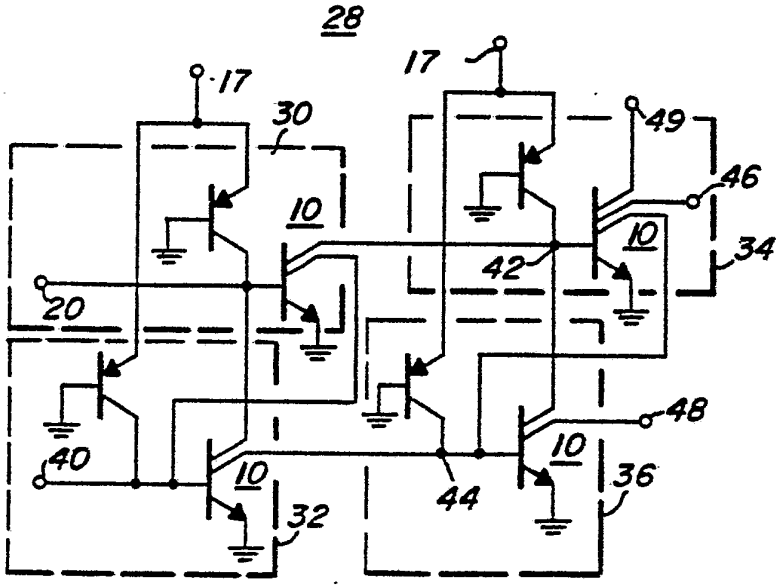
(72) Inventor: DAVIS, Walter, Lee; 142 Southwest 52nd Avenue, Plantation, FL 33317 (US).

(74) Agents: GILLMAN, James, William et al.; Motorola, Inc., Patent Department, 1303 East Algonquin Road, Schaumburg, IL 60196 (US).

(81) Designated States: AT (European patent), BR, CH (European patent), DE (European patent), FR (European patent), GB (European patent), JP, NL (European patent), SE (European patent).

Published
With international search report
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments

(54) Title: BISTABLE CIRCUIT AND SHIFT REGISTER USING INTEGRATED INJECTION LOGIC



(57) Abstract

A bistable circuit and shift register requiring less chip area and with greatly reduced current drain is realized with I2L logic gates. Each cell (28) of the register includes only four logic gates (10), connected as two binary R-S flip-flops, each gate consisting of a pair of merged PNP and NPN transistors. The two flip-flops are alternately energized by switching the current into the gate injectors in accordance with the phase of the clock signal. The use of fewer gates with simplified interconnections contribute to reduce chip area and current drain.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**KP**	Democratic People's Republic of Korea
AU	Australia	**LI**	Liechtenstein
BR	Brazil	**LU**	Luxembourg
CF	Central African Republic	**MC**	Monaco
CG	Congo	**MG**	Madagascar
CH	Switzerland	**MW**	Malawi
CM	Cameroon	**NL**	Netherlands
DE	Germany, Federal Republic of	**NO**	Norway
DK	Denmark	**RO**	Romania
FI	Finland	**SE**	Sweden
FR	France	**SN**	Senegal
GA	Gabon	**SU**	Soviet Union
GB	United Kingdom	**TD**	Chad
HU	Hungary	**TG**	Togo
JP	Japan	**US**	United States of America

BISTABLE CIRCUIT AND SHIFT REGISTER USING INTEGRATED INJECTION LOGIC

Background of the Invention

This invention relates to the field of bistable integrated circuits and, in particular, to the design of a shift register using bistable circuits on an IC chip.

A shift register is a binary device having a number of storage elements or cells, the number depending upon the particular application, and wherein data may be stored in the cells sequentially. That is, information in the form of voltages representing two logic levels, high (one) and low (zero), is stored in the first cell, shifted to the second cell by an applied clock or shift signal as another bit of data is entered into the first cell. A clock signal shifts all data bits down the register sequentially until, typically, the bits of data are "lost" from the last cell of the register. Since a particular register application may require many cells (100 is not unusual) and each cell may contain a number of gates, each comprising several transistors, the area required for this large number of transistors and the circuit interconnections therefor may be excessive. The cost of an IC chip is usually a direct function of its size.

Current drain is also an important consideration, particularly in very small, battery-powered devices such as personal pagers which may be turned on for long periods of time. Current drain per register cell is a function of both

the number of gates and the number of propagation delays. Therefore, reducing either the number of gates or the number of delays or both will reduce the current drain correspondingly.

There are two main types of shift registers in general use; i.e., those using clock flip-flop storage elements and those using master-slave memory techniques. In the former type, the elements are typically "D" flip-flops which have Clock and Data inputs and two outputs Q and $\overline{Q}$. When the logic level at the Clock input changes from a logic zero level to a logic one level, the flip-flop transfers the logic level on the Data input to the Q output and holds that level until the Clock input is again driven from a zero to a one level. When implemented with I^2L logic, the basic "D" flip-flop element or cell, with no set or reset inputs requires seven I^2L gates. In addition to the gate count, another important characteristic of the D flip-flop is that it has three propagation delays between the time the Clock input goes to a one level and the time the Q output reaches the proper value. The Clock input must remain high during this period. In I^2L logic, the propagation delay of a gate is inversely proportional to the current drain of the gate over a wide operating range. It can be shown that the current drain of the flip-flop, operating at a clock frequency f_c, is $42Kf_c$ where K is a constant determined by the fabrication method.

The master-slave configuration, as commonly implemented, requires two memory elements; e.g., R-S flip-flops, per cell with gates controlled by the clock signal and interconnected so that during one phase of the clock, information at the Data input is fed to the "master" element with the "slave" element disconnected from the master. During the second clock phase, the master element is disconnected from the data input and the slave element is coupled to the master output to receive the information stored therein. In an I^2L implementation of this arrangement, ten gates are

required and there are two propagation delays per clock phase. The current drain of this type of shift register at clock frequency f_c is therefore $40Kf_c$. With a gate increase of over 40% and a current drain reduction of only 5%, it may easily be seen why the latter device is generally less desirable than the former, though both types are costly of chip area and current.

Summary of the Invention

It is therefore an object of this invention to provide a bistable circuit and an I^2L shift register for IC implementation with fewer gates per cell and with greatly reduced power requirements.

This object and others are obtained in a cell for a shift register which includes a multiplicity of cascade-connected storage elements or cells and a clock which provides two clock signals, one the complement of the other. Each cell includes four NAND logic gates connected as two binary R-S flip-flops. The two flip-flops are alternately energized by the clock signals which are used to switch the current into the gate injectors. Since only two gates per cell are receiving injection current at one time, and there is only one propagation delay per phase of the clock signal, the current requirement is only one tenth that of prior shift registers using I^2L logic.

Brief Description of the Drawing

Fig. 1 is a schematic diagram of a basic I^2L gate.

Fig. 2 shows the structure of an I^2L gate.

Fig. 3 is a schematic diagram of the gate of Fig. 1 with multiple input signals on the single input.

Fig. 4 is a logic representation of Fig. 3.

Fig. 5 is a schematic diagram of a bistable cell in accordance with the present invention.

Fig. 6 is a diagram of a portion of a shift register using cells as in Fig. 5, and including a possible clock signal supply circuit.

Detailed Description of a Preferred Embodiment

Since the present invention is based on the characteristics of the basic I^2L (integrated injector logic) gate, these characteristics and the gate structure will be described first for better understanding of the circuit of the invention.

Figs. 1 and 2, showing the schematic diagram and structural diagram of one gate, will be considered together. The gate may be considered as a merged pair of NPN 10 and PNP 12 transistors, in which the base 14 of the PNP transistor is common with the emitter 14 of the NPN transistor and both are coupled to ground. The collector 16 of the PNP 12 is also the base 16 of the NPN 10. A current applied via terminal 17 to the emitter 18 of the PNP 12 causes that transistor to act as a current source for the NPN 10, supplying current to the base 16 of the NPN. Coupled to the base 16 is a control terminal 20. If terminal 20 is grounded (logic zero input), the current being supplied by the PNP 12 is diverted to ground and the NPN 10 is then left in a non-conducting state in which the collectors 22, 24 and 26 are floating; i.e., have no current sinking capability.

If the base 16 of the NPN 10 is floating; i.e., a logic one input, the current supplied by the PNP 12 flows into the base 16 of the NPN 10, which then becomes a current sink for any circuit connected to the NPN collectors 22, 24 or 26.

In Fig. 3, the gate of Fig. 1 is shown with the capability of coupling multiple devices to the base/collector 16. If all of the input devices are non-conducting (logic level one outputs) the input voltage at the control terminal 20 rises to a one level and the outputs 22, 24 and 26 are

driven to a zero level. If any of the input devices coupled to the control terminal 20 are conducting, the base/collector 16 is driven to a logic zero level and the outputs 22, 24 and 26 rise to a one level.

The gate of Fig. 3 may be represented logically as an inverting AND or NAND gate as shown in Fig. 4.

Fig. 5 is a schematic diagram of a bistable circuit in accordance with the invention and including four NAND gates 30, 32, 34 and 36, each in itself comparable to the NAND gate of Fig. 3. Each cell of the shift register would be represented by the circuit of Fig. 5. In a cell, gates 30 and 32 form one memory flipflop element and gates 34 and 36 form a second memory element. In operation, the two memory elements are alternately energized during the two phases of the clock signal by switching the current into the PNP devices of the gate (the gate injectors) in accordance with the clock signal. That is, the clock signal waveform is a square wave and when the clock level is high, injector current is fed to gates 30 and 32 while gates 34 and 36 have greatly reduced injector currents. Then, when the clock signal switches low, the injector current is switched to gates 34 and 36 and gates 30 and 32 receive greatly reduced injector currents. The bases of the NPN's 10 of the gates 30 and 32 are driven by an input signal and its inverse respectively as indicated by Data input terminal 20 and $\overline{\text{Data}}$ input 40. When the clock signal is high the outputs of gates 30 and 32 are driven to logic levels complementary to the input levels. Thus, if the input level at terminal 20 is a logic one, the collectors of the NPN 10 of gate 30 are driven to a zero state in which they conduct current, while the collectors of NPN 10 of gate 32 are driven to a one state in which they are non-conducting. Thus, input terminal 42 of gate 34 is quickly driven to a voltage level near ground while input terminal 44 of gate 36 is charged toward a logic one level by the slight injector current flowing in NPN 10 of gate 36.

When the clock signal changes to the second phase, i.e., a one level on $\overline{\text{clock}}$ terminal 17B, full injection current is applied to gates 34 and 36 and terminals 42 and 44 are charged toward a logic one level. Whichever of the terminals 42 and 44 reaches a one level first will quickly impose a zero level on the other terminal due to the interconnection of gates 34 and 36. In the above case, where terminal 44 was initially charged to a voltage above ground during the first phase of the clock, terminal 44 will be charged to a one level before terminal 42 during the second phase of the clock, and terminal 42 will quickly be forced to a zero level with terminal 44 remaining at the one level. The information placed on terminals 42 and 44 during phase one of the clock has been retained during the clock transition to phase two and the output terminals 46 and 48 are now "pre-charged" to logic levels corresponding to the complements of the levels on terminals 42 and 44. Thus, in the above example, terminal 48 is held at ground level by the one level on terminal 44 while terminal 46 is charged toward a logic one level. Note that after the clock transition from first phase to second phase, the information fed to the input terminal 20 now appears at the output terminal 46 and the collectors of the NPN 10 of gate 34 are off or in the one level. Naturally, all logic levels in the above example would be inverted if the original input level at terminal 20 had been zero.

On the next clock transition from the second phase to the first phase, gates 30 and 32 are again energized by the application of injector current and gates 34 and 36 are switched to the low current mode. New information is then fed into the first memory element of the cell and the cell (not shown) coupled to terminals 46 and 48 will shift in the data from the second memory element (gates 34 and 36) because of the pre-charged conditions on terminals 46 and 48. The signal appearing on the collectors of the NPN 10 of

gate 34 also appears on a cell output terminal 49, and may be coupled to any desired device or circuitry.

By interactively connecting cells in a chain as illustrated in Fig. 6, a shift register can be constructed with only four gates required per stage. In the new structure, the power drain of each stage is considerably reduced for several reasons. First, only two gates per cell are receiving injection at any one time and, secondly, this new array has only one qate propagation delay per phase of the clock. Since the period of the clock (t_p) is one half the clock frequency (f_c), $t_p = K/I$ where K is the aforementioned constant determined by the fabrication process, and I_g is the current required by one gate. Thus, I_g equals $2Kf_c$, and the current required for one cell (I_c) is $2(I_g)$ or $4Kf_c$. As mentioned hereinabove the prior art embodiments of I^2L shift register cells have required at least ten times this current drain.

Fig. 6 also includes a schematic diagram of a differential amplifier 50 having a square wave clock signal input to a terminal 52. As is known, the signals on the collectors of the differential amplifier transistors would then be C and $\overline{C}$, these complementary clock signals being coupled to the terminals 17A, 17B of each cell 28.

It is to be noted that the circuit described hereinabove is much simpler to lay out in integrated circuit form since the clock signals C and $\overline{C}$ are routed through the injector supply lines and no separate clock lines are required to be routed through the IC. With fewer gates required per shift register cell and simpler interconnections required, the cell of the invention is considerably smaller and therefore cheaper to construct than any other known shift register cell. It is also to be noted that the cell of Fig. 5 may have application in other circuits besides the shift register.

Thus, there has been shown and described a circuit for an I^2L bistable cell or shift register cell which requires

considerably less area on an integrated circuit chip and considerably less current. It will be obvious that other embodiments of the invention could be implemented using other logic variations equivalent to the embodiment shown herein, and it is intended to cover all such modifications and variations as fall within the spirit and scope of the appended claims.

Claims

1. A shift register comprising in combination:

first and second input means, the second input means coupled to the first input means and including inverter means for providing a signal which is the logical complement of the signal received at the first input means;

a plurality of cascade-connected cells, each cell having at least two inputs and at least three outputs and comprising four NAND gates, each gate having at least three inputs and at least two outputs;

the first NAND gate having a first input coupled to the first input means, the second NAND gate having a first input coupled to the second input means and a second input coupled to a first output of the first NAND gate and having a first output coupled to a second input of the first NAND gate;

the third NAND gate having a first input coupled to a second output of the first NAND gate and having a first output coupled to the first cell output means and the fourth NAND gate having a first input coupled to a second output of the second NAND gate and having a second input coupled to a second output of the third NAND gate, having a first output coupled to the second cell output means, and having a second output coupled to a second input of the third NAND gate;

the first and second cell outputs coupled to the respective inputs of the next cell in the register; and

means for energizing the first and second NAND gates alternately with the third and fourth NAND gates.

2. A shift register in accordance with claim 1 and wherein each NAND gate comprises a merged pair of NPN and PNP transistors, the base of PNP transistor being common with the emitter of the NPN transistor, and the collector of the PNP transistor being common with the base of the NPN transistor.

3. A shift register in accordance with claim 2 and wherein each PNP transistor is a current source when energized by the energizing means.

4. A shift register in accordance with claim 3 and wherein the energizing means is a clock supplying a square wave signal, and each pair of NAND gates is energized for one-half the clock signal period.

5. A shift register in accordance with claim 1 and wherein a third output of the third NAND gate is coupled to a third output means for providing external access to the cell output signal.

6. A shift register comprising in combination:

a series of cascade-connected cells, each for receiving, storing for a predetermined period of time, and outputting binary bits of information, each said cell including;

first and second input means wherein the signal at the second input means is the logical complement of the signal at the first input means;

first and second output means;

clock means for providing first and second clock signals wherein the second clock signal is the logical complement of the first clock signal;

first and second current sources coupled to receive the first clock signal;

first transistor means having a base coupled to the first current source and to the first input means, emitter coupled to ground, and having at least two output collectors;

second transistor means having a base coupled to the second current source and to the second input means and to a first collector of the first transistor means, an emitter coupled to ground, and having at least two output collectors, a first collector being coupled to the base of the first transistor means;

third and fourth current sources coupled to receive the second clock signal;

third transistor means having a base coupled to the third current source and to the second collector of the first transistor means, an emitter coupled to ground, and having at least two output collectors, the first collector being coupled to the first cell output means; and

fourth transistor means having a base coupled to the fourth current source, to the second collector of the second transistor means, and to the second collector of

the third transistor means, an emitter coupled to ground, and having at least two output collectors, a first collector coupled to the base of the third transistor means, and a second collector coupled to the second cell output means; and wherein the first and second output means of each cell are coupled to the first and second input means respectively of the subsequent cell in the register, except that the first and second output means of the last cell in the series are coupled to provide shift register output terminals.

7. A cell comprising four NAND gates and having two input means and at least two output means, the signal received by the first cell input means being the logical complement of the signal received by the second cell input means, the first NAND gate having a first input coupled to the first cell input means, the second NAND gate having a first input coupled to the second cell input means and a second input coupled to a first output of the first NAND gate and having a first output coupled to a second input of the first NAND gate, the third NAND gate having a first input coupled to a second output of the first NAND gate and having a first output coupled to the first output means and the fourth NAND gate having a first input coupled to a second output of the second NAND gate and having a second input coupled to a second output of the third NAND gate, having a first output coupled to the second output means, and having a second output coupled to a second input of the third NAND gate; and the first and second NAND gates being energized alternately with the third and fourth NAND gates.

8. A cell in accordance with claim 7 and wherein each NAND gate comprises a merged pair of NPN and PNP transistors, the base of PNP transistor being common with the emitter of the NPN transistor, and the collector of the PNP transistor being common with the base of the NPN transistor.

9. A cell in accordance with claim 8 and wherein each PNP transistor is a current source when energized by the energizing means.

10. A cell in accordance with claim 7 and wherein a third output of the third NAND gate is coupled to a third output means for providing external access to the cell output signal.

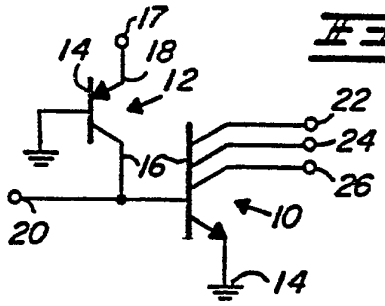


Fig.1

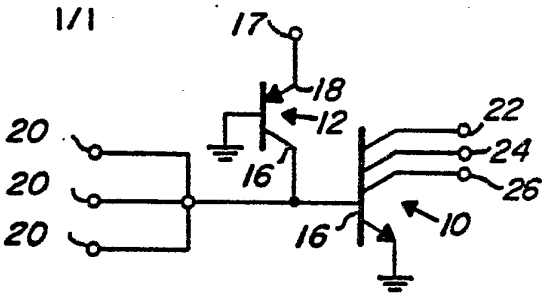


Fig.3

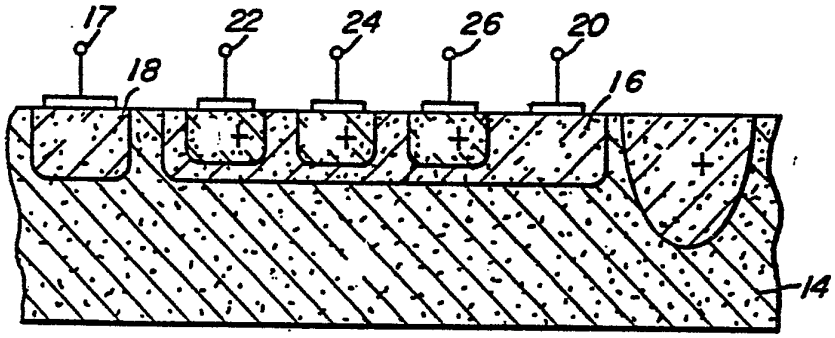


Fig.2

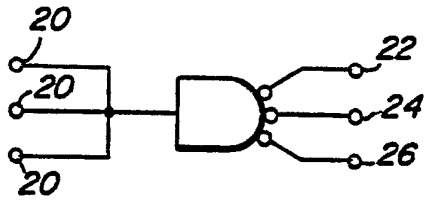


Fig.4

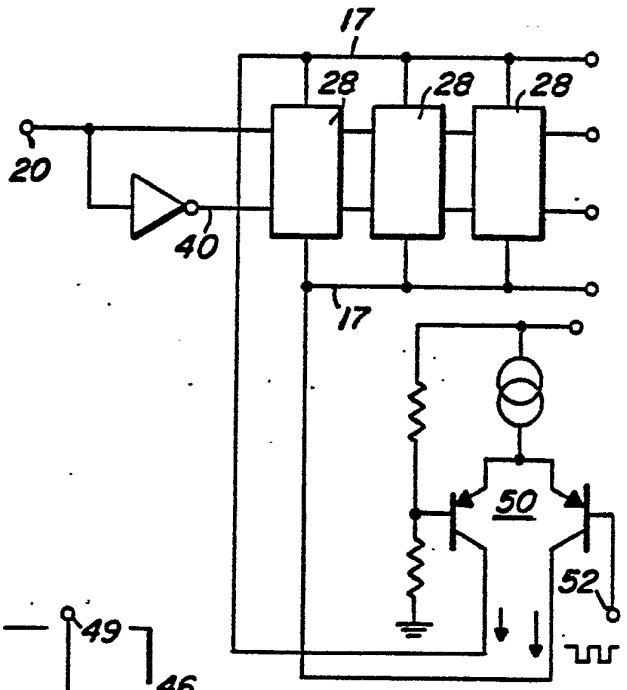


Fig.6

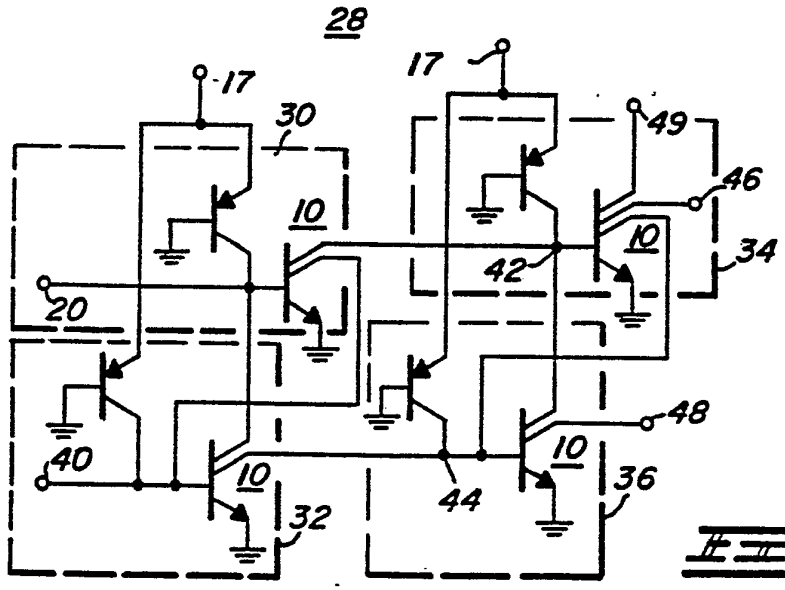


Fig.5

INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/ 00895

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. CL.[3] H03K 23/30; H03K 3/286

U.S. CL. 307/221R; 307/291

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	307/203, 215, 221R, 272A, 289, 291 357/92

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US, A, 4,150,392, Published 17 APRIL 1979, See Fig. 3, Nonaka.	1-10
X,P	US, A, 4,209,715, Published 24 JUNE 1980, See Figures 4-6, Aoki.	1-10
A	US, A, 4,099,263, Published 4 JULY 1978, See Figures 1-2, Scott.	
A	US, A, 4,156,154, Published 22 MAY 1979, See Figures 1-3,8,10,11-12 14,16, Iizuka.	
A	US, A, 3,655,999, Published 11 APRIL 1972, See Fig. 1, Wiedmann.	
A	US, A, 3,993,918, Published 23 NOVEMBER 1976, See Figures 12-13, Sinclair	
A	US, A, 4,056,736, Published 1 NOVEMBER 1977, Blatt.	
A	US, A, 4,160,173, Published 3 JULY 1979, Aoki.	
A,P	US, A, 4,197,470, Published 8 APRIL 1980, Banzhaf.	
X	DE,A1, 2,442,773, Published 18 MARCH 1976, See Fig. 1, Herrmann.	1-10

* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [2]
16 NOVEMBER 1980	11 DEC 1980
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	Larry A. Anagnos

Form PCT/ISA/210 (second sheet) (October 1977)