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DIGITAL TO ANALOG CONVERTER

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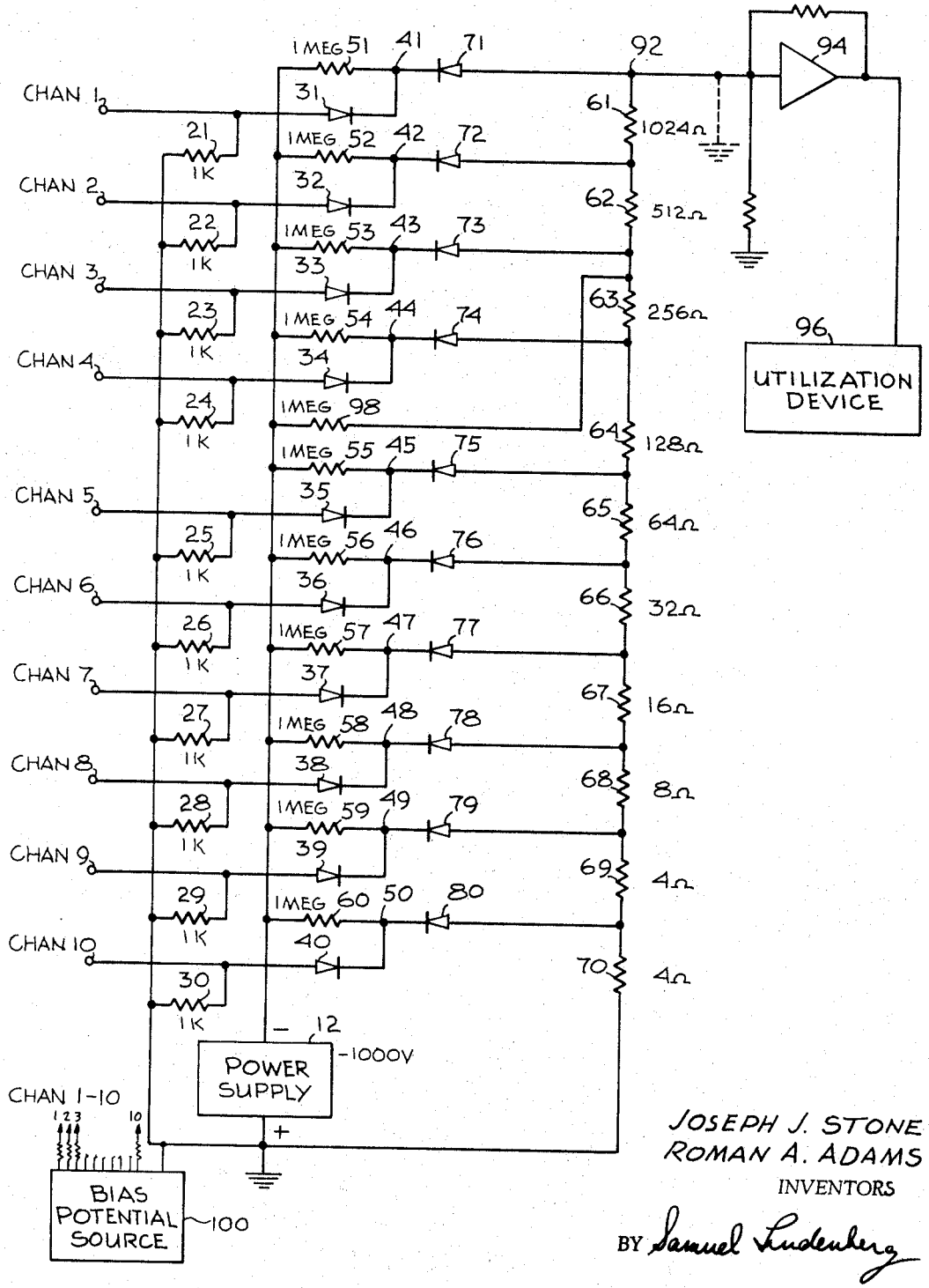

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DIGITAL TO ANALOG CONVERTER

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This invention relates to digital to analog converters and more particularly, to improvements therein.

An object of this invention is to provide a novel digital to analog converter circuit.

Another object of this invention is the provision of an accurate and stable digital to analog converter circuit.

Still another object of this invention is to provide an accurate and stable digital to analog converter which is relatively inexpensive.

These, and other objects of this invention, may be achieved by the provision of a circuit wherein a relatively stable power supply applies current to a plurality of gating networks. A resistive ladder network has tapping points therealong each of which is connected through a different one of the gating networks back to the power supply. One end of the resistive ladder is connected to the power supply and the other end to the summing point or junction of an operational amplifier. In the presence of an input signal to one of the gates, current is caused to flow through the ladder network in a manner such that the summing junction at one end of the ladder network receives current having an amplitude proportional to the tapping point on the ladder network connected to the gate which has received the input signal. A separate input terminal is provided for each digital signal and the summing junction receives an output current whose amplitude is established by the terminal to which the input signal is applied.

The novel features that are considered characteristic of this invention are set forth with particularity in the appended claims. The invention itself both as to its organization and method of operation, as well as additional objects and advantages thereof, will best be understood from the following description when read in connection with the accompanying drawings, in which the drawing is a circuit diagram of an embodiment of the invention.

Referring now to the drawing, which is a circuit diagram of an embodiment of the invention, it will be seen that provision is made for ten digital inputs respectively labeled Channel **1** through Channel **10**. A single power supply **12** is employed. It should be noted at this point that values of circuit components which were employed are shown on the drawing. These are shown by way of example, and are not to be construed as a limitation upon the invention.

Each input terminal from Channel **1** through Channel **10** is respectively connected through a load resistor respectively **21** through **30** to the positive end or ground side of the power supply **12**. Each of Channels **1** through **10** is also respectively connected through a diode respectively **31** to **40** to a junction point respectively **41** through **50**.

Each one of the junction points respectively **41** through **50** is connected through a separate bleeder resistor, respectively **51** through **60** to the negative terminal of the power supply **12**.

A ladder network is provided, comprising a series connected string of resistors respectively **61** through **70**. One end of the resistor ladder network is connected to the ground, or positive side, of the power supply **12**. The other end of the ladder network **92** is connected through a diode **71** to the junction point **41**. The junctions between the successive resistors in the series string are respectively connected by the respective diodes **72** through **80** to the respective junction points **42** through **50**. The top of the ladder network is also connected to a summing junction **92**. An operational amplifier **94** is connected to the summing junction. Its output is used to drive any desired utilization device **96**. Effectively, the resistive ladder is an input resistor for the operational amplifier.

It should be noted that the values of the resistors selected for the ladder network commencing with resistor **61** through resistor **69** are such that each succeeding resistor has a value one-half that of its preceding adjacent resistor. Thus, resistor **61** has a value of 1024 ohms and resistor **62** has a value of 512 ohms. Resistor **69** has a value of 4 ohms as does also resistor **70**. These values are chosen such that the value of current which will flow into the summing junction **92** will vary in a binary progression as the channel input associated therewith has a signal applied thereto. The ladder resistors, however, can have their values adjusted to provide any type of progression desired.

A trimming resistor **98** serves the function of trimming the current flow through the ladder network so that precise operation is obtained.

Initially assume that a slightly positive bias potential is applied to all channel input terminals (this need only exceed one volt), from bias potential source **100**. As a result, diodes **31** through **40** are biased conductive. There will then be a parallel current flow from the power supply through resistors **21** through **30**, through junction points **41** through **50**, through resistors **51** through **60** back to the power supply. This current through each path is substantially one milliampere in amplitude. The junction points are all sufficiently positive to bias off diodes **71** through **80** so that there is no current flow through the resistive ladder network.

Assume now that a digital signal is applied to one of the channel input terminals which is sufficiently negative (here, too, it need only exceed one volt negative) to bias off the one of the diodes connected to that channel input terminal. For example, assume that the negative input signal is applied to the channel two input. Diode **32** is biased off by the signal. This causes a switching of the current which flowed through diode **32** to a path which may be traced from the power supply through the one megohm resistor **52**, through junction **42** and through diode **72** to the tap on the resistive ladder network. Here there is a current division, part of the current returning to the power supply through the ladder network connected directly back to the power supply and the other part returning by way of the summing junction **92** in the input to the operational amplifier **94**.

As is well known, an operational amplifier operates in such a manner as to maintain the potential of its summing junction equal to zero. Thus, it may be described as being at a virtual ground potential. Current applied to a junction of the ladder network, such as the one between resistors **61** and **62** to which channel **2** input is

coupled, will divide between the actual ground and virtual ground (summing junction **92**) in proportion to the resistance values in each leg of the ladder network. In accordance with this invention, the ladder network is made an input resistor connecting to the summing junction of the operational amplifier.

Thus, a negative voltage signal applied to channel **1** causes one milliampere of current to flow into the summing point. A negative voltage signal applied to channel **2** causes one-half milliampere of current to flow into the summing point. A negative signal applied to channel **3** will result in one-quarter millampere of current being delivered to the summing point.

As each one of the channels in turn has a negative input signal applied thereto, the value of the current delivered at the summing point changes in accordance with progression. When a negative input signal is applied to channel **10**, the diode **40** is blocked and the current delivered to the summing point will have a value of $\frac{1}{512}$ milliamperes. The operational amplifier can then drive the utilization device **96** with an output signal which is an analog representation of the channel from which the digital signal was received.

The ladder resistors **61** through **70** can be adjusted for any type of progression, for instance, decimal. The polarity of the bleeder current can be reversed, along with the polarity of the switching diodes, and the direction of current can be reversed at the summing point to provide negative outputs. A combination of both polarities of bleeder currents can be used with the ladder extended from the summing point in the opposite direction for complementary operation. Analog inputs can also be handled where the bleeder resistance to the summing point from the input is adjusted for full scale analog voltage input, and of either polarity.

The arrangement for a digital to analog computer shown in the drawing provides a variation of weighting in the ratio of 512 to 1. The ladder network provides a means for obtaining an accurate current weighting. The accuracy of the entire system is associated with the stability and regulation of the power supply and the resistance accuracy of the bleeder and ladder network resistors. It is desirable to have a high ratio of bleeder resistance value to total ladder network resistance value. The circuit shown has been built and operates to convert digital inputs to corresponding current levels at the summing point at rates up to one megacycle.

There has accordingly been described and shown herein a novel, useful, accurate and relatively inexpensive analog to digital converter arrangement. It will be appreciated that, while the invention has been exemplified by showing ten channels of digital input being converted to a single analog output, fewer than, or more than, this number of channels may be handled without departing from the spirit and scope of this invention.

We claim:

1. A digital to analog converter circuit comprising an operational amplifier having an input summing junction, a ladder network connected to said input summing junction, said ladder network comprising a plurality of series connected resistors, a plurality of digital input terminals, a plurality of coupling means a different one of which couples a different one of said digital input terminals to a different one of the junctions between a different two of series connected resistors, each said coupling means including two serially connected, relatively oppositely poled diodes connected between a digital input terminal and a junction between two resistors, a first load resistor, and a current setting resistor, and a power supply having a first and second output terminal, means coupling each said first load resistor between a different digital input terminal and said first output terminal, and means coupling each said current setting resistor between each serially connected relatively oppositely poled diodes and said second output terminal, means for applying a signal to a predetermined one of said digital input terminals, and means within each of said coupling means responsive to the application of a signal to the digital input terminal coupled thereto for applying a predetermined current to the junction coupled thereby to cause a value of current to flow through said summing junction as determined by the resistance value of the series connected resistors on either side of the junction of resistors to which said predetermined current is applied.

2. A digital to anolog converter circuit comprising an operational amplifier having an input summing junction, a ladder network connected to said input summing junction, said ladder network comprising a plurality of series connected resistors, a plurality of digital input terminals, a plurality of coupling means a different one of which couples a different one of said digital input terminals to a different one of the junctions between a different two of said series connected resistors, means for applying a signal to a predetermined one of said digital input terminals, means within each of said coupling means for establishing a first current flow path which excludes the junction between two resistors to which said coupling means is coupled, and a second current flow path which includes said junction between said two resistors, means within each of said coupling means for establishing a predetermined current flow within said first current flow path, and means within each of said coupling means responsive to the application of a signal to the digital input coupled thereto for transferring said predetermined current flow to the second current path including the junction included therein to cause a value of current to flow through said summing junction as determined by the resistance value of the series connected resistors on either side of the junction of resistors to which said predetermined current is applied.

3. A digital to anolog converter network comprising a plurality of digital input terminals, an analog output terminal, a ladder network comprising a plurality of series connected resistors, there being as many resistors in said plurality as there are digital input terminals, a power supply having a pair of output terminals, means connecting one of said power supply output terminals to one end of said ladder network, summing junction means coupled to said one of said output terminals, means coupling the other end of said ladder network to said summing junction, a plurality of load resistors, a different load resistor being connected between each one of said input terminals and said one of said power supply output terminals, means coupling the junction between two adjacent resistors in said resistive ladder network to the other terminal of said power supply including first diode means connected in series with a resistance, and a separate, second diode means coupled between each input terminal and the junction between the first diode means and resistance connected to said power supply, the polarity of the coupling of the respective first and second diode means to one another being relatively opposite.

4. A digital to analog converter comprising a plurality of digital input terminals, an analog output terminal, a ladder network, a power supply having a first and second output terminal, means connecting said power supply first output terminal to one end of said ladder network, means connecting the other end of said ladder network to said analog output terminal, means coupling said analog output terminal to said power supply first output terminal, said ladder network comprising a plurality of separate resistors connected in series, there being as many resistors in said plurality as there are digital input terminals, each of said resistors being associated with a different one of said digital input terminals and having its value selected in accordance with the weighting of the analog output to be associated with the digital input terminal, means coupling each one of said digital input terminals to one end of the associated resistance in said ladder network, said means including a first diode means connected

in series with a second diode means, said series connected diode means being poled relatively oppositely to one another and connecting to each other at a junction, a different bleeder resistor connected between each junction and the second output terminal of said power supply, each said bleeder resistor having a resistance value which is large relative to the resistance value of said resistive ladder network, and a separate load resistor connected between each one of said input terminals and the first output terminal of said power supply.

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