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(54) Title: STACKING LAYERS WITH SUBSTRATES SUPPORTING MICROELECTRONIC DEVICES AND METHOD

(57) Abstract: A Neo layer (107, 285) is provided with at least one die (10) having a microelectronic device on an active surface (55) of the die (10). The dies (10) are supported on a support substrate (105, 300) that can be readily handled by machines in an automated manufacturing setting. Both of the die (10) and the substrate (105, 300) are encapsulated in a layer material to provide a distinctive Neo layer or Neo PEM. The different embodiments offer additional respective advantages of improved manufacturability. Further versatility is provided by enabling use of dies (10) from different sources including bare dies (10) and dies (10) that are already packaged in a Plastic Embedded Microcircuit (PEM), for example. The ongoing goal of providing a stackable array of Neo layers (107, 285) is still met.
STACKING LAYERS WITH SUBSTRATES SUPPORTING MICROELECTRONIC DEVICES AND METHOD

Cross Reference to Applications

This is a non-provisional Continuation-in-part patent application claiming the priority of US patent application Serial No. 09/770,864 filed January 26, 2001, entitled "A Stackable Microcircuit Layer Formed From a Plastic Encapsulated Microcircuit and Method of Making the Same" and a continuation application claiming priority of US provisional application Serial No. 60/302,306, filed July 02, 2001 entitled "Leadframe and Plastic Package Optimized for Stacking", both of which are incorporated herein by reference.

Background of the Invention

1. Field of the Invention

The instant invention relates generally to Neo layers and forming the same, and more specifically to Neo layers incorporating special structure so as to form a Neo PEM and the method of forming a Neo PEM.

2. Description of Prior Art and Related Information

In providing a system of micro-electronic devices, artisans of the past have developed a variety of conventional packages. The most common packages of which are cards or boards with a plurality of cards disposed thereon. The cards of the past typically extend vertically to some degree, but also extend lengthwise and therefore take up large areas on boards on which they are mounted. The lengthwise extension of the cards of the past is dependent upon the number and types of micro-electronic devices mounted on the card. For stability the past devices are generally kept low. This is because they are mounted on relatively thin substrates that become unstable if they extend too high. Furthermore, the length of the card must be increased as more devices are added. Therefore, the systems of devices of the past are deficient in providing a package that has a small lengthwise dimension on the supporting board. Simply stated, the systems of the past are deficient in providing the system in a small footprint since the overall area is a function of the length as well as the width of the card.
The assignee, Irvine Sensors, has developed a variety packages of vertically stacked devices including stacked layers containing bare silicon and stacked Neo chips. These packages have been successful, but have been somewhat deficient in manufacturability. That is, the stacked arrays of the past have been labor intensive and not amenable to automated or efficient traditional manufacturing methods. The stacked packages of the past have depended almost completely on multi-step lithographic processes and often require manually packaging a single device at a time. Hence, the vertically stacked packages of the past are deficient in enabling automation such as "pick and place" and automated injection molding. Furthermore, packages of the past are deficient in readily enabling processing of more than one device at a time. Also, the packages of the past are deficient in providing alternatives to lithographic metalization.
Summary of the Invention

The apparatus and method in accordance with the invention overcome the deficiencies of the past and fill a need in the art in that the apparatus of each embodiment has dies that are more accurately positioned due to the support substrates and the methods enabled by including the substrates. Furthermore, the method of making the instant invention overcomes major deficiencies in enabling efficient manufacture of stacked microcircuit layers. That is, the new Neo layers or Neo PEMs of the instant invention enable improved manufacturability. This is achieved by incorporating means for placement of the dies on a support substrate by way of machines. Furthermore, once the dies are on the support substrates, the substrates enable further ease of handling and automation since the substrates can be automatically handled by machines.

The invention can be summarized as a stack of micro-electronic layers abuttingly and supportingly stacked together with each micro-electronic layer having at least one micro-electronic device supported on a substrate. The micro-electronic device and substrate is covered with a material of the layer. The devices are electrically connected to each other. Furthermore, the micro-electronic devices can be embedded in the material of the layers. In any case, the layers are neo layers.

In one aspect, the micro-electronic layers include a plurality of neo layers that have respective edges. The side edges together form a side surface, and the micro-electronic devices in respective neo layers are connected to each other by at least one metalization on the side surface.

In another aspect, the micro-electronic layers have a plurality holes through the stack of micro-electronic layers, and the holes house an electrical conductor. The layers have a material for covering or encapsulating the devices and substrates of the layer. This material also provides a stacking area on an upper surface of the layer. The layers have ground down portions that expose ball bonds on the micro-electronic device, and metalization on the ground down portions of the layers electrically connects the ball bonds and the electrical conductor in the holes to electrically interconnect respective layers.

A method of packaging a system of micro-electronic devices includes providing a plurality of micro-electronic layers, in which each layer has at least one micro-electronic device. The device can be modified depending on its original dimensions and packaging. When the at least one device has been selected and/or sized, it is disposed
on a support substrate. Then the device and the substrate are encapsulated in a material of an associated layer, and the devices are selectively, electrically connected to structure that forms a via that spans the thickness of the layer.

In one aspect of the invention the substrate is provided as a die paddle. The method further comprises one or more of the preliminary steps of bonding wirebond balls on the micro-electronic device and grinding the layer to expose the balls on a first, active side of the micro-electronic device.

The device can be modified by at least one of adding material to the device and thinning a layer by grinding an inactive side of one of the devices. On the other hand, the step of encapsulating can include embedding at least one PEM in a plastic material of a respective micro-electronic layer.

In one aspect, the invention further entails a plurality alignment targets formed on each support substrate such that the alignment targets on one substrate mate with alignment targets on another substrate for aligning adjacent substrates with each other in a stacked configuration. This aligned positioning can aid in accurately dicing, masking, or stacking adjacent layers.

In another aspect of the invention, the plurality of micro-electronic devices are provided as a plurality of grid array packages. These grid array packages have dies supported on substrates and are advantageously adapted for customization by traditional wire bonding from the dies to printed circuitry on the substrates. In this case the layers can be electrically interconnected by forming a generally flat surface by aligning respective edges of the plurality of substrates and providing at least one metalization spanning at least two of the layers on the generally flat surface. Alternatively, the layers comprising grid array packages can be electrically interconnected by through holes spanning a plurality of layers and having metalization in the through holes which interconnects the micro-electronic devices in the plurality of layers.

While the invention entails the stack of Neo layers, the invention also includes the layers themselves. In a simple form the micro-electronic layer has at least one micro-electronic device supported on a substrate, and the micro-electronic device and the substrate are covered by a material of the layer. Furthermore, the layer has structure that spans a thickness of the layer and at least partially defines a metalization via.
As in the combination of a stacked plurality of layers, the structure that spans the thickness of the layer and at least partially defines the metalization via can be internal and define a through hole or external and define a portion of the side wall.

Similarly, a subcombination of the method of making a stack comprises packaging a micro-electronic device as a Neo PEM layer. This method of packaging includes providing at least one micro-electronic device and selectively thinning the device and/or layer by grinding a back, inactive side of the device. The method further includes disposing the micro-electronic device on a support substrate and covering the device and the substrate with a material. Then the device is electrically connected to a structure of the layer that defines a metalization via and that spans the thickness of the device, the support substrate, and the material. Further grinding may be implemented after the covering or encapsulation step.

In another aspect of the invention, the Neo layer includes a micro-electronic circuit having a plurality of bond pads. The bond pads have a plurality of conductive protrusions extending upwardly therefrom. A support substrate supports the micro-electronic circuit. An encapsulant surrounds the micro-electronic circuit, the protrusions, and the support substrate to provide a desired stacking area. The encapsulant has a plurality of exposed contact points on an upper surface of the encapsulant that expose portions of the plurality of conductive protrusions. Reroute metalization is formed on the upper surface of the encapsulant and is connected to the exposed portions of the conductive protrusions.

In this case, the micro-electronic circuits can comprise one or more of a bare dies, Plastic Embedded Microcircuits (PEMs), and Thin Small Outline Packages (TSOPs). The plurality of conductive protrusions can be provided as ball bonds.

The invention, now having been briefly summarized, may be better visualized by turning to the following drawings wherein like elements are referenced by like numerals.
Brief Description of the Drawings

FIG. 1 is a perspective view of a bare die;
FIG. 2a is a section view taken along lines 2-2 of FIG. 1;
FIG. 2b is a section view similar to FIG. 2a and having a wire bond ball I/O bond pad;
FIG. 3 is a perspective view of a Plastic Encapsulated Microcircuit (PEM) of the Thin Small Outline Package (TSOP) type;
FIG. 4a is a sectional view taken along lines 4-4 of FIG. 3;
FIG. 4b is a sectional view similar to FIG. 4a, but having a back or lower side of the device removed;
FIG. 4c is a sectional view similar to FIG. 4b, but having a front or top side of the device removed;
FIG. 4d is a sectional view similar to FIG. 4c, but having extraneous edge material cut off;
FIG. 5a is a perspective view showing a bare die and a modified PEM disposed on a die paddle of a lead frame;
FIG. 5b is a top plane view of a string of interconnected die paddles as they typically would be provided in a manufacturing setting;
FIG. 5c is a top plan view of a variety of details that can be incorporated into the die paddle at the region 5c of FIG. 5b;
FIG. 5d is a sectional view taken along lines 5d-5d of FIG. 5c;
FIG. 6 is an end plane view of the bare die and PEM being placed on the die paddle;
FIG. 7 is a sectional view taken along lines 7-7 of FIG. 5a;
FIG. 8 is a sectional view similar to FIG. 7, but having the PEM and die paddle encapsulated in plastic or another non-conductive encapsulant material;
FIG. 9 is a sectional view similar to FIG. 8, but having a top or front portion of the encapsulant removed;
FIG. 10a is a sectional view similar to FIG. 9, but further showing metalization from respective devices to opposite edges of the encapsulant material;
FIG. 10b is a sectional view similar to FIG. 10a, but further showing alternative metalization connecting the devices and extending to an edge of the encapsulant material;
FIG. 11 is a sectional view similar to FIG. 10a and further including a non-conductive layer covering the metalization;

FIG. 12 is a sectional view of a stack of encapsulated devices similar to those shown in FIGS. 10b and 11;

FIG. 13 is a perspective view of a Grid Array package in accordance with the invention;

FIG. 14a is a sectional view taken along lines 14-14 of FIG. 13;

FIG. 14b is a sectional view similar to FIG. 14a and further showing over-molding or encapsulation of the device and at least an upper surface of the support substrate on which the device is supported;

FIG. 14c is a sectional view of a stack of over-molded or encapsulated devices similar to that shown in FIG. 14b;

FIG. 14d is a sectional view of the stack shown in FIG. 14c and further showing the steps of drilling through holes and metalizing in the through holes;

FIG. 14e is a sectional view similar to FIG 14d and further showing ways of electrically connecting the stack to a board or the like;

FIG. 15 shows electrical attachment of the stack by a ball grid array on a lower surface of the lowermost layer of the stack; and

FIG. 16 shows a stack including devices from both embodiments of the stackable devices set forth above.

The invention and its various embodiments can now be better understood by turning to the following detailed description wherein illustrated embodiments are described. It is to be expressly understood that the illustrated embodiments are set forth as examples and not by way of limitations on the invention as ultimately defined in the claims.

**Detailed Description Of The Preferred Embodiments**

A Neo layer 107, 285 is provided with at least one die 10 having a micro-electronic device on an active surface 55 of the die as shown in FIGS. 11 and 14b. The dies 10 are supported on a support substrate 105, 300 that can be readily handled by machines in an automated manufacturing setting. Both of the die (10) and the substrate (105, 300) are encapsulated in a layer material to provide a distinctive Neo layer or Neo PEM. The different embodiments offer additional respective advantages of improved manufacturability. Further versatility is provided by enabling use of dies from different
sources including bare die 10 and die 10 that is already packaged in a Plastic Embedded Microcircuit (PEM), for example. The continuing goal of providing a stackable array of Neo layers or chips is met in an improved way as described below.

In accordance with a preferred embodiment of the invention, an exemplary bare die 10 having I/O bond pads 15 as shown in FIGS. 1 and 2a is modified by bonding wire bond balls 20 to I/O bond pads 15 as shown in FIG. 2b. FIG. 2a is a sectional view of the die of FIG. 1 taken along lines 2-2 of FIG. 1. The balls 20 are applied in a conventional manner in which wires 25 are normally connected from the balls to leads 30 as can be appreciated in FIG. 3. However, in the preferred embodiment no wires and no leads are connected to the balls 20 since they are not needed in the apparatus of the instant invention.

Stated alternatively, the preferred apparatus in accordance with the instant invention is achieved in part by one step, or a part of a step, in the method of making a Plastic Embedded Microcircuit (PEM) such as the Thin Small Outline Package (TSOP) 35 shown in FIG. 3. That is, wire bond balls are mounted on the bare die as shown in FIG. 2b. As will become clear in the further description below, the leads 30 and wires 25 are not needed and preferably are never connected to the device.

On the other hand, the stackable device of the instant invention can be provided from an already packaged TSOP 35 like that shown in FIG. 3. In order to achieve the stackable layer, the TSOP 35 must be modified. FIG. 4a shows a cross section of the TSOP 35 taken along lines 4-4 of FIG. 3 in an unmodified state. FIG. 4b shows the TSOP 35 having a bottom portion 40 of embedding material 45 removed. The removal of the usually plastic material 45 is typically accomplished by grinding. The inactive backside 50 of the die 10 can also be ground in this step as long as the microcircuit in a surface of an active side 55 of the die 10 is not damaged.

Further modification includes grinding down a top portion 60 of the embedding material 45 as shown in FIG. 4c. This step includes grinding off the leads 30 and the wires 25 and exposing the wire bond balls 20. Adhesive layers 70, 75 are also exposed in this step. Next, edge portions 80, 85 can be removed by cutting the modified TSOP 35 along lines 90, 95 as indicated in FIG. 4c to achieve the modified TSOP 100 of FIG. 4d.

It is to be understood that the unmodified TSOP 35 is illustrated by way of example and not by way of the limitation. Any of a variety of PEMS could equally be used in conjunction with the teachings of the instant invention. Furthermore, while the
conductive protrusion has been described in terms of wire bond balls 20, it is to be understood that any protrusions that are electrically connected to the bond pads 15 and extending upwardly away from the active surface of the die can be equally implemented within the spirit and scope of the invention. Still further, it is to be explicitly understood that modification of the PEM can include adding material to achieve a specific dimension.

As shown in FIG. 5a a support substrate in the form of a die paddle 105 is advantageously employed to form a Neo layer 107. The die paddle 105 typically includes a pan shaped portion 110 with raised portions for guiding and positioning the die 10 or modified PEM 100, and connecting ears 115. FIG. 5b shows a string 120 of die paddles 105. In this case, the die paddles are formed of sheet metal, although they could be formed of a PCB or other material. The die paddles 105 are temporarily connected to each other by a pair of ears 115 at each respective end 125, 130 of the die paddles 105. The string 120 of die paddles 105 facilitates automation during manufacturing. Such automation has not heretofore been available in the manufacture of Neo chips or layers. Now die paddles 105 can be advantageously used to properly position dies 10 and/or modified PEM 100 for encapsulation. The die 10 and modified TSOP 100 can be accurately placed on the die paddle 105 by machines as indicated by arrows 133 in FIG. 6. Typically this placement includes gluing the die 10 and/or modified TSOP 100 in place on the paddle 105.

It is to be explicitly understood that the number and types of dies 10 and modified PEMs 100 are not to be limited. While there are physical constraints imposed by the size of the die paddle and by the thicknesses of the die and modified TSOP to be placed on the die in a matching relation to be described in further detail below, the number and type of dies 10 are otherwise not to be limited.

To aid in placement of the die 10 or modified TSOP 100, proper heat transfer from the die, and other processes to be described below, the details of FIG. 5c can be applied to a region 5c in FIG. 5b as shown. Openings 135, 140, 145, 150, and 155 can be selectively provided in the die paddle 105 to provide the proper amount of heat transfer so that the cooling of the die paddle 105 occurs at approximately the same rate as do the materials of the die 105 and other surrounding elements. In addition to the raised edges of the pan shaped portion 110 of the die paddle 105, targets 160 may be used in positioning the die and modified TSOP 10, 100 on the die paddle. However, the main purpose of the targets 160 is to enable accurate stacking of die paddles 105 one
on top of the other as shown in the sectional view of FIG. 5d taken along lines 5d-5d of FIG. 5c. While the shapes of the targets are show as being generally conical in FIG 5d, and a tip end 163 comprise a cross shape as shown in FIG. 5c, any of a variety of shapes can be implemented. Furthermore, the tip end 163 can comprise a material that either visually or by its hardness aids in stopping a grinding process at a specific height 170 above a base 175 of the pan shaped portion 110.

The method of making a neo layer in accordance with the instant invention includes the step of placing the die and modified TSOP 10, 100 on the die paddle 105 as indicated in FIG. 6. FIG. 7 shows a cross sectional view taken along lines 7-7 of FIG 5a after placement of the die 10 and modified TSOP 100 thereon. It should be noted that the dies 10 and modified TSOP 100 need to be selected or modified to have substantially matching heights. That is, for example, the highest point of the ball 20 on the left hand die 10 of FIG. 7 must be at least as high as the lowest point to which the modified PEM 100 can be ground without damaging the micro-electronic circuits in the active surface 55 of the right hand die 10 of FIG. 7. This is the case in the illustration of FIG. 9.

Next the die 10, the modified TSOP 100, and the die paddle 105 are encapsulated in a molding material 180 as shown in FIG. 8. Preferably encapsulation is accomplished in an automated process including injection molding of a plastic material around the die 10, the modified TSOP 100, and the die paddle 105. The die paddles 105 aid by holding the dies 10, 100 in position during molding. This feature and the string of die paddles 120 enable automated manufacturing. After curing of the molding material 180, removal of a top portion 185 of the molding material 180 is typically achieved by grinding. This step of removing is for exposing the wire bond balls 20 in respective ground down portions 190, 195 corresponding generally to the die 10 and modified TSOP 100 on the die paddle as shown in FIG. 9. Note that the difference in height of the devices 10, 100 is small so that both wire bond balls can be accessed without damaging the active surface 55.

FIGS 10a and 10b show variations of metalization on ground down portions 190, 195. For example, FIG. 10a shows metalization 200, 205 from the die 10 and the modified TSOP 100 to respective side edges 210, 215 of the Neo layer 107 being formed. FIG. 10b has metalization 220 connecting devices of the die 10 and the modified TSOP 100 together and to a side edge 215. Fig. 11 shows the step of covering the ground portions 190, 195 and the metalizations 200, 205 with a non-
conductive layer 225. At this stage, a Neo layer 107 has been formed. It can be appreciated that the bottom portion 235 of the encapsulant material 180 can also be removed such as by grinding. In fact the die paddle 105 itself can be ground away to reduce the thickness of the layer 107, which has been formed. While the result is structurally and functionally different from conventional PEMs, the plastic embedding achieved by the encapsulating step is analogous to the embedding that PEMs undergo. Hence, the new stackable layers 107 achieved may be termed a Neo PEM layers.

FIG. 12 has a stack of Neo layers 107. As shown some of the layers incorporate the metalization 200, 205, while another of the layers incorporates metalization 220. Once the layers 107 have been glued together, metalization 240 can be made on a first exterior side surface 245. A metalization 250 can be applied to a second exterior side surface 247 or to the inside of respective through holes 255 spaced inwardly from an alternative third side wall 260. In the case of through holes 255, the holes can be drilled before or after stacking. As shown, a cap layer 265 and base layer 270 are applied to the stack. The cap layer can be a re-route layer and can have T-pads 275, 280 for connecting the stack to a board or other external sources. The through holes 255 are exemplary only, and it is to be understood that the through holes 255 may be located at any position in the layer 107 that does not interfere with the microcircuits in the dies 10.

The cap and base layers 265, 270 are typically formed of a ceramic material, although other non-electrically conducting materials can be utilized instead. All of the metalizations can be accomplished by known lithographic or printing methods.

In a second embodiment shown in FIGS. 13-15, Neo layers 285 comprise materially different elements and a different method from those of the preferred embodiment of FIGS. 1-12. The second embodiment layers 285 still form Neo PEM layers even though they have, to some degree, a different purpose from the Neo PEM layers 107 of the first embodiment. In the second embodiment, dies 290, 295 having wire bond pads 15 and are supported on a support substrate 300. The substrate 300 can be formed of typical Printed Circuit Board (PCB) or other material. The material for the support substrate 300 can comprise FR4, polyimide, ceramic, or even silicon with an isolation layer. The dies 290, 295 can be positioned and adhered to the substrate 300 by known manufacturing methods including optical means for accurately positioning the dies 290, 295.
Once the dies 290, 295 are placed on the substrate 300, the I/O wire bond pads 15 are electrically connected to printed circuitry 305 on the substrate 300 by wires 307 and conventional wire bonding methods. As shown in FIG. 13, the printed circuitry 305 can be utilized to connect the dies 290, 295 to each other and to a grid of large bond pads 310. The large bond pads 310 are normally lands for balls or pins of a Ball Grid Array (BGA), or a Pin Grid Array (PGA), and typically will be more numerous than the four lands illustrated for simplicity in FIG. 13. As shown in FIG. 14a, which is a sectional view taken along lines 14a-14a of FIG. 13, these large bond pads or lands 310 can be in the form of pre-drilled holes 315 shown as hidden lines or can simply be bond pads 310 on the surface. In the case of pre-drilled holes 315, the holes 315 can be metalized preliminarily. Generally, pre-drilling and metalizing of the holes 315 is not needed because of subsequent molding, drilling, and metalizing that will be further described below. However, pre-drilled holes 315 is advantageous in some applications.

It is of particular interest that the support substrates 300 can be purchased as off the shelf items such as flip chip and wire bondable grid array ICs. However, it is more probable that the substrates would be ordered for a particular standard configuration or set of configurations. Production for such an order is normally readily available and highly automated. Furthermore, the methods of connecting the dies to the printed circuit boards utilizes traditional automated methods. Therefore, while not typically an off-the-shelf or pre-packaged device, the grid array substrate does enable easy customization by traditional manufacturing methods including ball bonding of the dies to bonding pads on the substrate 300.

FIG. 14b. shows the step of encapsulating or over-molding the substrate 300 and dies 290, 295 with an encapsulating material 320. Preferably the molding process is automated and includes injection molding with a plastic material for labor reduction and increased speed and efficiency of production. However, the over-molding can be done by hand when necessary and can employ a pourable epoxy, for example. It should be noted that in both this and the preferred first embodiment, the substrate can be completely or partially surrounded by the molding material 45, 320 even though the first embodiment is shown completely surrounded by material 45 and the second embodiment is shown as only having a top surface 325 of the substrate 300 covered by the material 320.

Fig. 14c shows the layers 285 in a stacked configuration. The layers 285 can be selectively ground down on a top side 330 and a bottom side 335 prior to stacking the
layers 285. The layers 285 can then be aligned by aligning edges of the substrates 300, ball lands, or by positioning ball bonds 20 on the dies 290, 295. Then the layers 285 are glued or molded together. FIG. 14d depicts drilling through holes 345 with a drill 350 in the material 320. Drilling can be done by a mechanical or a laser drilling process and can be done to one or more of the layers 285 at a time. Metalizing in the through holes 345, 315 can be accomplished with a paste 355 as shown, by a sputtering process, or by a plating operation, for example.

FIG. 14e shows a variety of attachment means for connecting the stack 340 to the outside world. That is, a base 360 can act as a re-route layer or can simply provide I/O contact with a board 365 on which the stack 340 is supported. In this case, balls 370 connect the stack to aligned lands on the board as shown in FIG. 15. Alternative means includes a metalization 375 on an upper surface 380 of a top layer 285 as shown in FIG. 14e. This means includes a wire 385 connecting the metalization 375 to the board 365. A further alternative for connection between the layers 285 is a metalization 390 on an edge surface 395 of the layers 285. This metalization, of course, requires electrical connection from the dies to the edge surface 395.

FIG. 16 shows a stack 400 similar to stack 238, but having at least one layer 285 from the grid array embodiment. FIG. 16 illustrates how both of a die paddle based Neo PEM layers of the first embodiment and a Grid Array Neo PEM layers of the second embodiment can provide Neo layers in a common stack 400. FIG. 16 further illustrates an additional modification of metalization 405 and thus a distinct layer 405. In this case, the metalization 405 connects from one bond pad ball 20 of a modified PEM 410 to a die 10 and from another bond pad ball 20 of the modified PEM 410 to metalization 415 on an edge surface 420. Additionally, it should be noted that the metalization 250 can be all or partly replaced by pins 425 in the through holes 255. The pins can function as electrical connectors between the layers 107, 405, 285 and/or as positioning means for aligning two adjacent layers.

Many alterations and modifications may be made by those having ordinary skill in the art without departing from the spirit and scope of the invention. Therefore, it must be understood that the illustrated embodiments have been set forth only for the purposes of example and that it should not be taken as limiting the invention as defined by the following claims. The claims are thus to be understood to include what is specifically illustrated and described above, what is conceptionally equivalent, what can be obviously substituted and also what incorporates the essential idea of the invention.
What is claimed is:

1. A method of packaging a system of micro-electronic devices, comprising:
   providing a plurality of micro-electronic layers, each layer comprising at least
   one micro-electronic device;
   selectively modifying the micro-electronic device;
   disposing the micro-electronic device on a support substrate;
   encapsulating the device and the substrate in a material of an associated
   layer; and
   electrically connecting the device to a via that spans the thickness of the layer.

2. The method of packaging a system of micro-electronic devices as recited in Claim 1, wherein:
   the substrate is a die paddle; and further comprising the preliminary step of:
   bonding wire bond balls on the micro-electronic device.

3. The method of packaging a system of micro-electronic devices as recited in Claim 1, comprising:
   bonding wire bond balls on the micro-electronic device; and
   grinding the layer to expose the balls on a first, active side of the micro-
   electronic device.

4. The method of packaging a system of micro-electronic devices as recited in Claim 1, wherein the step of selectively modifying further comprises at least one of adding
   material to the device or thinning a layer by grinding an inactive side of one of the
   devices.

5. The method of packaging a system of micro-electronic devices as recited in Claim 1, wherein:
   the step of encapsulating further comprises embedding at least one PEM in a
   plastic material of a respective micro-electronic layer;
   aligning edges of the micro-electronic layers with each other to form a
   generally flat surface by said edges; and
connecting said devices to each other by at least one metalization spanning at least two of the plurality of layers.

6. The method of packaging a system of micro-electronic devices as recited in Claim 1, comprising the preliminary steps of:
   providing ball bonds in said pre-packaged micro-electronic devices;
   over-molding said micro-electronic devices and said ball bonds;
wherein at least one of the micro-electronic devices is an off-the-shelf device in which said steps of providing ball bonds and over-molding have already been taken.

7. The method of packaging a system of micro-electronic devices as recited in Claim 1, further comprising:
   providing holes through said layers;
   providing an electrical conductor in said holes;
   exposing electrically conductive protrusions on said micro-electronic device by grinding an upper surface of the material covering an active side of the device;
   metalizing on a portion of said upper surface that has been ground; and electrically connecting said protrusions and said electrical conductor at said holes of respective said layers to provide electrical continuity between layers.

8. The method of packaging a system of micro-electronic devices as recited in Claim 1, further comprising:
   forming a plurality of alignment targets on each support substrate such that said alignment targets on one substrate have structure that mates with alignment target structure on another substrate for aligning adjacent substrates with each other; and connecting electrical conductors of respective devices with each other and with circuitry external to the layers by mating said aligning target structures of adjacent substrates to each other so that the layers form a stack.
9. The method of packaging a system of micro-electronic devices as recited in Claim 1, further comprising:
   forming a plurality alignment targets on each support substrate such that said alignment targets on one substrate mate with alignment targets on another substrate for aligning adjacent substrates with each other in a stacked configuration; and
   positioning the devices for dicing, masking, or alignment with adjacent layers by means of the alignment targets.

10. The method of packaging a system of micro-electronic devices as recited in Claim 9, wherein said step of forming further comprises forming a stop for stopping the grinding at a preselected position on said device.

11. The method of packaging a system of micro-electronic devices as recited in Claim 1, wherein:
   said step of providing a plurality of micro-electronic layers further comprises providing said micro-electronic devices as grid array packages;
   said plurality of layers have respective edges; and
   forming a generally flat surface by aligning said respective edges of said plurality of substrates; and
   connecting said devices to each other by at least one metalization spanning at least two of the layers.

12. The method of packaging of Claim 11, further comprising:
   forming a through hole in the plurality of layers; and wherein the step of metalizing comprises metalizing in the through holes.

13. The method of packaging a system of micro-electronic devices as recited in Claim 11, wherein said step of providing further comprises providing said grid array packages as commercial off-the-shelf flip chip and wire bondable grid array ICs.
14. The method of packaging a system of micro-electronic devices as recited in Claim 11, wherein:
   said step of providing comprises providing said micro-electronic devices as laminates having wire bond ball bonds;
   further providing a ball guided alignment means by said ball bonds; and
   bonding said layers together by gluing or molding.

15. The method of packaging a system of micro-electronic devices as recited in Claim 1, wherein said step of providing a plurality of micro-electronic layers further includes providing layers comprising a processor, a memory device, a controller, and a passive.

16. A method of packaging a micro-electronic device as a Neo PEM, comprising:
   providing at least one micro-electronic device;
   selectively thinning by grinding a back, inactive side of the device;
   disposing the micro-electronic device on a support substrate;
   covering the device and the substrate with a material; and
   electrically connecting the device to a structure that defines a metalization via
   and that spans the thickness of the device, the support substrate, and the material.

17. The method of packaging a micro-electronic device as recited in Claim 16, wherein the step of electrically connecting comprises electrically connecting the device to a through hole.

18. The method of packaging a micro-electronic device as recited in Claim 16, wherein the step of electrically connecting comprises electrically connecting the device to a side wall.

19. The method of packaging a micro-electronic device as recited in Claim 16, wherein:
   the step of selectively thinning further comprises selectively grinding a back side of at least one bare die having a micro-electronic device thereon;
the step of disposing further comprises positioning the die on a die paddle;
and
the method further comprises:
attaching wirebond balls to the die; and
selectively grinding the material.

20. The method of packaging a micro-electronic device as recited in Claim 16, wherein
the device is a prepackaged device and further comprising modifying the device by at
least one of grinding, cutting, and adding material thereto prior to the step of disposing.

21. A stack of micro-electronic layers, comprising:
a plurality of said micro-electronic layers, each micro-electronic layer
comprising at least one micro-electronic device supported on a substrate;
and
the at least one micro-electronic device and substrate covered with a material
of the layer; wherein:
the devices are electrically connected to each other; and
the layers are abuttingly and supportingly stacked together.

22. The stack of micro-electronic layers of Claim 21, wherein:
said micro-electronic devices are embedded in a material of said layers such
that said layers are neo layers;
said plurality of neo layers have respective edges, together forming a side
surface; and
the micro-electronic devices in respective said neo layers are connected to
each other by at least one metalization on said side surface.

23. The stack of micro-electronic layers of Claim 22, wherein:
at least one of the neo-layers has a plurality of common layer micro-electronic
devices therein;
said at least one of the neo-layers has a ground down portion exposing
protrusions connected to I/O pads on each of the plurality of the common
layer devices; and
a circuit is metalized on the ground down portion to electrically interconnect the plurality of the common layer devices.

24. The stack of micro-electronic layers of Claim 21, wherein:
   said micro-electronic devices have protrusions connected to I/O pads;
   at least one of said micro-electronic devices is a pre-packaged device and has a ground down portion exposing the protrusions; and further comprising:
   metalized circuits on said ground down portion of said pre-packaged micro-electronic device electrically connecting said protrusions to other protrusions or to vias that electrically connect the layers.

25. The stack of micro-electronic layers of Claim 24, wherein the pre-packaged device is a commercial off-the-shelf device.

26. The stack of micro-electronic layers of Claim 24, each of said layers comprising a plurality alignment targets for dicing, masking, and for aligning adjacent layers with each other.

27. The stack of micro-electronic layers of Claim 26, wherein said alignment targets comprise protruding parts of the substrate that extend to a height between the devices and the upper extent of the balls such that the targets thereby act as stops during layer grinding.

28. The stack of micro-electronic layers of Claim 21, comprising a plurality holes through the stack of micro-electronic layers, said holes housing an electrical conductor; ground down portions on said layers exposing ball bonds on the micro-electronic device; and metalization on said ground down portions of said layers electrically connecting the ball bonds and the electrical conductor housed in said holes.

29. The stack of micro-electronic layers of Claim 21, wherein:
the substrate in at least one of the layers is a die paddle supporting the at
least one micro-electronic device in a selected position on the die paddle;
and
an over-molding material encapsulates the micro-electronic device and at
least part of the paddle.

30. The stack of micro-electronic layers of Claim 29, wherein the die paddle is formed
of a thin sheet of metal or a circuit board material.

31. The stack of micro-electronic layers of Claim 21, wherein:
   the device is a pre-packaged device having first and second ground down
   portions on opposite faces of the pre-packaged device.

32. The stack of micro-electronic layers of Claim 21, wherein:
   said devices are pre-packaged grid array packages;
   said plurality of layers have structure defining respective through holes
   containing metalization; and
   said devices are electrically connected to each other by wiring in each layer
   connected to said metalization in said holes.

33. The stack of micro-electronic layers of Claim 32, wherein said grid array packages
   comprise commercial off-the-shelf flip chip and wire bondable grid array ICs.

34. The stack of micro-electronic layers of Claim 32, wherein:
   said grid array packages comprise laminates having wire bonded ball bonds;
   said ball bonds provide a ball guided alignment means; and
   said grid array packages are bonded together by gluing or molding.

35. The stack of micro-electronic layers of Claim 21, further comprising at least one
   custom made micro-electronic device.

36. The stack of micro-electronic layers of Claim 21, wherein said devices include at
   least one of: a processor, a memory device, a controller chip, and a passive.
37. The stack of micro-electronic layers of Claim 21, wherein at least one of the layers comprises a device that is different from the devices of another of said layers;

38. A packaged micro-electronic device, comprising:
   a micro-electronic layer having at least one micro-electronic device supported on a substrate; and
   the micro-electronic device and substrate covered by a material of the layer;
   wherein:
   the layer has structure spanning a thickness of the layer and at least partially defining a metalization via.

39. The packaged micro-electronic device of Claim 38, wherein:
   the structure defines a through hole containing metalization; and
   the device is electrically connected to said metalization in the through hole.

40. The packaged micro-electronic device of Claim 38, wherein:
   the structure is provided by a portion of a side wall of the layer; and
   the device is electrically connected to the portion of the side wall for connection to a metalization on said portion of said wall.

41. A Neo layer comprising:
   a micro-electronic circuit having a plurality of bond pads;
   a plurality of conductive protrusions extending from said plurality of bond pads;
   a support substrate supporting said micro-electronic circuit; an encapsulant surrounding said micro-electronic circuit, said protrusions, and said support substrate to provide a desired stacking area;
   a plurality of exposed contact points on an upper surface of said encapsulant exposing portions of said plurality of conductive protrusions; and reroute metallization formed on the upper surface of said encapsulant and connected to said exposed portions of said conductive protrusions.
42. The Neo layer of Claim 41, wherein:
   the micro-electronic circuit comprises a bare die; and
   the plurality of conductive protrusions comprise ball bonds.

43. The Neo layer of Claim 41, wherein the micro-electronic circuit comprises a plastic-encapsulated microcircuit (PEM) package.

44. The Neil layer of Claim 43, wherein:
   the PEM is a thin small outline package (TSOP); and
   the plurality of conductive protrusions comprise ball bonds.