

Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 1

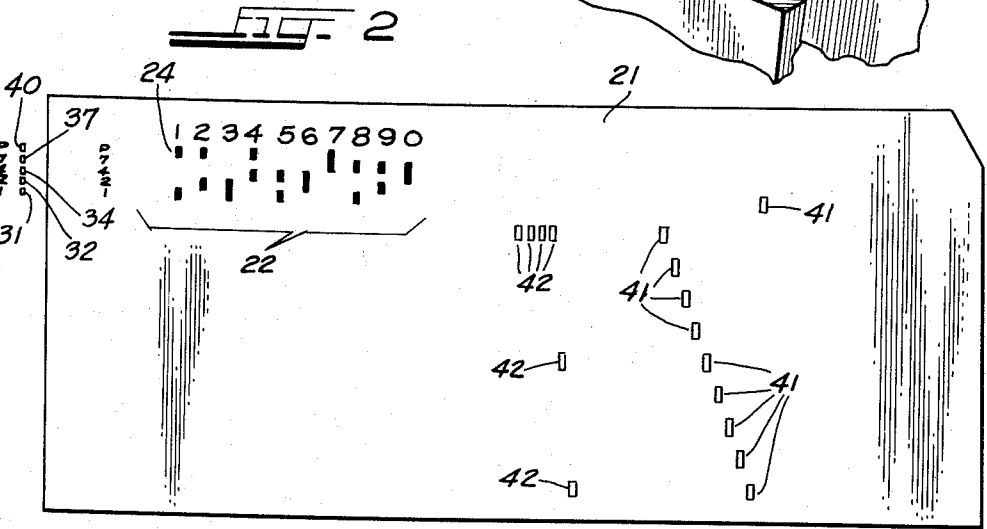
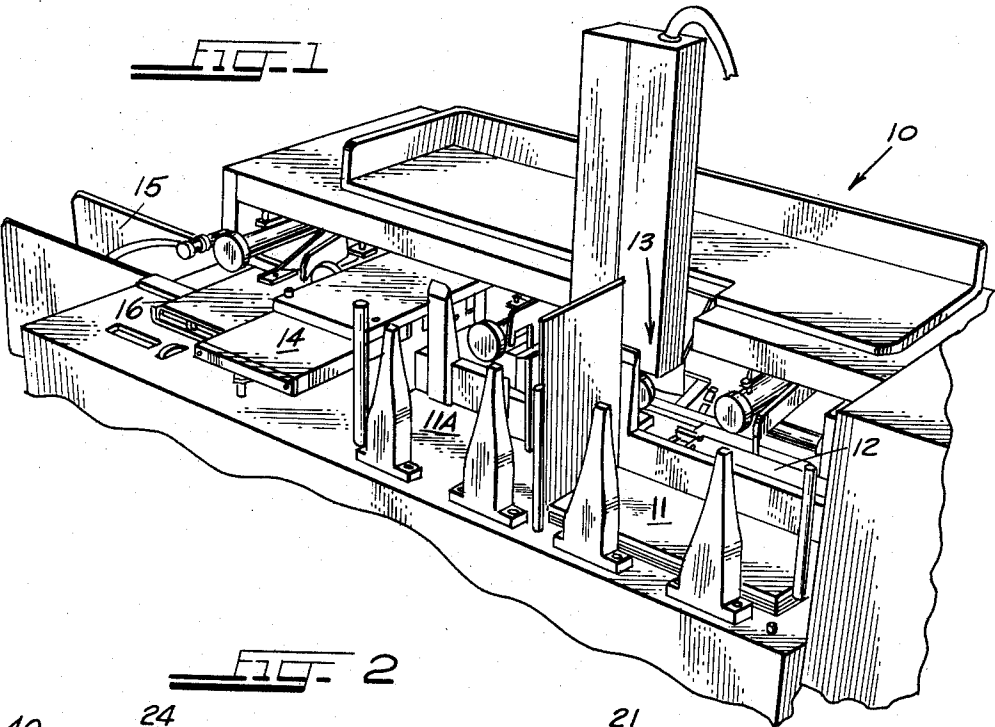


FIG. 3

NUMBER

	0	1	2	3	4	5	6	7	8	9
9										
8										
6										
4										
2										

CODE DESIGNATION

INVENTOR.
MAX E. SALLACH
BY
Wallace, Kinger and Dorn
ATTYS.

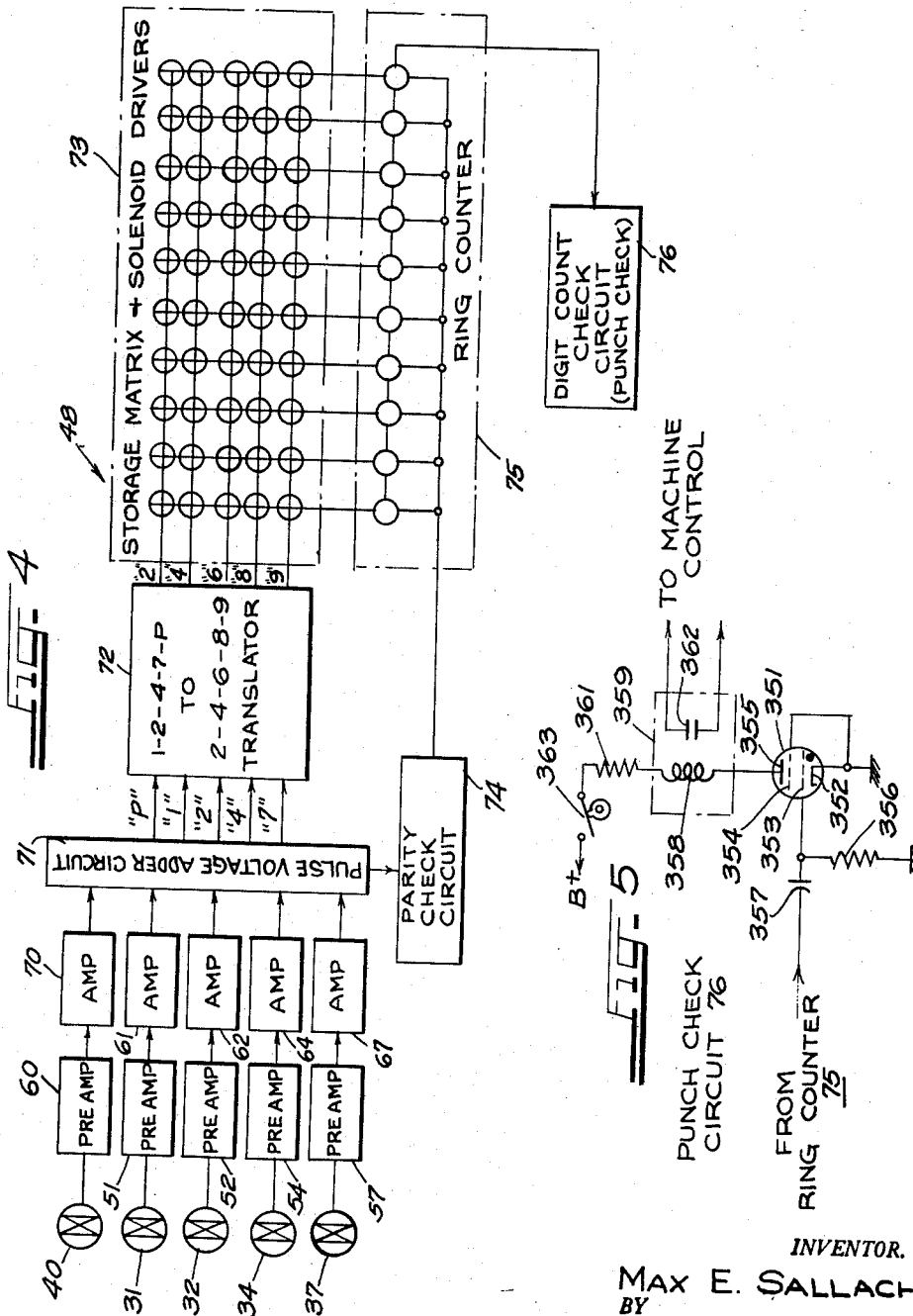
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 2



INVENTOR.

MAX E. SALLACH
BY

Wallace, Kinger and Born
ATTORNEYS.

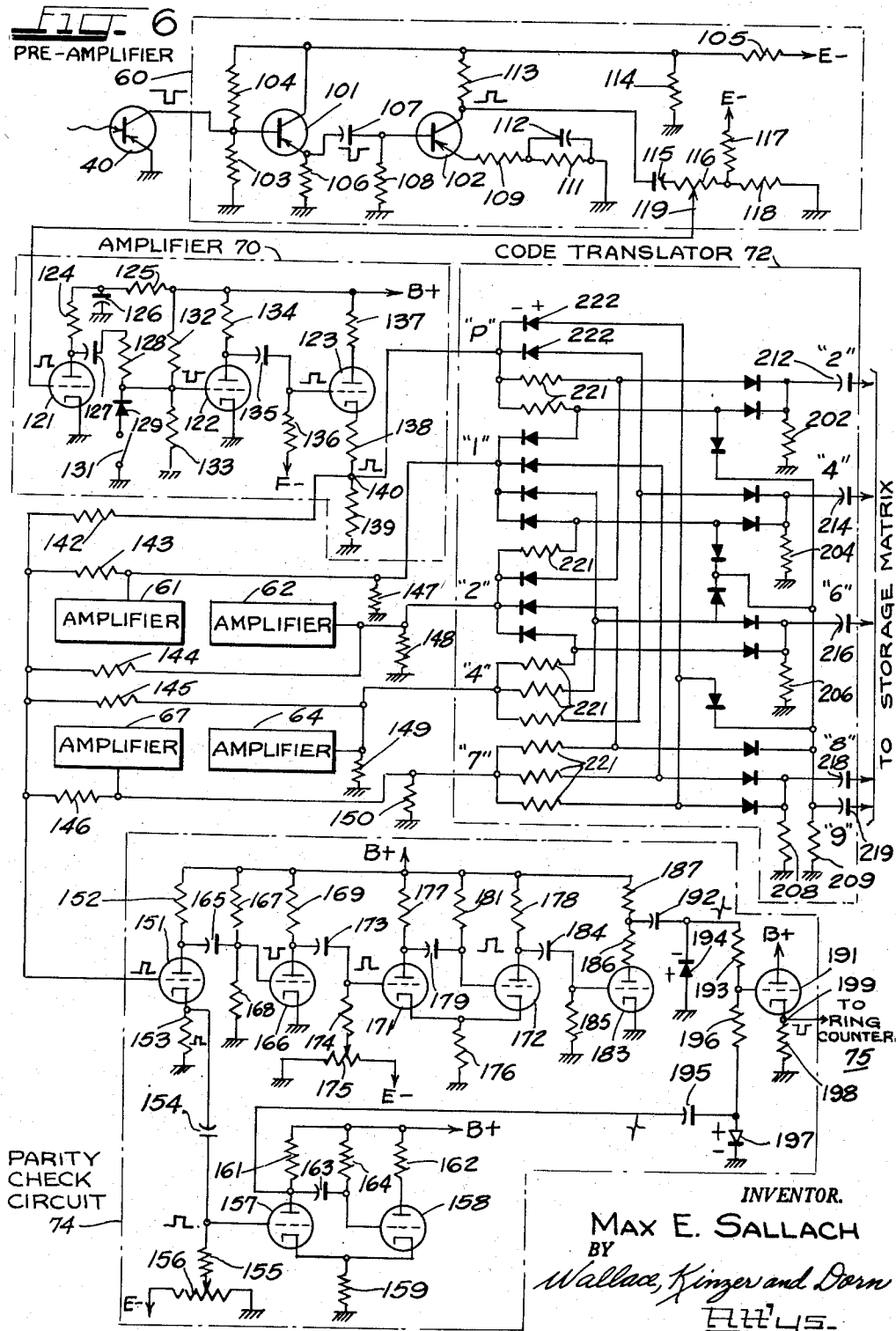
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 3



Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 4

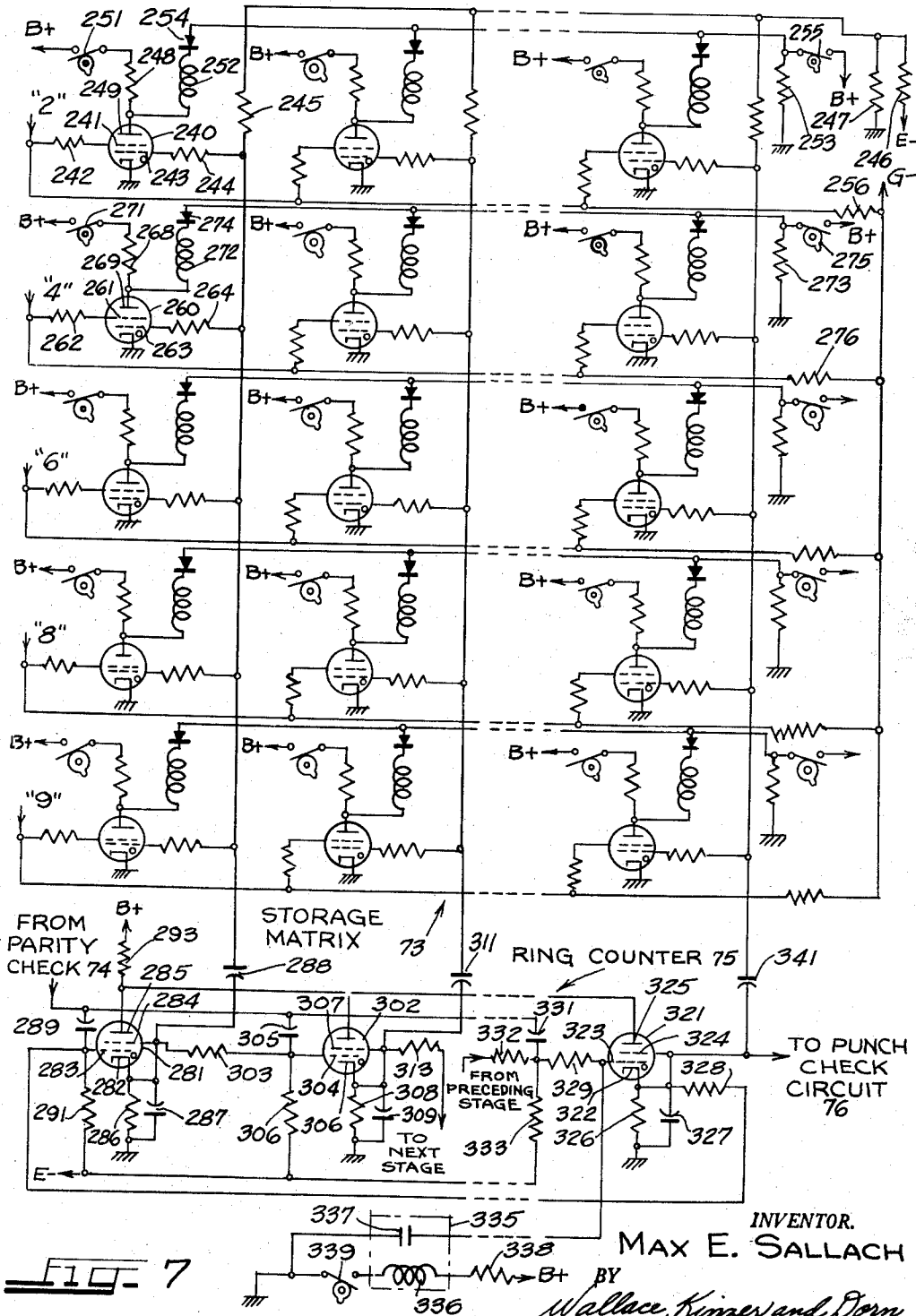


FIG. 7

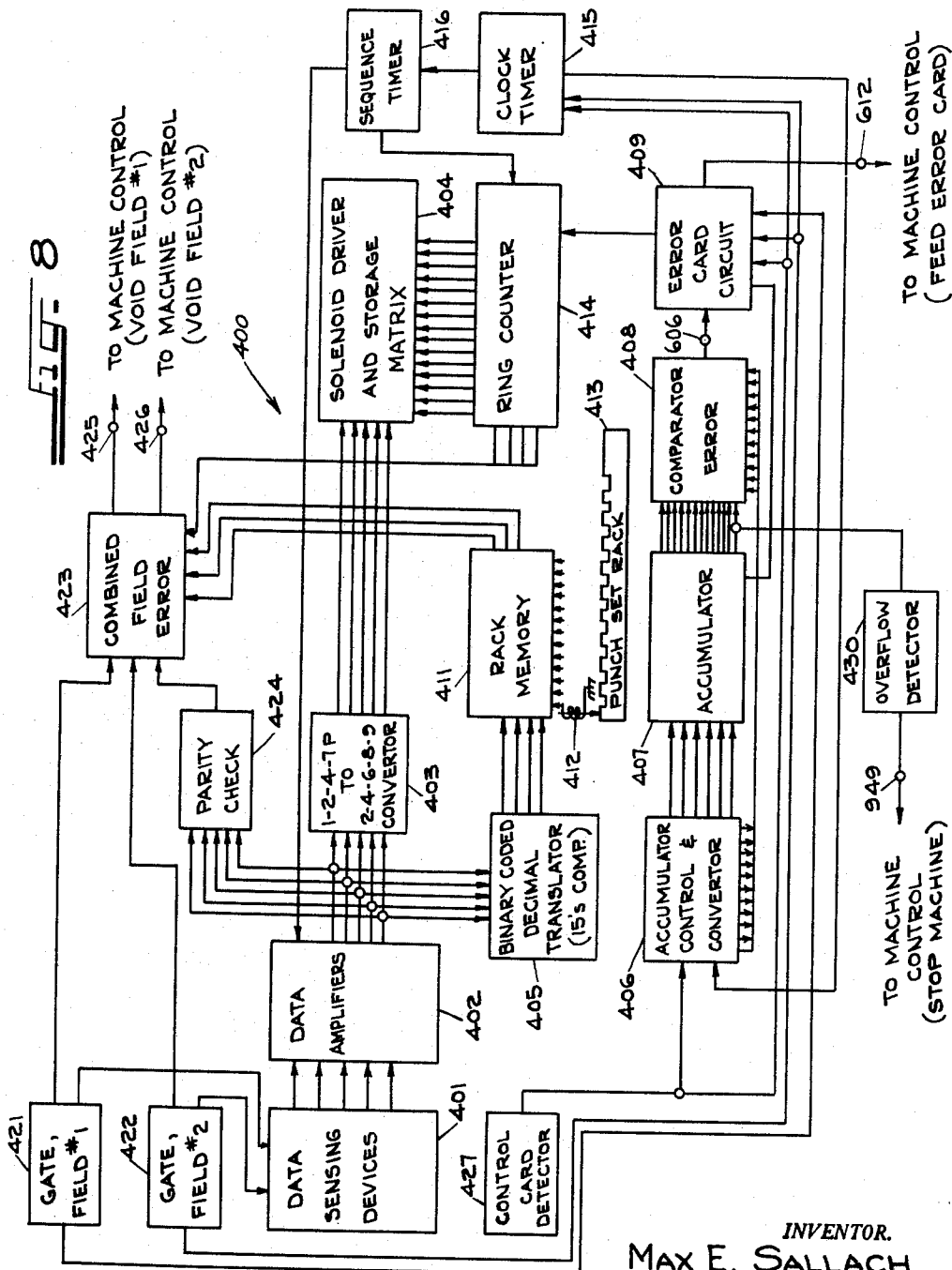
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 5



INVENTOR.
MAX E. SALLACH
BY
Wallace, Koenig & Horn
ATTORNEYS.

Dec. 18, 1962

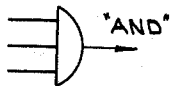
M. E. SALLACH
PUNCHING MACHINES

3,069,075

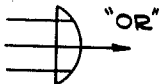
Filed June 14, 1961

15 Sheets-Sheet 6

 9A



 9B



 9C

D.C. AMPLIFIER
NO INVERSION



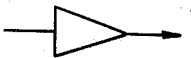
 9D

D.C. INVERTING
AMPLIFIER;
"NOT"



 9E

A.C. AMPLIFIER
NO INVERSION

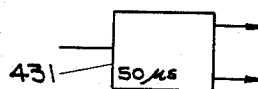


 9F

A.C. INVERTING
AMPLIFIER



 9G



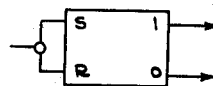
ONE-SHOT
MULTIVIBRATOR

 9H



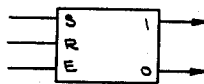
FLIP-FLOP

 9I



BINARY
FLIP-FLOP

 9J



FLIP-FLOP
WITH AUXILIARY
RESET

INVENTOR.

MAX E. SALLACH

BY

Wallace, Kenger & Dorn

ATTY-S.

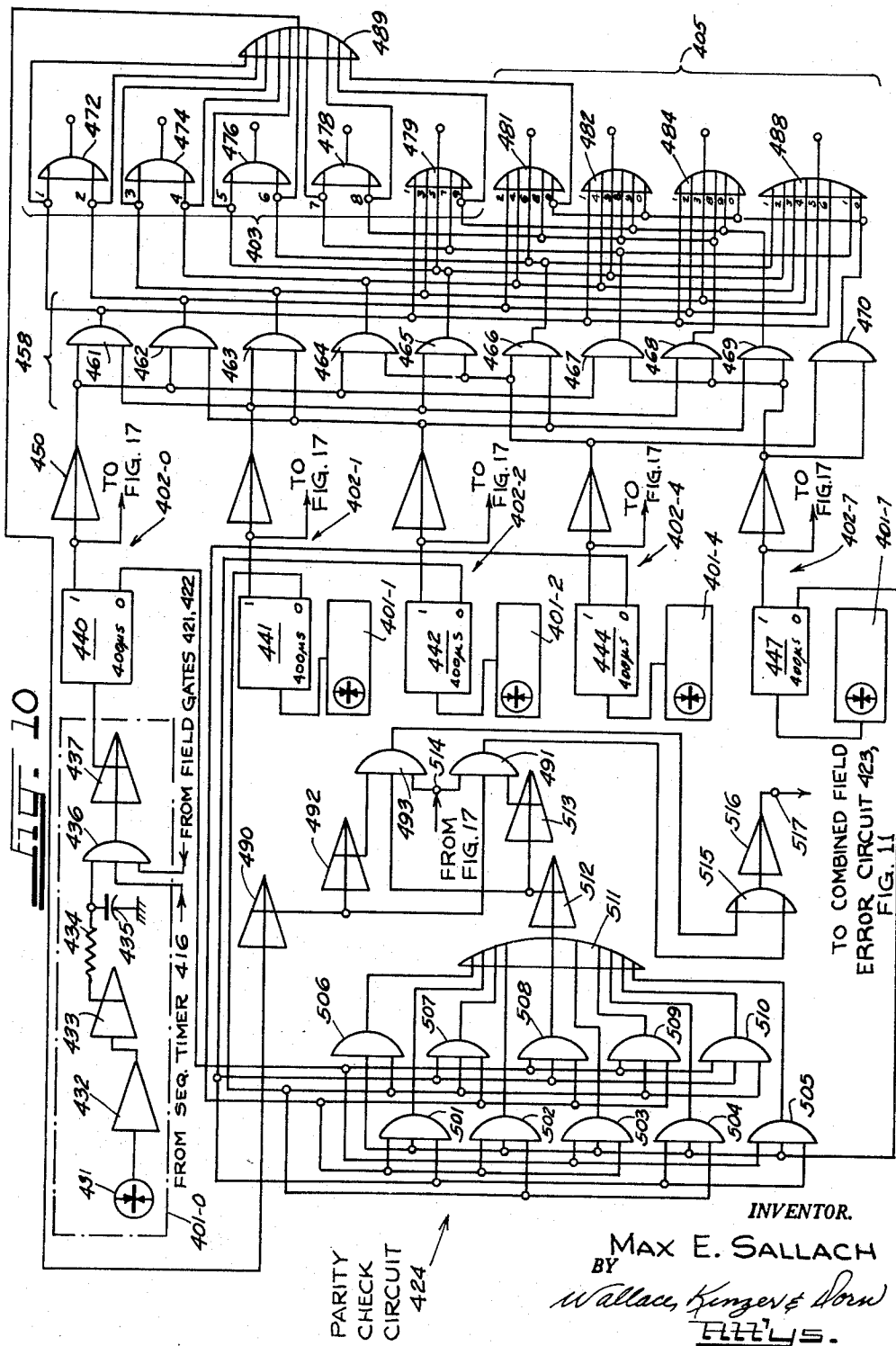
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 7



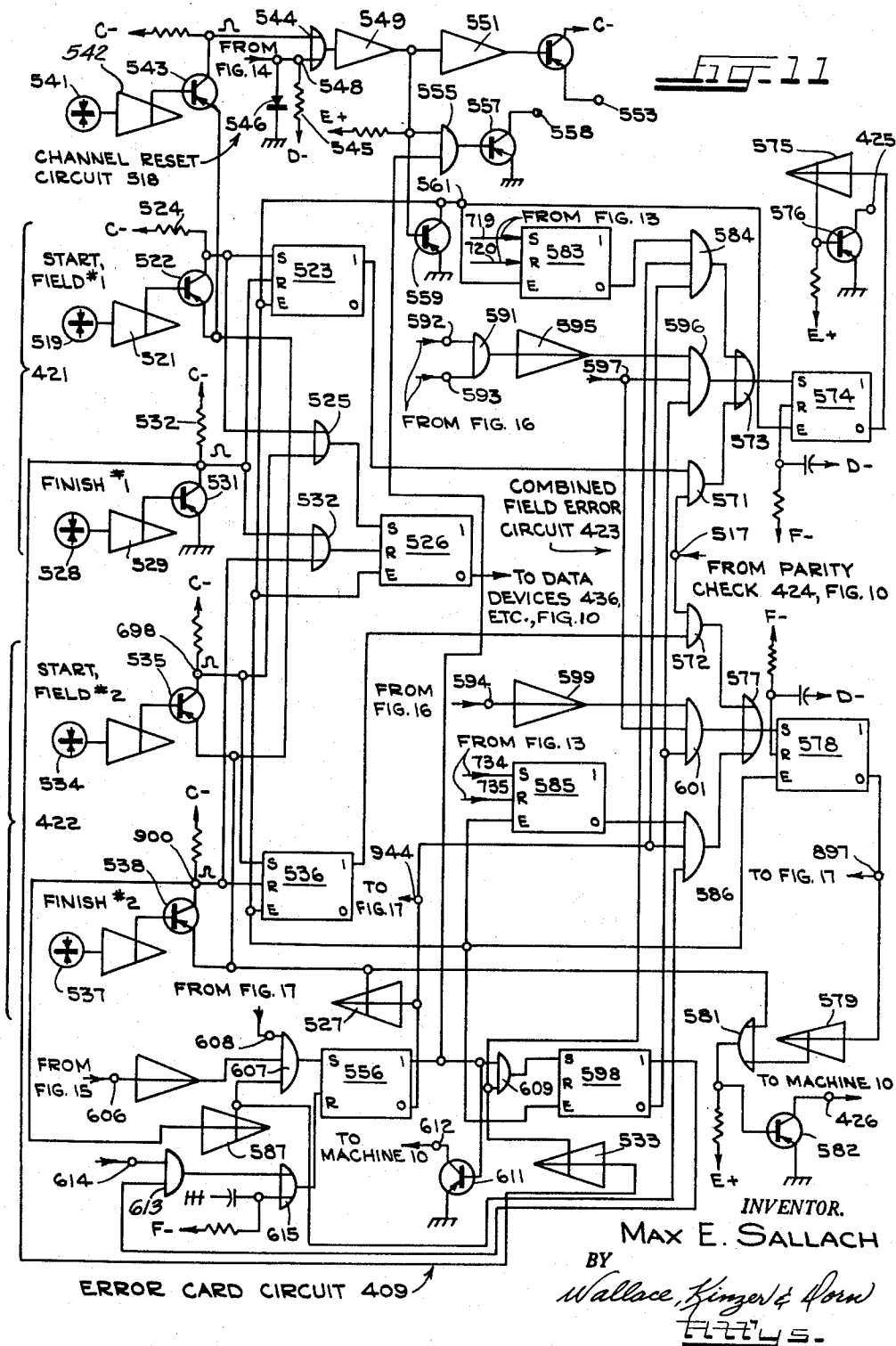
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 8



Dec. 18, 1962

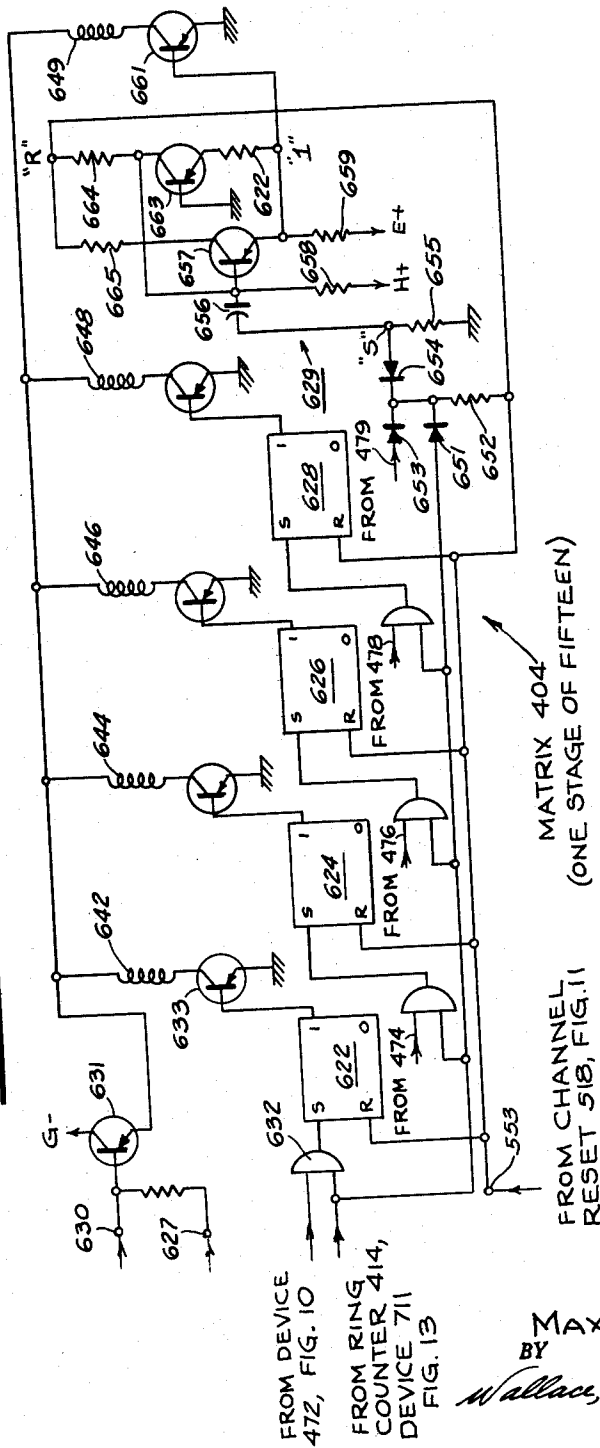
M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 9

FIG- 12



INVENTOR.

MAX E. SALLACH
BY

Wallace, Kenger & Fourn
ATTORNEYS.

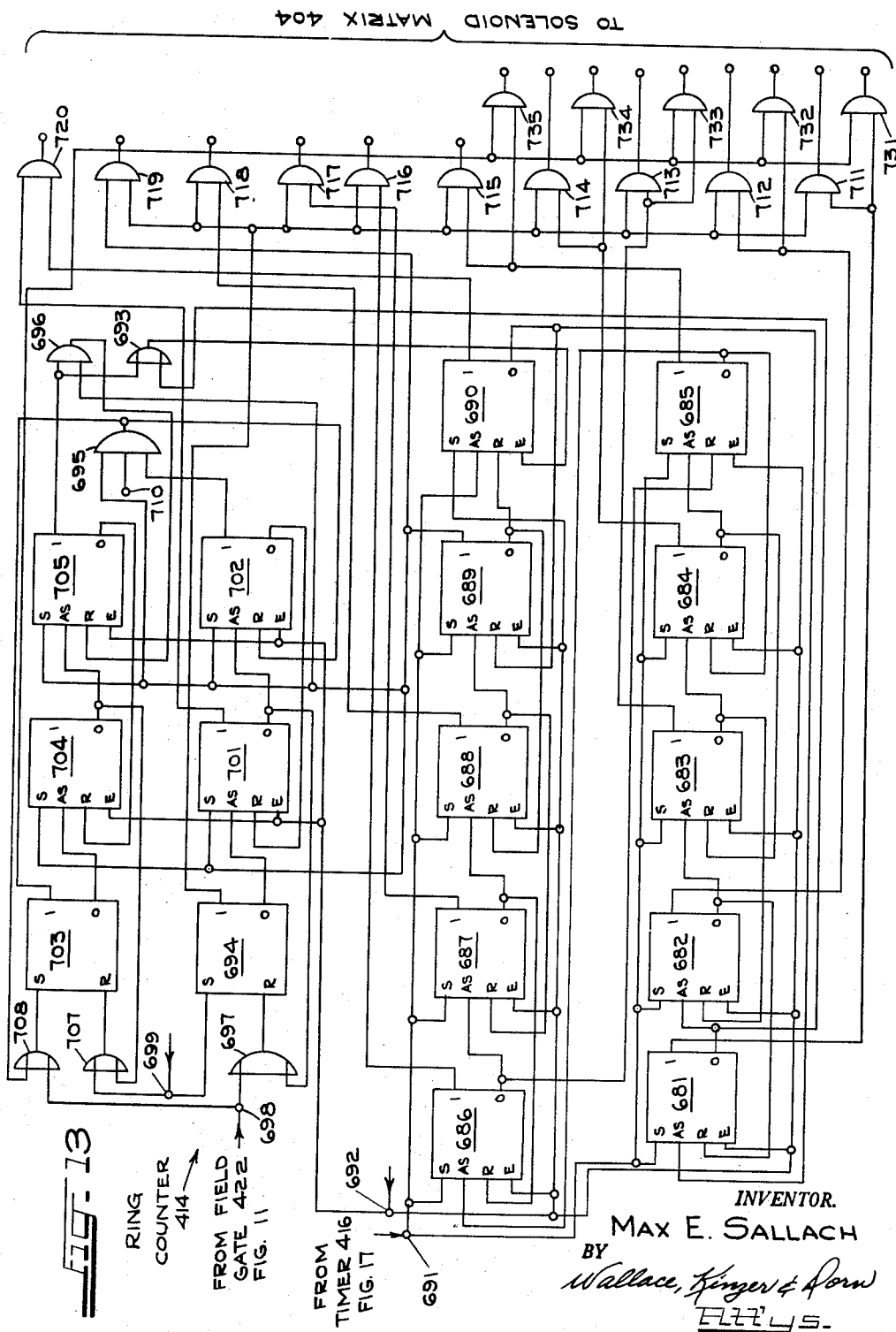
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 10



Dec. 18, 1962

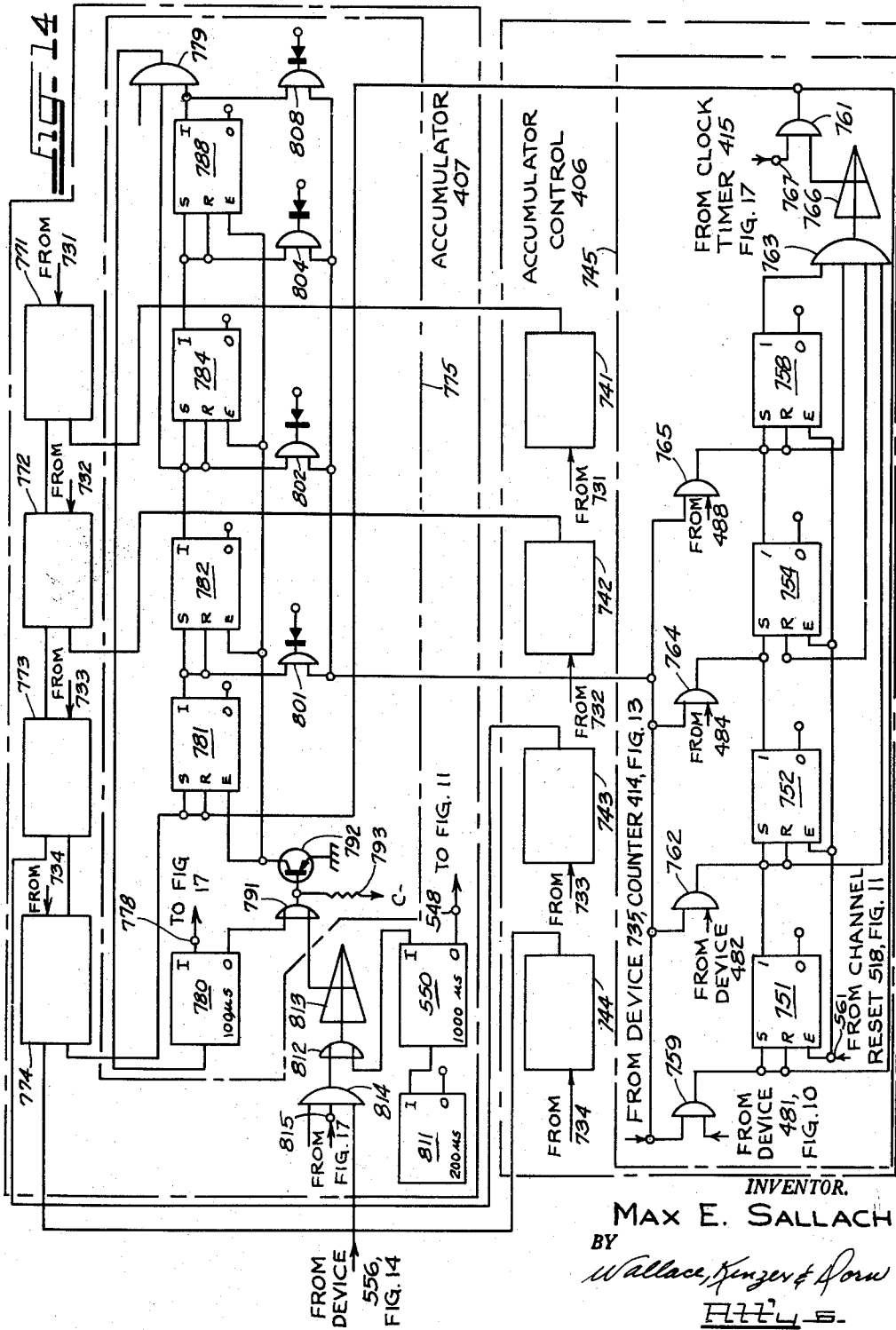
M. E. SALLACH

3,069,075

PUNCHING MACHINES

Filed June 14, 1961

15 Sheets-Sheet 11



Dec. 18, 1962

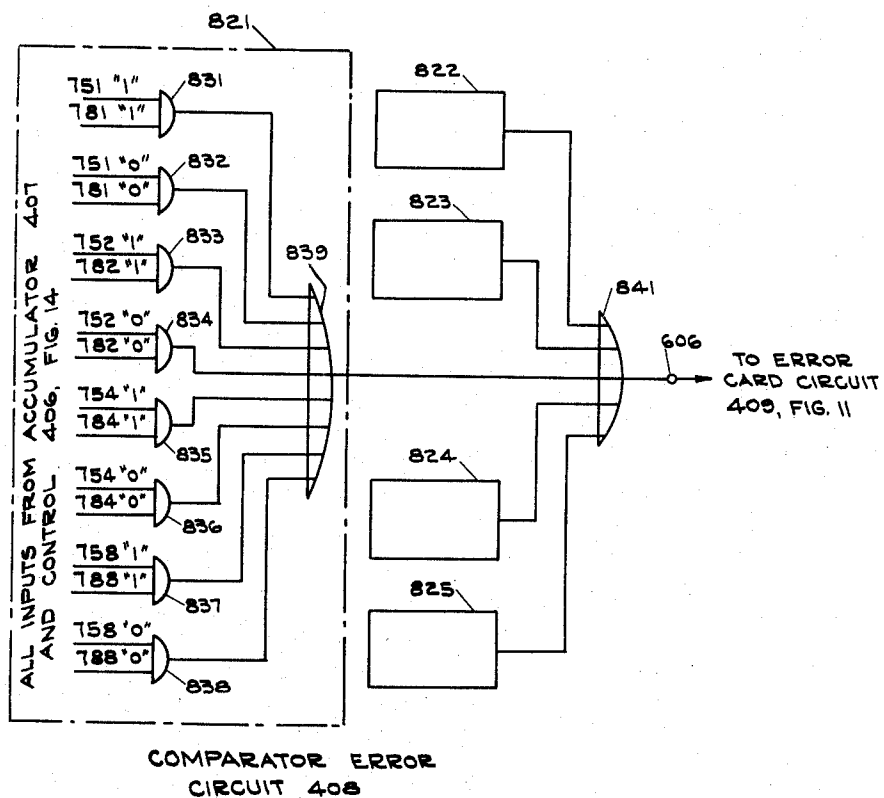
M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 12

FIG. 15



INVENTOR.

MAX E. SALLACH

BY

Wallace, Kinger & Pore

ATT'YS.

Dec. 18, 1962

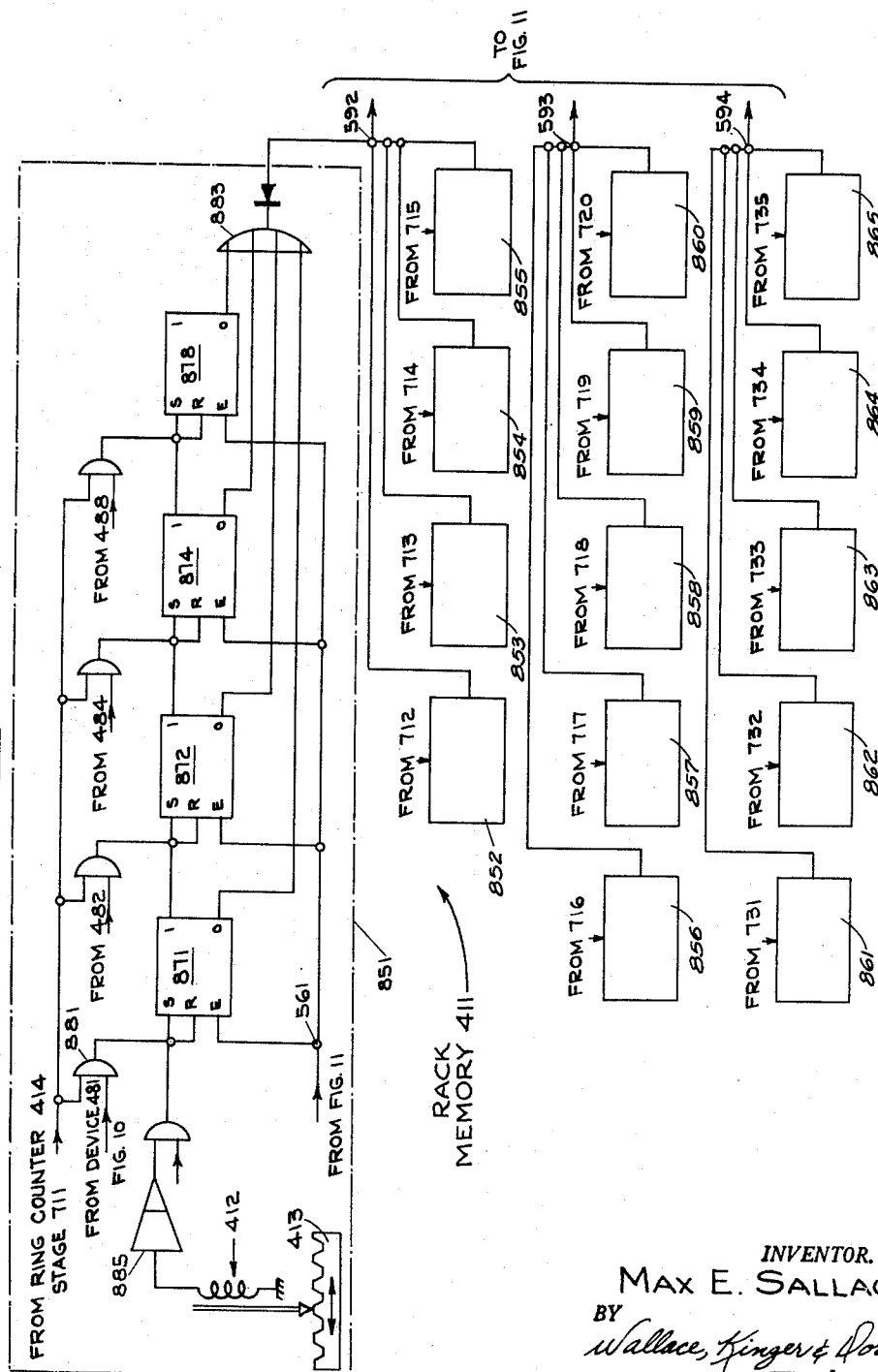
M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 13

FIG. 16



INVENTOR.
MAX E. SALLACH
BY
Wallace, Kinger & Dorn
ATT'YS.

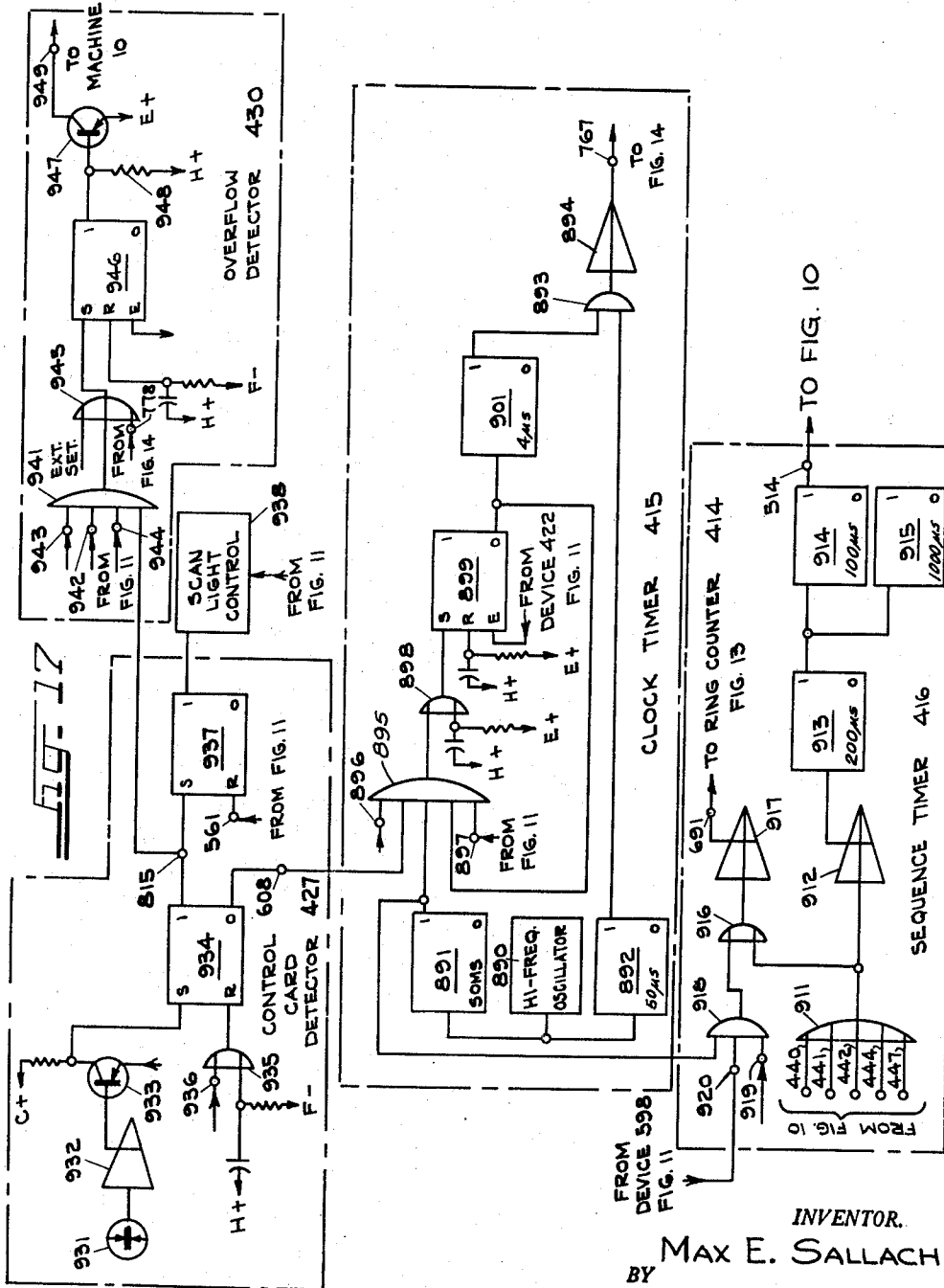
Dec. 18, 1962

M. E. SALLACH
PUNCHING MACHINES

3,069,075

Filed June 14, 1961

15 Sheets-Sheet 14



INVENTOR.
BY MAX E. SALLACH
Wallace, Kinger & Horn
ATTORNEYS.

1

3,069,075

PUNCHING MACHINES

Max E. Sallach, Chesterland, Ohio, assignor to Addressograph-Multigraph Corporation, Cleveland, Ohio, a corporation of Delaware

Filed June 14, 1961, Ser. No. 120,127

13 Claims. (Cl. 234—34)

This invention relates to a new and improved control system for a data-controlled record punch, and more particularly to a new and improved translation and control system for controlling the operation of a punching apparatus to punch record cards, in accordance with a given code, with information corresponding to and representative of a code data that is pre-printed on the record cards in accordance with a parity code. This application is a continuation-in-part of application Serial No. 30,601, filed May 20, 1960, now abandoned.

In credit systems, and in similar record keeping systems, it is frequently desirable to record the initial data as rapidly as possible and in a form which permits subsequent conversion to a data code, or "machine language" that can be used by accounting machines, computers, and like business machines. In one business system of this kind, which is specifically intended to handle credit information, a record card is imprinted with the requisite data at the time of the credit transaction. The required information, which may include the serial number of the person receiving credit, the serial number of a branch business establishment, the amount of the transaction, and other pertinent data, is printed on a record card in coded form; it may also be printed in visually readable form at the same time. Preferably, the code employed is a relatively simple one and occupies a minimum of space, since at least some parts of the code data may necessarily be applied to a relatively small embossed printing device used as a credit card. Subsequently, it is necessary to convert the printed code data into a form which may be used with conventional accounting machines or like apparatus. In the specific example described hereinafter, the initial code data is ultimately converted to a conventional decimal code of the kind used in many accounting machines, although other forms of machine-usable code may also be employed. The present invention is directed to a translation and control system for the control of a reproducing punch which is effective to punch the pre-printed data in the record cards for subsequent use by accounting machines.

In a credit system, particularly where a large number of branch offices or establishments are involved, as in the case of filling stations, there are several requirements which must be met in a control system of the kind with which the present invention is concerned. It goes without saying that the control of the reproducing punch must be quite accurate in order to preserve the basic integrity of the accounting information. This accuracy must also be maintained in situations where the pre-printed record cards may be accumulated over a period of time and may become smeared, marked, or otherwise defaced. Furthermore, the control system must maintain substantial accuracy even when the pre-printed data marks are displaced slightly from their normal reference positions on the record cards. Displacement of the data may be occasioned by variations in alignment of the record cards in the printing machines employed to print the code data on the cards. The individual operators using these data printing machines may, in at least some instances, affect their operation by the manner in which they operate the machines. On the other hand, the requirement for accuracy of operation under adverse conditions is no more important than the requirement that the control system be susceptible of high speed operation. In many credit

2

systems, the volume of data is quite substantial, to say the least, so that the speed at which the reproducing punch operates is a critical factor in determining the economic utility of the entire credit system.

It is an object of the present invention, therefore, to provide a new and improved control system for a punching apparatus which is effective to punch data in record cards, in accordance with a given data code and in response to information which is pre-printed on the cards in a substantially different code. Specifically, the printed data code comprises a two-element parity code, although other parity codes could be used.

A further object of the invention is to assure accurate and effective operation of a reproducing record card punch, actuated in accordance with code data that is pre-printed on the cards being punched, despite the presence of extraneous marks on the cards.

Another object of the invention is to provide a continuous and effective check of the data being punched in record cards, to make sure that all of the requisite data is punched and that no extraneous data is punched in the cards.

An additional object of the invention is to provide a new and improved control system for a reproducing punch utilized to punch accounting and similar data in record cards in accordance with code data pre-printed on the cards and to render that control system substantially independent of any requirement for precise positioning of the data in a reference area on each record card. That is, it is an object of the invention to permit at least some variation in the positioning and alignment of the pre-printed code data on the record cards without adversely affecting operation of the punch control system.

An additional object of the invention is to provide a new and improved control system for a reproducing punch constructed to operate in accordance with a given code or "machine language" without requiring that the control system itself be actuated by the same data code.

A particular object of the invention is to provide for high speed operation of a control system for a card punch actuated by pre-printed code data on the record cards being punched without entailing any sacrifice in accuracy of operation and without requiring undue precision or the absence of extraneous markings in the preparation of the record cards themselves.

Another object of the invention is to provide a direct and accurate comparison of the setting of individual punch elements, in a control system for a card punch, with the original data supplied to the set-up apparatus that actuates the punch.

An additional object of the invention is to permit rapid and effective comparison of the total of all code data from a series of detail cards, in a card punch, with the corresponding data from a control or summary card, and to actuate the card punch to afford a positive indication of error if the comparison shows any difference.

A specific object of the invention is to provide a new and improved translation and control system, for a high speed card punch, that inherently and effectively protects the integrity of the punched data with respect to additions to or omissions from the input data supplied thereto.

Thus, the control system of the present invention is applied to a punching apparatus, operable in accordance with a given machine code, which is utilized to punch data in record cards in accordance with a given data code that is different from the machine code, the punched data corresponding to and being representative of data which are pre-printed on the cards in accordance with a parity code. A two-element parity code is preferred, but others can be used. In most instances, the parity code is substantially different from both the punched data code and the machine code. A control system constructed in

accordance with the invention comprises means for feeding the pre-printed record cards in sequence through a scanning station to a punching station. The scanning station includes photoelectric sensing means which are employed to scan the pre-printed code data on each of the cards and to develop parity code signals representative of that data. The parity-code signals are applied to a parity checking circuit which develops a control signal indicative of the presence of extraneous marks or of the absence of any of the required code marks on each of the cards. The parity-code signals are also applied to a code translator or convertor which is coupled to the photo-electric scanning means; this code translator is employed to translate the parity-code signals into machine-code signals. The code translator, in turn, is coupled to a storage matrix which stores the machine-code signals. In addition, the control system includes actuation means, coupled to the storage matrix, which are effective to actuate the punching apparatus in accordance with the stored machine code signals upon advancement of each record card from the scanning station to the punching station. The parity checking circuit, on the other hand, may be employed to interrupt operation of the machine, to at least some extent, or to warn the machine operator when a discrepancy is detected with respect to the required pattern of parity code marks.

Other and further objects of the present invention will be apparent from the following description and claims and are illustrated in the accompanying drawings which, by way of illustration, show preferred embodiments of the present invention and the principles thereof and what is now considered to be the best mode for applying these principles. Other embodiments of the invention embodying the same or equivalent principles may be made as desired by those skilled in the art without departing from the present invention and the purview of the appended claims.

In the drawings:

FIG. 1 is a perspective view of a punching apparatus in which a control system constructed according to the present invention may be incorporated;

FIG. 2 illustrates a record card containing pre-printed code data utilized by the control systems of the present invention, and also shows the same data in punched decimal-code form in the record card;

FIG. 3 is an illustrative diagram utilized to explain the machine code or "language" for the punching apparatus of FIG. 1;

FIG. 4 is a block diagram of a translation and control system constructed in accordance with one embodiment of the present invention;

FIG. 5 is a detail schematic diagram of a punch check circuit employed in the system shown in FIG. 4;

FIG. 6 is a schematic diagram showing, in detail, a member of different circuits employed in the system of FIG. 4, including the sensing, amplification, code translation, and parity checking circuits;

FIG. 7 is a detail schematic diagram showing several stages of the data storage matrix and associated counter for the embodiment of FIG. 4;

FIG. 8 is a block diagram of a translation and control system constructed in accordance with a preferred embodiment of the present invention;

FIGS. 9A through 9J are explanatory figures used to illustrate the significance of symbolic circuit element representations used in succeeding drawings;

FIG. 10 is a logic circuit diagram showing the data sensing devices and certain code translation and error detection apparatus of the system of FIG. 8;

FIG. 11 is a logic circuit diagram of further error detection and control devices of the system of FIG. 8;

FIG. 12 illustrates a driver and storage circuit matrix incorporated in the system of FIG. 8;

FIG. 13 is a logic circuit diagram of a ring counter used to control the driver matrix of FIG. 12;

FIG. 14 illustrates a translation, control, and accumulator circuit employed in the system of FIG. 8;

FIG. 15 is a logic diagram for an error detection circuit incorporated in the system of FIG. 8;

FIG. 16 illustrates a storage circuit employed to verify the setting of punch actuation elements under control of the system of FIG. 8;

FIG. 17 is a logic diagram showing several auxiliary control circuits incorporated in the system of FIG. 8; and

FIGS. 18 and 19 are detailed schematic diagrams of typical operating circuits that may be used in the system of FIGS. 8-17.

FIG. 1 illustrates a punch apparatus or mechanism 10 that is actuated under the control of a translation and control system according to the present invention. The machine 10 is used to punch data in record cards, in accordance with a conventional data code (in this instance a decimal code) and in response to code data previously printed upon the cards. The reproducing punch 10 comprises a first storage magazine 11 within which a quantity of pre-printed record cards are stored. From the storage magazine 11, the cards are individually fed to a conveyor or transfer mechanism generally indicated by reference numeral 12. The transfer mechanism 12 feeds the cards sequentially through a scanning station 13 to a punching station 14. The conveyor 12 also feeds the punched cards from the punching station 14 outwardly of the machine to a receiving hopper 15.

The mechanical aspects of the reproducing punch 10 are essentially similar to the punching machine described and claimed in Patent No. 2,710,406 to Walter T. Gollwitzer issued June 7, 1955. Accordingly, it is unnecessary to afford a detailed description or illustration of the mechanical operating elements of the punch. Briefly, pre-printed record cards are fed sequentially from the magazine 11 to the conveyor 12. Each record card, when it reaches the conveyor, is fed through the scanning station 13. In the scanning station, the pre-printed code markings on the card are sensed photoelectrically, as described in detail hereinafter. The code signals developed by the sensing apparatus at the station 13 are translated from the parity code used on the record cards into code signals corresponding to the machine code normally used to control the reproducing punch 10. The code signals developed by the sensing apparatus at the station 13 are translated from the parity code used on the record cards into code signals corresponding to the machine code normally used to control the reproducing punch 10. The code signals are stored, in a storage matrix described hereinafter, until the record card reaches the punching station 14. When the record card is in the desired position in the punching station 14, the stored data are employed to actuate the punch mechanism, which punches the record card in accordance with the same data that it carries in printed form. Thereafter, the card is removed from the punching station and deposited in the hopper 15.

In some instances it may be necessary or desirable to effect an auxiliary printing operation in the machine 10. For this purpose, a printing station 16 may be incorporated in the reproducing punch 10, preferably intermediate the punching station 14 and the receiving hopper 15. Inasmuch as a suitable printing apparatus is described in complete detail in the aforementioned Gollwitzer patent, and since the control system of the present invention is not concerned with the printing operation, no further description of the printing station 16 is provided herein.

FIG. 2 illustrates a record card 21 which is pre-printed with accounting or other data in accordance with a parity code, in this instance a two-of-five code. The card 21 represents a preferred form of card employed in the control system of the present invention. In this regard, the actual size and shape of the card 21 are not particularly important, nor is the location of the pre-printed code data 22 on the card especially critical. However, the

5

code markings employed for the data 22 are of some importance with respect to the operation of the control system and, accordingly, require description in detail. The illustrative code data 22 shows the individual markings employed for each of the numbers one through ten. In each instance, the numerical value is represented by two code marks, the actual numerical value being set forth immediately above the corresponding code markings. The code employed is a parity code; that is, there are no code designations which include more than two marks and there are no code designations which comprise less than two marks. Starting from bottom to top, the five code levels or columns for the code data 22 correspond generally to the numerals 1, 2, 4 and 7, the top column being the parity column and being identified by the letter P. The same designations apply to the alignment of the photocells used to sense the data 22. The alignment of the photocells at the sensing station is shown at the left-hand side of FIG. 2, the photocells being designated by the reference characters 31, 32, 34, 37 and 40 respectively.

The card 21 is also punched with the same information as the pre-printed code data 22 in the form of punched data apertures 41. The punched data code, in this instance, is a conventional decimal code of the kind used by a wide variety of accounting machines. It will be recognized that the punched data 41 corresponds exactly to the pre-printed data 22. In addition, the punch unit 14 (FIG. 1) may include manually settable punch members for punching additional data in the card, as indicated in FIG. 2 by the further punched data 42. Furthermore, the reproducing punch 10 may be provided with additional and independent control means for controlling the auxiliary punch data 42 if desired.

FIG. 3 illustrates the basic machine code or language employed to control operation of the reproducing punch in the aforementioned Gollwitzer patent. This data code, which is commonly used in connection with printing devices employed in addressing machines and the like, is substantially different from the parity code used for the data 22 (FIG. 2). Consequently, it is not possible to control the reproducing apparatus 10 directly from the sensing of the data 22, and the translation and control system of the present invention provides for translation from the pre-printed code data 22 to the basic machine code illustrated in FIG. 3. Of course, it would be possible to use the code of FIG. 3 for the pre-printed data on the cards, but the control system for the present invention affords substantial advantages as compared with an arrangement of this kind. Moreover, it would also be possible to construct the reproducing punch 10 for direct actuation by the parity code shown in FIG. 2, but this would prevent the use of conventional coded printing devices in control of the reproducing punch.

FIG. 4 illustrates, in block diagram form, the basic control system of one embodiment of the present invention. The photocells 31, 32, 34, 37 and 40 are shown in FIG. 4 as a part of the control system 48; the order of alignment of the photocells is slightly different than in FIG. 2 in order that they may correspond to the circuit alignment described hereinafter in connection with FIG. 6. The photocell 31 is connected to a pre-amplifier circuit 51 which, in turn, is connected to an amplifier circuit 61, the output of the amplifier 61 being connected to a pulse voltage adder circuit 71. The photocell 32 is connected in circuit with a pre-amplifier 52 and an amplifier 62, the amplifier 62 having its output stage connected to the adder circuit 71. The circuit for the photocell 34 comprises a pre-amplifier 54 and an amplifier 64, whereas the circuit for the photocell 37 includes a pre-amplifier 57 and an amplifier 67. The operating circuit for the parity photocell 40 is essentially the same and includes a pre-amplifier 60 and an amplifier 70. The individual operating circuits for the photocells are carried through the adder circuit 71 to a translator 72 which is effective to translate the 1-2-4-7-P parity code of the pre-printed data (FIG. 2)

6

to the 2-4-6-8-9 machine code required by the reproducing punch and illustrated in FIG. 3. The relative code values of the input and output circuits of the translator 72 are designated in FIG. 4 for convenience. The output of the translator 72 is coupled to a storage matrix 73 which, in the illustrated arrangement, includes ten storage stages each having five individual storage levels corresponding to the five significant elements in the output code of the translator. The storage matrix 73 also includes the driving circuits for the reproducing punch, this portion of the control system being described in greater detail hereinafter in connection with FIG. 7.

The adder circuit 71 is coupled to a parity check circuit 74 which, in turn, is coupled to a ring counter 75. The ring counter 75 is utilized to control the timing of recording in the storage sections of the storage matrix 73. In addition, the ring counter 75 is coupled to a digit count check circuit or punch check circuit 76 which is utilized to make sure that each record card includes all of the necessary pre-printed code data, and no excess data, before a punch operation is effected.

In considering operation of the system illustrated in FIG. 2, it may first be assumed that the first column 24 of the pre-printed data 22 (FIG. 2) is moved into sensing position relative to the sensing photocells 31, 32, 34, 37 and 40. At this position, the photocells sense the presence of code markings in the first and parity columns; that is, the photocells 31 and 40 are effective to produce output signals indicating the presence of pertinent code markings. Since there are no code markings in the other three rows of the pre-printed data code column 24, similar signals are not generated by the photocells 32, 34 and 37. The two significant voltage signals are applied to the voltage adder circuit 71 which supplies to the parity check circuit 74 a signal that is representative of the sum of the two applied signals. The parity check circuit 74 is included in the system to make sure that two, and only two, marks are sensed. If this condition is maintained, the parity check circuit applies a pulse signal to the ring counter 75, actuating the counter to apply a conditioning signal to the first column in the storage matrix 73.

The two significant data code signals are also applied to the code translator 72, which translates these signals into the machine code (FIG. 3). In this instance, significant output signals from the translator would appear on the output lines designated as lines 2 and 9 in FIG. 4, since this is the equivalent to the coded numerical value "one" that appears in column 24 of the pre-printed code data 22 (FIG. 2). In this manner, by a joint action of the ring counter 75 and the translator 72, the number "one" is recorded in the first stage of the storage matrix 73.

This process is repeated until all of the code data 22 are recorded, in translated form, in the storage matrix 73. When the recording operation is complete, the ring counter applies an output signal to the punch check circuit 76 which may be utilized to condition the reproducing punch for a punching operation. Conversely, if some portion or stage of the recording operation is not completed satisfactorily, and the ring counter does not count out, a punch operation is not effected. In this manner the punch check circuit 76 prevents a punching operation except when the control system has determined that the desired number of data items, as represented by the full number of stages in the matrix 73, have been sensed, translated, and recorded in the storage matrix.

In some instances the printing machine or other means utilized to apply the pre-printed code data 22 to one or more record cards may fail to operate properly, or some other accident may occur which prevents accurate printing of one of the code designations. As a consequence, it may be that only one input signal is applied to the adder circuit 71, resulting in a low-amplitude output signal to the parity check circuit 74. When this happens, the parity check circuit 74 does not apply the requisite

conditioning pulse to the ring counter 75. As a consequence, at the end of a sensing operation, the counter does not count out completely and a punch operation cannot be effected. Instead, the machine may be interrupted in operation or a warning signal may be actuated to let the operator know that a card has traversed the punching machine without being punched.

Similarly, in some instances additional code markings, smudges, or other undesirable markings may be interposed in the data code field of the card 21 (FIG. 2). If an extraneous marking of this kind is one to which the photocells are sensitive, and if the marking is positioned in alignment with one of the data columns, it may be that three or more of the photocells will develop significant output signals. In this event, the amplitude of the output signal from the adder circuit 71 to the parity check circuit 74 is also modified and again represents an erroneous operation. The parity check circuit 74, in this instance, again fails to apply the necessary actuating signal to the ring counter 75 and thus again prevents an erroneous punching operation.

FIG. 6 illustrates, in substantial detail, a number of the specific operating circuits incorporated in a preferred embodiment of the control system 48 shown in block form in FIG. 4. More specifically, the circuit shown in FIG. 6 includes the complete construction of the pre-amplifier 60 associated with the parity photocell 40, the amplifier 70, the adder circuit 71, the code translator 72, and the parity check circuit 74. In this figure, the amplifiers 61, 62, 64 and 67 are also shown; however, since these circuits are essentially similar to the amplifier 70, they are not illustrated in detail. For the same reason, it is deemed unnecessary to repeat the pre-amplifier and photocell circuits in FIG. 6.

In the specific circuit arrangement illustrated in FIG. 6, the photocell 40 is shown as a phototransistor. It should be understood, however, that this photocell may comprise a solid state photo-sensitive diode or any other suitable photoelectric sensing device if desired. Furthermore, other forms of radiation-sensitive pick-up may be employed, depending upon the nature of the code markings applied to the record cards. However, photoelectric pick-ups are preferred and particularly solid state devices because these are quite small in size, permitting condensation of the code data 22 (see FIG. 2) into a minimum size without adversely affecting the accuracy and response speed of the system.

The pre-amplifier 60, as shown in FIG. 6, may comprise two stages including a first transistor 101 and a second transistor 102. The base electrode of the first-stage transistor 101 is connected to the collector electrode of the photocell 40, the emitter of the photocell being grounded. A suitable bias voltage is applied to the base electrode of the transistor 101, the biasing circuit comprising a resistor 103 connected from the base electrode to ground and a second resistor 104 connected to a negative D.C. supply. In this instance, the D.C. supply comprises a voltage divider including two resistors 105 and 114 connected in series with each other between ground and a suitable source of uni-directional operating potential herein designated as E—.

The collector electrode of the transistor 101 is connected to the D.C. supply source E— through the voltage divider 105, 114. The emitter electrode in the first stage is returned to ground through a resistor 106 and is also coupled to the base electrode of the second transistor 102 through a coupling capacitor 107. The base electrode in the second stage of the pre-amplifier is returned to ground through an input resistor 108. The emitter electrode of the transistor 102 is returned to ground through a biasing circuit comprising a pair of resistors 109 and 111 which are connected in series with each other, the resistor 111 being by-passed by a capacitor 112.

The collector electrode of the second-stage transistor

102 in the pre-amplifier 60 is connected to the D.C. supply source E— through a circuit comprising, in series, a resistor 113 and the voltage divider 105, 114. The output circuit for the pre-amplifier includes a coupling capacitor 115 which is connected to the collector of the transistor 102 and to a potentiometer 116, the other fixed terminal of the potentiometer being connected to the center terminal of a voltage divider comprising a pair of resistors 117 and 118 connected in series between the negative D.C. supply E— and ground. The variable tap 119 on the potentiometer 116 constitutes the output terminal for the pre-amplifier 60.

The amplifier 70 is a three stage amplifier comprising three vacuum triodes 121, 122 and 123. The output terminal 119 of the pre-amplifier is connected to the control electrode of the first triode 121. The cathode of the first stage triode is grounded. The anode is connected to a suitable source of positive-polarity unidirectional operating voltage B+ through a circuit comprising, in series, a resistor 124 and a resistor 125. The resistor 125 is bypassed to ground by a capacitor 126.

The output circuit for the first stage triode 121 comprises a coupling capacitor 127 which is connected in series with a resistor 128 between the anode of the triode 121 and the control electrode of the second stage triode 122. The control electrode of the triode 122 is also returned to ground through a circuit comprising, in series, a diode 129 and a single-pole, single-throw switch 131. A positive bias is applied to the control electrode of the second stage in the amplifier 70 by a voltage divider circuit comprising two resistors 132 and 133 connected in series with each other between the B+ supply and ground, the common terminal of the two resistors being connected to the control electrode of the tube 122. The cathode of the second stage triode is grounded. The anode of this stage is connected to the B+ supply through a load resistor 134. The output circuit to the third stage comprises a coupling capacitor 135 which is connected between the anode of the triode 122 and the control electrode of the output stage 123. The control electrode of the third stage triode 123 is also returned to a negative supply voltage, herein designated as F—, through an input resistor 136.

The anode of the third stage triode 123 in the amplifier 70 is connected to the B+ supply through a resistor 137. This stage of the amplifier comprises a cathode follower. Thus, the output circuit comprises a pair of resistors 138 and 139 which are connected in series with each other between the cathode and ground, the output terminal being the common terminal of these two resistors as indicated by reference numeral 140. The output terminal 140 of the amplifier 70 is connected through a resistor 142 to the first stage of the parity check circuit 74, which is described in detail hereinafter. Similarly, the output terminals of the amplifiers 61, 62, 64 and 67 are connected through corresponding resistors 143, 144, 145 and 146, respectively, to the parity check circuit. Moreover, the output terminals of these amplifiers are individually returned to ground through the resistors 147, 148, 149 and 150. Thus, the resistors 142-146 comprise a voltage adder for the output signals from the amplifiers 61, 62, 64, 67 and 70 and thus constitute the adder circuit 71 (see FIG. 4).

The input stage of the parity check circuit 74 comprises a triode 151, the control electrode of this triode being connected to each of the resistors 142-146 of the voltage adder circuit. The anode of the input triode 151 in the parity check circuit is connected to the B+ supply through a resistor 152. The cathode is returned to ground through a resistor 153. Both the anode and cathode circuits of the triode 151 are utilized as output circuits, so that the triode functions both as a conventional amplifier and as a cathode follower.

The cathode follower output circuit for the triode 151 comprises a coupling capacitor 154 which is connected to the cathode of the tube, the coupling capacitor being con-

ected through a resistor 155 to the movable tap on a potentiometer 156. One fixed terminal on the potentiometer is connected to the negative supply voltage E—, whereas the other fixed terminal of the potentiometer is returned to ground. The coupling capacitor 154 is also connected to the control electrode of a triode 157 which is combined with a second triode 158 in a one-shot multi-vibrator circuit. Thus, the biasing circuit comprising the resistor 155 and the potentiometer 156 affords a negative bias on the control electrode of the multivibrator tube 157.

The multi-vibrator circuit comprising the triodes 157 and 158 is substantially conventional in construction. The cathodes of the two triodes are connected together and are returned to ground through a resistor 159. The anode of the triode 157 is connected to the B+ supply through a load resistor 161, the anode of the triode 158 being connected to B+ through a resistor 162. The coupling circuit between the two triodes comprises a coupling capacitor 163 connected between the anode of the first triode of the control electrode of the second triode, the control electrode of the second triode being connected to the B+ supply through a resistor 164. The circuit parameters are such that the triode 157 is normally maintained non-conductive, the triode 158 normally being held conductive. When a positive-going pulse signal is applied to the triode 157, and when this pulse signal exceeds a given threshold amplitude, the tube 157 is driven conductive and the triode 158 is momentarily cut off. Upon completion of the applied pulse signal, the tube 158 is again driven to conduction and the tube 157 is cut off.

The anode output circuit for the input triode 151 of the parity check circuit 74 comprises a coupling capacitor 165 which is connected from the anode of the tube 151 to the control electrode of an amplifier triode 166. The control electrode of the triode 166 is also connected to a voltage divider comprising a pair of resistors 167 and 168, the resistors 167 and 168 being connected between the B+ supply and ground to afford a positive bias for the control electrode. The cathode of the triode 166 is returned to ground and the anode of this tube is connected to the B+ supply through a load resistor 169.

The inverter or amplifier stage comprising the triode 166 is a coupled to a one-shot multi-vibrator circuit, comprising a pair of triodes 171 and 172, which is essentially similar to the multi-vibrator including the triodes 157 and 158. Thus, the anode of the triode 166 is coupled to the control electrode of the tube 171 by a coupling capacitor 173. The control electrode of the tube 171 is provided with a negative bias by means of a circuit comprising a resistor 174 connected from the control electrode to the movable tap on a potentiometer 175. The potentiometer 175 is connected between the E— supply and ground. As before, the cathodes of the two triodes 171 and 172 are connected to each other and are returned to ground through a resistor 176. The anodes of the triodes 171 and 172 are connected to the B+ supply through two resistors 177 and 178, respectively. The anode of the tube 171 is coupled to the control electrode of the triode 172 by a coupling capacitor 179. The control electrode of the tube 172 is connected to the B+ supply through a bias resistor 181. The circuit parameters are again selected to afford a one-shot operation as described hereinabove.

The one-shot multi-vibrator comprising the triodes 171 and 172 is coupled to an inverter amplifier stage comprising a triode 183. The coupling circuit comprises a coupling capacitor 184 that is connected between the anode of the tube 172 and the control electrode of the triode 183. The control electrode of the tube 183 is returned to ground through an input resistor 185. The cathode of the tube is grounded and the anode is connected to the B+ supply through a pair of resistors 186 and 187 that are connected in series with each other.

The final stage of the parity check circuit 74 comprises

a triode 191 having an input circuit coupled to the inverter stage 183 and to the one-shot multi-vibrator 157, 158. The coupling circuit from the triode 183 comprises a capacitor 192 that is connected to the junction of the resistors 186 and 187 in the anode circuit of the triode. The capacitor 192 is also coupled to the control electrode of the tube 191 through an input resistor 193. A diode 194 is connected from the common terminal of the capacitor 192 and the resistor 193 to ground. The other coupling or input circuit to the tube 191 is similar, and comprises a capacitor 195 and a resistor 196 connected in series with each other between the anode of the multi-vibrator tube 157 and the control electrode of the output tube 191. A diode 197 is connected from the common terminal of the impedances 195 and 196 to ground.

The output tube 191 of the parity check circuit 74 is connected in a cathode follower circuit of quite simple configuration. Thus, the anode of the triode is connected to the B+ supply. The cathode of the tube, which in this instance is the output electrode, is returned to ground through a load resistor 198. The output terminal of the final stage in the parity check circuit is indicated by reference numeral 199, and this output terminal is connected to the ring counter 75, which is described in detail hereinafter in connection with FIG. 7.

As noted hereinabove, each of the amplifiers 61, 62, 64, 67 and 70 is coupled to the code translator 72, in addition to the connection to the parity check circuit 74. In FIG. 6, the individual output circuits from the amplifiers to the code translator 72 are identified by the code designations of the amplifiers, these being the code designations "1," "2," "4," "7" and "P" relating back to the code designations for the data 22 (FIG. 2). The code translator 72 is provided with five output circuits comprising the output resistors 202, 204, 206, 208 and 209. These output resistors are individually connected to output coupling capacitors 212, 214, 216, 218 and 219, respectively. The output circuit from the code translator 72 which comprises the resistor 202 and the capacitor 212 is the output circuit for signals corresponding to the code designation "2" in the machine code illustrated in FIG. 3. Similarly, the capacitor 214 and the resistor 204 are the circuit elements which form the "4" code designation circuit under the machine code. The machine code designations are shown in association with the output circuits from the code translator 72 in FIG. 6.

Between the input and output circuits of the code translator, a resistor-diode matrix is provided which performs the necessary translation. The translator resistors are generally represented by the reference numeral 221, and the coupling diodes of the translator by the reference character 222. All of the coupling resistors in the translator are approximately equal in resistance, and the diodes 222 are also essentially identical with each other. Furthermore, the system shown in FIG. 6 for the code translator 72 requires that the resistors 221 be substantially larger than the ground-return resistors, such as the resistor 139, in the input circuits to the code translator. Furthermore, it is also necessary that the resistors 221 be substantially smaller than the output resistors 202, 204, 206, 208 and 209.

In considering the operation of the circuits illustrated in FIG. 6, it may first be noted that the phototransistor 40 is normally maintained conductive, since the photocell is ordinarily illuminated by light reflected from unprinted areas of the record card. When this normal condition is changed, as when a code marking is interposed in the illumination path for the photocell, the photocell is rendered non-conductive, producing a negative-going pulse signal on the base electrode of the translator 101 in the pre-amplifier 60. This negative-going pulse signal appears in the output circuit of the emitter follower stage comprising the transistor 101 and is A.C. coupled to the base electrode of the second stage transistor 102 in the pre-amplifier. The pulse signal is inverted in polarity

11

and appears, at the collector electrode of the transistor 102, as a positive-going pulse. This positive-going pulse is applied to the input circuit of the amplifier 70; an A.C. coupling circuit is employed in this instance so that a positive polarity pulse may be applied to the control electrode of the first triode in the amplifier 70.

The amplifier 70 is substantially conventional in operation. The positive-polarity input signal to the tube 121 is inverted and amplified and is applied to the control electrode of the second stage triode 122. In this stage, the pulse signal is again amplified, inverted in polarity, and applied to the control electrode of the third or output stage comprising the triode 123. Since the output stage is a cathode follower, the output signal from the amplifier 70 appears as a positive-polarity pulse at the output terminal 140. As noted hereinabove, the photocell 40, the pre-amplifier 60, and the amplifier 70 are representative of and are typical of the corresponding circuits used to sense the other code positions in the printed data code illustrated in FIG. 2. Thus, for each sensing operation, it is necessary that two positive polarity pulses appear in the output circuits of the amplifiers 61, 62, 64, 67 and 70.

The output pulses from the amplifiers are added together, in the adding circuit comprising the resistors 142-146, and are applied to the control electrode of the input triode 151 in the parity check circuit 74. The input signal is, of course, a positive-polarity pulse signal, the amplitude being equal to the sum of the output signals from the amplifiers. This positive-polarity input signal is amplified and inverted in the circuit comprising tube 151, and appears as a negative-polarity pulse signal on the control electrode of the triode 166. In the circuit comprising tube 166, the signal is again inverted and amplified, so that the output signal from the tube 166 that is applied to the control electrode of the triode 171 is a positive-going pulse. It should be noted that A.C. coupling is employed between the tubes 166 and 171 and that the tube 171 is normally provided with a negative bias on the control electrode by means of the circuit 174, 175. Assuming that the pulse signal applied to the control electrode of the triode 171 is of sufficient amplitude to drive the tube to conduction, the normal condition when two code markings are sensed, the tube 171 conducts, the tube 172 is driven to cut-off, and a positive-going pulse is produced in the output circuit of the one-shot multi-vibrator. This positive-going pulse is A.C.-coupled to the control electrode of the amplifier tube 183, which amplifies the signal further. The output circuit of the tube 183 is a differentiating circuit; consequently, the output signal from this circuit contains both positive and negative pulses. The negative-going portion of the signal is effectively by-passed to ground through the diode 194. Consequently, the signal effectively applied to the control electrode of the output stage of the parity check circuit 74, which comprises the triode 191, is a positive-going pulse. Consequently, a positive-polarity pulse signal is produced at the output terminal 199 of the tube 191. It is thus seen, that during each cycle of normal operation, the parity check circuit 74 operates to supply a positive-going control pulse or timing signal to the ring counter 75 to advance the counter through one stage, as described more fully hereinafter.

In some instances, it may be that only one code marking is sensed at a given code position. By the same token, there may be an extraneous mark between individual columns of the data code markings 22 on the card 21 (FIG. 2). Under other circumstances, it is apparent that only one of the photocells, such as the photocell 40 in FIG. 6, is cut off from illumination. This being the case, only one of the amplifiers produces an output signal, with the result that the pulse signal applied to the input stage 151 of the parity check circuit 74 is only one-half the normal amplitude. When this occurs, the output signal from the tube 151 that is applied to the multi-vibrator

12

tube 171 is not of sufficient amplitude to cut off the tube 171 and render the tube 172 conductive. Accordingly, no useful output signal is developed at the multi-vibrator and there is no effective control signal applied to the ring counter 75. If the marking has occurred at an incorrect position in the data code (that is, if it results from an undesirable pencil mark, smudge, or some other marking between the data markings) this simply means that the ring counter is not advanced, no data is recorded in the storage matrix, as explained hereinafter, and the normal operation of the control system continues uninterrupted. On the other hand, if the failure of the parity check circuit to apply a control signal to the ring counter 75 results from improper printing of one of the necessary code markings of the pre-printed data code, the result is that the counter 75 does not count out completely during the scanning of the code data on a particular card. When this happens, machine operation may be interrupted, a warning signal may be actuated to notify the operator that an erroneous operation has occurred, or a punching operation may be omitted as explained hereinafter. Thus, the portion of the parity check circuit 74 comprising the multi-vibrator 171, 172 effectively protects the control system against any situation in which one code marking is sensed instead of the two markings of the parity code required for accurate operation.

It may also happen that an additional marking of some kind may occur, interspersed with the code data 22, at a position such that illumination to three or more of the photocells is interrupted (see FIG. 2). When this happens, three or more of the amplifiers 61, 62, 64, 67 and 70 produce positive-polarity output signals which are applied, through the adder circuits 142-146, to the control electrode of the tube 151. Of course, this excessive-amplitude input signal to the parity check circuit 74 actuates the multi-vibrator 171, 172 in essentially the same way as the normal actuating signal produced by two code markings. However, an input signal of this amplitude also actuates the other one-shot multi-vibrator comprising the triodes 157 and 158. As a consequence, the tube 157 is driven conductive, the tube 158 is cut off, and a pulse signal is produced in the output circuit of the multi-vibrator. The differentiating circuit coupling the multi-vibrator to the output stage of the parity check circuit produces both positive and negative-going pulses, but the positive pulse is by-passed to ground through the diode 197. Consequently, the effective signal applied to the control electrode of triode 191 is a negative-going pulse which effectively subtracts from the normal positive pulse applied to tube 191 from the tube 183. As a result, when too many code markings are sensed, the necessary actuating signal for the ring counter is not developed in the parity check circuit 74. The ring counter fails to advance, and a punch operation is prevented as explained in greater detail hereinafter.

It is thus seen that the lower portion of the circuit 74, comprising the one-shot multi-vibrator 157, 158, protects the control system against malfunction which might otherwise result from the presence of additional extraneous markings interspersed with desired markings in the pre-printed code data on the cards. Of course, the circuits comprising triodes 151 and 166 also operate to apply a similar input signal to the triode 157 when only two code markings are present at a given scanning position on the card, but this signal is not of sufficient amplitude to actuate the multivibrator 157, 158 and, consequently, normal operation is permitted as described hereinbefore.

To illustrate the operation of the code translator 72, one or two examples of specific translation operations should be sufficient. For example, the number "one" is represented in the data code markings 22, by code marks in the "1" and "P" positions (see FIG. 2). Consequently, when this code marking is sensed, a positive-polarity signal appears at the code translator input terminals

marked "P" and "1." The signal appearing at the "P" terminal is applied to the output resistor 202, with the result that a positive-going signal pulse is transmitted through the coupling capacitor 212. At the same time, a positive-polarity pulse signal is supplied to the output resistor 209, resulting in the transmission of a positive pulse to the capacitor 219. Thus, signals corresponding to the machine-code values "2" and "9" are generated in the output of the translator. Because a positive-polarity pulse is applied to the "1" input terminal "one" of the code translator, the four diodes connected to this input terminal are maintained non-conductive; consequently, the pulse signal applied to the uppermost one of these diodes from the resistor 221 encounters an extremely high resistance and cannot be by-passed to ground through those diodes and the resistor 147 in the operating circuit of the amplifier 61. Of course, the positive-polarity signals applied to the "1" input terminal cannot be translated effectively through the diodes. As a result, output signals are produced only at the "2" and "9" outputs of the translator, thus indicating the presence of a code "one" in the machine code of FIG. 3.

As a second example, it may be considered that the number "two" is represented in the data code markings 22. In this case, positive-polarity output signals appear at the code translator input terminals marked "P" and "2." The signal appearing at the "P" terminal is applied to the output resistor 202 through the operating circuit comprising the uppermost one of the input resistors 221 in the "P" channel of the translator. However, no signal is effectively applied to the output resistor 209 because the lowermost one of the coupling resistors connected to the "P" input terminals is returned to ground through a low-resistance circuit comprising the "1" input terminal of the translator and the resistor 147 connected thereto. In this regard, it should be remembered that the resistors 147-150, as well as the resistor 139, are all much smaller in resistance than resistors 202, 204, 206, 208 and 209. A similar return circuit to ground is not effected through the "2" input terminal of the input translator because of the positive-polarity input signal applied to this terminal. On the other hand, the only output circuit from the "2" input terminal of the translator 72 is also returned to ground through a low-impedance circuit comprising the resistor 147. Accordingly, this input signal does not develop an output signal at either of the output resistors 202 and 209. Consideration of all of the possible code combination and signals which may appear at the input to the translator shows that the translator effectively converts the input data from the parity code in which it is printed on the cards, such as the card 21 of FIG. 2, to the machine code illustrated in FIG. 3.

FIG. 7 illustrates, in substantial detail, the storage matrix 73 and the ring counter 75 of the control system. Where the control data is in the form of a ten-digit number, as illustrated by the pre-printed code data 22 in FIG. 2, ten storage and counter stages are required. Of course, and as noted hereinabove, more or less stages may be utilized depending upon the number of individual data items employed to actuate the control system. In FIG. 7, only three stages are shown for the storage matrix 73 and for the ring counter 75. However, each of the other seven stages intermediate those illustrated is essentially similar to the stages shown in the drawings.

The storage matrix 73 is arranged in ten columns formed by five rows of storage circuits, only the first, second and tenth columns being illustrated. The individual rows correspond to the code values "2", "4", "6", "8", and "9" of the machine code, and are individually connected to the corresponding output lines of the code translator 72 (FIG. 6). The initial storage stage in the first column and first row of the storage matrix comprises a thyatron 240. The cathode of the thyatron 240 is grounded. The screen electrode 241 of the thya-

tron is connected to the "2" output of the translator 72, being coupled thereto by the capacitor 212 (FIG. 6). An input resistor 242 is connected in series in the input circuit to the electrode 241. The control electrode 243 of the thyatron 240 is connected to a negative-polarity biasing circuit through a connecting circuit comprising, in series, a resistor 244 and a resistor 245. The biasing circuit, in this instance, comprises a voltage divider including a pair of resistors 246 and 247 connected in series with each other between the negative D.C. source E- and ground, the resistor 245 being connected to the common terminal of the resistors 246 and 247.

The anode circuit of the storage tube 240 includes a resistor 248 that is connected between the anode 249 and the B+ supply. A cam-controlled switch 251 is included in series in this circuit. In addition, the anode 249 is also connected to a punch control solenoid, represented by the coil 252. The other terminal of the coil 252 is returned to ground through a resistor 253, a diode 254 being connected in series in this circuit. There is a parallel circuit to the resistor 253 comprising a cam-actuated switch 255 which, when closed, connects the solenoid 252 to the B+ supply. The initial stage of the storage matrix also includes a biasing circuit for the screen electrode 241, this biasing circuit comprising a connection from the resistor 242 through a resistor 256 to a suitable negative D.C. supply designated as G-.

The second stage in the first column of the storage matrix, the initial stage in the "4" row, is essentially similar to the circuit for the tube 240 described immediately hereinabove. Thus, this stage of the storage matrix comprises a thyatron 260, the cathode of the thyatron being grounded. The screen electrode 261 of the thyatron is connected through a resistor 262 to the capacitor 214 in the code translator 72 (see FIG. 6). In addition, the electrode 261 is connected through the resistor 262 and a series resistor 276 to the G- bias supply.

The control electrode 263 of the thyatron 260 is connected through a resistor 264 and the resistor 245 to the negative bias supply comprising the voltage divider 246, 247. The anode 269 of the tube 260 is connected to the B+ supply through a circuit comprising, in series, a resistor 268 and a cam-actuated control switch 271. The anode 269 is also connected to a control solenoid 272 and a circuit comprising, in series, a diode 274 and a resistor 273, the resistor 273 being returned to ground. As in the previously described stage, the solenoid circuit is also connected to the B+ supply, in this instance through a cam-actuated control switch 275.

From the foregoing description, and by comparing the stages comprising the tubes 240 and 260 with the remaining stages in the storage matrix, it is seen that all of these individual storage circuits are essentially identical. In each instance, the input electrode to the stage, from the code translator 72, is connected to the screen electrode of the thyatron. Each of these screen electrodes, which are used as control electrodes, is normally subject to a negative bias through the connection to the G- source. The first control electrode in each stage, such as the electrodes 243 and 263, is also normally biased negatively by the connection to the biasing circuit comprising the resistors 246 and 247. The anode circuits of the tubes are provided with switches for interrupting conduction in the tubes, as described more fully hereinafter, the principal control switch in each instance being connected to the anode of the tube through a suitable resistor. The operating solenoids which are used to set the punches in the machine punch 10, on the other hand, are also connected to the anodes of the various stages and are connected to the B+ supply only upon the closing of cam-actuated switches controlled by the machine itself. In each row of the storage matrix a single switch, such as the switch 255, controls all of the punch-setting solenoids. A similar arrangement could

be employed for the main anode circuits, but the circuit illustrated in FIG. 7 provides a separate cam-actuated switch for each stage in the storage matrix.

The lower portion of FIG. 7 shows three stages of the ring counter 75, these being the first, second, and tenth stages of the counter and corresponding to the illustrated columns of the storage matrix in this figure. The initial stage in the ring counter comprises a thyatron 281 having a cathode 282, a first control electrode 283, a second control electrode or screen electrode 284, and an anode 285. The screen electrode 284 is connected to the cathode 282, the cathode 282 being returned to ground through a resistor 286 that is by-passed by a capacitor 287. The cathode 282 is also connected through a coupling capacitor 288 to the first control electrode or grid in each of the thyatrons in the first column of the storage matrix 73. That is, the coupling capacitor 288 is connected between the cathode 282 of the ring counter tube 281 and the electrode 243 of the storage tube 240 in a circuit that includes, in series, the resistor 244. Essentially the same circuit, but comprising the resistor 264 instead of the resistor 244, is used to couple the first stage of the ring counter to the storage tube 260. Similar circuits connect the first stage of the counter to each of the remaining three stages in the first column of the storage matrix.

The control electrode 283 of the ring counter thyatron 281 is coupled to the parity check circuit 74 through a coupling capacitor 289. That is, the capacitor 289 is connected between the electrode 283 and the output terminal 199 of the parity checking circuit 74 (see FIG. 6). A negative bias is normally applied to the control electrode 283 by means of a biasing circuit comprising a resistor 291 that connects the electrode 283 to the negative D.C. supply E-. In addition, the input or control electrode 283 is also connected to the final stage of the ring counter, this coupling circuit being described in greater detail hereinafter. The anode circuit of the ring counter thyatron 281 comprises a resistor 293 that connects the anode 285 to the B+ supply.

The thyatron 281 is coupled to a second stage thyatron 302 in the ring counter 75 by means of a coupling resistor 303 that is connected from the cathode in the first stage to the main control electrode 304 of the second stage tube. The control electrode 304, like the electrode 283 in the preceding stage, is connected to the parity check circuit 74 through a coupling circuit comprising a capacitor 305. In addition, the electrode 304 is returned to the E-bias supply through a resistor 306 corresponding to the first stage resistor 291.

The cathode 306 and the second control electrode 307 are connected together, in the circuit of the tube 302, these electrodes being returned to ground through a parallel RC circuit comprising a resistor 308 and a capacitor 309. The output circuit from the ring counter tube 302 is also similar to that of the first stage and comprises a coupling capacitor 311 that couples the cathode, and the screen electrode of the tube 302 to the control electrode of each of the thyatrons in the second column of the storage matrix 73. As before, a suitable resistor is connected in series in the input circuit to each of the storage matrix thyatrons. The anode of the tube 302 is returned to B+ through the resistor 293. The output circuit of the tube 302 is essentially the same as for the tube 281 and comprises an output resistor 313 that corresponds to the resistor 303 and is employed to couple the cathode of the tube 302 to the control electrode in the next stage.

As noted hereinabove, only the two initial stages and the final stage of the ring counter 75 are shown in FIG. 7. The intervening seven stages, however, are essentially identical to those described hereinabove and shown in FIG. 7 in connection with the thyatrons 281 and 302. Moreover, the final stage of the ring counter is essentially similar, but is shown in detail in order to illustrate the

connection back to the first stage of the counter and also to shown the reset circuit for the counter.

Thus, the final stage of the ring counter 75 comprises a thyatron 321 having a cathode 322, a control electrode 323, a screen electrode 324, and an anode 325. As before, the anode 325 is connected to the B+ supply through the resistor 293. The screen electrode 324 is connected to the cathode 322, these electrodes being returned to ground through a resistor 326 that is by-passed by a capacitor 327. In this instance, the output resistor 328 for the tube is again connected to the cathode, but is connected back to the control electrode 283 in the first stage, since there is no succeeding stage in the counter.

The input circuit to the final stage of the counter, comprising the thyatron 321, is slightly modified as compared with the preceding stages. Thus, a resistor 329 is interposed in series in the input circuit to the control electrode 323, between the control electrode and the coupling capacitor 331 that couples the control electrode back to the parity check circuit 74. The coupling resistor connecting the input circuit of the final stage to the preceding stage is indicated by reference numeral 332, and the bias resistor which returns the control electrode to the E- bias supply is identified by reference numeral 333. The control electrode 323 in the final stage of the ring counter is also connected to a reset circuit comprising a relay 335 having an operating coil 336 and a pair of contacts 337. The contacts 337 are connected in a series circuit which returns the control electrode 323 to ground. The operating coil 336 is connected in series with a current-limiting resistor 338 and a cam-actuated switch 339 between the B+ supply and ground. This reset circuit is utilized to reset the ring counter at the beginning of each cycle of operation, as described more fully hereinafter. The output circuit of the final stage is essentially similar to the previously described stages, and comprises a coupling capacitor 341 which couples the cathode 322 and the screen electrode 324 to the control electrode of each of the thyatrons in the final column of the storage matrix 73. As before, a suitable resistor is inserted in series with the capacitor 341 in each of these coupling circuits.

In considering the operation of the storage matrix 73 and ring counter 75, as illustrated in FIG. 7, it should first be noted that all of the thyatrons in the storage matrix are normally non-conductive. This is because both the control electrode and the suppressor electrode, in each of the individual storage thyatrons, is normally held at a negative potential sufficient to prevent conduction in the tube regardless of whether or not the anode circuit is closed. At the beginning of each cycle, and as described more fully hereinafter, only the thyatron 321 in the final stage of the ring counter is held conductive, this condition being necessary for an accurate counting and recording operation.

At the beginning of a recording operation, in the interpretation of the code data 22 on the record card 21 (see FIG. 2), three signals are applied to the circuits shown in FIG. 7. Thus, the data item first sensed in reading the pre-printed code data 22 is the numerical value "one." The sensing of this data item causes positive-polarity signals to be applied to the "2" and "9" inputs of the storage matrix 73 from the translator 72, as described hereinabove. At the same time, a positive-polarity signal is also applied to the control electrode in each stage of the ring counter 75 from the parity check circuit 74. In the ring counter, however, because the tube 321 is conductive, the control electrode 283 of the initial thyatron 281 is at a higher potential than the control electrodes of the other ring counter thyatrons, including tube 321. This difference is occasioned by the connection from the cathode of the tube 321 to the control electrode 283 of the tube 281, there being a substantial voltage drop across the cathode resistor in the final stage of the counter. Consequently, the signal

from the parity check circuit 74 causes only the thyatron 281 to become conductive. When the first stage thyatron conducts, the total voltage drop across the resistor 293 increases, dropping the anode voltage on the tube 321 to an extent sufficient to extinguish conduction in this tube. Furthermore, conduction in the tube 281 is effective to develop a positive potential on the cathode and the screen electrode in this tube, due to the voltage drop across the resistor 286. Thus, a positive-polarity signal is applied to the control electrode in each stage of the first column of the storage matrix 73. This signal does not cause the "4," "6," or "8" stages in the first column of the storage matrix to become conductive, since the negative bias applied to the screen electrode in each of the tubes in these stages is sufficient to prevent ionization within the tubes. However, the positive-polarity signal from the first stage of the ring counter coincides in time with the positive-polarity signals applied to the "2" and "9" stages in the first column of the storage matrix, with the result that the thyatrons in each of these stages are rendered conductive. Of course, it is necessary that the cam-actuated switches in the anode circuits of these tubes, such as the switch 251 in the "2" stage, be closed. These switches are maintained closed in all columns and stages of the storage matrix throughout the recording operation. However, the cam-actuated switches in the solenoid circuits are not closed at this time, examples of these switches being the switches 255 and 275. It is thus seen that, upon sensing the first item of the pre-printed data 22, the numeral value "one" is recorded in the storage matrix 73 in the machine code of FIG. 3, since recording is effected in the "2" and "9" stages of the first column in the storage matrix.

When the next data item is sensed, positive-polarity input signals are applied to the circuit of FIG. 7 at just two places. That is, an input signal is applied to the ring counter 75 from the parity check circuit 74, and a positive-polarity data signal is applied to the input "2" of the storage matrix. There are no other data input signals to the storage matrix, since the numerical value "two" is represented by only the "2" input in the machine code. When these signals are applied to the circuit of FIG. 7, the second-stage thyatron 302 in the ring counter is driven conductive. Only the tube 302 is driven to conduction by the input signal to the parity check circuit 74, because the control electrode 304 in this tube has previously been held at a higher potential than the input electrodes to the other tubes, due to the fact that the first-stage thyatron 281 has been conductive and the control electrode 304 is connected back through the resistor 303 to the cathode of the first-stage thyatron. As before, conduction in the tube 302 causes the anode voltage to drop to a sufficient extent to extinguish the preceding tube 281, thereby stepping the ring counter through one count. Furthermore, conduction in the second stage 302 of the counter results in the application of a positive-polarity pulse signal to the control electrode in each of the thyatrons in the second stage of the storage matrix 73.

In the second stage of the storage matrix 73, as in the first stage, two coincident signals are required to render any of the thyatrons conductive. The only thyatron in this stage of the storage matrix to which two input signals are applied is the "2" stage thyatron at the top of the second column. Accordingly, only this tube is rendered conductive, in the second stage of the storage matrix, recording the desired numerical value therein. This process is continued until the final-stage thyatron 321 is rendered conductive and the final data item is recorded in the tenth column of the storage matrix 73. In the final stepping action of the ring counter 75, an output signal is also applied to the punch check circuit 76 (FIG. 5) and this signal is utilized to trigger the punch check circuit and actuate a punch operation, as described more fully hereinafter.

When the control system is first placed in operation, after having been completely shut down, it is difficult to predict, with any certainty, which stage of the ring counter 75 may be rendered conductive, if any. On the other hand, and as noted hereinabove, effective operation requires that the final thyatron 321 be conductive at the beginning of any operation of the control system. To achieve this purpose, the reset relay 325 is energized by closing of the switch 339, thereby closing the contacts 327. When this is done, a positive-polarity signal is applied to the control electrode 323 of the ring counter stage 321. Consequently, the tube 321 is effectively ionized and this tube becomes conductive. Inasmuch as only one thyatron can conduct, in the ring counter, at any given time, the operation of the reset relay 335 is effective to provide a positive reset control and make sure that only the final stage of the ring counter is energized at the beginning of each sensing cycle. Since it is possible that the ring counter will not count out completely in any given sensing operation, as noted hereinbefore, due to the operation of the parity check circuit 74, the switch 339 is closed to reset the ring counter at the beginning of each sensing operation. The switch 339 can, for example, be actuated by a cam driven in synchronism with the feeding of cards from the magazine 11 in the punching mechanism 10 (FIG. 1) to assure accurate synchronization of this part of the operation with the remainder of the system.

The punch check circuit 76 is illustrated in FIG. 5, and comprises a thyatron 351 having a cathode 352, a control electrode 353, a screen electrode 354, and an anode 355. The screen electrode 354 is connected to the cathode 352, these two electrodes being returned to ground. The input circuit to the control electrode 353 includes an input resistor 356 connected between the control electrode and ground and a series coupling capacitor 357 that is connected back to the final stage of the ring counter 75 (see FIG. 7). The anode 355 of the tube 351 is connected through the operating coil 358 of a control relay 359, and through a resistor 361, to the B+ supply. The control relay 359 may include one or more pairs of contacts, such as the normally open contacts 362, that are connected in the operating circuit of the punching apparatus 10 to initiate or control a punching cycle.

At the end of each sensing cycle, as noted hereinbefore, if the ring counter 75 counts out completely, the final stage of the ring counter applies a positive-polarity signal to the control electrode 353 of the punch check circuit 76 (FIG. 5). As a consequence, the thyatron 351 is rendered conductive, energizing the control relay 359. Actuation of the relay closes the contact 362 and initiates a punch cycle in the apparatus 10 (FIG. 1). Of course, some means such as a cam-actuated switch 363 must be incorporated in the punch check circuit to extinguish the thyatron 351 and de-energize the punch check circuit after the punching operation has been initiated and before the next sensing cycle of the control system. The switch 363 may, for example, be actuated by a suitable cam mechanism driven in synchronism with the punch apparatus 14 of the punching unit (FIG. 1). The switch 363 should be timed to open before closing of the switch 339 in the operating circuit of the reset relay 335 in order to avoid false triggering of the punch check circuit in the event that the counter 75 does not count out completely.

With the punch mechanism actuated by the above described operation of the punch check circuit 76, the cam-controlled switches in the solenoid circuits of the storage matrix 73 are closed. Consequently, those storage matrix solenoids, such as the solenoids 252 and 272, which are connected to storage thyatrons that have been rendered conductive are actuated to set the desired combination of punches in the punch unit 14. In those instances where a thyatron in the storage matrix is not previously energized, however, closing of the operating circuit to

19

the solenoid is not effective to actuate the solenoid, since no effective return circuit to ground is provided. It is thus seen that the closing of the switches such as the switches 255 and 275 is effective to "read out" the stored data from the matrix 73 and to set the desired combination of punches in the punch mechanism. Thereafter, the record card such as the card 21 is transported into and is punched with the data 41 in the punch unit 14 (see FIGS. 1 and 2). After punching, the card is fed to the receiving hopper 15; a printing operation may be effected at the printing station 15 if desired. When the punching operation is completed, the normal cyclical control for the punch mechanism 10 is effective to open all of the main control switches 251, 271, and the like in the storage matrix 73. The solenoid circuit switches, such as the switches 255 and 275 are also opened. Consequently, those thyatrons in the storage matrix 73 which have previously been conductive are now rendered non-conductive and the storage matrix is cleared for the receipt of information from the next sensing of the pre-printed data on the next card.

From the foregoing description, it is believed that it will be apparent how the control system of the present invention can be connected to the punching apparatus of the aforementioned Gollwitzer Patent No. 2,710,406 to control the card punch. However, to assist in correlating the control system with the punch apparatus, it may be desirable to point out certain specific inter-connections therebetween. For example, the individual driver solenoids in the storage matrix 73, such as the solenoids 255 and 272, may be provided with suitable armatures (not shown) which are mechanically connected to the setting pins 761 for the punch unit in the Gollwitzer punch apparatus. Thus, the driver solenoids of the storage matrix are effectively employed to replace the normal setting mechanism for these pins, and are used instead of the sensing mechanism of the aforementioned patent. The control relay 359 of the punch check circuit 76 (FIG. 5) is preferably connected in the energizing circuit for the solenoid SOL-5 that controls the action of the punch ram in the punch apparatus of the aforementioned Gollwitzer patent. In this way, the punch check circuit can be utilized to prevent a punching operation without otherwise interrupting operation of the machine 10 (FIG. 1). However, and as noted hereinabove, the punch check circuit 76 could also be employed to stop the machine completely, to actuate an alarm signal, or otherwise to alter the operation of the punching apparatus by suitable electrical connection to the controls of the card punch.

It is also desirable to consider the general cyclical operation of the punch apparatus 10 in relation to the control system of the present invention. During a first cycle of operation of the punch apparatus 10, a first card is fed from the magazine 11 into the transport mechanism or conveyor 12. During this same cycle, this first card is passed through the sensing station 13 to sense the pre-printed code data thereon, this data being recorded in translated form in the storage matrix 73. Near the end of the cycle, the first card enters the punch unit 14. In the second cycle of operation, the first card is punched in accordance with the data previously stored in the matrix 73 of the control system 48 (see FIG. 4). During this second cycle, a second card is fed from the magazine 11 and is transported into the scanning station 13, the data on the card being sensed and recorded in the storage matrix after the storage matrix has been cleared for punching of the first card. Near the end of this second cycle, the first card is fed outwardly of the punch unit 14 and the second card is conveyed into the punch unit.

In the third cycle of operation, a third card is fed from the magazine 11 into the transport mechanism 12. During this cycle, the third card is sensed and the pre-printed data thereon is recorded in the storage matrix. Before this sensing and recording operation takes place,

20

however, the previously recorded data in the storage matrix is read out and the second card is punched. Furthermore, during this third cycle the first card may be printed with any desired data at the printing station 16. It is thus seen that, at any given time, three different cards may be passing through the card punch 10 at different stages thereof, the specific timing cycle for the punch 10 being set forth in detail in the above-identified Gollwitzer patent.

In order to afford a more complete illustration of this embodiment of the invention, certain circuit data are set forth hereinafter. These data are provided solely by way of illustration and in no sense as a limitation on the invention:

Amplifier 70

Resistor 136	470 kilohms.
Resistor 137	1 kilohm.
Resistors 138, 139	3.3 kilohms

Code Translator 72

Resistors 221	27 kilohms.
Resistors 202, 204, 206, 208, 209	560 kilohms.
Diodes 222	Hughes Type 2257.

Party Check Circuit 74

Resistors 152, 153	47 kilohms.
Resistors 155, 168, 174	470 kilohms.
Resistors 156, 161, 162, 169, 175	100 kilohms.
Resistor 159	5.6 kilohms.
Resistors 177, 178, 185	100 kilohms.
Resistors 164, 181, 193, 196	1 megohm.
Resistor 167	820 kilohms.
Resistor 186	39 kilohms.
Resistor 187	68 kilohms.
Resistor 198	56 kilohms.
All triodes	½ Type 5965.
Capacitors 154, 163, 192	0.1 microfarad.
Capacitors 165, 195	1.0 microfarad.
Capacitor 173	0.001 microfarad.
Capacitor 179	0.0022 microfarad.
Capacitor 184	0.0005 microfarad.

Storage Matrix 73

Resistor 248	68 kilohms.
Resistors 242, 244	820 kilohms.
Resistors 245, 256	82 kilohms.
Resistor 246	22 kilohms.
Resistor 247	5.6 kilohms
Resistor 253	1 kilohm.
Thyatrions 240, etc.	Type 5696.

Counter 75

Resistors 286	8.2 kilohms.
Resistor 291	120 kilohms.
Resistor 303	82 kilohms.
Resistor 329	68 kilohms.
Thyatrions 281, etc.	Type 5696.

Voltage Supplies

B+	+150 volts.
E-	-75 volts
F-	-27 volts.
G-	-24 volts.

General Description, FIG. 8

FIGS. 8 through 20 illustrate, in substantial detail, another and preferred embodiment of the present invention. FIG. 8 is a block diagram of the basic translation and control system of this embodiment, and the overall construction and operation of the translation and control system 400 illustrated therein are first explained in connection with this particular figure. It should be understood that only the principal circuit interconnections are indicated in FIG. 8, others being described in connection with subsequent figures.

The translation and control system 400 of FIG. 8 comprises a plurality of individual data sensing devices indicated generally by the circuit unit 401. As explained more fully hereinafter, the data sensing devices of the circuit unit 401 may each comprise an individual photocell and an associated pre-amplifier circuit, the arrangement being similar to the correspondingly identified elements in the system illustrated in FIG. 4. The individual data sensing devices are connected to a series of suitable data amplifiers, generally indicated by reference numeral 402. The data signal amplifiers, in turn, are coupled to a first translation or convertor circuit 403 that serves the same basic function as the circuit 72 in the system of FIG. 4. That is, the convertor 403 (FIG. 8) translates the parity-code signals received from the data amplifiers 402 into machine-code signals. The machine-code signals are supplied to a solenoid driver and storage matrix 404 that corresponds generally to the circuit 73 in the previously described embodiment but is substantially different in construction, as described more fully hereinafter.

The parity-code signals from the data amplifiers 402 are also supplied to a second translator circuit 405 and are there translated into binary-coded decimal form. Actually, the translation operation in this instance converts the parity-code signals into the fifteens complement of the numerical value of each signal as expressed in binary-coded decimal form. The translator 405 is coupled to an accumulator control and convertor circuit 406 which, in turn, is connected to an accumulator circuit 407. Both the accumulator control and convertor circuit 406 and the accumulator 407 are coupled to a comparator error circuit 408. The comparator error circuit 408, in turn, is connected to an error card circuit 409.

The translator circuit 405, in addition to its connection to the convertor circuit 406, is coupled to a rack memory circuit 411. The rack memory device 411 is also connected to a plurality of individual sensing devices 412 that are associated with respective punch set racks 413 in the reproducing punch 10. The construction and use of the punch-set racks 413 is clearly described in the aforementioned patent to Gollwitzer No. 2,710,406, these racks being utilized to position the punch-setting elements that determine the punches to be actuated in each column of the punch mechanism.

The system 400 illustrated in FIG. 8 also comprises a ring counter 414 that is functionally similar to the ring counter 75 in the system of FIG. 4, although the actual construction is quite different. The ring counter 414 is connected to an output circuit from the error card circuit 409. A clock timer 415 is provided, being coupled to a sequence timer 416 that is coupled to the ring counter 414. In addition, the sequence timer 416 is coupled to the data amplifier 402. The clock timer 405, on the other hand, is provided with an additional output connection to the accumulator control and convertor circuit 406.

In this embodiment of the invention, the input data that is scanned and reproduced, in punched form, in the record cards, is subdivided into the two different fields. Accordingly, the system 400 includes two field control circuits identified in FIG. 8 as gate circuit 421 and gate circuit 422, the two circuits being used in controlling the sensing and utilization of data from the first and second data fields respectively. The division of the input data into the two fields is essentially arbitrary; that is, the number of bits of information relegated to each field can be selected to fit the requirements of any particular credit system or other accounting system as described. In the system described in detail hereinafter, it is assumed that the total number of data items is fifteen, ten in the first field and five in the second.

The field gates 421 and 422 are connected to the data sensing devices 401 to control their operation. Each of the field gates is also coupled to the error card circuit

409 to condition that circuit for operation as described hereinafter. In addition, each of the two field gates is coupled to a combined field error circuit 423 that is employed to interrupt machine operation, to the extent of preventing the punching of data in the record cards, in response to input signals indicating a variety of different kinds of error. The combined field error circuit 423 receives the signals necessary for the error checking operations that it performs from the rack memory circuit 411 and from a parity-check circuit 424 that is connected to the outputs of the data amplifiers 402. Parity-check circuit 424 is thus utilized to perform a function substantially similar to that of the circuit 74 in the first-described embodiment, but in this instance the output from the parity-check circuit is utilized in a different manner. The combined field error circuit 423 is provided with two individual output terminals 425 and 426 that are connected to the basic control apparatus of the reproducing punch 10 to prevent the punching of data in the first and second fields of the record card, respectively.

The transmission and control system 400 also includes a control card detector 427 that determines the presence of a card that is substantially different from the ordinary detail card processed by the machine 10. These control cards, sometimes referred to as summary cards, are similar to the detail cards in that they include data printed thereon in accordance with the same parity-code as is used on the detail cards. Moreover, the pre-printed code data on the control cards is of similar nature except that it represents a previously prepared summary of data from a substantial number of detail cards. For example, in a given credit system, individual detail cards would be prepared to represent each individual transaction. At the time the detail cards are to be forwarded to a centralized accounting center, a control card is prepared and is pre-printed with data representing the sum of the total transactions on the detail cards. The control or summary card is differentiated from the detail cards in a manner that can be detected by the control system 400; for example, the summary card might be different in color or might include a separate additional code marking located at some point on the card different from the pre-printed code data 22 (see FIG. 2) to permit automatic detection of the presence of the summary card.

The control card detector 427 is connected to the accumulator control and convertor circuit 406 and to the error card circuit 409. It is also coupled to the clock timer 415 to afford a means for delaying actuation of the ring counter 414.

The initial operation of the control system 400 is substantially similar to that of the system described hereinabove in connection with FIGS. 4-7. That is, a plurality of record cards, including several groups of detail cards each followed by a summary or control card, are stacked in the main hopper 11 of the reproducing punch 10. At the same time, a plurality of blank error cards are stacked in the second or auxiliary hopper 11A of the machine. To initiate operation, a first detail card is fed from the bottom of the stack in the main hopper 11 and is conveyed by the transport 12 toward the data sensing station 13 of the machine, at which the data sensing devices 401 are located. Thus, the basic feed system for the cards is essentially the same as that described hereinabove.

When the first detail card enters the sensing station 13, the gate circuit 421 controlling sensing of the first field on the card is actuated. In the circuit described in detail hereinafter, actuation of field gate 421 is accomplished by the masking of a photocell by the leading edge of the card. When this occurs, the field gate circuit 421 produces output signals that are supplied to the combined field error circuit 423 and to the data sensing devices 401 to condition these portions of the system 400 for a data sensing and error checking operation. The timing of the system is such that the gate circuit 421 for

the first field is actuated to produce the aforementioned output signals in time coincidence with movement of the first column of code data in the first field into alignment with the data sensing devices 401.

As the detail record card continues to move through the sensing station 13, the individual code markings in the first field (which may comprise anywhere from one to all of the code markings as noted hereinabove) are scanned by the data sensing devices 401. As in the first-described embodiment of the invention, sensing is effected on an item-by-item basis and the data signals that are developed by the sensing devices 401 are applied to the data amplifiers 402. The initial data signals, or parity-code signals as usually referred to herein, are amplified in the data amplifiers 402 and are supplied to the parity-check circuit 424, to the machine-code translator or converter circuit 403, and to the fifteens complement binary coded decimal translator circuit 405.

The parity-check circuit 424 checks each set of parity-code input signals, representing individual data items, to determine whether there are more than two or less than two code markings that have been sensed in each instance. In the event that the circuit 424 determines that a given item includes more than two or less than two individual marks, it produces an output signal that is supplied to the combined field error circuit 423. The field error circuit 423 then develops an output signal that is supplied to the reproducing punch 10, or rather to a control mechanism included therein, to prevent punching of the sensed data from the first field of the record card. The requisite connection to the reproducing punch 10 may be accomplished through any conventional electrically actuated machine control device, such as a solenoid or other form of electrically actuated clutch. In normal operation, of course, the parity-code signals supplied to the circuit 424 will ordinarily indicate that the code markings are correct from a parity standpoint. In this event, there is no significant output signal from the parity-check circuit 424 that would be effective to void the first field of punched data by operation of the combined field error circuit 423.

The parity-code signals supplied to the machine code converter 403 are translated therein from the 1-2-4-7-P parity-code of the record cards (see FIG. 2) to the 2-4-6-8-9 machine code (see FIG. 3). The translated signals are supplied to the solenoid driver and storage matrix 404 and are recorded therein. The recording sequence, in the storage matrix 404, is controlled by the ring counter 414 which, in turn, is actuated by the sequence timer 416. The clock timer 415 also enters into the control of recording of data in the matrix 404, as described in further detail hereinafter. The clock timer 415 is started in operation at the beginning of the data sensing cycle by a suitable signal from the field gate circuit 421, and, in turn, initiates operation of the sequence timer 416. The accumulator 407, the comparator error circuit 408, and the error card circuit 409 do not enter into control of the system 400 in the course of the normal punching of data in the detail cards, but are used only in conjunction with summary cards and error cards as described hereinafter.

As the detail card continues its movement through the sensing station 13, it reaches a point where the sensing of data from the first field of the pre-printed code data is completed. The completion of sensing of data from the first field is determined by the gate circuit 421, which develops an output signal that interrupts the data sensing operation being performed by the sensing devices 401. This is done to prevent erroneous actuation of the field error circuit 423 in response to the presence of extraneous non-significant markings on the card that might occur between the first and second fields of pre-printed code data. The same signal is supplied to the clock timer 415 to interrupt the continuing sequential actuation of the various stages of the ring counter 414. At this point,

sensing and recordation of parity-code data from the first field is completed.

The continued movement of the detail card through the sensing station 13 next actuates a start gate, incorporated in the gate circuit 422, for the second field of pre-printed code data. Again, the starting signal is preferably produced by the masking of a photocell by the leading edge of the detail card. Thereafter, the steps described hereinabove for the sensing, translation, and recordation of data from the first field are repeated for the second field of code data from the card. At the same time, of course, each data item is checked in the parity-check circuit 424, which actuates the combined field error circuit 423 to prevent punching of data from the second field in the event of a discrepancy from the normal parity-code. Upon completion of the sensing of data from the second field, the gate circuit 422 is again actuated to supply a suitable signal to the combined field error circuit 423 to prevent erroneous actuation thereof.

In the system 400, the accumulator 407 and associated circuits are used only to monitor data from the second field. This is accomplished with the signals from the translator 405. The parity-code signals applied to the translator circuit 405 are translated therein into a modified form of decimal code. Actually, the output signals from the translator 405 are in the form of the fifteens complement of binary-coded decimal signals. The fifteens complement data signals are applied to the accumulator control and converter circuit 406 parallel-by-bit. The recorded fifteens complement signals are read out from the circuit 406 serial-by-bit in ordinary decimal form and are recorded in the accumulator 407 for future use.

From the foregoing description, it is seen that the movement of the detail card through the sensing station 13 results in the sensing of data from the card in accordance with two separate data fields which may be determined arbitrarily to suit the requirements of the accounting system. The data from both fields are translated and recorded in machine code form in the solenoid driver and storage matrix 404. The same data are recorded in fifteens complement binary-coded decimal form in the rack memory 411. The data from the second field are recorded in conventional decimal code in the accumulator 407. At this point, however, and assuming that the pre-printed data are accurately delineated on the record card, there has been no output signal to the machine 10 and punching of the card has not yet been initiated.

After the sensing and recording operations described above, movement of the record card through the machine 10 from the sensing station 13 continues; that is, the detail record card moves toward the punching station 14 (FIG. 1). During this interval, a cam switch incorporated in the machine 10, and comprising one of a plurality of cam switches that control cyclic operation of the machine, is actuated to read out the data from the solenoid driver and storage matrix 404. Each stage of the matrix 404 is electrically connected to an individual punch selection solenoid incorporated in the machine 10 as described hereinabove in connection with the first embodiment of the invention. Each such solenoid actuates a punch set member, such as the punch set rack 413 in FIG. 8. The movements of the punch set racks establish the setting of the punches in accordance with the data previously recorded in the matrix 404.

The movements of the individual punch setting elements, such as the punch set rack 413, produce a series of pulse signals in the rack sensing devices 412. Thus, movement of the rack 413 to a given punch setting produces an output signal in the sensing device 412 that comprises a series of pulses, the number of pulses developed identifying the ultimate setting of the punch set rack. These signals are supplied to the individual stages of the rack memory 411 and are recorded therein in cumulative manner with respect to the previously recorded code data

supplied to the rack memory from the translator circuit 405. If the setting of the punch set rack 413 is correct, the first stage of the rack memory 411 receives a series of pulse signals which cause this stage to count out to a predetermined value, in this instance the number fifteen. That is, the identifying data for the first punch setting is recorded initially in the rack memory as the fifteens complement of the number to be punched and the signal supplied from the sensing device 412 causes the same stage of the rack memory to count out to the total number fifteen. This same action takes place with respect to each stage of the rack memory 411.

When the detail record card reaches the punching station 14 in the machine, the combined field error circuit 423 is supplied with an actuating signal from a cam-controlled switch actuated in timed relation to the position of the card. In response to this actuating signal, the combined field error circuit determines whether all stages of the rack 411 have counted out completely to the total number fifteen. If any discrepancy occurs, and some other number is recorded in any stage of the rack memory 411, the field error circuit 423 operates to supply an output signal to one of the machine terminals 425 and 426 to void the setting of the punches in the first or second field of the punch mechanism, depending upon the portion of the rack memory that exhibits the discrepancy. Thus, at this point the translation and control system 400 effectively determines whether the punch mechanism has been set up accurately in accordance with the information from the pre-printed code data on the record cards and, if this has not been accomplished, operates to prevent the punching of erroneous data. In addition, the field error circuit 423 performs a count check to make sure that one punch has been set for each bit of information from the pre-printed code data; that is, the circuit 423 determines whether the precise desired number of data items are present and have been set up in the punch control mechanism of the machine. In this respect, the combined field error circuit 423 performs the same basic function as the digit count check circuit 76 in the embodiment of FIG. 4. Assuming that all of the verification and checking processes of the system 400 have been satisfied, the detail card is punched at this time.

The foregoing sequence of operations is repeated for each of the detail cards, independently of the other detail cards. In each instance, however, the code data from the second data field of each card is added to that already present in the accumulator 407 so that, at any time, the accumulator records the total of the data from all preceding detail cards in the group.

After a group of detail cards has been fed through the machine and all cards have been punched, a summary card pertaining to the group is fed from the hopper 11 to the transport 12 (FIG. 1). The presence of this summary card is detected by the control card detector 427. As noted hereinabove, detection of the summary card may be based upon any desired characteristic such as the color of the card or a special code marking on the card. The control card detector 427 then applies a conditioning signal to the circuits 406, 408 and 409 to condition them for a summary card operation, which is somewhat different from that entailed with respect to the detail cards.

The continued movement of the summary card into the sensing station 13 again triggers the first field gate, circuit 421, so that sensing of the pre-printed code data on the summary card is initiated in the same way as in the case of a detail card. In fact, the parity-code signals produced upon sensing of the code markings on the summary card are treated in much the same way as the corresponding signals derived from the sensing of data from a detail card except that the summary card data (second field) are not recorded in the accumulator 407. The conditioning signal from the control card detector 427 actuates the circuit 406 to prevent the accumulator control and converter circuit from supplying the summary card data to the accu-

mulator. Instead, the output of the circuit 406 is now supplied to the comparator error circuit 408, which compares each bit of data from the summary card with the corresponding previously recorded data in the accumulator 407.

Ordinarily, the data from the summary card should correspond precisely with that previously recorded in the accumulator 407 as the result of the sensing and recording therein of data from the preceding and related group of detail cards. During the sensing of data from the summary card, of course, a parity-check is continuously carried out by the circuit 424 and the summary card data are translated to machine code and recorded in the solenoid driver and storage matrix 404. Consequently, and where no error appears between the summary card data and the accumulated data in the circuit 407, the summary card is punched in exactly the same manner as the detail card. In addition, the accumulator 407 is cleared for further operations. Operation of the machine is then continued with the initiation of sensing and punching of the first detail card from the next group.

On the other hand, it may happen that one or more stages of the accumulator 407 record data that do not correspond to the related data from the summary card. If such a discrepancy appears, it is detected by the comparator error circuit 408 and an error signal is supplied to the error card circuit 409. As a consequence, the error card circuit 409 actuates the auxiliary card feed mechanism of the machine 10 to feed an error card from a second or auxiliary card hopper 11A into the transport 12 of the machine. The error card circuit 409 also applies an inhibiting signal to the ring counter 414 to prevent punching of the original summary card. Consequently, the summary card is discharged unpunched from the machine and the error card is punched with the data from the solenoid driver and storage matrix 404 during the next machine cycle.

The circuit arrangement of FIG. 8 can also be modified to produce a somewhat different result upon the detection of a difference between the accumulated data in the circuit 407 and the corresponding data from a summary or control card. Thus, the accumulator 407 may be coupled to the solenoid driver and storage matrix 404 through a circuit arrangement which is not normally effective during the sensing and punching of detail cards but which is conditioned for operation by a suitable signal from the control card detector 427 whenever a summary card is fed into the machine. This way, data from the accumulator 407 may be supplied to the circuit matrix 404 in the same manner as actual sensed data; of course, this necessitates a translation stage between the accumulator 407 and the solenoid driver and storage stage 404 to translate the data from the accumulator into the machine code. In this manner, it is possible to punch the error card with data from the accumulator rather than from the summary card. As will be apparent, the circuit can be modified to assure punching of the summary card with its own data, regardless of comparison with that of the accumulator 407, coupled with subsequent punching of the error card with the data from the accumulator 407 in the next machine cycle.

The accumulator 407 is of finite capacity, of course, and in some instances it may happen that the total amount of data from the detail cards exceeds the storage capacity of this circuit. When this occurs, the accumulator supplies an output signal to an over-flow detector circuit 430 which actuates a warning signal and stops the machine. The overflow detector 430 also stops the machine upon occurrence of other conditions as set forth hereinafter.

Logic Symbols

FIGS. 9A through 9J illustrate a variety of logic circuit symbols that are employed in FIGS. 10 through 17

in the illustration of the major circuits of the system 400 of FIG. 8. In general, these individual figures are self-explanatory. Thus, FIG. 9A illustrates the symbol for an AND circuit, FIG. 9B shows the form employed to indicate an OR circuit, FIG. 9C illustrates a direct coupled amplifier that does not provide for inversion of the input signal, and FIG. 9D is the symbol for a D.C. inverting amplifier or NOT circuit. FIG. 9E shows the symbol employed for an A.C. amplifier that does not invert the input signal, whereas FIG. 9F is the symbol utilized for an A.C. inverting amplifier. FIG. 9G illustrates the symbol for a one-shot (monostable) multi-vibrator, the effective operating interval for the circuit being indicated within the symbol as shown by the reference numeral 431. It should be noted that the two outputs of the multi-vibrator are identified as the "1" and "0" outputs. FIG. 9H employs a similar symbol to illustrate a conventional bistable flip-flop or trigger circuit, the difference being that in this instance there are two inputs to the device, one being the "set" input identified by the letter "S" and the other being the "reset" input identified by the letter "R." Essentially the same symbol, with a common set and reset circuit, is shown in FIG. 9I, illustrating a binary flip-flop or trigger circuit. Finally, FIG. 9J shows another form of flip-flop that is essentially similar to that of FIG. 9H except that it is provided with an auxiliary reset circuit identified by the letter "E," which has been selected because this is usually an emitter reset circuit in the transistor devices employed in the preferred embodiment of the invention.

Data Sensing, Translation, and Parity Check Devices, FIG. 10

FIG. 10 illustrates the basic logic circuit arrangement of several of the principal stages of the translator and control system 400 of FIG. 8. In particular, FIG. 10 includes the individual data sensing devices 401, the data amplifiers 402, the parity-code to machine-code converter 403, the binary-coded fifteens complement translator circuit 405, and the parity-check circuit 424. The symbols of FIGS. 9A-9J are utilized in FIG. 10, and in the succeeding figures, to afford a more complete and explicit illustration of the circuits than could be conveniently accomplished with conventional circuit symbols.

In FIG. 10, the data sensing devices 401 are shown as individual circuits 401-0, 401-1, 401-2, 401-4 and 401-7, only the device 401-0 being shown in detail. Thus, the data sensing device 401-0 comprises a photocell 431 that is connected to a pre-amplifier comprising a pair of A.C. amplifier stages 432 and 433. The output of the amplifier 433 is connected through a coupling circuit comprising a series resistor 434 and a shunt capacitor 435 to an AND circuit 436. The AND circuit 436 has two additional inputs, one of which is connected to the sequence timer circuit 416, the other being connected to the field gates 421 and 422. The output of the AND circuit 436 is connected through a D.C. amplifier 437 to a one-shot multi-vibrator 440 that comprises the input stage of the data amplifier 402-0. The data amplifier 402-0 further includes a non-inverting D.C. output amplifier stage 450.

The remainder of the data sensing devices 401-1 through 401-7 are essentially similar to the circuit 401-0. As shown in FIG. 10, each includes a sensing device (in this instance a solid-state photodiode) together with a series of circuits corresponding to the elements 432-437 described hereinabove in connection with the first or parity data sensing device 401-0. The individual data sensing devices are connected to a corresponding series of multi-vibrator circuits 441, 442, 444 and 447 which, in turn, are connected to the D.C. amplifiers 451, 452, 454 and 457 respectively.

FIG. 10 also shows an intermediate translator stage 458, interposed between the outputs of the data amplifiers and the individual stages of the convertor 403 and the translator 405, that changes the parity-code signals at the

outputs of the amplifiers 450-457 into signals encoded in accordance with conventional decimal notation. Thus, the output stages 450 and 451 of the two data amplifiers 402-0 and 402-1 are connected together in the input of an AND circuit 461. From the foregoing description of the parity code used for the pre-printed data on the record cards, it is apparent that the decimal value "one" is represented by marks in the parity or "0" area and in the "1" area (see FIG. 2). Thus, whenever output signals are produced simultaneously by the two sensing devices 401-0 and 401-1, they are supplied through the associated amplifiers stages 450 and 451 to the AND circuit 461 which produces an output signal indicative of the sensing of a decimal value of "one." Similarly, a further series of AND circuits 462-470 are connected to the outputs of the data amplifiers and afford a direct decimal indication of the numerical values of the sensed data.

Conversion to the machine code is effected by the series of OR circuits that comprises the parity-code to machine-code convertor 403 shown in this figure. It will be recalled from the foregoing description that the machine code is a 2-4-6-8-9 code (see FIG. 3). To translate to this particular notation, the output stages of each of the AND circuits 461 and 462 are connected to the OR circuit 472. Similarly, the AND circuits 463 and 464 are connected to an OR circuit 474, the devices 465 and 466 are connected to an OR circuit 476, and the AND circuits 467 and 468 are connected to the inputs of an OR circuit 478. The coding for the "nine" component of the machine code is somewhat more complex, and comprises an OR circuit 479 having five individual inputs that are coupled to the AND circuits 461, 463, 465, 467 and 469, respectively, of the decimal translation stage 458. Consideration of the logic involved and the functions carried out by the individual OR circuits 472-479 shows that the output signals produced by these OR circuits are directly representative of the code data initially sensed by the sensing devices 401-0 et. seq., except that the data is now organized in the machine code.

The binary-coded fifteens complement decimal translator 405, as illustrated in FIG. 10, is similar in principle to the convertor 403 but requires the use of a plurality of multiple-input OR circuits. Since binary coding is entailed, and it is necessary to have four binary stages to represent the numerical value fifteen, there are four stages in the translator 405. The first stage comprises an OR circuit 481 having inputs connected to the decimal AND circuits 462, 464, 466, 468 and 470. The next stage, the second binary level in the fifteens complement translator, is an OR circuit 482 having inputs connected to the decimal AND circuits 461, 464, 465, 468, 469 and 470. The third binary level is an OR circuit 484; in this instance, the inputs are connected to the decimal AND devices 461, 462, 463, 468, 469 and 470. The fourth and final stage of the translator 405 is the OR circuit 488, the input connections in this instance being from the AND circuits 461 through 467 and 470.

As noted above, FIG. 10 also illustrates the logic for the parity-check circuit 424. One of the inputs to the parity-check circuit 424 comprises an OR circuit 489 that is provided with ten individual inputs, one connected to each of the decimal AND circuits 461-470. The output of the OR circuit 489 is connected to a NOT or D.C. inverter stage 490. The output of the amplifier 490 is coupled directly to an AND circuit 491. In addition, the output of the amplifier 490 is connected through an additional D.C. inverting amplifier 492 to an AND circuit 493.

The signals supplied to the decimal translator 458 and thence to the convertor circuits 403 and 405 are taken from the "1" terminals of the trigger circuits 440-447 in the data amplifiers. A portion of the parity-check circuit 424, however, is actuated by signals derived from the "0" terminals of these trigger circuits. Thus, the parity-check circuit 424 includes ten AND circuits 501-510 that

are connected in every possible combination of three connections to the "0" output terminals of the triggers 440-447. The outputs of all of the AND circuits 501-510 are connected to an OR circuit 511, the output of which is coupled to a D.C. inverting amplifier stage 512. The output of the amplifier 512 is connected directly to the AND circuit 493. It is also connected through a further inverting D.C. amplifier stage 513 to the AND circuit 491. Each of the two AND circuits 491 and 493 is also provided with a further input circuit, from the sequence timer 416, at the terminal 514 (FIG. 17). The outputs of the AND circuits 491 and 493 are connected to an OR circuit 515 which is connected through a non-inverting D.C. amplifier 516 to the combined field error circuit 423 that is described in detail hereinafter in connection with FIG. 11, the common terminal between the two circuits being identified as terminal 517.

Before reviewing the operation of the parity-check circuit 424, operation of the AND circuits 491 and 493 may first be considered. To produce a significant output signal from either AND device, it may be assumed that all three inputs must be driven to a given polarity, by a signal of given minimum amplitude relative to a reference potential, simultaneously. In the present instance, negative-going signals are required; a similar circuit based on the use of positive-going signals could, of course, be constructed. Thus, the circuits 492 and 512 are arranged to maintain a reference potential at their outputs, and the circuits 490 and 513 also maintain an output approximately at the reference. The significant output signals from the devices 489 and 511 may then comprise negative-going signals.

In considering the operation of the parity-check circuit 424, attention may be directed initially to the portion of the circuit that determines whether more than two code marks have been sensed in any given instance. The initial portion of the parity-check circuit utilized for this function comprises the AND circuits 501-510. In any given instance in which three or more of the trigger circuits 440-447 are actuated by the sensing of a code mark, at least one of the AND circuits 501-510 is actuated to produce an output signal that is supplied to the circuit 512 through the OR circuit 511. Under the same circumstances, of course, at least one output signal will be developed by the AND circuits 461-470, since these represent all possible combinations of two sensed signals. As a consequence, the AND circuit 493 has supplied thereto a negative-going input signal from the amplifier 492 and a negative-going input signal is also supplied to the circuit 493 from the amplifier 512. Consequently, a suitable signal appearing at terminal 514 of the circuit 491 produces an output signal that is supplied to the combined field error circuit 423 through the circuits 515 and 516 to indicate that a discrepancy in the parity count has occurred and to trigger the field error circuit to prevent punching of erroneous data.

The principal check for the occurrence of only one code marking, without the second required by the parity code, is effected by the OR circuit 489. Thus, it should be remembered that there can be no significant output from any of the decimal AND circuits 461-470 unless these devices receive input signals indicative of the occurrence of two code marks as sensed by the data sensing device. Consequently, if there is less than two marks present, there is no significant output signal from the circuit 489. At the same time, there is a corresponding lack of significant output from the OR circuit 511, which requires the presence of an input signal indicating the sensing of at least three data marks. Under the conditions set forth above, however, this results in the application of negative signals, relative to the reference, to the inputs of AND circuit 491 that are connected to the circuits 490 and 513. Hence, when a suitable signal appears at terminal 514, circuit 491 produces an output

signal. In other words, the assembly of circuits comprising the amplifiers 490-493 and 512-513 functions much like a half adder to supply a signal to the amplifier 516 whenever either an overcount or an undercount, with respect to parity conditions, occurs. In the case of an undercount, the requisite output signal is supplied from the AND circuit 491. The result, with respect to actuation of the error circuit 423, is identical to an overcount, as described hereinafter. On the other hand, if circuit 489 produces an output signal but circuit 511 does not, which indicates the sensing of just two marks, AND circuit 493 is still blocked by the signal from circuit 512, AND circuit 491 is blocked by the signal from circuit 490, and no error signal is developed.

Field Gates, Reset, and Error Circuits, FIG. 11

FIG. 11 illustrates, in substantial detail, the principal circuit units identified in FIG. 8 as the gate 421 for the first field of data, the corresponding gate 422 for the second data field, the combined field error circuit 423, and the error card circuit 409, together with a channel reset circuit 518 which controls the timing of a number of operations in each of the other circuits.

The first field gate circuit 421 comprises a start sensing photocell 519 that is connected through an A.C. inverting amplifier 521 to the base electrode of a gate transistor 522. The collector of the transistor 522 is connected to the set terminal of a bistable flip-flop or trigger circuit 523 and is also connected to a D.C. source, identified as C—, through a load resistor 524. The collector is also connected to an OR circuit 525 that, in turn, is connected to the set terminal of a flip-flop circuit 526. The emitter of the gate transistor 522, on the other hand, is returned to ground through the error card circuit, and specifically through an amplifier or NOT device 527 included therein, as described more fully hereinafter.

The finish-determining circuit for the first data field, included in the gate device 421, is similar and comprises a photocell 528 that is coupled to an A.C. inverting amplifier 529 connected to the base electrode of a gate transistor 531. In this instance, the collector of the transistor is connected to the C— supply through a load resistor 522 and is connected to the reset terminal of the flip-flop 523. In addition, the collector electrode of the gate transistor 531 is connected to an OR circuit 532. Moreover, a circuit connection is provided from the collector of the transistor 531 to an amplifier 533 in the error card circuit 409, as explained more fully hereinafter. The emitter of the transistor 531 is returned to system ground.

The start portion of the gate device 422 for the second field of code data is similar to the corresponding circuit in the gate device 421. Thus, it comprises a photodiode 534 connected through a suitable A.C. amplifier to a gate transistor 535. The collector of the gate transistor 535 is connected to the C— supply through a suitable load resistor and is also connected to the OR circuit 525. Furthermore, the collector of the transistor 535 is connected to the set terminal of a flip-flop circuit 536. The emitter is returned to ground through the amplifier circuit 527 in the error card circuit 409.

The finish-determining device in the gate circuit 422 include a photodiode 537 connected through an A.C. amplifier to the base electrode of a gate transistor 538. The collector electrode is provided with the usual load circuit connection to the C— supply and is connected to the reset terminal of the flip-flop 536 and to one of the inputs of the OR circuit 532. As in the case of the transistors 522 and 525, the emitter of the transistor 538 is returned to the amplifier circuit 527. The outputs of the two OR circuits 525 and 532 are connected to the set and reset terminals of the flip-flop circuit 526. The "0" output terminal of the flip-flop circuit 526 is connected to the data sensing devices 401 and specifically to one of the inputs of the AND circuit 436 in the data sensing device 401-0 and to the corresponding circuits in the other data

sensing devices (see FIG. 10). The output signal supplied to the AND circuits such as the circuit 436 of FIG. 10 is utilized to preclude operation of the data sensing devices except when one or the other of the data fields is being passed through the data sensing station of the machine.

Thus, each time a detail or summary card is passed through the sensing station, the photodiode 519 is masked at the time the first data item in the first field comes into alignment with the data sensing devices. As a consequence, a positive-going output signal is supplied from the gate transistor 522 to the OR circuit 525, and is supplied from that circuit to the set terminal of the flip-flop 526 to drive the latter from its "1" to its "0" operating condition. As a result, an actuating signal is supplied to the AND circuit 436 (of sensing device 401-0) (FIG. 10) and to the corresponding circuits in the other data sensing devices, conditioning those devices for a data sensing operation by actuating the AND circuits to permit translation of data signals from the photodiodes used for data sensing. This condition is maintained throughout sensing of the first field and until the flip-flop 526 (FIG. 11) is reset by a signal supplied thereto from the circuit comprising the "finish" photodiode 528, the gate transistor 531, and the OR circuit 532. Sensing of the next field does not start until the photodiode 534 is masked by the leading edge of the card, the construction of the system being such that this takes place as soon as the first data item in the second field comes into sensing position. Again, a signal is supplied from the photodiode 534 and the gate 535 to set the flip-flop 526 and condition the data sensing devices for operation. Moreover, this condition is again maintained until sensing of the field is completed, at which time an output signal from the diode 537 and the associated gate 538 triggers the flip-flop 526 and resets it, again disabling the data sensing devices and preventing further and erroneous operation. The channel reset circuit 518 provides a positive means for resetting a number of the different control circuits of the system 400 (FIG. 8). As illustrated, in FIG. 11, it comprises a photodiode 541 connected through an A.C. inverting amplifier 542 to the base electrode of a gate transistor 543. The emitter of the gate transistor is returned to the amplifier 527 in the error card circuit 409. As in the field gate circuits, the collector of the transistor is connected to the C— supply through a suitable load resistor. The collector of the gate transistor is also connected to an OR circuit 544. The OR circuit 544 is provided with a second input terminal 548 that is connected to a negative-polarity D.C. supply, designated as D—, through a resistor 545; terminal 548 is also returned to ground through a diode 546. In addition, the terminal 548 is connected to a multi-vibrator 550 that comprises a part of the timing circuits of the system but is illustrated in FIG. 14 in conjunction with the accumulator 407.

The output of the OR circuit 544 is connected to a non-inverting A.C. amplifier 549 having an output connected to a further amplifier stage 551. The amplifier 551 is coupled to the base electrode of a gate transistor 552 having its collector connected to the C— supply. The emitter terminal 553 of the transistor 552 is utilized as a source of gating signals in other circuits of the system, as noted hereinafter.

The output circuit of the amplifier 549 is also connected to a D.C. supply E+ through a resistor 554 and to an OR circuit 555. The OR circuit 555 is provided with a second input terminal that is connected to a flip-flop circuit 556 in the error card circuit 409. The output of the OR circuit 555 is connected to the base electrode of a further gate transistor 557. The emitter of this transistor is returned to system ground and the collector is connected to an output terminal 558 to afford a further source of gating signals to control system operations.

A third circuit connection is provided to the output of the amplifier 549 and this comprises the connection to the

base electrode of another gate transistor 559. The emitter of this transistor is returned to system ground. The collector electrode of the transistor is connected to the emitter reset terminals of the flip-flops 523, 526 and 536 in the field gate circuits 421 and 422. The collector electrode terminal 561 of the gate transistor 559 is also connected to other portions of the circuits illustrated in FIG. 11, and in various other FIGURES, as described more fully hereinafter.

The function of the channel reset circuit 578 is relatively simple. Each time a new card, whether a detail card or a summary card, begins its movement through the sensing station, the diode 541 is masked by the leading edge of the card. This occurs before any data sensing, with respect to that card, is initiated. As a consequence, a reset signal is produced at each of the output terminals 553, 558 and 561 of the channel reset circuit. With respect to the field gate circuits 421 and 422, the signal appearing in the output terminals 561 of the channel reset circuit is effective to reset each of the trigger circuits 523, 526 and 536 to make sure that they are properly conditioned for the beginning of the data sensing operation each time a new card cycle is initiated. By the same token, the channel reset circuit 578 develops a similar reset signal each time operation of the control system is initiated, by virtue of the connection at the terminal 548 of the OR circuit 544. That is, whenever the system is placed in operation, a signal impulse is supplied to the terminal 548 that has the same effect as the signals normally developed by the gate transistor 543. This arrangement assures resetting of the various control circuits connected to the channel reset device 518, including the field gate flip-flops, before the first card is fed into the machine.

The combined field error circuit 423 provides a major link between the control system 400 (see FIG. 8) and the punching machine. It is this circuit which prevents erroneous operation of the machine in response to a variety of different kinds of errors which may occur as the result of improper recodation of data on the record cards or other errors. As noted above, the terminal 517 from the parity-check circuit 424 (FIG. 10) is connected to the combined field error circuit 423, comprising one input terminal for each of a pair of AND circuits 571 and 572. The AND circuit 571 is provided with a second input that is connected to the "1" terminal of the flip-flop 523 in the first field gate 421. Similarly, the AND circuit 572 includes a second input connected to the "1" terminal of the trigger 536 in the control gate 422 for the second data field. It is thus seen that the AND circuit 571 produces an output signal only during sensing of the first data field, in response to a signal appearing at the terminal 517 and indicative of an error in the parity code markings. By the same token, and AND circuit 572 produces an output signal, upon occurrence of a parity error, only when the second data field is being scanned.

The AND circuit 571 is connected through an OR circuit 573 to the set terminal of a flip-flop circuit 574. The "0" output terminal of the flip-flop 574 is connected through a D.C. inverting amplifier 575 to the base circuit of a gate transistor 576. The collector electrode of the gate transistor 576 is identified by the reference character 425, since it is this terminal which provides an output signal to the machine 10 to clear or void the setup of punches in the first field. That is, the terminal 425 comprises the first output from the combined field error circuit 423 to afford a control signal direct to the machine (see FIG. 8). Accordingly, any time that the flip-flop 574 is actuated from its normal operating condition to its set condition, the first field of data punches in the machine are reset or otherwise actuated to prevent the punching of any data in a record card in this field.

An essentially similar construction is utilized in the other section of the combined field error circuit 423.

Thus, the AND circuit 572 is connected through an OR circuit 577 to the set terminal of a flip-flop circuit 578. The "0" terminal of the circuit 578 is connected through a D.C. inverting amplifier 579 and through an OR circuit 581 to the base electrode of a gate transistor 582. Again, the collector of the transistor comprises one of the principal output terminals, the terminal 426, utilized to provide control signals to the card punching apparatus. The signal appearing at terminal 426 is effective to void any setup data in the punch mechanism to prevent the punching of data in the second field of a card. It is thus seen that either one or both fields may be cleared independently of each other upon occurrence of a parity error in the sensed data for that particular field.

As noted hereinabove, the combined field error circuit 423 is also employed to prevent the punching of data in either one or both of the data fields upon occurrence of other kinds of errors in the operation of the system. For example, it may happen that one or more data items are not properly recorded and that, accordingly, there is an undercount with respect to significant and required bits of data. Actuation of the field error circuit in this regard is accomplished by a suitable connection to the ring counter 414. Thus, the combined field error circuit 423 includes a flip-flop or trigger circuit 583 having its set and reset terminals connected to the outputs of the last two stages, respectively, in the first field portion of the ring counter 414. That is, the set and reset terminals are connected to the devices 719 and 720, respectively, in the ring counter circuit 414 (FIG. 13). In this connection, and in the following description relating to the different fields, it is assumed that the total number of data items is fifteen and that the first ten data items constitute the first data field and the remaining data items constitute the second data field. It will be recognized that the total number of data items and the number assigned to each field could be different without affecting the basic operation of the control system.

The "0" output of the trigger circuit 583 is connected to an AND circuit 584. The AND circuit 584 includes a second input that is connected through the amplifier 533 to the finish gate transistor 531 in the first field gate device 421. The AND circuit 584 is also provided with an additional input from the error card circuit 409 and specifically from the "0" terminal of the flip-flop 556 included therein. The circuit arrangement is such that the AND circuit 584 normally receives a continuous enabling signal from the error card flip-flop 556, the connection to the field gate being utilized only to prevent actuation of the circuit 584 under certain circumstances as described hereinafter. In the usual operation, an AND circuit 584 receives an actuating signal from the flip-flop 583 when an insufficient number of individual data items are sensed in the first field. Consequently, and upon occurrence of an output signal from the amplifier 533 upon completion of scanning of the first field, the AND circuit 584 produces an error signal that is supplied through the OR circuit 573 to the flip-flop 574 to clear the punches for the first field and prevent punching of data therein. Of course, if the full required complement of data items is sensed in the first field, the flip-flop 583 is reset to its original condition before the occurrence of any input signal from the amplifier 533, signifying completion of sensing of this field. Under these circumstances, no output signal is produced by the AND circuit 584 and punching of the first field data is permitted.

A similar arrangement is used with respect to the second data field. The circuit in this instance comprises a trigger circuit 585 having its set and reset terminals connected to the last two stages in the second field portion of the ring counter 414 (FIG. 13). That is, the set and reset terminals of the flip-flop 585 of FIG. 11 are connected to devices 734 and 735 respectively. The "0" output terminal of the flip-flop 585 is connected to an AND circuit 586. The AND circuit 586 includes two additional

inputs, one of which is connected to an amplifier 587 that, in turn, is connected to the collector of the gate transistor 538 in the finish circuit of the control gate 422 for the second data field. The third input to the AND circuit 586 is again connected to the flip-flop 556 in the error card circuit, which normally provides an enabling signal to the AND circuit 586. The output of the AND circuit 586 is connected through the OR circuit 577 to the set input of the flip-flop 578. This circuit arrangement operates to prevent punching of data in the second data field when an insufficient number of data items has been sensed, in the same manner as the corresponding circuit arrangement described hereinabove for the first field.

The combined field error circuit 423 may also be actuated to prevent punching of data in either one or both fields in the event that there are more data items in a given field than those assigned to that field. This may happen if extraneous markings are interspersed with the desired pre-printed data markings on the record cards, or may result simply from an erroneous recording operation. For the first data field, the overcount arrangement in the detailed illustration of circuit 423 (FIG. 11) comprises an AND circuit 591 having two input terminals 592 and 593 that are connected to the rack memory circuit 411 described in detail hereinafter in connection with FIG. 16. The AND circuit 591 is connected through a non-inverting D.C. amplifier 595 to one of the inputs of an AND circuit 596. The AND circuit 596 is provided with a second input, indicated by the terminal 597, that receives a suitable actuating signal, once during each operating cycle, in response to actuation of a cam switch on the main shaft of the machine 10 that controls operation of the various machine devices such as the transport 12 and the punching station 14 (FIG. 1). In addition, the AND circuit 596 is provided with a third input circuit connected to the "0" terminal of a flip-flop 598 that is incorporated in the error card circuit 409. Again, this connection is provided to afford a means for disabling the AND circuit 596 during the feeding of an error card. That is, under normal circumstances, an enabling signal is supplied from the flip-flop 598 to the AND circuit 596, and this signal is interrupted when an error card operation occurs.

In the event of an overcount in the rack memory 411, actuation signals are developed at both of the terminals 592 and 593. As a consequence, an output signal is supplied from the AND circuit 591 through the amplifier 595 to the AND circuit 596. Upon closing of the cam switch connected to the terminal 597, which occurs once during each card cycle, the AND circuit 596 is actuated and supplies a control signal to the set terminal of the flip-flop 574. This results in the voiding of the field one information for the card being processed; that is, the data is not punched because an overcount has occurred with respect to the number of data items present in the first field.

Essentially the same system is utilized in connection with the second field except that in this instance only one circuit connection is provided to the rack memory 411, this being at the terminal 594. The terminal 594 is connected through a D.C. amplifier 599 to an AND circuit 601. The AND circuit 601 is connected to the terminal 597 in the same manner as the AND circuit 596. Furthermore, the AND circuit 601 is provided with a third input circuit that is returned to the "0" terminal of the flip-flop 598 in the error card circuit, the presence of an overcount signal at the terminal 594 results in the voiding of the second data field, in the same manner as in the case of the first data field.

Of course, means must be provided to reset the combined field error circuit 423 in each cycle of machine operation. This is accomplished by the connection of the emitter reset terminal of each of the flip-flop devices 574, 578, 583 and 585 to the output terminal 561 of the channel reset circuit 518. With respect to the two output flip-flop circuits, it is also desirable to assure resetting of

these circuits to the initial operation condition at the time that the machine is placed in operation. This is accomplished by a suitable circuit connection to the power supply from the reset circuit of each of the devices 574 and 578.

As noted hereinabove, a principal function of the error card circuit 409 is to cause the feeding of an error card from the second hopper 11A of the machine (see FIG. 1) whenever it is determined that there is a difference between the data recorded in the accumulator 407 and the data sensed from a summary card fed through the machine following the sensing of a related group of detail cards. As shown in FIG. 11, the error card circuit includes an input amplifier 605 having an input terminal 606 that is connected to the comparator error circuit 409, shown in detail in FIG. 15. The output of the amplifier 605 is connected to one of three inputs for an AND circuit 607. A second input for the AND circuit 607 is connected to the output of the amplifier 587 actuated by the finish gate transistor 538 of the gate control device 422 for the second data field. The third input for the AND circuit 607 is connected to an output terminal 608 of the control card detector 427, described in detail hereinafter in connection with FIG. 17. The output of the AND circuit 607 is connected to the set terminal of the flip-flop circuit 556. The "1" output terminal of the trigger circuit 556 is connected to the AND circuit 555 in the channel reset device 518, as noted above. Moreover, this same output terminal for the flip-flop 556 is connected to an AND circuit 609 having an additional input coupled to the output of the amplifier 533 that is controlled from the finish gate for the first field. The output of the AND circuit 609 is connected to the set terminal of the trigger circuit 598.

There is an additional circuit connection to the "1" terminal of the intermediate flip-flop 556 in the error card circuit 409. This connection goes to the base electrode of a gate transistor 611. The collector electrode of this transistor is connected to the actuating mechanism, in the machine 10, that is effective to initiate feeding of an error card from the auxiliary hopper 11A to the machine transport. Thus, the collector terminal 612 corresponds to the output terminal identified by the same reference numeral in the overall system diagram of FIG. 8.

As noted hereinabove, the "0" terminal of the trigger circuit 556 is connected to the AND circuits 584 and 586 in the combined field error circuit 423; it is also connected to the amplifier 527. The "0" output of flip-flop 598 is connected to the AND circuits 596 and 601 in the combined field error circuit. The "1" output terminal of the trigger circuit 598 is connected to an AND circuit 613 having a second input terminal 614 that is actuated in each cycle of machine operation by cam switch or similar device actuated by the drive mechanism of the punching machine. The output of the AND circuit 613 is connected through an OR circuit 615 to the reset terminal of the trigger circuit 556.

For actuation of the error card circuit 409, it is first necessary that a conditioning signal be received from the control card detector, since the error card circuit is not intended to control system operation during the sensing and punching of detail cards but is utilized only in connection with the summary cards. Each time a control card is fed to the machine, therefore, an initial actuating signal is supplied to the AND circuit 607 from the terminal 608 of the control card detector.

Usually, the data sensed from the second field of the summary card will correspond with that accumulated in the accumulator 407 (see FIG. 8), indicating that the pre-recorded data on the summary card is correct. Under these circumstances, no significant output signal is produced at the common terminal 606 of the comparator error circuit and the error card circuit. In the event that the comparison of the accumulated data from the detail

cards and the pre-printed code data from the summary card shows a discrepancy, however, an actuating signal appears at the terminal 606 and is supplied through the amplifier 605 to the AND circuit 607. Consequently, when a further actuating signal is supplied to the AND circuit 607 from the amplifier 587 upon completion of sensing of the second field of the summary or control card, an output signal is developed by the AND circuit 607 and applied to the set terminal of the trigger circuit 556.

Upon triggering of the flip-flop 556, an output signal from the "1" terminal of the flip-flop is supplied to the gate transistor 611, which produces an actuating signal to initiate the feeding of an error card from the second supply hopper 11A of the machine (FIG. 1). Of course, the machine control apparatus is arranged to prevent simultaneous feeding of a record card from the other or main supply 11. At the same time, an enabling signal is supplied to the AND circuit 609 and to the OR circuit 555 in the channel reset device 518. Moreover, the actuation of the trigger circuit 556 to its second stable state cuts off the normal enabling signal supplied to the AND circuits 584 and 586 in the combined field error circuit 423. This is done in order to make it possible to punch data in the error card, since otherwise a sensing operation with respect to the error card would fail to actuate the ring counter 414, which would result in voiding of the punch mechanism through this portion of the combined field error circuit. In addition, the normal circuit connections for the emitters of the field gate transistors 552, 535 and 538 are effectively changed by the signal supplied from the "0" terminal of the flip-flop 556 to the amplifier 527. This is done to prevent a sensing operation with respect to the error card, which is blank and contains no pre-recorded data. Finally, the connection from the amplifier 527 to the OR circuit 581 provides for the voiding of punched data with respect to the second data field.

With the circuit arrangement shown in FIG. 11, the photodiode 528 normally employed to detect the completion of sensing of the first data field is also utilized to detect the passage of an error card through the machine and it is for this reason that the emitter of the gate transistor is returned directly to ground rather than through the amplifier 527. As the error card moves through the sensing station, and the leading edge masked the diode 528, an output signal is supplied through the devices 529, 531 and 533 to the AND circuit 609. This signal, in conjunction with the actuating signal from the flip-flop 556, triggers the device 598 from its first stable condition to its second condition. This cuts off the normal enabling signal for the AND circuits 596 and 601 in the error device 423, preventing an undesired voiding of the punch setting for the error card that might otherwise result from the extraneous signals supplied from the rack memory 411 as described hereinabove. Moreover, triggering of the device 598 produces an output signal at the "1" terminal which is supplied to the AND circuit 613. Thereafter, and near the end of the cycle, a second actuating signal is supplied to the AND circuit 613, by operation of a cam-actuated switch or like timing device, through the terminal 614. The resulting output signal from the AND circuit 613 is effective to reset the trigger 556 and re-condition this portion of the error card circuit 409 for subsequent operation with respect to additional cards. Resetting of the second trigger device 598 in the error card circuit 409 is accomplished by a suitable circuit connection to the channel reset circuit 518 and specifically to terminal 561 therein. Of course, it is desirable to provide a means for assuring the desired setting of the flip-flop 556 upon placing the system in operation, and this is accomplished by a suitable circuit connecting the OR circuit 615, in the reset input to the trigger device 556, to the power supply of the system.

Solenoid Driver Matrix, FIG. 12

FIG. 12 illustrates one stage of the solenoid driver and

storage matrix 404. It should be understood that there are as many such stages as there are individual data items in the combined two fields on the record cards. Thus, with an initial field of ten items and a second field of five items as discussed hereinabove, there would be fifteen stages in the solenoid driver and storage matrix 404, each identical to the single stage shown in FIG. 12.

The section of the accumulator 404 that is illustrated in FIG. 12 comprises five individual storage and driver circuits 622, 624, 626, 628 and 629, the terminal digit in each reference character corresponding to the associated level of the machine code utilized to drive the punching machine 10. The set input to the circuit 622 comprises an AND circuit 632 having one input terminal connected to the OR circuit 472 of the machine code translator 403 (see FIG. 10). The other input of the AND circuit 632 is connected to the first stage of the ring counter 414 (FIG. 13) and specifically to the device 711. The reset input for the device 622, on the other hand, is connected to the output terminal 553 of the channel reset circuit 518 that is illustrated in FIG. 11. The "1" output of the device 622 is connected to the base electrode of a gate transistor 633. The emitter electrode of the transistor 633 is returned to system ground. The collector electrode is connected through a solenoid 642 to the emitter of a gate transistor 631. The base electrode of the transistor 631 is connected to an input terminal 630 and to another input terminal 627, the latter connection being made through a suitable resistor. The collector of the transistor 631 is connected to a negative D.C. supply identified as G—.

The circuit connections for the stages 624, 626 and 628 are essentially the same, and hence are not described in detail. Briefly, the output of each of the devices 624, 626 and 628 comprises a solenoid, these being the solenoids 644, 646, and 648 respectively, the connection in each instance being afforded by a suitable gate transistor. The set input for the stages 624, 626 and 628 comprises, in each instance, an AND circuit having one input connected to the device 711 in the first output stage of the ring counter 414 of FIG. 13. The other inputs to the AND circuits associated with each of devices 624, 626 and 628 come from the OR circuits in the output of the machine code translator 403, and specifically from the devices 474, 476 and 478 (see FIG. 10).

The functional illustration for each of the devices 622 through 628, as shown in FIG. 12, corresponds to that for an ordinary flip-flop circuit (see FIG. 9H). However, instead of conventional trigger circuits, a preferred form of the present invention utilizes a unique control circuit for this particular component of the control system. This novel circuit arrangement, which is described and claimed in the co-pending application of Max E. Sallach, Serial No. 117,171 filed concurrently herewith, is illustrated in detailed schematic form in connection with the final stage 629 of the illustrated portion of the accumulator 404.

The input AND stage for the device 629 comprises a first diode 651 that is connected to the output device 711 of the ring counter 414 and is returned to the terminal 553 through a resistor 652. The second input for the AND circuit comprises a diode 653 that is connected to the device 479 that comprises the final stage of the transistor 403 (FIG. 10). The two diodes 651 and 653 are connected together and are connected to an additional diode 654 that is returned to system ground through a resistor 655. The junction of the circuit between the diode 654 and the resistor 655 comprises the set input terminal "S" of the device 629.

The set input terminal "S" is connected through a coupling capacitor 656 to the base electrode of a transistor 657. The base electrode of the transistor 657 is connected to a positive-polarity D.C. supply, identified as H+, through a resistor 658. The emitter electrode of this transistor is connected to the E+ supply through a load resistor 659. The emitter of the transistor 657

also comprises the "1" output terminal of the device and is connected to the base electrode of the output or gate transistor 661. As before, the gate transistor 661 has a grounded emitter and is connected to the gate device 631 through an operating solenoid 649.

The emitter electrode of the first transistor 657 is also connected through a resistor 662 to the emitter of a second transistor 663. The transistor 663 is incorporated in a grounded-base circuit with the collector returned to the channel reset terminal 553 through a load resistor 664. The collector of the first stage transistor 657 is also returned to the channel reset terminal 553, in this instance by means of a resistor 665. In addition, a feedback connection is provided from the collector of the transistor 663 to the input or base electrode of the first transistor 657.

The initial stage of the circuit 629, following the input AND device, is a conventional emitter follower amplifier. The output of the device, the gate transistor 661, is simply a transistor switch which, to all intents and purposes, is normally open. That is, the device 661 is normally maintained substantially non-conductive and can be triggered to conduction by a signal supplied to the base electrode thereof.

The bias conditions for the transistor 657 are also such that this transistor is normally non-conductive. In the presence of a negative-going input signal supplied to the set input terminal, however, the transistor 657 is momentarily driven to conduct. The output signal appearing at the terminal "1" is, of course, a negative-going signal, since the emitter follower stage comprising the transistor 657 does not invert the polarity of the amplified signal. Moreover, the grounded-base stage comprising the transistor 663 also functions as a non-inverting amplifier, producing a negative-going output signal that is fed back to the base electrode of the transistor 657. Thus, once a negative-going input signal is supplied to the set terminal "S" of the device 629, the device is triggered from its normal or quiescent stable state to a second or actuated state in which it is also stable, the device 657 being maintained conductive and the device 663 being maintained cut off by the feedback loop comprising the connection from the collector electrode of the transistor 663 to the base electrode of the device 657. Furthermore, the output signal from the "1" terminal actuates the gate transistor 661 and renders it conductive so that the solenoid 649 can be energized upon completion of an external circuit through the code transistor 631 to the G-supply.

As set forth in greater detail in the aforementioned co-pending application of Max E. Sallach, the circuit 629 shown as one stage of the device 404 in FIG. 12 is quite advantageous, as compared with a conventional trigger or flip-flop circuit, because it draws little or no current until triggered by an input signal. Moreover, even after actuation to its second stable state, the device 629 draws only a limited input current until such time as the solenoid 649 is energized by actuation of the gate device 631. Thus, the total power requirements of the solenoid driver and storage matrix 404 are greatly reduced as compared to an arrangement using conventional trigger circuits.

From the foregoing description, it can be seen that, in any given sensing operation, a selected one (or a selected combination of two) of the devices 622, 624, 626, 628 and 629 may be triggered to their second stable state in response to the machine-code output signals from the device 403 of FIG. 10. The input signals from the ring counter 414 serve only to determine that the information is recorded in the illustrated stage of the matrix 404 rather than in some other stage. The connection to the channel reset circuit 518, terminal 553, the solenoid driver matrix upon completion of each operating cycle of the system. The inputs supplied to the terminals 627 and 630 perform only a timing function for energization of the solenoids 642 et seq. that perform the actual punch

selection by moving the individual punch selection racks (such as the rack 413 of FIG. 8) in setting up the punch operation for the machine 10.

The Ring Counter, FIG. 13

The logic arrangement for the ring counter 414 is shown in substantial detail in FIG. 13. Beginning at the lower left-hand corner of this figure, there are illustrated ten individual trigger devices 681 through 690, and these comprise the first ten stages of the ring counter, corresponding to the first data field in the data arrangement described hereinabove. The initial stage 681 is provided with a connection to its set input terminal from the sequence timer 416 of FIG. 17, the connection being indicated by the terminal 691. The reset terminal of the stage 681 is connected to the "0" output terminal of the next stage, the device 682. The auxiliary reset input "E" of the device 681 is connected to a circuit that provides a reset signal, at terminal 692, on the basis of operation of a cam-actuated switch controlled by the printing machine 10. In addition to the usual complement of input terminals, the device 681 is provided with an auxiliary set input terminal "AS" that is connected to the "0" output of the final stage 690.

The succeeding stages 682 through 689 of the ring counter are generally similar to stage 681. That is, each stage has its set terminal connected to the terminal 691. In each instance the reset terminal is connected to the "0" output of the next succeeding stage. The auxiliary reset connection is the same in each instance, being made to the terminal 692. The auxiliary set connection for each of these stages comes from the "0" output of the preceding stage.

The final device 10 in the first decade of the ring counter 414 is, as might be expected, somewhat different in its circuit connections. In this instance, the set input is connected to the terminal 692. The auxiliary set input is connected to the terminal 691. The reset connection is made to the "0" output of the preceding stage 689. The auxiliary reset connection is made from an OR circuit 693 described in further detail hereinafter.

In addition to the first decade comprising the stages 681-690, the ring counter 414 includes an auxiliary stage 694 and five additional stages 701, 702, 703, 704 and 705. The stages 701, 702, 704 and 705 are generally similar to each other. Thus, the set input connections of these devices are connected in common, and all are connected to the "1" output of the penultimate stage 689 in the initial decade of the counter. In each instance, the auxiliary set input is connected to the "0" output of the preceding stage, the auxiliary set input of the device 701 being connected to the device 694. The auxiliary reset circuit for each of the devices 701, 702, 704 and 705 is connected to the terminal 692 that is, in turn, connected to a cam-actuated switch circuit as noted hereinabove. The auxiliary reset circuit of the device 701 is connected to the "0" output of the next stage, and this is equally true of the reset input for the device 704. The main reset input for the device 702 is connected to the output of an AND circuit 695, the input arrangements for this AND circuit being described hereinafter. The reset circuit for the device 705, on the other hand, is connected to the output of an AND circuit 696. One input to the AND circuit 696 comes from the "1" output of the trigger circuit 705. The other input to this AND circuit comes from the "1" output of the device 689 in the initial portion of the ring counter. The "1" output of the device 705 is also connected to the OR circuit 693. The OR circuit 693 has a second input which is derived from the "0" output of the first stage 681 in the counter.

The auxiliary stage 694 of the ring counter is provided with a reset input from an OR circuit 697. One input to the circuit 697 is from the "0" output of the ring counter device 701. The other input to the OR circuit 697 is taken from the output terminal 698 of the start gate 535

for the second data field, illustrated in FIG. 11. The set terminal for the device 694 is connected to a terminal 699 to receive an actuating signal from a cam-operated switch or similar timing device in the punching machine 10.

The cam-actuated input terminal 699 is also connected to an OR circuit 707 that is connected to the reset terminal of stage 703 of the ring counter. The OR circuit 707 is provided with a second input that is connected to the "0" output terminal of the succeeding stage 704. The set terminal of the device 703 is connected to an OR circuit 708 having two inputs. One input to the OR circuit 708 comes from the AND circuit 695 and the other input is taken from the terminal 698 in the second field start gate of FIG. 11.

The AND circuit 695, referred to hereinabove, is provided with three inputs. One of these inputs is taken from the "1" output terminal of stage 702 of the counter. Another is connected to the "1" output of the stage 689. The third input to the device 569 is derived from the error card circuit 409, and specifically the flip-flop 598 (FIG. 11), as indicated by the common terminal 920.

The output stages of the ring counter 414 are shown at the right-hand side of the drawing. They comprise the individual AND circuits 711 through 720 and 731 through 735. Each of the AND circuits includes two input connections. For the AND circuits 711 through 719, in each instance one input is connected to the "1" output of the auxiliary stage 694 of the ring counter. The remaining input to each of these AND circuits is connected to an individual respective one of the units stages 681 through 689. That is, the second input of the AND circuit 711 is connected to the "1" output terminal of the device 681, the AND circuit 712 is connected to the device 682, and so on. The tenth stage in the first decade in the output, the device 720, has its two input circuits connected to the "1" output terminals of the ring counter flip-flops 690 and 701 respectively.

Each of the AND circuits 731-735 in the second rank of the ring counter is provided with one input that is connected to the "1" output of the trigger circuit 703. The second input of the device 731 is connected to the "1" output of the units device 681, the second input of the AND circuit 732 is connected to the "1" output terminal of the device 682, and so on. It will be recognized that additional stages could be added to the ring counter and that the limited number shown are used because there are only fifteen data items to be checked in the system under consideration. In actual construction, it is usually preferable to provide an individual amplifier stage in the output of each of the AND circuits of the ring counter, but these have been omitted from FIG. 13 in order to simplify the drawing.

The operation of the ring counter 414 will be generally apparent to those experienced in the construction and use of circuits of this general kind, and is therefore described only briefly. When sensing of the first data field has been initiated, a set signal is supplied to each stage of the first decade of the counter through the terminal 691 from the sequence timer 416 described hereinafter in connection with FIG. 17. The setting of each stage is dependent upon two input signals, this being the purpose of the auxiliary set input in each instance. Thus, when the first signal is received at the terminal 691, only the first stage 681 is actuated from its initial operating condition to its second stable state. This action proceeds progressively down the chain to the final stage 690 in the first decade, after which the stages at the top of the drawing in FIG. 13 come into operation. These stages operate in much the same manner except that the circuit arrangement is such that they cannot start the counting sequence until an input signal is received at the terminal 698, indicating the initiation of sensing of the second data field. Of course, it is necessary to provide for resetting of the counter, and this is accomplished with respect to each stage, during the

counting operation, by the indicated connection to the reset terminals. The auxiliary reset arrangement provided for most of the circuits is used to assure clearing of the ring counter prior to initiation of operation with respect to each card passed through the machine. This is accomplished through the connection, at the terminal 692, to a cam-actuated switch incorporated in the machine itself. The connection to the terminal 920 in the error card circuit makes it possible to inhibit operation of the second-field output devices 731-735 during an error card operation. Of course, other ring counter arrangements could be employed in the system instead of the particular sequence of circuits illustrated in FIG. 13.

Accumulator and Control, FIG. 14

The accumulator control devices 406 and the accumulator 407 of the system 400 (FIG. 8) are shown in substantial detail in FIG. 14. The accumulator control device 406 comprises five individual stages 741, 742, 743, 744 and 745. Because the individual stages are essentially identical with each other, with the exception of input signal connections only the final stage 745 is shown in detail. This stage of the accumulator control comprises the binary trigger circuits 751, 752, 754 and 758, the accumulator control being arranged for binary operation. Accordingly, the set and reset terminals of each trigger circuit are connected to each other. The binary circuit 751 has its set and reset terminals connected to an AND circuit 759 having two inputs. The first input comes from the device 481 in the binary coded decimal translator 405 (FIG. 10). The other input to the AND circuit 759 comes from the ring counter 414 (FIG. 13) and specifically from the output AND circuit 735 of the ring counter. In addition, a further connection is provided to the set and reset input terminals of the trigger circuit 751 from an AND circuit 761 that is described more fully hereinafter. The auxiliary or emitter connection for the device 751 comes from the channel reset circuit 518 (FIG. 11) and specifically from terminal 561 therein.

The second flip-flop 752 in the stage 745 of the accumulator control is essentially similar to the first trigger circuit 751. That is, the set and reset inputs for the device 752 are connected together and are connected to an AND circuit 762. One input for the AND circuit 762 comes from the device 735 in the ring counter. The other input is connected to the device 482 in the binary convertor 405 (FIG. 10). In addition, the set and reset inputs to the devices 752 are connected to the "1" output of the first trigger circuit 751, which is also connected to an AND circuit 763. As before, the emitter or auxiliary reset connection is made to the channel reset circuit 518 of FIG. 11.

The connections for the next binary flip-flop 754 in the chain are similar, the set-reset circuit entailing the use of an AND circuit 764 having inputs from the ring counter output device 735 and from the convertor output device 484. Again, the set and reset inputs are connected to the "1" output of the preceding stage, a further connection being made from that output circuit to the AND circuit 763. The fourth and final stage in the binary chain, the device 758, is essentially similar and utilizes an input AND circuit 765. In this instance, one of the inputs of the AND circuit 765 is connected to the device 488 in the convertor 405 of FIG. 10. The only connection made to the "1" output is that to the AND circuit 763, this being the last stage of the binary chain.

The output of the AND circuit 763 is connected through a D.C. inverting amplifier 766 to one of the two inputs of the AND circuit 761. The second input for the AND circuit 761, at the terminal 767, comes from the clock timer 415 of FIG. 17.

The other stages 741 through 744 in the accumulator control device 406 may be identical with the stage 745. The only exception is that instead of the connection from the device 735 in the ring counter, each of the stages 741 through 744 is provided with a connection from the corre-

sponding one of the devices 731 through 734 in the ring counter.

The accumulator 407, like the control circuit 406, comprises five stages 771 through 775 that are essentially identical with each other except for their input connections. Accordingly, only the stage 775 is shown in detail. The stage 775 of the accumulator 407 comprises a one-shot multi-vibrator 780. The input to the multi-vibrator 780 is taken from an AND circuit 779, the connections to the AND circuit being described in greater detail hereinafter. The "1" output of the one-shot multi-vibrator 780, is connected, at the terminal 778, to the overflow detector 430 (see FIG. 17). The "0" output of the multi-vibrator is connected through an OR circuit 791 to the base electrode of a gate transistor 792. The base electrode of the transistor 792 is returned, through a resistor 793, to the C— supply. The emitter of the device 792 is grounded and the collector electrode is connected to the auxiliary reset input of each of the four binary flip-flop circuits 781, 782, 784 and 788.

The binary flip-flop device 781 has its set and reset input terminals connected to the output of the AND circuit 761 in stage 745 of the accumulator control device 406. The "1" output is connected to the set and reset terminals of the next binary flip-flop 782. In turn, the "1" output of the device 782 is connected to the set and reset inputs of the next stage 784, and a similar connection is made from the "1" output of the device 784 to the input of the binary circuit 788. Thus, a complete binary chain is provided.

The carry circuit for stage 775 in the accumulator 407 comprises the AND circuit 779. The first input to this AND circuit is taken from the "1" output of the second binary circuit 782. A second input for the AND circuit 779 is derived from the "1" output of the final binary circuit 788. The third input to the AND circuit 779 is derived from a cam-actuated timing circuit, this third input being applied at the terminal 794. As noted hereinabove, the output of the AND circuit is connected back to the input of the preliminary stage 780 for the binary chain.

As noted hereinabove in connection with the description of FIG. 8, it may be desirable to afford a means for supplying data from the accumulator 407 to the solenoid driver and storage matrix 404 to permit the punching of data in either a summary or error card that is derived from the accumulator rather than from pre-printed code data as in the case of the normal detail cards. Where this modification of the system is to be employed, the necessary data signals are derived from the accumulator 407 by a series of AND circuits 801, 802, 804 and 808. The first input to the AND circuit 801 is derived from the ring counter 414 and specifically from the device 735 therein. A corresponding timing or actuating input connection is made to each of the AND circuits 802, 804 and 808. The second input to each of these circuits is derived from an individual one of the binary devices 781, 782, 784 and 788 in the accumulator proper. Of course, the output signals derived by the AND circuits 801, 802, 804 and 808 are still encoded in accordance with binary notation, and would require translation to the machine code before being applied to the solenoid driver and storage matrix 404.

The remaining stages 771 through 774 of the accumulator 407 are essentially identical with the fully illustrated stage 775 except for changes in input connections. Thus, stage 771 of the accumulator is provided with an input connection from device 731 in the ring counter 414 instead from the device 735 as in the case of the stage 775. Similarly, the stages 772, 773 and 774 are provided with input connections from the ring counter devices 732, 733 and 734 respectively. The input connection from the accumulator control for each of the devices 771 through 774 is taken from the corresponding one of the stages 741 through 744. Moreover, each of the individual stages in the chain comprising the accumulator 407 is connected to the preceding stage. Thus, an input connection to the

device 781 in the fully illustrated stage 775 is effected from the "1" output of the auxiliary multivibrator corresponding to the device 780 but incorporated in the stage 774. Similar connections are made along the chain from each stage to the next.

In considering the normal operation of the accumulator control circuit 406 and the accumulator 407, it should be remembered that the data from the converter 405 of FIG. 10 is in binary decimal form but also in the form of the fifteens complement of the actual numerical data. It is believed that the operation can best be understood by consideration of a specific example. Thus, if the actual numerical value to be recorded in the accumulator 407 is six, then the fifteens complement would be nine. In accordance with conventional binary notation, this may be represented by the number 1001, with significant digits in the one and eight levels of the binary notation. Thus, this particular numerical value would be supplied to the accumulator control device 406 from the converter 405 of FIG. 10 in the form of signals from the individual output devices 481 and 488 of the converter 405. These input signals are supplied to the AND circuits 759 and 765 simultaneously with timing signals from the ring counter 414, and specifically from the device 735 therein (see FIG. 13). Accordingly, the binary flip-flops 751 and 758 are actuated from their normal or "zero" operating condition to their set or "one" condition, recording in the stage 745 the binary numeral 1001.

The construction of the circuits 761 and 766 is such that the AND circuit 761 normally receives an enabling signal from the D.C. amplifier circuit 766. Consequently, when a signal comprising a series of pulses is received from the clock timer 415 at the terminal 767, each of these pulse signals is passed by the AND circuit 761 until such time as the input from the amplifier 766 is cut off. Moreover, each of these pulses is supplied from the output of the AND circuit 761 to the first circuit 781 in the chain 775 in the accumulator 407 and also to the initial binary flip-flop 751 in stage 745 of the accumulator control.

Considering what happens in the accumulator control stage 745, the first pulse from the AND circuit 761 resets the binary device 751, thereby producing an output signal that sets the device 752. Thus, after the first signal pulse from the AND circuit 761, the binary number recorded in the accumulator control stage 745 is 1010. The second pulse from the AND circuit 761 again sets the binary device 751. No output signal is produced, in this instance, so that the recorded binary number is now 1011.

The third pulse output signal from the AND circuit 761 again resets the initial binary circuit 751. This produces an output signal that resets the second circuit 752 in the chain and this circuit in turn produces an output signal that sets the circuit 754. Accordingly, at this point, the recorded binary numeral in the control stage 745 is 1100. The fourth signal pulse from the clock timer that is translated by the AND circuit 761 again sets the initial binary circuit 751, changing the recorded number to 1101. On the next pulse, the first stage 751 is again reset, producing an output signal that sets the device 752, the recorded number now being 1110. The sixth pulse is then applied to the circuit 751, again setting the first binary circuit 751, and resulting in recordation in the accumulator control stage 745 of the binary number 1111. When this level of recordation is achieved, the output connections from the "1" terminals of each of the binary devices 751, 752, 754 and 758 produce an output signal from the AND circuit 763 that actuates the amplifier 766 to cut off the enabling signal to the AND circuit 761. Accordingly, it is seen that the AND circuit 761 will pass no further pulse signals. Furthermore the total number of pulse signals that have been passed are equal to the desired numerical value of six, and these pulse signals have also been applied to the binary chain 775 in the accumulator 407 and are recorded therein. Thereafter, the binary

chain 745 is cleared by a reset signal from the channel reset device 518 of FIG. 11 and is ready for the next conversion and control operation. Of course, the accumulator binary chain 775 is not cleared, but continues to receive the signal impulses from the control stage 745 for each detail card and to cumulatively record the numerical values from the cards.

It is necessary to effect a reset operation with respect to the accumulator 407 under certain circumstances. Thus, the accumulator must be cleared prior to initiation of machine operation. This is accomplished by means of a pair of multi-vibrator circuits 811 and 550. The "1" output of the device 811 is connected to the input of the device 558. The "1" output of the multi-vibrator 550 is connected through an OR circuit 812 to a D.C. inverting amplifier 813 that, in turn, is connected to the OR circuit 791 connected in the auxiliary reset input circuit for all of the binary devices 781, 782, 784 and 788. The initial one-shot multi-vibrator 811 receives a signal input from the power supply build-up when the control system is placed in operation. As a result, it produces an output signal that triggers the device 550. After a considerable time delay, the device 550 produces an output signal that is translated through circuits 812, 813 and 791 to supply a reset pulse to each binary circuit in the accumulator stage 775. Of course, a similar reset arrangement would be utilized in connection with the other accumulator stages 771 through 774 and, indeed, the necessary connection can be taken from the amplifier 813 without requiring duplication of the associated circuit arrangement.

It is also desirable to assure complete clearing of the accumulator after translation of an error card through the machine. This is accomplished by means of an AND circuit 814 that is also connected to the OR circuit 812 and the amplifier 813 to the emitter or auxiliary reset circuits of the individual components in the binary chains. One input for the AND circuit 814 is derived from the error card circuit 409 of FIG. 11 and specifically from the "0" output terminal (terminal 944) of the trigger circuit 556 included therein. A second input for the AND circuit 814 is taken from the control card detector 427 of FIG. 17 and specifically from terminal 815 therein. A third input is provided for the AND circuit 814, and this comes from a signal source actuated by a cam switch controlled by the operating elements of the punching machine. The signal supplied to the accumulator 407 through the AND circuit 814 are effective to clear the accumulator following the passage of an error card through the machine as described hereinabove.

Comparator Error Circuit, FIG. 15

FIG. 15 illustrates the comparator error circuit 408 which is utilized to actuate the error card circuit 409. As illustrated in FIG. 15, the comparator error circuit 408 is quite simple in construction. It entails five stages 821, 822, 823, 824 and 825. Because the stages 821 through 824 are essentially identical to the stage 825 except for the input circuit connection, only the stage 825 is shown in detail.

The initial stage 825 of the comparator error circuit 408 comprises a series of eight AND circuits 831 through 838. Each of the AND circuits 831-838 is provided with two inputs. The first circuit 831 is connected to the "1" output terminals of the devices 751 and 781 in the accumulator control circuit 406 and the accumulator 407 of FIG. 15. The next AND circuit 832 is connected to the "1" output terminals of the same two binary circuits in the accumulator and accumulator control devices. The AND circuit 833 is connected to the "1" outputs of the binary flip-flop devices 752 and 782 of FIG. 14. The next AND circuit 834 is connected to the "0" output terminals of the same two binary devices. This connection pattern is continued, so that all of the "1" outputs of the accumulator control 745 and the accumulator stage 775

are connected to the comparator error stage 821, the "1" outputs always being paired and the "0" outputs also always being paired.

All of the AND circuits 831 and 838 are connected to an OR circuit 839 which, in turn, is connected to an OR circuit 841. The construction of each of the remaining stages 821 through 824 of the comparator error circuit 408 is the same as described for stage 825, except that they are associated with different levels of the accumulator control and accumulator circuits. That is, the comparator error stage 821 is connected to the individual binary devices in the accumulator control stage 741 and the accumulator stage 771 of FIG. 14. The comparator error stage to the accumulator control stage 742 and the accumulator stage 772, and so on. As noted hereinabove, the output terminal 606 of the OR circuit that is common to all stages is connected to the error card circuit 409 of FIG. 11.

As will be apparent from the logic diagram, the circuit 408 compares data already recorded in the accumulator 407 with data recorded in the control 406. Since in the one instance the data is in binary-coded decimal notation (accumulator 407) and in the other in complemental form (control 406), the corresponding stages in each chain of each device should always be in opposite stable operating conditions. Any variation from this condition produces an output signal from one or more of the multiple AND circuits of the comparator 408, triggering an error card operation.

The rack memory 411 that is utilized to check the setting of the punches in the machine 10 against the input data is shown in FIG. 16. This device includes fifteen substantially similar stages 851 through 865. Because all of the stages are substantially identical except for input circuit connections, only the initial stage 851 corresponding to the first data item is shown in detail.

The binary counter stage 851 includes four binary flip-flops 871, 872, 874 and 878. The first binary device 871 has its set and reset terminals connected to an AND circuit 881. The AND circuit 881 is provided with a first input from the ring counter 414, and specifically from the first output stage 711 of the ring counter 414 (FIG. 13). The other input to the AND circuit 881 is from the device 481 of FIG. 10, this being the initial output of the fifteens complement binary coded decimal translator 405.

The "1" output of the binary device 871 is connected to the set and reset terminals of the next device in the chain, the flip-flop 872. The "0" output of the flip-flop 871 is connected to an OR circuit 883. The auxiliary reset terminal of the device 871 is connected to the channel reset circuit 518 of FIG. 11, and specifically to terminal 561 therein.

The circuit connections for the succeeding circuits in stage 851 of the rack memory 411 are essentially similar to those for the first stage. Thus, each of the devices 872, 874 and 878 is provided with an input connection to the preceding stage in the chain. In addition, each is provided with an input connection to an AND circuit actuated conjointly by a first signal from the ring counter 414 and a second signal from a respective one of the output stages of the fifteens complement decimal translator 405. In each instance, the "0" output of the binary flip-flop is connected to the OR circuit 883, the auxiliary reset inputs all being connected to the terminal 561.

In addition to the foregoing, a further input circuit is provided for the first device 871 in the binary chain. This input circuit comprises an AND circuit 884 having one input actuated by a suitable timing switch or the like. The second input to the device 884 is taken from the sensing device 412 associated with the first punch rack 413 in the machine, an amplifier 885 being included in this circuit. As noted hereinabove, the device 412 is

arranged to provide a series of output signal impulses indicative of the setting of the punch rack 413, the total number of pulses representing the decimal value of the rack setting.

In operation of the initial stage 851 of the rack memory 411, the incoming data signals derived from sensing of the record cards are first recorded in the binary devices 871, 872, 874 and 878; more accurately, the fifteens complement of the first data item is recorded in the binary chain. Thus, the recording is essentially similar to that described hereinabove for the accumulator control device 406. When the punches are actually set, the pulse signals developed by the sensing devices 412 are supplied to the binary chain through the amplifier 885 and the AND circuit 884. Consequently, the chain counts out and, if the setting of the punch rack matches the initial input data, the result is the actuation of each of the devices 871, 872, 874 and 878 to "set" condition. Stated differently, the net result for a correct setting of the punch rack would be the recording of the binary number 1111 in the chain 851. The connection to the OR circuit 883 is such that the OR circuit produces an output signal whenever any of the individual binary flip-flops is not set in this manner. Consequently, if there is any error in the comparison operation effected by the first stage 851 of the rack memory, then an output signal appears at the terminal 592 that is connected to the OR circuit 883.

The same construction and operation are employed in connection with the remaining stages of the rack memory, each being controlled in accordance with a different stage of the ring counter 414. It is thus seen that if all punches are set accurately, no output signal appears at any of the three output terminals 592-594. This is the condition achieved in normal operation. Of course, if any discrepancy appears in the entailed comparison of punch settings with input data, then an output signal does appear at one or more of the terminals 592-594, and it is this signal that is supplied to the combined field error circuit 423 of FIG. 11 and utilized therein to prevent an erroneous punching operation, as described hereinabove.

Timing and Related Circuits, FIG. 17

FIG. 17 illustrates a number of circuits from the system 400 of FIG. 8, including particularly the control card detector 427, the clock timer 415, the sequence timer 416, and the overflow detector 430.

One of the basic circuits illustrated in FIG. 17 is the clock timer 415. This device comprises a high-frequency oscillator 390 that is connected to a pair of substantially similar monostable multi-vibrators 891 and 892. The "1" output of the device 892 is connected to an AND circuit 893, and the AND circuit in turn is connected through an amplifier 894 to the output terminal 767 that supplies counting pulses to the accumulator control device 406 of FIG. 14. The output of the other multi-vibrator 891 is connected to an AND circuit 895 having five individual input circuits. One of these, indicated at terminal 896, is connected to a cam-actuated switch controlled by the cyclic operation of the punching machine. Another input of the device 895 is connected to the output terminal 608 of the control card detector 427. Another input for the AND circuit 895, indicated by the terminal 897, is connected to the "0" output of the trigger circuit 578 in the combined field error circuit 423 (FIG. 11).

The output of the AND circuit 895 is connected to an OR circuit 898, the OR circuit 898 having a second input connected to the power supply of the system. The OR circuit 898 is connected to the set input of a flip-flop device 899. The reset circuit of the device 899 is connected to a pulse developing circuit in the power supply. The device 899 further includes an auxiliary reset input taken from terminal 900 in the second field gate device 422 (FIG. 11).

The "0" output of the flip-flop 899 is connected back to the AND circuit 895 in one of the inputs thereto. It is also connected to the input of a one-shot multi-vibrator 901. The "1" output terminal of the multi-vibrator 901 provides the second input to the AND circuit 893.

In operation, the oscillator 890 of the clock timer 415 is operated continuously, producing a high frequency output signal. This signal may be of the order of 25 kilocycles per second, although higher or lower frequencies can be used if desired. The oscillator drives the two one-shot multi-vibrators which, as a result, produce output pulses of fixed frequency, determined by the operating periods of the multi-vibrators.

The output signal from the device 891 is supplied to the AND circuit 895. The device 895 also receives an input signal from the cam input 896, limiting the transmission time for the AND circuit to a restricted portion of the machine cycle. Ordinarily, the AND circuit 895 receives an enabling signal from the control card detector 427, this signal being cut off when a control or summary card is fed to the machine. The signal supplied to the AND circuit 895 from the terminal 897 restricts operation of the AND circuit to periods in which no error card is being fed through the machine. Thus, an output signal from the AND circuit 895 is available only under limited circumstances corresponding to those in which it is desired to actuate the accumulator control 406 to produce a recording operation in the accumulator 407 as described hereinabove. The output from the AND circuit 895 is the normal control for the trigger circuit 899 and the one-shot multi-vibrator 901. On the other hand, the power supply pulse circuit connections provide a means for resetting the trigger circuit 899 at the beginning of system operation. In each cycle of operation, of course, the circuit 899 is reset by a signal from the second field gate circuit 422 (FIG. 11) to initiate the clock timer operation at the proper point with respect to scanning of the second data field, since only this data field is concerned with data to be handled by the accumulator 407 in the system as described hereinabove.

The sequence timer 416 is relatively simple in construction. The principal input is an OR circuit 911 that is connected to the output terminal of each of the data code multi-vibrators 440, 441, 442, 444 and 447 in the data amplifiers 402 as illustrated in detail in FIG. 10. The output of the OR circuit 911 is connected to a D.C. inverting amplifier 912 which, in turn, is connected to the input of a one-shot multi-vibrator 913. The multi-vibrator 913, in turn, is connected to the inputs of two one-shot devices 914 and 915 comprising sources of timing signals for the system.

The output of the OR circuit 911 is also connected to an OR circuit 916. The OR circuit 916 has a second input connected to the AND circuit 918. A first input for this AND circuit is taken from the "1" output of the one-shot multi-vibrator 891 in the clock timer 415. A second input, terminal 919, comes from a cam-actuated timing switch in the punching machine. The third input to the device 918 is taken from the "1" output of the flip-flop 930 in the error card circuit 409 (FIG. 11), the common terminal being identified by the reference character 920. The output of the OR circuit 916 is utilized to drive a D.C. amplifier 917 having an output terminal 691. The amplifier 917, therefore, is the source of the timing signals supplied to the ring counter 414 (FIG. 13).

FIG. 17 also includes the control card detector 427, illustrated in the upper left-hand corner of the drawing. This comprises a sensing device, the photodiode 931, which is coupled through an A.C. inverting amplifier 932 to the base electrode of a gate transistor 933. The emitter of the gate transistor is returned to ground through a cam-actuated switch circuit, the details of which are not

illustrated in the drawing, the switch being controlled by the cyclic movement of the operating mechanism in the punching machine 10. The collector of the transistor 933 is returned to the C— supply through a suitable load resistor and is connected to the set terminal of a flip-flop circuit 934.

The reset terminal of the flip-flop 934 is connected to an OR circuit 935. The OR circuit 935 has two inputs, one of which is a pulse developing circuit of conventional form utilized to develop an input signal upon energization of the system power supply. The other input is from a timing switch, at the terminal 936, and is used to reset the flip-flop 934 in the control card detector 427 (terminal 608) is used for several different purposes as described hereinabove. The "1" output (terminal 815) is connected to the set terminal of a second flip-flop 937 and also to other circuits in the control system as noted in the foregoing description of those circuits. The reset terminal of the flip-flop 937 is connected to the channel reset device 518 of FIG. 11 and specifically to terminal 561 of that device. The flip-flop 937 is employed to control the scanning lamps that illuminate the various photocells at the scanning station 13 of the machine 10 (see FIG. 1), the light control circuit 938 not being shown in detail.

The function of the control card detector 427 is relatively simple and should be apparent from the logical diagram of FIG. 17. Briefly, the photocell 931 is actuated in the presence of a control card, being constructed to differentiate between the control or summary card and the other cards used in the system by virtue of the card color or a special control marking on each summary card. The photodiode 931 produces an output signal that actuates the gate transistor 933, the output signal from the transistor in turn being used to actuate the flip-flop 934. The output signals from the terminals 608 and 815 of the device 934 control the circuit operations in various component circuits of the system, as described hereinabove.

The last circuit illustrated in FIG. 17 is the overflow detector 430. The input of this device comprises an AND circuit 941 having one input connected to terminal 815 in the control card detector 427. A second input signal to the AND circuit 941, the terminal 942, is connected to a cam-actuated timing switch controlled by the cyclic operation of the punching mechanism. Another input 943 is connected to a sensing switch, not shown, that is located at the discharge end of the machine and produces a control signal when the card receiver is nearly filled to capacity. Finally, there is a fourth input to the AND circuit 941 that is taken from FIG. 11, and specifically from the "0" output of the trigger circuit 556 in the error card circuit 409, this input being identified as terminal 944.

The output of the AND circuit 941 is connected to an OR circuit 945. The circuit 945 has a second input taken from the output terminal 778 of the one-shot multi-vibrator 780 in the accumulator 407 (FIG. 14). The OR circuit 945 also has a third input from an external switch-controlled circuit that may be actuated by the machine operator.

The output from the OR circuit 945 is coupled to the set input of an overflow trigger circuit 946. The reset circuit of the device 469 is connected to the power supply by means of a conventional pulse-generating circuit that produces an input pulse upon energization of the power supply. The device 946 is also provided with an auxiliary reset circuit that may be actuated by a switch accessible to the machine operator. The "1" output of this trigger circuit is connected to the base electrode of a gate transistor 947, the base electrode also being returned to the H+ supply through a resistor 948. The emitter electrode is connected to the E+ supply. The collector is the output electrode for the gate and is con-

connected to a terminal 949, the terminal 949 being in turn connected to the main operating electrical circuit of the punching machine 10 to provide a means for stopping machine operation.

When the punching machine is in operation, it is of course undesirable to continue passing cards through the machine for punching when the card receiver at the end of the machine exceeds its capacity, because the cards would inevitably be mixed and perhaps damaged under these conditions. On the other hand, it is not desirable to stop the machine mid-way through the sensing and punching of a related group of detail cards. When the card receiver of the machine is nearly filled, the sensing switch associated therewith (not shown) is actuated to supply the input signal to the AND circuit 941. This signal is developed when the card receiver nears its capacity but can still receive some additional cards. The next time a control card is detected by the device 427, a further input signal is supplied to the AND circuit 941. An enabling signal is normally continuously supplied to the AND circuit from the error card circuit (FIG. 11) through the terminal 944, and a further actuating signal is supplied cyclically to the AND circuit through the terminal 942. Thus, when the card receiver is nearing its capacity, passage of a control card through the machine produces an output signal from the AND circuit 941 that is translated to the overflow trigger circuit 946 through the OR circuit 945. Actuation of the trigger circuit 946 produces an output signal that actuates the gate 947, stopping the machine by means of an output signal supplied to the terminal 949. The purpose of the connection to the error card circuit, through the terminal 944 of the AND circuit 941, is to defer this action one more cycle where an error card is to be run through the machine due to an error in the summary card data.

The overflow detector can also be actuated by a signal from terminal 778 of the accumulator 407, FIG. 14. Thus, it may happen that the total data from the detail card may exceed the capacity of the accumulator. When this happens, a suitable actuating signal is supplied through the OR circuit 945 to the overflow trigger circuit 946 to stop the machine. The machine operator can also interrupt operation in the same manner by actuating a switch to supply an input signal to the system through the external set connection of the OR circuit 945. Resetting of the trigger circuit 946 requires manual actuation of a separate switch by the machine operator, since the overflow detector 430 only operates when some condition occurs which requires attention on the part of the operator.

Circuit Examples, FIGS. 18 and 19

FIG. 18 illustrates, in substantial detail, a particular example of a circuit arrangement that may be utilized in constructing one of the sensing devices utilized for data sensing purposes, together with the associated trigger circuit and output amplifier. That is, FIG. 18 shows a complete construction for the amplifier and timing circuits of the device 401-0, the associated flip-flop circuit 440 and the amplifier 450 (see FIG. 10).

The initial pre-amplifier 432 comprises a transistor 951 having its base electrode connected to the diodes 431. The collector of the transistor 951 is connected to the C— supply. The emitter is returned to ground through a load resistor 952. The coupling circuit to the next stage 433 comprises a coupling capacitor 953 that is connected from the emitter of the transistor 951 to the base electrode of a second transistor 954. The base electrode of the transistor 954 is also connected to the C— supply through a resistor 955.

In the second pre-amplifier section 433, the emitter electrode of the transistor 954 is grounded. The collector electrode is connected to the C— supply through a load resistor 956. The collector electrode is also connected to the coupling circuit comprising the resistor 434 and

the capacitor 435. The AND circuit 436 is of relatively simple construction and comprises a pair of diodes 957 and 958 that couple the sequence timer 416 and the field gate circuits 421, 422, respectively, to the common terminal 959 of the resistor 434 and the capacitor 435. The terminal 959, which comprises the output terminal of the AND circuit 436, is connected to the base electrode of a transistor 961 incorporated in the amplifier stage 437. The emitter of this transistor is returned to the F— supply and the collector is connected to the C— supply through a load resistor 962.

The one-shot multi-vibrator 440 comprises a pair of transistors 963 and 964. The emitter electrodes of these two devices are grounded. The collectors of these transistors 963 and 964 are connected to the C— supply by means of the resistors 965 and 966, respectively. The base electrode of the transistor 963 is connected to the collector of the transistor 964 by a capacitor 967. The base electrode of the transistor 963 is also connected to the H+ supply through a resistor 968 and to the C— supply by means of a resistor 969. The base electrode of the device 963 is also returned to the F— supply through a resistor 971 and is coupled to the sequence timer 416 by means of a coupling capacitor 972.

The input for the device 440 comprises a diode 973 that is connected between the collector electrode of the transistor 961 in the preceding stage and the collector of the transistor 963. The collector electrode of the device 963 also serves as the "0" output to the parity-check circuit 424. This collector electrode is connected to the base of the transistor 964 through a parallel R-C circuit comprising a resistor 974 and a capacitor 975. The "1" output for the device 440 is the connection provided by the coupling capacitor 972. A second "1" output is provided at the collector of the transistor 964, which is connected to the next succeeding stage 450 by a coupling resistor 976 that is connected to the base electrode of a transistor 977.

The base electrode of the transistor 977 that comprises the first stage of the amplifier 450 is connected to the E+ supply through a resistor 978. The emitter of the transistor 977 is grounded and the collector is connected to the C— supply by means of a resistor 979. The output circuit to the next stage comprises a coupling resistor 981 that is connected between the collector of the transistor 977 and the base electrode of a second stage transistor 982. The second stage of the device 450 is completed by a load resistor 983 that is connected from the collector electrode of the transistor 982 to the C— supply. The emitter of this stage is grounded.

The individual circuits incorporated in the arrangement illustrated in FIG. 18 are quite well known; accordingly, only a brief description of their operation is deemed necessary herein. Thus, the first amplifier stage 432 comprising the transistor 951 is a conventional emitter follower that is A.C.-coupled by the capacitor 953 to the second stage 433 comprising the transistor 954. The second stage 433 is equally conventional, and comprises a grounded-emitter stage which, of course, effects a signal inversion with respect to polarity. The output signal from the stage 433 is coupled to the transistor 961 of the amplifier 437. Ordinarily, however, an output signal from the amplifier 433 is not effective to trigger the transistor 961 to conduction because the two diodes 957 and 958 represent low-impedance paths in the input to the base of the transistor. In the presence of suitable signals on both of these diode inputs, however, a signal from the amplifier 433 is effective to render the transistor 961 conductive and produce an output signal pulse that is supplied to the one-shot multi-vibrator 440. It should be noted that the input signal from the timer 416 is of quite short duration compared to the time required for a data mark to move past the sensing photodiode (FIG. 10), so that narrow-angle sampling of the data marks is achieved.

The one-shot multi-vibrator 440 is also of familiar construction and operation. Thus, the biasing arrangement of this circuit is such that the transistor 963 is normally maintained in a conductive condition and the transistor 964 is biased to cut off. An incoming signal from the preceding stage, through the diode 973, drives the transistor 964 conductive. At the same time, the initial transistor 963 is driven to cut off. This changed or "set" condition obtains for a predetermined time interval determined by the impedances of the circuit, and particularly the impedance of the capacitor 967 in relation to the resistor 969. Thereafter, the multi-vibrator 440 automatically resets itself to its original operating condition.

When the transistor 964 is driven conductive, a positive-going signal is developed at the collector electrode and is applied to the base electrode of the initial stage 977 in the amplifier 450. This positive pulse signal is amplified in the two stages of the amplifier 450 and is supplied to the code convertor circuits. The duration of the signal is, of course, determined by the time constant of the multi-vibrator 440.

FIG. 19 illustrates a typical bi-stable flip-flop that may be employed in any one of a number of different individual circuits in the system 400; the particular circuit illustrated is the device 702 from the ring counter 414 of FIG. 13. The flip-flop comprises a pair of transistors 984 and 985 having their collector electrodes returned to the C— supply through the resistors 986 and 987 respectively. The collector electrode of the transistor 984 is connected to the base of the transistor 985 through the parallel R-C circuit 988, 990. A similar parallel R-C circuit 989, 991, connects the collector of the second transistor 985 back to the base of the first transistor. The base electrode of the two devices are individually connected to the H+ supply through the resistors 992 and 993. A diode 994 connected to the base of the first transistor 984 affords the set input circuits for the device, the diode 994 being connected to the "S" terminal through a capacitor 996 and to the "AS" terminal through a resistor 997. A diode 995 is utilized to afford the reset circuit for the device, being directly connected to the reset terminal "R" which is returned to the F— supply through a resistor 998.

FIG. 19 also shows the details of the construction of the AND circuit 695. The first input to the AND circuit 695 comprises the diode 999 that is connected from the "1" terminal of the flip-flop 702, the collector of the transistor 784, to the output terminal 1004, being returned to the C— supply through a resistor 1002. The output circuit for the AND circuit 695 comprises a capacitor 1003 that is coupled from the output terminal 1004 of the AND circuit to the "R" terminal of the flip-flop 702.

The second input for the AND circuit 695 is derived from the "S" terminal of the flip-flop 702, this being the terminal connected back to the device 689 in the ring counter 414 (see FIG. 13). The third input comprises the connection to the terminal 920 from the field error circuit, this connection being made to the diode 1001. The diodes 1000 and 1001 in the second and third inputs for the AND circuit are, of course, connected to the output terminal 1004 in accordance with conventional practice to afford a circuit that produces an output signal only when input signals are applied to all three of the diodes 999-1001.

In normal operation, the initial stable condition of the device 702 is established with the transistor 984 conductive and the transistor 985 non-conductive. This starting condition can be determined by suitable external control, in this instance, such control is achieved in the emitter circuit of the transistor 985 as indicated by the switch illustrated at the "E" terminal of the flip-flop. This switch is opened momentarily to establish the desired starting condition but remains closed during normal operation. A suitable actuating signal applied to either the "AS" or the "S" terminal of the flip-flop drives the transistor 984

to cut off and renders the transistor 985 conductive. This, of course, produces a positive-going pulse signal at the "0" output terminal and results in the "1" terminal being driven negative with respect to its normal operating potential. This condition is maintained until such time as a suitable actuating signal is supplied to the "R" terminal, or until the conductive path for the transistor 985 is broken at the "E" terminal. Under either circumstance, the conduction conditions in the two transistors are again reversed, producing a positive-going output signal at the "1" terminal and a negative-going signal at the "0" terminal. Inasmuch as devices of this kind are quite familiar in the art, no further detailed explanation of circuit operating conditions is considered necessary in this specification.

In order to afford a more complete illustration of the present invention, certain specific circuit data are set forth in detail hereinafter. These data are presented solely by way of illustration and in no sense as a limitation on the invention.

Voltage supplies:

	Volts
C—	—20
D—	—10
E+	+3
F—	—3
G—	—35
H+	+12

Resistors:

	Kilohms
952	15
955	68
956, 434	4.7
962, 969, 983, 1002	10
965, 966, 976, 986, 987	3.9
968, 992, 993	33
971	22
978, 980	6.8
979, 981	2.7
988, 989	12
997	47

Capacitors:

	Microfarads
953	20
435	15
967	0.04
972, 1003	0.001
975, 990, 991	100
996	1470

¹ Micromicrofarads.

Transistors and Diodes

FIGS. 18 and 19; all transistors except device 963 are Type 2N382; transistor 963 is Type 2N414. All diodes are Type GTO-3.

Hence, while preferred embodiments of the invention have been described and illustrated, it is to be understood that they are capable of variation and modification, and I therefore do not wish to be limited to the precise details set forth, but desire to avail myself of such changes and alternations as fall within the purview of the following claims.

I claim:

1. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data printed on said cards in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the printed code data on each of said cards and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to said scan-

ning means, for checking the parity-code signals to develop a parity control signal indicative of the presence of extraneous code marks or the absence of code marks on each of said cards; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage device, coupled to the code translator, for storing the machine code signals; and actuation means, coupled to the storage device and the parity-checking circuit, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station.

2. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data printed on said cards in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the printed code data on each of said cards and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to said scanning means, for checking said parity-code signals to develop a parity control signal indicative of the presence of the exact number of code marks required for each data item in said parity code; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage matrix coupled to the code translator, for storing the machine code signals; means, coupled to said parity checking circuit and to said storage matrix, for preventing recordation of any data item in the storage matrix except in the presence of said parity control signal; and actuation means, coupled to said storage device, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station.

3. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data printed on said cards in accordance with a parity code substantially different from the machine code, each card bearing a predetermined number of parity-coded data items, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the printed code data on each of said cards item-by-item and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to said scanning means, for checking said parity-code signals to develop a parity control signal indicative of the presence of the exact number of code marks required for each data item in said parity code; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; an electrically-actuated storage matrix, coupled to the code translator, for storing the machine code signals including a plurality of groups of stages equal in number to said printed data items; means, comprising a counter having a corresponding plurality of stages individually coupled to respective groups of stages in said storage matrix, and coupled to said parity checking circuit, for conditioning said storage matrix to record machine-coded data only in the presence of said parity control signal; and actuation means, coupled to the storage matrix, for setting said card punch in accordance

with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station.

4. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code substantially different from said data code, for determining the data punched in the record cards, a control system for actuating the punch in response to data in the form of individual items, each including a given number of marks, on said cards in accordance with a parity code substantially different from both the machine code and the punch data code, said control system comprising: means for feeding record cards bearing parity code marks sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the code data marks on each of said cards and for developing parity-code signals representative of the code data marks; an adding circuit, coupled to said scanning means, for adding said parity-code signals together to develop an actuation signal having an amplitude determined by the total number of marks present in each code item; a parity-checking circuit, coupled to said adding circuit, for developing a parity control signal indicative of the presence of said given number of marks in any given data item; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage device, coupled to the code translator, for storing the machine code signals; means, comprising a storage-conditioning circuit coupled to said parity checking circuit and to said storage device, for preventing recordation in said storage device except in the presence of said parity control signal; and actuation means, coupled to the storage device, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station.

5. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data recorded on said cards in the form of data marks and in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding the record cards sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the code data marks on each of said cards and for developing parity-code signals representative of the code data marks; a parity-checking circuit, coupled to said scanning means, for checking said parity-code signals to develop a parity control signal indicative of the presence of extraneous code marks or the absence of code marks one each of said cards; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage matrix comprising a plurality of electrically actuated storage elements, coupled to the code translator, for storing the machine code signals; actuation means, comprising a corresponding plurality of actuating solenoids individually electrically coupled to said storage element, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station; and control means, coupled to said parity-checking circuit, for preventing actuation of the card punch in response to erroneous data marks on said cards.

6. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a

control system for actuating the punch in response to data items in the form of groups of marks, on said cards, arranged in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding said record cards sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the code data marks on each of said cards and for developing parity-code signals representative of the code data marks; parity-checking means coupled to said scanning means, for checking said parity-code signals to develop a parity control signal only in response to sensing of a preselected number of data marks in a given data item, said parity checking means including an output circuit responsive to an applied signal, a pair of one-shot multi-vibrators coupled to said output circuit in bucking relation to each other and having substantially different input signal amplitude threshold levels, and voltage adder means for developing an input signal having an amplitude proportional to the number of marks sensed in a given data item and for applying said input signal to each of said multi-vibrators; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage device, coupled to the code translator, for storing the machine code signals; actuation means, coupled to the storage device, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record card from the scanning station to the punching station; and means, coupled to said parity checking means, for modifying operation of the card punch in response to said parity control signal.

7. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data marks on said cards arranged in discrete items in accordance with a two-of-five parity code that is substantially different from the machine code and the punched data code, said control system comprising: means for feeding record cards bearing code data marks sequentially through a sensing station to a punching station; photoelectric sensing means, located at said sensing station, for sensing the code data marks on each of said cards and for developing parity-code signals representative of the code data items; a parity-checking circuit, coupled to said scanning means, for checking the parity-code signals to develop a parity control signal only in response to parity-code signals, two code marks in each data item on a card; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; storage means, coupled to the code translator, and to the parity checking circuit, for storing the machine code signals only in response to co-incident application thereto of the parity control and machine code signals; actuation means, coupled to the storage device, for setting the card punch in accordance with the machine code signals stored in the storage device upon advancement of a record card from the sensing station to the punching station; and means for actuating the card punch to punch the card in response to sensing of a predetermined number of parity code items each including only two marks.

8. In a card punch for punching data in record cards in accordance with a predetermined data code including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data printed on said cards in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric

scanning means, located at said scanning station, for scanning the printed code data on each of said cards and for developing parity-code signals representative of the printed code data; a voltage adder, coupled to said scanning means, for adding said parity-code signals to develop a parity signal having a given amplitude in response to two parity-code signals but a substantially different amplitude in response to either more or less than two parity code signals; parity-checking means comprising an amplitude sensitive circuit, coupled to said voltage adder developing a parity control signal only in response to a parity signal of said given amplitude; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage device, coupled to the code translator, for storing the machine code signals; and actuation means, coupled to the storage device and the parity-checking circuit, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of a record card from the scanning station to the punching station, said actuation means including means for preventing actuation of the card punch until a preselected number of parity-control signals have been applied thereto.

9. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data to be punched in the record cards, a control system for actuating the punch in response to data items of predetermined number printed on said cards in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the printed code data on each of said cards and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to said scanning means, for checking the parity-code signals to develop a parity control signal indicative of the presence of extraneous code marks or the absence of code marks on each of said cards; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine-code signals; a storage device, coupled to the code translator, for storing the machine code signals; actuation means, coupled to the storage device, for actuating the card punch in accordance with the machine code signals stored in the storage device upon advancement of each record from the scanning station to the punching station; and error circuit means, coupled to said parity-checking circuit and to said actuation means, for preventing punching of the card in response to said parity control signal, and for preventing punching of the card upon occurrence of any deviation from the aforesaid predetermined number of printed data items.

10. In a card punch for punching data in record cards in accordance with a predetermined data code, including means, operable in accordance with a given machine code, for determining the data punched in the record cards, a control system for actuating the punch in response to data items of predetermined number printed on said cards in accordance with a parity code substantially different from the machine code, said control system comprising: means for feeding record cards bearing printed code data sequentially through a scanning station to a punching station; photoelectric scanning means, located at said scanning station, for scanning the printed code data on each of said cards and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to said scanning means, for checking said parity-code signals to develop a parity control signal indicative of any discrepancy from the exact number of code marks required for each data item in said parity

code; a code translator, coupled to said photoelectric scanning means, for translating the parity-code signals into machine code signals; a storage matrix coupled to the code translator, for storing the machine code signals; setting means, coupled to said storage device, for setting the card punch in accordance with the machine code signals stored in the storage device; actuation means for actuating the card punch; means, coupled to said parity checking circuit and to said storage matrix, for preventing punching of any data item in the record card in the presence of said parity control signal; and means for preventing punching of said data in said record card in the event of any discrepancy between the actual number of data items sensed and said predetermined number.

11. In a card punch for punching data in record cards in accordance with a predetermined data code, including means for determining the data to be punched in accordance with a given machine code, a translation and control system for actuating the punch in response to data items of predetermined number pre-printed on the record cards in accordance with a parity-code substantially different from the machine code, said system comprising: scanning means for scanning the printed code data on said cards and for developing parity-code signals representative of the printed code data; a parity-checking circuit, coupled to the scanning means, for developing a parity control signal indicative of any deviation in the parity-code signals from the parity-code; code translator means, coupled to said scanning means, for translating the parity-code signals into machine code signals; storage means, coupled to the code translator means, for storing the machine code signals; means for setting the punch determining means in accordance with data stored in said storage means; means for comparing the actual punch settings with the initial data derived by scanning the printed code data, said comparing means including means for storing the data in predetermined complementary form; actuation means for actuating the card punch; and error circuit means, connected to said parity-checking circuit and to said comparing means, for preventing punching of the record card in response both to the parity control signal and to any indication of erroneous punch setting from the comparing means.

12. In a card punch for punching data in record cards in accordance with a predetermined data code, including means for determining the data to be punched in accordance with a given machine code, a translation and control system for actuating the punch in response to data items of predetermined number pre-printed on the record cards in accordance with a parity-code substantially different from the machine code, said system comprising: scanning means for scanning the printed code data on said cards and for developing parity-code signals representative of the printed code data; code translator means, coupled to said scanning means, for translating the parity-code signals into machine code signals; storage

means, coupled to the code translator, for storing the machine code signals; means for setting the punch determining means in accordance with data stored in said storage means; means for comparing the actual punch settings with the initial data derived by scanning the printed code data, said comparing means including means for storing the data signals in predetermined form, means for sensing the actual punch settings to develop setting signals complementary to said predetermined form, and means for adding the data and setting signals; actuation means for actuating the card punch; and error circuit means, connected to said comparing means, for preventing punching of the record card in response to any indication of erroneous punch setting from the comparing means.

13. In a card punch for punching data in record cards in accordance with a predetermined data code and including groups of detail cards each followed by a summary card, said punch including means for determining the data to be punched in accordance with a given machine code, a translation and control system for actuating the punch in response to data items of predetermined number pre-printed on the record cards in accordance with a parity-code substantially different from the machine code, said system comprising: scanning means for scanning the printed code data on said cards and for developing parity-code signals representative of the printed code data; code translator means, coupled to said scanning means, for translating the parity-code signals into machine code signals; storage means, coupled to the code translator, for storing the machine code signals; means for setting the punch determining means in accordance with data stored in said storage means; means for comparing the actual punch settings with the initial data derived by scanning the printed code data, said comparing means including means for storing the data signals in predetermined complementary form; actuation means for actuating the card punch; accumulator means, coupled to said scanning means, for accumulating data from the detail cards; additional scanning means for sensing the presence of a summary card; means for comparing the data from a summary card with the accumulated data in said accumulator; and error circuit means, connected to said comparing means, for preventing punching of a record card in response to an indication of erroneous punch setting from the comparing means and in response to an indication of a discrepancy between accumulated data in the accumulator and data derived from the summary card.

References Cited in the file of this patent

UNITED STATES PATENTS

Re. 22,394	Moore et al. -----	Nov. 23, 1943
2,841,221	Cunningham -----	July 1, 1958
2,943,787	Cartwright -----	July 5, 1960
2,964,238	King et al. -----	Dec. 13, 1960