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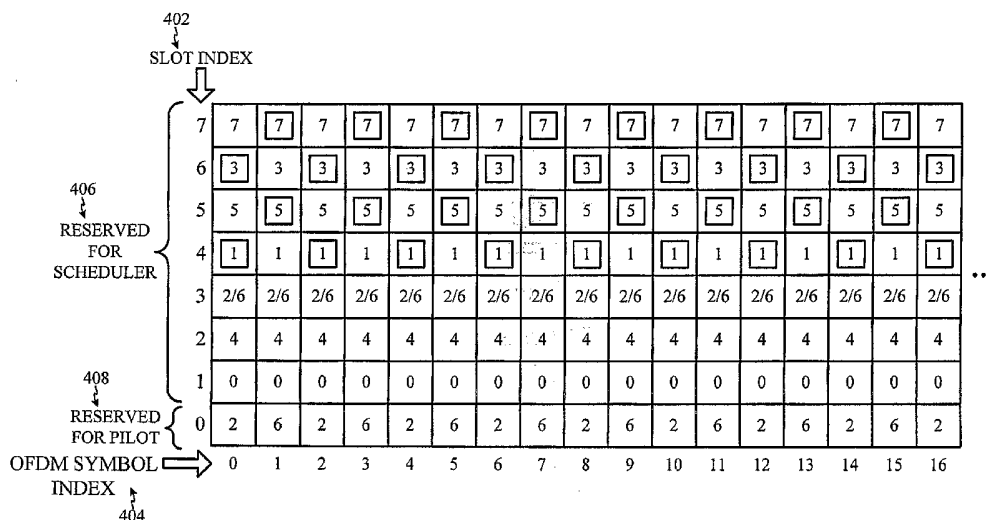
(57) Abstract: A system and method for time diversity uses interleaving. To simplify the operation at both transmitters and receivers, a formula can be used to determine the mapping from slot to interlace at a given OFDM symbol time.

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SYSTEM AND METHOD FOR TIME DIVERSITY

Claim of Priority under 35 U.S.C. §119

[0001] The present Application for Patent claims priority to Provisional Application No. 60/592,999 entitled "METHOD OF CHANNEL INTERLEAVING IN A OFDM WIRELESS COMMUNICATIONS SYSTEM" filed July 29, 2004, and assigned to the assignee hereof and hereby expressly incorporated by reference herein.

BACKGROUND

Field

[0002] The present disclosed embodiments relates generally to wireless communications, and more specifically to channel interleaving in a wireless communications system.

Background

[0003] Orthogonal frequency division multiplexing (OFDM) is a technique for broadcasting high rate digital signals. In OFDM systems, a single high rate data stream is divided into several parallel low rate substreams, with each substream being used to modulate a respective subcarrier frequency. It should be noted that although the present invention is described in terms of quadrature amplitude modulation, it is equally applicable to phase shift keyed modulation systems.

[0004] The modulation technique used in OFDM systems is referred to as quadrature amplitude modulation (QAM), in which both the phase and the amplitude of the carrier frequency are modulated. In QAM modulation, complex QAM symbols are generated from plural data bits, with each symbol including a real number term and an imaginary number term and with each symbol representing the plural data bits from which it was generated. A plurality of QAM bits are transmitted together in a pattern that can be graphically represented by a complex plane. Typically, the pattern is referred to as a "constellation". By using QAM modulation, an OFDM system can improve its efficiency.

[0005] It happens that when a signal is broadcast, it can propagate to a receiver by more than one path. For example, a signal from a single transmitter can propagate along a straight line to a receiver, and it can also be reflected off of physical objects to

2

propagate along a different path to the receiver. Moreover, it happens that when a system uses a so-called "cellular" broadcasting technique to increase spectral efficiency, a signal intended for a received might be broadcast by more than one transmitter. Hence, the same signal will be transmitted to the receiver along more than one path. Such parallel propagation of signals, whether man-made (i.e., caused by broadcasting the same signal from more than one transmitter) or natural (i.e., caused by echoes) is referred to as "multipath". It can be readily appreciated that while cellular digital broadcasting is spectrally efficient, provisions must be made to effectively address multipath considerations.

[0006]   Fortunately, OFDM systems that use QAM modulation are more effective in the presence of multipath conditions (which, as stated above, must arise when cellular broadcasting techniques are used) than are QAM modulation techniques in which only a single carrier frequency is used. More particularly, in single carrier QAM systems, a complex equalizer must be used to equalize channels that have echoes as strong as the primary path, and such equalization is difficult to execute. In contrast, in OFDM systems the need for complex equalizers can be eliminated altogether simply by inserting a guard interval of appropriate length at the beginning of each symbol. Accordingly, OFDM systems that use QAM modulation are preferred when multipath conditions are expected.

[0007]   In a typical trellis coding scheme, the data stream is encoded with a convolutional encoder and then successive bits are combined in a bit group that will become a QAM symbol. Several bits are in a group, with the number of bits per group being defined by an integer "m" (hence, each group is referred to as having an "m-ary" dimension). Typically, the value of "m" is four, five, six, or seven, although it can be more or less.

[0008]   After grouping the bits into multi-bit symbols, the symbols are interleaved. By "interleaving" is meant that the symbol stream is rearranged in sequence, to thereby randomize potential errors caused by channel degradation. To illustrate, suppose five words are to be transmitted. If, during transmission of a non-interleaved signal, a temporary channel disturbance occurs. Under these circumstances, an entire word can be lost before the channel disturbance abates, and it can be difficult if not impossible to know what information had been conveyed by the lost word.

[0009]   In contrast, if the letters of the five words are sequentially rearranged (i.e., "interleaved") prior to transmission and a channel disturbance occurs, several letters

3

might be lost, perhaps one letter per word. Upon decoding the rearranged letters, however, all five words would appear, albeit with several of the words missing letters. It will be readily appreciated that under these circumstances, it would be relatively easy for a digital decoder to recover the data substantially in its entirety. After interleaving the m-ary symbols, the symbols are mapped to complex symbols using QAM principles noted above, multiplexed into their respective sub-carrier channels, and transmitted.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1a shows a channel interleaver in accordance with an embodiment;

[0011] FIG. 1b shows a channel interleaver in accordance with another embodiment;

[0012] FIG. 2a shows code bits of a turbo packet placed into an interleaving buffer in accordance with an embodiment;

[0013] FIG. 2b shows an interleaver buffer arranged into an N/m rows by m columns matrix in accordance with an embodiment;

[0014] FIG. 3 illustrates an interleaved interlace table in accordance with an embodiment;

[0015] FIG. 4 shows a channelization diagram in accordance with an embodiment;

[0016] FIG. 5 shows a channelization diagram with all one's shifting sequence resulting in long runs of good and poor channel estimates for a particular slot, in accordance with an embodiment; and

[0017] FIG. 6 shows a Channelization diagram with all two's shifting sequence resulting in evenly spread good and poor channel estimate interlaces; and

[0018] FIG. 7 shows a wireless device configured to implement interleaving in accordance with an embodiment.

4

DETAILED DESCRIPTION

[0019] In an embodiment, a channel interleaver comprises a bit interleaver and a symbol interleaver. Figure 1 shows two types of channel interleaving schemes. Both schemes use bit interleaving and interlacing to achieve maximum channel diversity.

[0020] Figure 1a shows a channel interleaver in accordance with an embodiment. Figure 1b shows a channel interleaver in accordance with another embodiment. The interleaver of figure 1b uses bit-interleaver solely to achieve m-ary modulation diversity and uses a two-dimension interleaved interlace table and run-time slot-to-interlace mapping to achieve frequency diversity which provides better interleaving performance without the need for explicit symbol interleaving.

[0021] Figure 1a shows Turbo coded bits 102 input into bit interleaving block 104. Bit interleaving block 104 outputs interleaved bits, which are input into constellation symbol mapping block 106. Constellation symbol mapping block 106 outputs constellation symbol mapped bits, which are input into constellation symbol interleaving block 108. Constellation symbol interleaving block 108 outputs constellation symbol interleaved bits into channelization block 110. Channelization block 110 interlaces the constellation symbol interleaved bits using an interlace table 112 and outputs OFDM symbols 114.

[0022] Figure 1b shows Turbo coded bits 152 input into bit interleaving block 154. Bit interleaving block 154 outputs interleaved bits, which are input into constellation symbol mapping block 156. Constellation symbol mapping block 15 outputs constellation symbol mapped bits, which are input into channelization block 158. Channelization block 158 channelizes the constellation symbol interleaved bits using an interleaved interlace table and dynamic slot-interlace mapping 160 and outputs OFDM symbols 162.

5

[0023] Bit Interleaving for modulation diversity

[0024] The interleaver of figure 1b uses bit interleaving 154 to achieve modulation diversity. The code bits 152 of a turbo packet are interleaved in such a pattern that adjacent code bits are mapped into different constellation symbols. For example, for 2m-Ary modulation, the N bit interleaver buffer are divided into N/m blocks. Adjacent code bits are written into adjacent blocks sequentially and then are read out one by one from the beginning of the buffer to the end in the sequential order, as shown in Figure 2a (Top). This guarantees that adjacent code bits be mapped to different constellation symbols. Equivalently, as is illustrated in Figure 2b (Bottom), the interleaver buffer is arranged into an N/m rows by m columns matrix. Code bits are written into the buffer column by column and are read out row by row. To avoid the adjacent code bit to be mapped to the same bit position of the constellation symbol due to the fact that certain bits of a constellation symbol are more reliable than the others for 16QAM depending on the mapping, for example, the first and third bits are more reliable than the second and fourth bits, rows shall be read out from left to right and right to left alternatively.

[0025] Figure 2a shows code bits of a turbo packet 202 placed into an interleaving buffer 204 in accordance with an embodiment. Figure 2b is an illustration of bit interleaving operation in accordance with an embodiment. Code bits of a Turbo packet 250 are placed into an interleaving buffer 252 as shown in figure 2b. The interleaving buffer 252 is transformed by swapping the second and third columns, thereby creating interleaving buffer 254, wherein m=4, in accordance with an embodiment. Interleaved code bits of a Turbo packet 256 are read from the interleaving buffer 254.

[0026] For simplicity, a fixed m=4 may be used, if the highest modulation level is 16 and if code bit length is always divisible by 4. In this case, to improve the separation for QPSK, the middle two columns are swapped before being read out. This procedure is depicted in Figure 2b (Bottom). It would be apparent to those skilled in the art that any two columns may be swapped. It would also be apparent to those skilled in the art that the columns may be placed in any order. It would also be apparent to those skilled in the art that the rows may be placed in any order.

[0027] In another embodiment, as a first step, the code bits of a turbo packet 202 are distributed into groups. Note that the embodiments of both figure 2a and figure 2b also distribute the code bits into groups. However, rather than simply swapping rows or columns, the code bits within each group are shuffled according to a group bit order for

6

each given group. Thus, the order of four groups of 16 code bits after being distributed into groups may be {1, 5, 9, 13} {2, 6, 10, 14} {3, 7, 11, 15} {4, 8, 12, 16} using a simple linear ordering of the groups and the order of the four groups of 16 code bits after shuffling may be {13, 9, 5, 1} {2, 10, 6, 14} {11, 7, 15, 3} {12, 8, 4, 16}. Note that swapping rows or columns would be a regressive case of this intra-group shuffling.

[0028] **Interleaved Interlace for frequency diversity**

[0029] In accordance with an embodiment, the channel interleaver uses interleaved interlace for constellation symbol interleaving to achieve frequency diversity. This eliminates the need for explicit constellation symbol interleaving. The interleaving is performed at two levels:

[0030] · Within or Intra Interlace Interleaving: In an embodiment, 500 subcarriers of an interlace are interleaved in a bit-reversal fashion.

[0031] · Between or Inter Interlace Interleaving: In an embodiment, eight interlaces are interleaved in a bit-reversal fashion.

[0032] It would be apparent to those skilled in the art that the number of subcarriers can be other than 500. It would also be apparent to those skilled in the art that the number of interlaces can be other than eight.

[0033] Note that since 500 is not power of 2, a reduced-set bit reversal operation shall be used in accordance with an embodiment. The following code shows the operation:

[0034]	`vector<int> reducedSetBitRev(int n)`
[0035]	`{`
[0036]	`int m=exponent(n);`
[0037]	`vector<int> y(n);`
[0038]	`for (int i=0, j=0; i<n; i++,j++)`
[0039]	`{`
[0040]	`int k;`
[0041]	`for (; (k=bitRev(j,m))>=n; j++);`
[0042]	`y[i]=k;`
[0043]	`}`
[0044]	`return y;`

[0045]   }

[0046] where n=500, m is the smallest integer such that $2^m > n$ which is 8, and bitRev is the regular bit reversal operation.

[0047] The symbols of the constellation symbol sequence of a data channel is mapped into the corresponding subcarriers in a sequential linear fashion according to the assigned slot index, determined by a Channelizer, using the interlace table as is depicted in Figure 3, in accordance with an embodiment.

[0048] Figure 3 illustrates an interleaved interlace table in accordance with an embodiment. Turbo packet 302, constellation symbols 304, and interleaved interlace table 306 are shown. Also shown are interlace 3 (308), interlace 4 (310), interlace 2 (312), interlace 6 (314), interlace 1 (316), interlace 5 (318), interlace 3 (320), and interlace 7 (322).

[0049] In an embodiment, one out of the eight interlaces is used for pilot, i.e., Interlace 2 and Interlace 6 is used alternatively for pilot. As a result, the Channelizer can use seven interlaces for scheduling. For convenience, the Channelizer uses *Slot* as a scheduling unit. A slot is defined as one interlace of an OFDM symbol. An *Interlace Table* is used to map a slot to a particular interlace. Since eight interlaces are used, there are then eight slots. Seven slots will be set aside for use for Channelization and one slot for Pilot. Without loss of generality, Slot 0 is used for the Pilot and Slots 1 to 7 are used for Channelization, as is shown in Figure 4 where the vertical axis is the slot index 402, the horizontal axis is the OFDM symbol index 404 and the bold-faced entry is the interlace index assigned to the corresponding slot at an OFDM symbol time.

[0050] Figure 4 shows a channelization diagram in accordance with an embodiment. Figure 4 shows the slot indices reserved for the scheduler 406 and the slot index reserved for the Pilot 408. The bold faced entries are interlace index numbers. The number with square is the interlace adjacent to pilot and consequently with good channel estimate.

[0051] The number surrounded with a square is the interlace adjacent to the pilot and consequently with good channel estimate. Since the Scheduler always assigns a chunk of contiguous slots and OFDM symbols to a data channel, it is clear that due to the inter-interlace interleaving, the contiguous slots that are assigned to a data channel will

8

be mapped to discontinuous interlaces. More frequency diversity gain can then be achieved.

[0052] However, this static assignment (i.e., the slot to physical interlace mapping table1 does not change over time) does suffer one problem. That is, if a data channel assignment block (assuming rectangular) occupies multiple OFDM symbols, the interlaces assigned to the data channel does not change over the time, resulting in loss of frequency diversity. The remedy is simply cyclically shifting the Scheduler interlace table (i.e., excluding the Pilot interlace) from OFDM symbol to OFDM symbol.

[0053] Figure 5 depicts the operation of shifting the Scheduler interlace table once per OFDM symbol. This scheme successfully destroys the static interlace assignment problem, i.e., a particular slot is mapped to different interlaces at different OFDM symbol time.

[0054] Figure 5 shows a channelization diagram with all one's shifting sequence resulting in long runs of good and poor channel estimates for a particular slot 502, in accordance with an embodiment. Figure 5 shows the slot indices reserved for the scheduler 506 and the slot index reserved for the Pilot 508. Slot symbol index 504 is shown on the horizontal axis.

[0055] However, it is noticed that slots are assigned four continuous interlaces with good channel estimates followed by long runs of interlaces with poor channel estimates in contrast to the preferred patterns of short runs of good channel estimate interlaces and short runs of interlaces with poor channel estimates. In the figure, the interlace that is adjacent to the pilot interlace is marked with a square. A solution to the long runs of good and poor channel estimates problem is to use a shifting sequence other than the all one's sequence. There are many sequences can be used to fulfill this task. The simplest sequence is the all two's sequence, i.e., the Scheduler interlace table is shifted twice instead of once per OFDM symbol. The result is shown in Figure 6 which significantly improves the Channelizer interlace pattern. Note that this pattern repeats every $2 \times 7 = 14$ OFDM symbols, where 2 is the Pilot interlace staggering period and 7 is the Channelizer interlace shifting period.

[0056] To simplify the operation at both transmitters and receivers, a simple formula can be used to determine the mapping from slot to interlace at a given OFDM symbol time

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1 The Scheduler slot table does not include the Pilot slot.

[0057] $i = \Re'\{(N - ((R \times t)\%N) + s - 1)\%N\}$

where

[0058] · $N = I - 1$ is the number of interlaces used for traffic data scheduling, where I is the total number of interlaces;

[0059] · $i \in \{0, 1, \cdots, I - 1\}$, excluding the pilot interlace, is the interlace index that Slot s at OFDM symbol t maps to;

[0060] · $t = 0, 1, \cdots, T - 1$ is the OFDM symbol index in a super frame, where T is the total number of OFDM symbols in a frame2;

[0061] · $s = 1, 2, \cdots, S - 1$ s is the slot index where S is the total number of slots;

[0062] · R is the number of shifts per OFDM symbol;

[0063] · $\Re'$ is the reduced-set bit-reversal operator. That is, the interlace used by the Pilot shall be excluded from the bit-reversal operation.

[0064] Example: In an embodiment, I=8, R=2. The corresponding Slot-Interlace mapping formula becomes

[0065] $i = \Re'\{(7 - ((2 \times t)\%7) + s - 1)\%7\}$

[0066] where $\Re'$ corresponds to the following table:

$$x \Rightarrow \Re'\{x\}$$
$$0 \Rightarrow 0$$
$$1 \Rightarrow 4$$
$$2 \Rightarrow 2 \text{ or } 6$$
$$3 \Rightarrow 1$$
$$4 \Rightarrow 5$$
$$5 \Rightarrow 3$$

[0067] $6 \Rightarrow 7$

[0068] This table can be generated by the following code:

[0069] int reducedSetBitRev(int x, int exclude, int n)

[0070] {

[0071]   int m=exponent(n);

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2 OFDM symbol index in a superframe instead of in a frame gives additional diversity to frames since the number of OFDM symbols in a frame in the current design is not divisible by 14.

[0072]   int y;

[0073]   for (int i=0; j=0; i<=x; i++, j++)

[0074]   {

[0075]   for (; (y=bitRev(j, m))==exclude; j++);

[0076]   }

[0077]   return y;

[0078]   }

[0079] where m=3 and bitRev is the regular bit reversal operation.

[0080] For OFDM symbol t=11, Pilot uses Interlace 6. The mapping between Slot and Interlace becomes:

[0081] · Slot 1 maps to interlace of $\Re'\{(7-(2\times11)\%7+1-1)\%7\}=\Re\{6\}=7$;

[0082] ·Slot 2 maps to interlace of $\Re'\{(7-(2\times11)\%7+2-1)\%7\}=\Re\{0\}=0$;

[0083] ·Slot 3 maps to interlace of $\Re'\{(7-(2\times11)\%7+3-1)\%7\}=\Re\{1\}=4$;

[0084] ·Slot 4 maps to interlace of $\Re'\{(7-(2\times11)\%7+4-1)\%7\}=\Re\{2\}=2$;

[0085] ·Slot 5 maps to interlace of $\Re'\{(7-(2\times11)\%7+5-1)\%7\}=\Re\{3\}=1$;

[0086] ·Slot 6 maps to interlace of $\Re'\{(7-(2\times11)\%7+6-1)\%7\}=\Re\{4\}=5$;

[0087] ·Slot 7 maps to interlace of $\Re'\{(7-(2\times11)\%7+7-1)\%7\}=\Re\{5\}=3$.

[0088] The resulting mapping agrees with the mapping in Figure 6. Figure 6 shows a Channelization diagram with all two's shifting sequence resulting in evenly spread good and poor channel estimate interlaces.

[0089] In accordance with an embodiment, an interleaver has the following features:

[0090] The bit interleaver is designed to taking advantage of m-Ary modulation diversity by interleaving the code bits into different modulation symbols;

[0091] The "symbol interleaving" designed to achieve frequency diversity by INTRA-interlace interleaving and INTER-interlace interleaving;

[0092] Additional frequency diversity gain and channel estimation gain are achieved by changing the slot-interlace mapping table from OFDM symbol to OFDM symbol. A simple rotation sequence is proposed to achieve this goal.

[0093] Figure 7 shows a wireless device configured to implement interleaving in accordance with an embodiment. Wireless device 702 comprises an antenna 704, duplexer 706, a receiver 708, a transmitter 710, processor 712, and memory 714. Processor 712 is capable of performing interleaving in accordance with an embodiment. The processor 712 uses memory 714 for buffers or data structures to perform its operations.

[0094] The attached chapter describes details of further embodiments.

[0095] Those of skill in the art would understand that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0096] Those of skill would further appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the embodiments disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

[0097] The various illustrative logical blocks, modules, and circuits described in connection with the embodiments disclosed herein may be implemented or performed with a general purpose processor, a digital signal processor (DSP), an application specific integrated circuit (ASIC), a field programmable gate array (FPGA) or other programmable logic device, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform the functions described herein. A general purpose processor may be a microprocessor, but in the alternative, the processor may be any conventional processor, controller, microcontroller, or state machine. A processor may also be implemented as a combination of computing devices, e.g., a combination of a DSP and a microprocessor, a plurality of

12

microprocessors, one or more microprocessors in conjunction with a DSP core, or any other such configuration.

[0098] The steps of a method or algorithm described in connection with the embodiments disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor. The processor and the storage medium may reside in an ASIC. The ASIC may reside in a user terminal. In the alternative, the processor and the storage medium may reside as discrete components in a user terminal.

[0099] The previous description of the disclosed embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other embodiments without departing from the spirit or scope of the invention. Thus, the present invention is not intended to be limited to the embodiments shown herein but is to be accorded the widest scope consistent with the principles and novel features disclosed herein.

1   **5 PHYSICAL LAYER**

2   This section includes the specification of the FLO Physical layer.

3   **5.1 Physical Layer Packets**

4   5.1.1 Overview

5   The transmission unit of the Physical layer is a Physical layer packet. A Physical layer
6   packet has a length of 1000 bits. A Physical layer packet carries one MAC layer packet.

7   5.1.2 Physical Layer Packet Format

8   The Physical layer packet shall use the following format:

9

Field	Length (bits)
MAC Layer Packet	976
FCS	16
Reserved	2
TAIL	6

10   MAC Layer Packet   - MAC layer packet from the OIS, Data or
11   Control Channel MAC protocol

12   FCS   - Frame check sequence (see 5.1.4)

13   Reserved   - The FLO network shall set this field to
14   zero. The FLO device shall ignore this field.

15   TAIL   - Encoder tail bits. This field shall be set to
16   all '0's.

17   Figure 5.1.2-1 illustrates the format of the Physical layer packet.
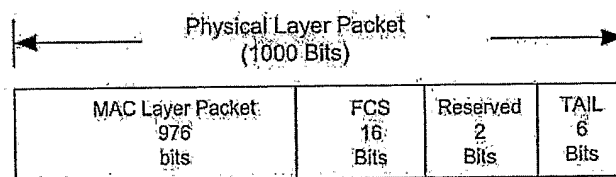
Figure 5.1.2-1 Physical Layer Packet Format

20   5.1.3 Bit Transmission Order

21   Each field of the Physical layer packet shall be transmitted in sequence such that the most
22   significant bit (MSB) is transmitted first and the least significant bit (LSB) is transmitted
23   last. The MSB is the left-most bit in the figures of the document.

5.1.4 Computation of the FCS Bits

The FCS computation described here shall be used for computing the FCS field in the Physical layer packet.

The FCS shall be a CRC calculated using the standard CRC-CCITT generator polynomial:

$$g(x) = x^{16} + x^{12} + x^5 + 1.$$

The FCS shall be equal to the value computed according to the following procedure as shown in Figure 5.1.4-1:

- All shift-register elements shall be initialized to '1's[19].

- The switches shall be set in the up position.

- The register shall be clocked once for each bit of the physical layer packet except for the FCS, Reserved and TAIL bits. The physical layer packet shall be read from the MSB to LSB.

- The switches shall be set in the down position so that the output is a modulo-2 addition with a '0' and the successive shift-register inputs are '0's.

- The register shall be clocked an additional 16 times for the 16 FCS bits.

- The output bits constitute all fields of the Physical layer packets except the Reserved and TAIL fields.
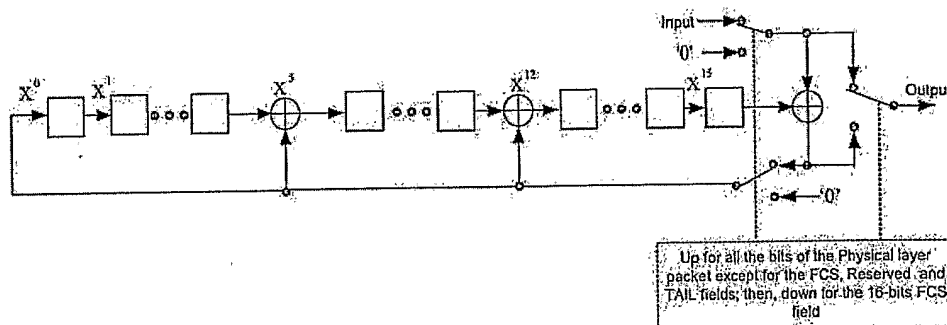
Figure 5.1.4-1 FCS Computation for the Physical Layer Packet

5.2 FLO Network Requirements

This section defines requirements specific to the FLO network equipment and operation.

5.2.1 Transmitter

The following requirements shall apply to the FLO network transmitter.

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[19] Initialization of the register to ones causes the CRC for all-zero data to be non-zero.

1   5.2.1.1 Frequency Parameters

2   5.2.1.1.1 Transmit Frequency

3   The transmitter shall operate in one of eight 6 MHz wide bands[20]. Each 6 MHz wide
4   transmit band allocation is called a FLO RF Channel. Each FLO RF Channel shall be
5   denoted by an index $j \in \{1,2,..8\}$. The transmit band and the band center frequency for
6   each FLO RF channel index shall be as specified in Table 5.2.1.1.1-1.

7   Table 5.2.1.1.1-1 FLO RF Channel Number and the Transmit Band Frequencies

FLO RF Channel Number j	FLO Transmit Band (MHz)	Band Center Frequency fc (MHz)
1	698 - 704	701
2	704 - 710	707
3	710 - 716	713
4	716 - 722	719
5	722 - 728	725
6	728 - 734	731
7	734 - 740	737
8	740 - 746	743

8   5.2.1.1.2 Frequency Tolerance

9   The maximum frequency difference between the actual transmit carrier frequency and the
10   specified transmit frequency shall be less than $\pm 2 \times 10^{-9}$ of the band center frequency in
11   Table 5.2.1.1.1-1.

12   5.2.1.1.3 In Band Spectral Characteristics

13   TBD.

14   5.2.1.1.4 Out of Band Spectrum Mask

15   TBD.

16   5.2.1.1.5 Power Output Characteristics

17   The transmit ERP shall be less than 46.98 dBW[21] (see [3]).

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20 The FLO system also supports transmit bandwidths of 5, 7, and 8 MHz (see 6.1).

21 This corresponds to 50 kW.

1   5.2.1.2   OFDM Modulation Characteristics

2   5.2.1.2.1 Overview

3   The modulation used on the air-link is Orthogonal Frequency Division Multiplexing
4   (OFDM). The smallest transmission interval corresponds to one OFDM symbol period. The
5   OFDM transmit symbol is comprised of many separately modulated sub-carriers.

6   5.2.1.2.2 Sub-carriers

7   The FLO system shall use 4096 sub-carriers, numbered 0 through 4095.

8   5.2.1.2.2.1 Sub-carrier Groups

9   These sub-carriers are divided into two separate groups as follows:

10   5.2.1.2.2.1.1 Guard Sub-carriers

11   Of the available 4096 sub-carriers, 96 shall be unused. These unused sub-carriers are
12   called guard sub-carriers. No energy shall be transmitted on the guard sub-carriers.

13   Sub-carriers numbered 0 through 47, 2048, and 4049 through 4095 shall be used as
14   guard sub-carriers.

15   5.2.1.2.2.1.2 Active Sub-carriers

16   The active sub-carriers shall be a group of 4000 sub-carriers with indices
17   $k \in \{48..2047, 2049..4048\}$.

18   Each active sub-carrier shall carry a modulation symbol.

19   5.2.1.2.2.2 Sub-carrier Spacing

20   In the FLO system, the 4096 sub-carriers shall span a bandwidth of 5.55 MHz at the center
21   of the 6 MHz FLO RF Channel. The sub-carrier spacing, $(\Delta f)_{SC}$ shall be given by:

22   $$(\Delta f)_{SC} = \frac{5.55 \times 10^6}{4096} = 1.35498046875 \text{ kHz}$$

23   5.2.1.2.2.3 Sub-carrier Frequency

24   The frequency of the sub-carrier with index i in the kth FLO RF Channel (see Table
25   5.2.1.1.1-1), $f_{SC}(k,i)$, shall be computed as per the following equation:

26   $$f_{SC}(k,i) = f_C(k) + (i - 2048) \times (\Delta f)_{SC}$$

27   where

28   $f_C(k)$ is the center frequency for the kth FLO RF Channel,

29   $(\Delta f)_{SC}$ is the sub-carrier spacing.

1 5.2.1.2.2.4 Sub-carrier Interlaces

2 The active sub-carriers shall be sub-divided into 8 interlaces indexed from 0 through 7.
3 Each interlace shall consist of 500 sub-carriers. The sub-carriers in an interlace shall be
4 spaced $[8 \times (\Delta f)_{SC}]$ Hz apart[22] in frequency, with $(\Delta f)_{SC}$ being the sub-carrier spacing.

5 The sub-carriers in each interlace shall span 5.55 MHz of the FLO RF Channel bandwidth.
6 An active sub-carrier with index i shall be allocated to interlace I_j, where $j = i \bmod 8$. The
7 sub-carrier indices in each interlace shall be arranged sequentially in ascending order. The
8 numbering of sub-carriers in an interlace shall be in the range $0, 1, \ldots 499$.

9 5.2.1.2.3 Frame and Channel Structure

10 The transmitted signal is organized into superframes. Each superframe shall have duration
11 T_{SF} equal to 1s, and shall consist of 1200 OFDM symbols. The OFDM symbols in a
12 superframe shall be numbered 0 through 1199. The OFDM symbol interval T_s shall be
13 $833.33\ldots \mu s$. The OFDM symbol consists of a number of time-domain baseband samples,
14 called OFDM chips. These chips shall be transmitted at a rate of 5.55×10^6 per second.

15 The total OFDM symbol interval T_s' is comprised of four parts: a useful part with duration
16 T_U, a flat guard interval with duration T_{FGI} and two windowed intervals of duration T_{WGI}
17 on the two sides, as illustrated in Figure 5.2.1.2.3-1. There shall be an overlap of T_{WGI}
18 between consecutive OFDM symbols (see Figure 5.2.1.2.11.3-1).

19 The effective OFDM symbol interval shall be $T_s = T_{WGI} + T_{FGI} + T_U$,

20 where $\begin{cases} T_U = 4096 \text{ chips} = \dfrac{4096}{5.55 \times 10^6} = 738.018018\ldots \mu s \\[2mm] T_{FGI} = 512 \text{ chips} = \dfrac{512}{5.55 \times 10^6} = 92.252252\ldots \mu s \\[2mm] T_{WGI} = 17 \text{ chips} = \dfrac{17}{5.55 \times 10^6} = 3.063063\ldots \mu s \end{cases}$

---

22 With the exception of interlace zero, where two sub-carriers in the middle of this interlace are
separated by $16 \times (\Delta f)_{SC}$, since the sub-carrier with index 2048 is not used.
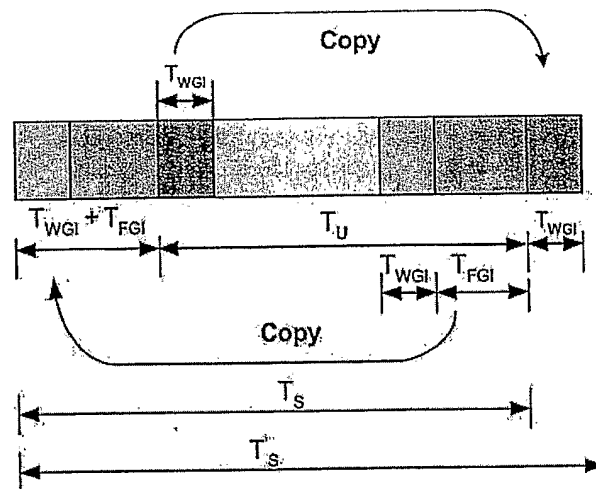
Figure 5.2.1.2.3-1 OFDM Symbol Duration

The total symbol duration shall be $T_s' = T_s + T_{WGI}$.

The effective OFDM symbol duration shall henceforth be referred to as the OFDM symbol interval. During an OFDM symbol interval, a modulation symbol shall be carried on each of the active sub-carriers.

The FLO Physical layer channels (see Figure 1.5-1) are the TDM Pilot Channel, the FDM Pilot Channel, the OIS Channel, and the Data Channel. The TDM Pilot Channel, the OIS Channel, and the Data Channel shall be time division multiplexed over a superframe. The FDM Pilot Channel shall be frequency division multiplexed with the OIS Channel and the Data Channel over a superframe as illustrated in Figure 5.2.1.2.3-2.

The TDM Pilot Channel is comprised of the TDM Pilot 1 Channel, the Wide-area Identification Channel (WIC), the Local-area Identification Channel (LIC), the TDM Pilot 2 Channel, the Transition Pilot Channel (TPC) and the Positioning Pilot Channel (PPC). The TDM Pilot 1 Channel, the WIC, the LIC and the TDM Pilot 2 Channel, shall each span one OFDM symbol and appear at the beginning of a superframe. A Transition Pilot Channel (TPC) spanning one OFDM symbol shall precede and follow each Wide-area and Local-area Data or OIS Channel transmission. The TPC flanking the Wide-area Channel (Wide-area OIS or Wide-area Data) is called the Wide-area Transition Pilot Channel (WTPC). The TPC flanking the Local-area channel (Local-area OIS or Local-area Data Channel) transmission is called the Local-area Transition Pilot Channel (LTPC). The WTPC and the LTPC shall each occupy 10 OFDM symbols and together occupy 20 OFDM symbols in a superframe. The PPC shall have variable duration and its status (presence or absence and duration) shall be signaled over the OIS Channel. When present, it shall span 6, 10 or 14 OFDM symbols at the end of the superframe. When PPC is absent, two OFDM symbols shall be reserved at the end of the superframe.

The OIS Channel shall occupy 10 OFDM symbols in a superframe and shall immediately follow the first WTPC OFDM symbol in a superframe. The OIS Channel is comprised of the Wide-area OIS Channel and the Local-area OIS Channel. The Wide-area OIS Channel and

1   the Local-area OIS Channel shall each have duration of 5 OFDM symbols and shall be
2   separated by two TPC OFDM symbols.

3   The FDM Pilot Channel shall span 1174, 1170, 1166 or 1162 OFDM[23] symbols in a
4   superframe. The FDM Pilot channel is frequency division multiplexed with Wide-area and
5   Local-area OIS and Data Channels.

6   The Data Channel shall span 1164, 1160, 1156 or 1152 OFDM[24] symbols. The Data
7   Channel transmission plus the 16 TPC OFDM symbol transmissions immediately preceding
8   or following each data channel transmission are divided into 4 frames.

9   Let

10 P be the number of OFDM symbols in the PPC or the number of Reserved OFDM
11 symbols in the case where the PPC is absent in a superframe.

12 W be the number of OFDM symbols associated with the Wide-area Data Channel in a
13 frame.

14 L be the number of OFDM symbols associated with the Local-area Data Channel in a
15 frame.

16 F be the number of OFDM symbols in a frame.

17 Then these frame parameters shall be related by the following set of equations:

$$F = 295 - \frac{P-2}{4}$$

18

$$F = W + L + 4$$

19 Figure 5.2.1.2.3-2 illustrates the superframe and the channel structure in terms of P, W
20 and L.

---

[23] These values correspond to either 2 Reserved OFDM symbols or 6, 10 and 14 PPC OFDM symbols, respectively, being present in each superframe.

[24] These values correspond to either 2 Reserved OFDM symbols or 6, 10 and 14 PPC OFDM symbols, respectively, being present in each superframe.
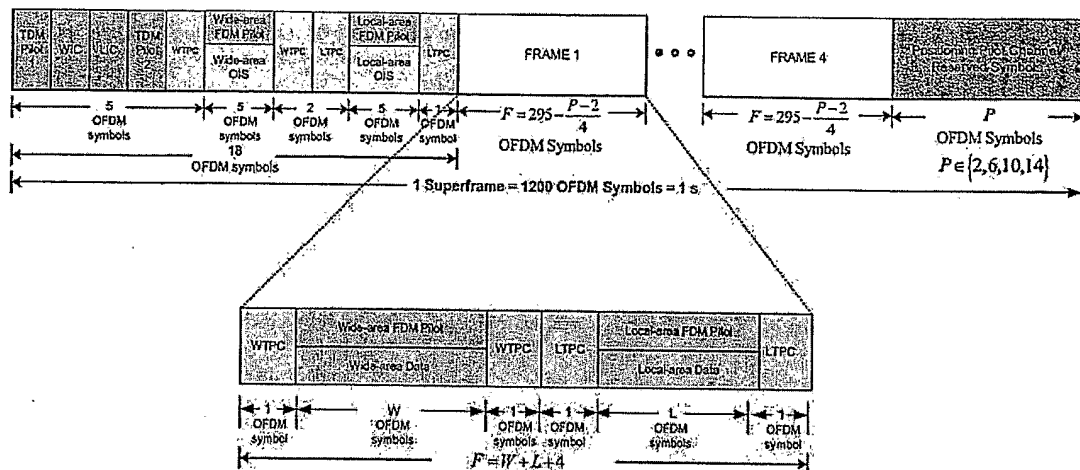
Figure 5.2.1.2.3-2 FLO SuperFrame and Channel Structure

When the PPC is absent, each frame shall span 295 OFDM symbols and have duration T_F equal to 245.8333... ms (see Figure 5.2.1.2.3-2); note there are two Reserved OFDM symbols at the end of each superframe. When the PPC is present at the end of the superframe, each frame shall span a variable number of OFDM symbols as specified in Table 5.2.1.2.3-1.

Table 5.2.1.2.3-1 Frame Duration for Different Number of PPC OFDM Symbols

Number of PPC OFDM Symbols	Frame Duration (F) in units of OFDM symbols	Frame Duration in ms
6	294	245
10	293	244.166...
14	292	243.333...

The Data Channel during each frame shall be time division multiplexed between the Local-area Data Channel and the Wide-area Data Channel. The fraction of the frame allocated to Wide-area Data is $\frac{W}{W+L} \times 100\%$ and may vary from 0 to 100%.

The Physical layer packets transmitted over the OIS Channel are called OIS packets and the Physical layer packets transmitted over the Data Channel are called Data packets.

5.2.1.2.4 Flow Components and Layered Modulation

The audio or video content associated with a flow multicast over the FLO network may be sent in two components, i.e. a base (B) component that enjoys widespread reception and an enhancement (E) component that improves upon the audio-visual experience provided by the base component over a more limited coverage area.

The base and the enhancement component Physical layer packets are jointly mapped to modulation symbols. This FLO feature is known as layered modulation.

1   5.2.1.2.5 MediaFLO Logical Channel

2   The Data packets transmitted by the Physical layer are associated with one or more virtual

3   channels called MediaFLO Logical Channels (MLC). An MLC is a decodable component of a

4   FLO service that is of independent reception interest to a FLO device. A service may be sent

5   over multiple MLCs. However, the base and enhancement component of an audio or video

6   flow associated with a service shall be transmitted over a single MLC.

7   5.2.1.2.6 FLO Transmit Modes

8   The combination of modulation type and the inner code rate is called the "transmit mode".

9   The FLO system shall support the twelve transmit modes listed in Table 5.2.1.2.6-1.

10   In the FLO network, the transmit mode is fixed when an MLC is instantiated and is

11   changed infrequently. This restriction is imposed in order to maintain a constant coverage

12   area for each MLC.

13

Table 5.2.1.2.6-1 FLO Transmit Modes

Mode Number	Modulation (see 5.2.1.2.9.6.1.6.1, 5.2.1.2.9.6.1.6.2, 5.2.1.2.9.7.1.6.3)	Turbo Code Rate (see 5.2.1.2.9.6.1.1 & 5.2.1.2.9.2.1)
0	QPSK	1/3
1	QPSK	1/2
2	16-QAM	1/3
3	16-QAM	1/2
4	16-QAM	2/3
5[25]	QPSK	1/5
6	Layered Modulation with energy ratio 4	1/3
7	Layered Modulation with energy ratio 4	1/2
8	Layered Modulation with energy ratio 4	2/3
9	Layered Modulation with energy ratio 6.25	1/3
10	Layered Modulation with energy ratio 6.25	1/2
11	Layered Modulation with energy ratio 6.25	2/3

14   5.2.1.2.7 FLO Slots

15   In the FLO network, the smallest unit of bandwidth allocated to a MLC over an OFDM

16   symbol corresponds to a group of 500 modulation symbols. This group of 500 modulation

17   symbols is called a slot. The scheduler function (in the MAC layer) allocates slots to MLCs

---

[25] This mode is used for the OIS channel only.

22

1   during the data portion of the superframe. When the scheduler function allocates
2   bandwidth for transmission to a MLC in an OFDM symbol, it does so in integer units of
3   slots.

4   There are 8 slots during every OFDM symbol[26]. These slots shall be numbered 0 through 7.
5   The WIC and LIC channels shall each occupy 1 slot. The TDM Pilot 2 Channel shall occupy
6   4 slots. The TPC (Wide-area and Local-area) shall occupy all 8 slots. The FDM Pilot Channel
7   shall occupy 1 slot with index 0 and the OIS/Data Channel may occupy up to 7 slots with
8   indices 1 through 7. Each slot shall be transmitted over an interlace. The mapping from
9   slot to interlace varies from OFDM symbol to OFDM symbol and is described in 5.2.1.2.10.

10   5.2.1.2.8 FLO Data Rates

11   In the FLO system the calculation of data rates is complicated by the fact that different
12   MLCs may utilize different modes. The computation of data rates is simplified by assuming
13   that all MLCs use the same transmit mode. Table 5.2.1.2.8-1 gives the Physical layer data
14   rates for the different transmit modes assuming all 7 data slots are used.

15   Table 5.2.1.2.8-1 FLO Transmit Modes and Physical Layer Data Rates

Transmit Mode	Slots per Physical Layer Packet	Physical Layer Data Rate[27] (Mbps)
0	3	2.8
1	2	4.2
2	3/2	5.6
3	1	8.4
4	3/4	11.2
5	5	1.68
6	3	5.6
7	2	8.4
8	3/2	11.2
9	3	5.6
10	2	8.4
11	3/2	11.2

---

[26] Except for the TDM Pilot 1 Channel in a superframe.

[27] The overhead due to the TDM Pilot channel and the outer code is not subtracted. This is the rate at which data is transmitted during the Data channel. For modes 6 through 11, the rate quoted is the combined rate of the two components. The rate for each component will be half of this value.

1   5.2.1.2.9 FLO Physical Layer Channels

2   The FLO Physical layer is comprised of the following sub-channels:

3   • The TDM Pilot Channel.

4   • The Wide-area OIS Channel.

5   • The Local-area OIS Channel.

6   • The Wide-area FDM Pilot Channel.

7   • The Local-area FDM Pilot Channel.

8   • The Wide-area Data Channel.

9   • The Local-area Data Channel.

10   5.2.1.2.9.1 TDM Pilot Channel

11   The TDM Pilot Channel is comprised of the following component channels.

12   5.2.1.2.9.1.1 TDM Pilot 1 Channel

13   The TDM Pilot 1 Channel shall span one OFDM symbol. It shall be transmitted at the
14   OFDM symbol index 0 in the superframe. It signals the start of a new superframe. It may be
15   used by the FLO device for determining the coarse OFDM symbol timing, the superframe
16   boundary and the carrier frequency offset.

17   The TDM Pilot 1 waveform shall be generated in the transmitter using the steps illustrated
18   in Figure 5.2.1.2.9.1.1-1.
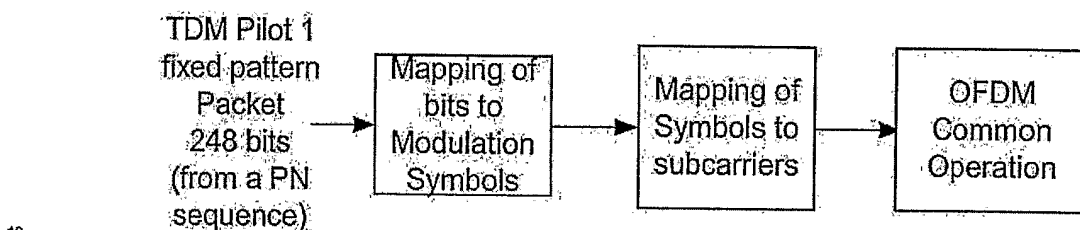
19

20   **Figure 5.2.1.2.9.1.1-1 TDM Pilot 1 Packet Processing in the Transmitter**

21   5.2.1.2.9.1.1.1 TDM Pilot 1 Sub-carriers

22   The TDM Pilot 1 OFDM symbol shall be comprised of 124 non-zero sub-carriers in the
23   frequency domain, which are uniformly spaced among the Active sub-carriers (see
24   5.2.1.2.2.1.2). The ith TDM Pilot 1 sub-carrier shall correspond to the sub-carrier index j
25   defined as follows:

26
$$j = \begin{cases} 64 + (i) \times 32, \forall\ i \in \{0,1..61\} \\ 64 + (i+1) \times 32, \forall\ i \in \{62,...123\}. \end{cases}$$

27   Note that the TDM Pilot 1 Channel does not use the sub-carrier with index 2048.

5.2.1.2.9.1.1.2 TDM Pilot 1 Fixed Information Pattern

The TDM Pilot 1 sub-carriers shall be modulated with a fixed information pattern. This pattern shall be generated using a 20-tap linear feedback shift register (LFSR) with generator sequence $h(D) = D^{20}+D^{17}+1$ and initial state '11110000100000000000'. Each output bit shall be obtained as follows: if the LFSR state is the vector $[s_{20}s_{19}s_{18}s_{17}s_{16}s_{15}s_{14}s_{13}s_{12}s_{11}s_{10}s_9s_8s_7s_6s_5s_4s_3s_2s_1]$ then, the output bit shall be $[s_{19} \oplus s_4]$, where $\oplus$ denotes modulo-2 addition[28]. The LFSR structure shall be as specified in Figure 5.2.1.2.9.1.1.2-1.

The fixed information pattern shall correspond to the first 248 output bits. The first 35-bits of the fixed pattern shall be '11010100100110110111001100101100001', with '110' appearing first.
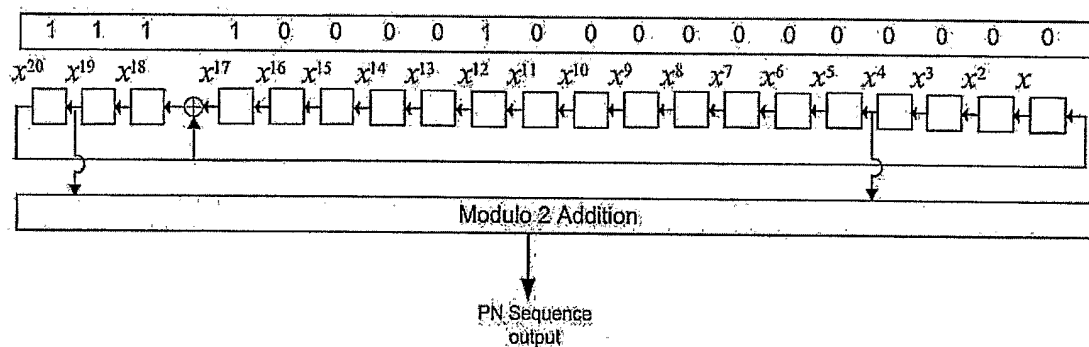
Figure 5.2.1.2.9.1.1.2-1 PN Sequence Generator for Modulating the TDM Pilot 1 Sub-carriers.

The 248-bit TDM Pilot 1 fixed pattern is called the TDM Pilot 1 Information packet and is denoted as P1I.

Each group of two consecutive bits in the P1I packet shall be used to generate QPSK modulation symbols.

5.2.1.2.9.1.1.3 Modulation Symbols Mapping

In the TDM Pilot 1 information packet, each group of two consecutive bits, P1I(2i) and P1I(2i+1), i = 0,1,...123, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol MS= (m_I, m_Q) with D = 4 as specified[29] in Table 5.2.1.2.9.1.1.3-1. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

---

[28] This corresponds to the mask associated with slot 1 (see Table 5.2.1.2.9.1.2.3-1).

[29] This factor is calculated using the fact that only 124 of the 4000 available carriers are being used.

$$\sqrt{\frac{1}{2} \times \frac{4000}{124}} \cong 4$$

Table 5.2.1.2.9.1.1.3-1 QPSK Modulation Table

Input bits		Modulation Symbols MS	
s_1	s_0	m_I	m_Q
0	0	D	D
0	1	-D	D
1	0	D	-D
1	1	-D	-D
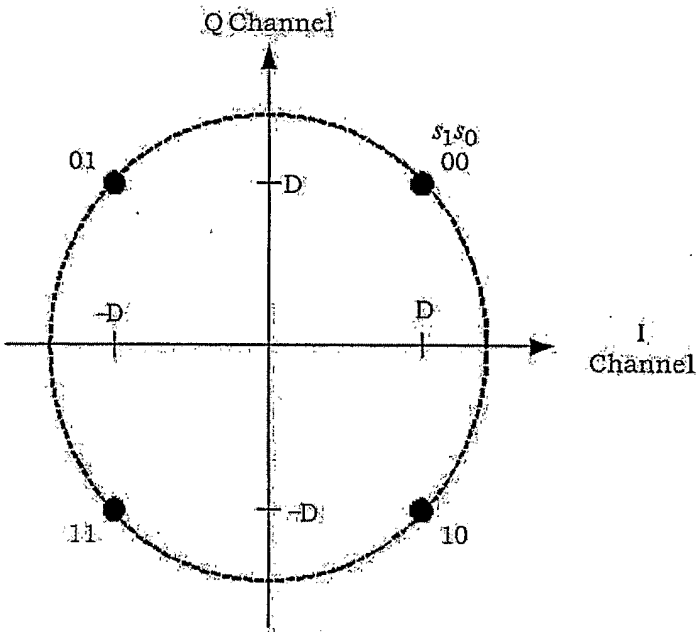
Figure 5.2.1.2.9.1.1.3-1 Signal Constellation for QPSK Modulation

5.2.1.2.9.1.1.4 Modulation Symbols to Sub-carrier Mapping

The ith modulation symbol MS(i), i = 0,1,...,123, shall be mapped to the sub-carrier with index j as specified in 5.2.1.2.9.1.1.1.

5.2.1.2.9.1.1.5 OFDM Common Operation

The modulated TDM Pilot 1 sub-carriers shall undergo common operations as specified in 5.2.1.2.11.

5.2.1.2.9.1.2 Wide-area Identification Channel (WIC)

The Wide-area Identification Channel (WIC) shall span one OFDM symbol. It shall be transmitted at OFDM symbol index 1 in a superframe. It follows the TDM Pilot 1 OFDM symbol. This is an overhead channel that is used for conveying the Wide-area Differentiator

1   information to FLO receivers. All transmit waveforms within a Wide-area[30] shall be
2   scrambled using the 4-bit Wide-area Differentiator corresponding to that area.

3   For the WIC OFDM symbol in a superframe only 1 slot shall be allocated. The allocated slot
4   shall use as input a 1000-bit fixed pattern, with each bit set to zero. The input bit pattern
5   shall be processed according to the steps illustrated in Figure 5.2.1.2.9.1.2-1. No
6   processing shall be performed for the un-allocated slots.

```
┌─────────────────────────────┐     ┌──────────────┐      ┌──────────────┐
│ Fixed Pattern for TDM Pilot 2/WIC/ │     │ Filling Bits │      │ Slot Buffer  │
│ LIC/FDM Pilot/TPC/Unallocated ────▶│  into        │─────▶│ Scrambling   │
│ Slots in Data Channel/Reserved │     │ Slot Buffers │      │              │
│    OFDM Symbols             │     └──────────────┘      └──────────────┘
└─────────────────────────────┘                                    │
                                                                   │
┌──────────────┐   ┌──────────────┐   ┌──────────────┐   ┌──────────────┐
│    OFDM      │   │ Mapping of   │   │ Mapping of   │   │ Mapping of   │
│   Common   ◀─│   Symbols to  ◀─│   slots to    ◀─│   bits to    │◀──┘
│  Operation   │   │ Interlace    │   │ interlaces   │   │ Modulation   │
│              │   │ subcarriers  │   │              │   │ Symbols      │
└──────────────┘   └──────────────┘   └──────────────┘   └──────────────┘
```

7
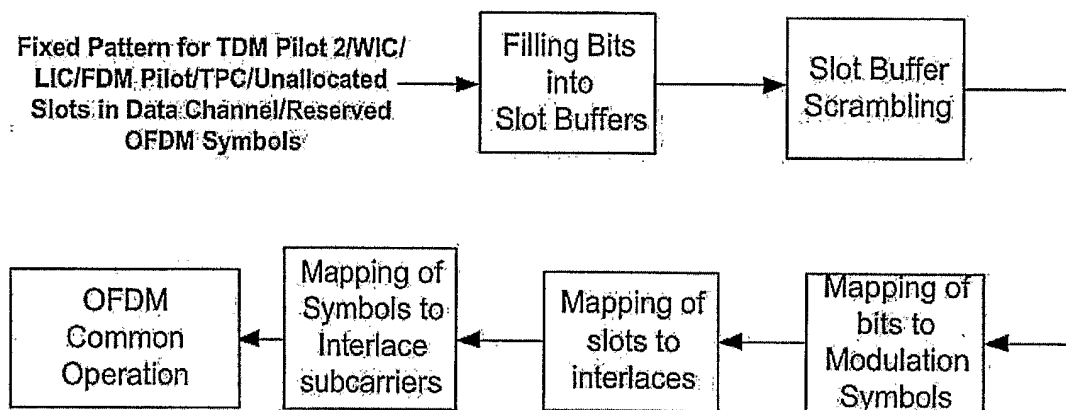
8   **Figure 5.2.1.2.9.1.2-1 TDM Pilot 2 /WIC/LIC/FDM Pilot/TPC/Unallocated Slots in**
9   **Data Channel/Reserved OFDM Symbol Fixed Pattern Processing in the Transmitter**

10   5.2.1.2.9.1.2.1 Slot Allocation

11   The WIC shall be allocated the slot with index 3. The allocated and un-allocated slots in the
12   WIC OFDM symbol are illustrated in Figure 5.2.1.2.9.1.2.1-1. The slot index chosen is the
13   one that maps to interlace 0 for OFDM symbol index 1 (see 5.2.1.2.10).

---

[30] Including Local-area channels but excluding the TDM Pilot 1 Channel and the PPC..

slot 7	Un-allocated
slot 6	Un-allocated
slot 5	Un-allocated
slot 4	Un-allocated
slot 3	Fixed Pattern
slot 2	Un-allocated
slot 1	Un-allocated
slot 0	Un-allocated

OFDM Symbol Index 1
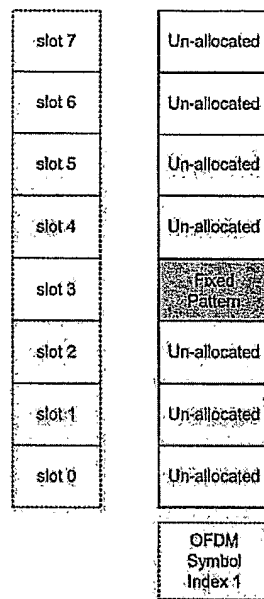
Figure 5.2.1.2.9.1.2.1-1 WIC Slot Allocation

5.2.1.2.9.1.2.2 Filling of Slot Buffer

The buffer for the allocated slot shall be completely filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'. The buffers for the un-allocated slots shall be left empty.

5.2.1.2.9.1.2.3 Slot Scrambling

The bits of each allocated slot buffer shall be XOR'd sequentially with the scrambler output bits to randomize the bits prior to modulation. The scrambled slot buffer corresponding to slot index i is denoted as SB(i), where i ∈ {0,1,...,7}. The scrambling sequence used for any slot buffer depends on the OFDM symbol index and the slot index.

The scrambling bit sequence shall be equivalent to one generated with a 20-tap linear feedback shift register (LFSR) with the generator sequence $h(D) = D^{20}+D^{17}+1$, as shown in Figure 5.2.1.2.9.1.2.3-1. The transmitter shall use a single LFSR for all transmissions.

At the start of every OFDM symbol, the LFSR shall be initialized to the state $[d_3d_2d_1d_0c_3c_2c_1c_0b_0a_{10}a_9a_8a_7a_6a_5a_4a_3a_2a_1a_0]$, which depends on the channel type (the TDM Pilot or the Wide-area or the Local-area Channel), and the OFDM symbol index in a superframe.

Bits '$d_3d_2d_1d_0$' shall be set as follows:

- For all the Wide-area channels (the WIC, the WTPC, the Wide-area OIS and the Wide-area Data Channel), the Local-area channels (the LIC, the LTPC, the Local-area OIS and the Local-area Data Channel), the TDM Pilot 2 Channel and the 2 Reserved OFDM symbols when the PPC is absent, these bits shall be set to the 4-bit Wide-area Differentiator (WID).

1 Bits 'c3c2c1c0' shall be set as follows:

2 • For the TDM Pilot 2 Channel, the Wide-area OIS Channel, the Wide-area Data
3   Channel, the WTPC and the WIC these bits shall be set to '0000'.

4 • For the Local-area OIS Channel, the LTPC, the LIC, the Local-area Data Channel
5   and the 2 Reserved OFDM symbols when the PPC is absent, these bits shall be set
6   to the 4-bit Local-area Differentiator (LID).

7 Bit b_0 is a reserved bit and shall be set to '1'.

8 Bits a_{10} through a_0 shall correspond to the OFDM symbol index number in a superframe,
9 which ranges from 0 through 1199.

10 The scrambling sequence for each slot shall be generated by a modulo-2 inner product of
11 the 20-bit state vector of the sequence generator and a 20-bit mask associated with that
12 slot index as specified in Table 5.2.1.2.9.1.2.3-1.

13

Table 5.2.1.2.9.1.2.3-1 Mask Associated with Different Slots

Slots Index	m_{19}	m_{18}	m_{17}	m_{16}	m_{15}	m_{14}	m_{13}	m_{12}	m_{11}	m_{10}	m_9	m_8	m_7	m_6	m_5	m_4	m_3	m_2	m_1	m_0
0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
2	1	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0	0	1	1
3	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
4	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
5	1	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0
6	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1	1	0	0
7	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

14 The shift register shall be reloaded with a new state [$d_3d_2d_1d_0c_3c_2c_1c_0b_0a_{10}a_9a_8a_7$
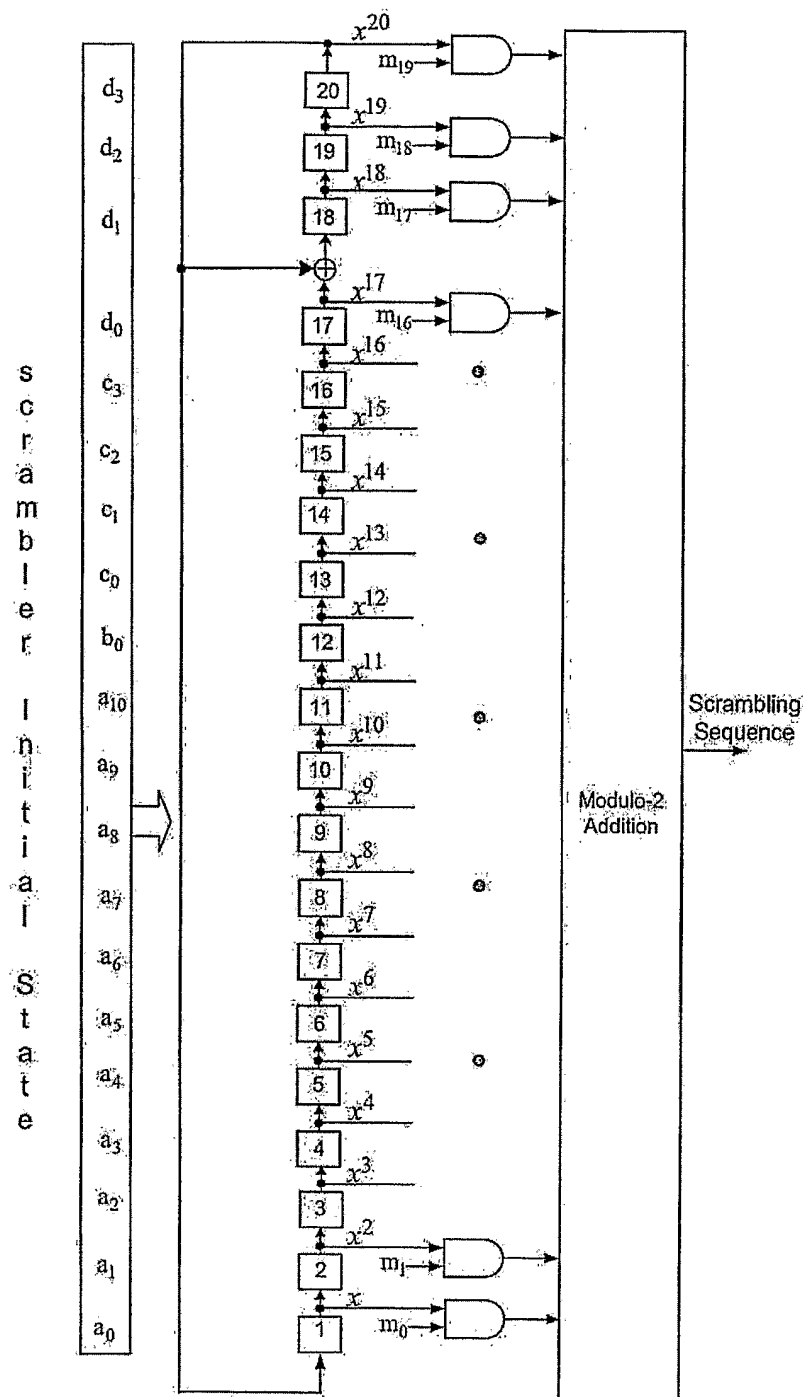15 $a_6a_5a_4a_3a_2a_1a_0$] for each slot at the start of every OFDM symbol.

Figure 5.2.1.2.9.1.2.3-1 Slot Bit Scrambler

5.2.1.2.9.1.2.4 Modulation Symbol Mapping

Each group of two consecutive bits from the i-th scrambled slot buffer, SB(i, 2k) and SB(i, 2k + 1), i=3, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be

1   mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table
2   5.2.1.2.9.1.1.3-1 with[31] D = 2. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for
3   the QPSK modulation.

4   5.2.1.2.9.1.2.5 Slot to Interlace Mapping

5   The mapping of slots to interlaces for the WIC OFDM symbol shall be as specified in
6   5.2.1.2.10.

7   5.2.1.2.9.1.2.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

8   The 500 modulation symbols in the allocated slot shall be sequentially assigned to 500
9   interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)
10 shall be mapped to the ith sub-carrier of that interlace.

11 5.2.1.2.9.1.2.7 OFDM Common Operation

12 The modulated WIC sub-carriers shall undergo common operations as specified in
13 5.2.1.2.11.

14 5.2.1.2.9.1.3 Local-area Identification Channel (LIC)

15 The Local-area Identification Channel (LIC) shall span one OFDM symbol. It shall be
16 transmitted at OFDM symbol index 2 in a superframe. It follows the WIC channel OFDM
17 symbol. This is an overhead channel that is used for conveying the Local-area Differentiator
18 information to FLO receivers. All Local-area transmit waveforms shall be scrambled using a
19 4-bit Local-area Differentiator, in conjunction with the Wide-area Differentiator,
20 corresponding to that area.

21 For the LIC OFDM symbol in a superframe only a single slot shall be allocated. The
22 allocated slot shall use a 1000-bit fixed pattern as input. These bits shall be set to zero.
23 These bits shall be processed according to the steps illustrated in Figure 5.2.1.2.9.1.2-1.
24 No processing shall be performed for the un-allocated slots.

25 5.2.1.2.9.1.3.1 Slot Allocation

26 The LIC shall be allocated the slot with index 5. The allocated and un-allocated slots in the
27 LIC OFDM symbol are illustrated in Figure 5.2.1.2.9.1.3.1-1. The slot index chosen is the
28 one that maps to interlace 0 for OFDM symbol index 2 (see 5.2.1.2.10).

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[31] The value of D is chosen to keep the OFDM symbol energy constant, since only 500 of the 4000 available sub-carriers are used.
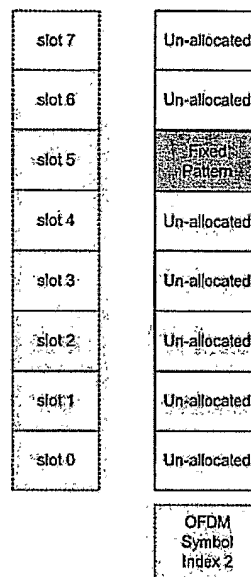
Figure 5.2.1.2.9.1.3.1-1 LIC Slot Allocation

5.2.1.2.9.1.3.2 Filling of Slot Buffer

The buffer for the allocated slot shall be completely filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'. The buffers for the un-allocated slots shall be left empty.

5.2.1.2.9.1.3.3 Slot Scrambling

The bits of the LIC slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB_i

5.2.1.2.9.1.3.4 Modulation Symbol Mapping

Each group of two consecutive bits from the ith scrambled slot buffer, $SB(i, 2k)$ and $SB(i, 2k + 1)$, i=5, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol $MS= (m_I, m_Q)$ as specified in Table 5.2.1.2.9.1.1.3-1 with[32] D = 2. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

5.2.1.2.9.1.3.5 Slot to Interlace Mapping

The mapping of slots to interlaces for the LIC OFDM symbol shall be as specified in 5.2.1.2.10.

---

[32] The value of D is chosen to keep the OFDM symbol energy constant, since only 500 of the 4000 available sub-carriers are used.

1   5.2.1.2.9.1.3.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

2   The 500 modulation symbols in the allocated slot shall be sequentially assigned to 500
3   interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)
4   shall be mapped to the ith sub-carrier of that interlace.

5   5.2.1.2.9.1.3.7 OFDM Common Operation

6   The modulated LIC sub-carriers shall undergo common operations as specified in
7   5.2.1.2.11.

8   5.2.1.2.9.1.4 TDM Pilot 2 Channel

9   The TDM Pilot 2 Channel shall span one OFDM symbol. It shall be transmitted at OFDM
10   symbol index 3 in a superframe. It follows the LIC OFDM symbol. It may be used for fine
11   OFDM symbol timing corrections in the FLO receivers.

12   For the TDM Pilot 2 OFDM symbol in each superframe only 4 slots shall be allocated. Each
13   allocated slot shall use as input a 1000-bit fixed pattern, with each bit set to zero. These
14   bits shall be processed according to the steps illustrated in Figure 5.2.1.2.9.1.2-1. No
15   processing shall be performed for the un-allocated slots.

16   In Figure 5.2.1.2.9.1.2-1, the mapping of slots to interlaces (see 5.2.1.2.10) ensures that
17   the allocated slots are mapped into interlaces 0, 2, 4, and 6. Therefore, the TDM Pilot 2
18   OFDM symbol is comprised of 2000 non-zero sub-carriers which are uniformly spaced
19   among the Active sub-carriers (see 5.2.1.2.2.1.2). The ith TDM Pilot 2 sub-carrier shall
20   correspond to the sub-carrier index j defined as follows:

21
$$j = \begin{cases} 48 + (i) \times 2, \forall\ i \in \{0,1..999\} \\ 48 + (i+1) \times 2, \forall\ i \in \{1000,...1999\} \end{cases}$$

22   Note that the TDM Pilot 2 Channel does not use the sub-carrier with index 2048.

23   5.2.1.2.9.1.4.1 Slot Allocation

24   For the TDM Pilot 2 OFDM symbol, the allocated slots shall have indices 0, 1, 2 and 7.

25   The allocated and un-allocated slots in the TDM Pilot 2 OFDM symbol are illustrated in
26   Figure 5.2.1.2.9.1.4-1.
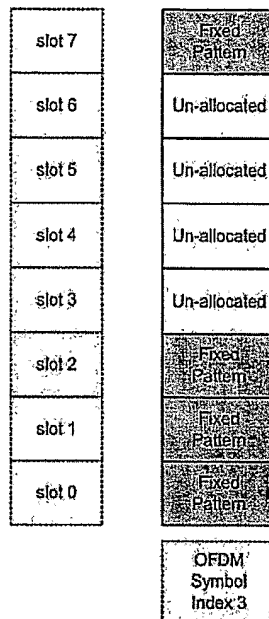
Figure 5.2.1.2.9.1.4-1 TDM Pilot 2 Slot Allocation

5.2.1.2.9.1.4.2 Filling of Slot Buffer

The buffer for each allocated slot shall be completely filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'. The buffers for the un-allocated slots shall be left empty.

5.2.1.2.9.1.4.3 Slot Scrambling

The bits of the TDM Pilot 2 Channel slot buffers shall be scrambled as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

5.2.1.2.9.1.4.4 Modulation Symbol Mapping

Each group of two adjacent bits from the ith scrambled slot buffer, $SB(i,2k)$ and $SB(i, 2k + 1)$, $i=0,1,2,7$, $k = 0,1,...,499$, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol $MS = (m_I, m_Q)$ as specified in Table 5.2.1.2.9.1.1.3-1 with[33] $D = 1$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

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[33] The value of D is chosen to keep the OFDM symbol energy constant, since only 2000 of the 4000 available sub-carriers are used.

1   5.2.1.2.9.1.4.5 Slot to Interlace Mapping

2   The mapping of slots to interlaces for the the TDM Pilot 2 Channel OFDM symbol shall be
3   as specified in 5.2.1.2.10.

4   5.2.1.2.9.1.4.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

5   The 500 modulation symbols in an allocated slot shall be sequentially assigned to 500
6   interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)
7   shall be mapped to the ith sub-carrier of that interlace.

8   5.2.1.2.9.1.4.7 OFDM Common Operation

9   The modulated TDM Pilot 2 Channel sub-carriers shall undergo common operations as
10   specified in 5.2.1.2.11.

11   5.2.1.2.9.1.5 Transition Pilot Channel (TPC)

12   The Transition Pilot Channel consists of 2 sub-channels: the Wide-area Transition Pilot
13   Channel (WTPC) and the Local-area Transition Pilot Channel (LTPC). The TPC flanking the
14   Wide-area OIS and the Wide-area Data channel is called the WTPC. The TPC flanking the
15   Local-area OIS and the Local-area Data Channel is called the LTPC. The WTPC spans 1
16   OFDM symbol on either side of every Wide-area channel transmission[34] (the Wide-area
17   Data and the Wide-area OIS Channel) in a superframe. The LTPC spans 1 OFDM symbol
18   on either side of every Local-area Channel transmission[35] (the Local-area Data and the
19   Local-area OIS Channel). The purpose of the TPC OFDM symbol is two-fold: to allow
20   channel estimation at the boundary between the Local-area and the Wide-area channels
21   and to facilitate timing synchronization for the first Wide-area (or Local-area) MLC in each
22   frame.
23   The TPC spans 20 OFDM symbols in a superframe, which are equally divided between the
24   WTPC and the LTPC as illustrated in Figure 5.2.1.2.3-2. There are nine instances where
25   the LTPC and the WTPC transmissions occur right next to each other and two instances
26   where only one of these channels is transmitted. Only the WTPC is transmitted after the
27   TDM Pilot 2 Channel, and only the LTPC is transmitted prior to the Positioning Pilot
28   Channel (PPC)/Reserved OFDM symbols.

29   Let

30   P be the number of OFDM symbols in the PPC or the number of Reserved OFDM
31   symbols in the case where the PPC is absent in a superframe.

32   W be the number of OFDM symbols associated with the Wide-area Data Channel in a
33   frame.

34   L be the number of OFDM symbols associated with the Local-area Data Channel in a
35   frame.

---

[34] With the exception of the WIC.

[35] With the exception of the LIC.

1   F be the number of OFDM symbols in a frame.

2   The values of P shall be 2, 6, 10 or 14. The number of Data Channel OFDM symbols in a
3   frame shall be $F-4$. The exact locations of the TPC OFDM symbols in a superframe shall
4   be as specified in Table 5.2.1.2.9.1.5-1.

5   Table 5.2.1.2.9.1.5-1 TPC Location Indices in a Superframe

Transition Pilot Channel	Index for the WTPC OFDM Symbol	Index for the LTPC OFDM Symbol
TDM Pilot 2 Channel $\rightarrow$ Wide-area OIS Channel	4	---
Wide-area OIS Channel $\rightarrow$ Local-area OIS Channel	10	11
Local-area OIS Channel $\rightarrow$ Wide-area Data Channel	18	17
Wide-area Data Channel $\rightarrow$ Local-area Data Channel	$19 + W + F \times i,$ $\{i = 0,1,2,3\}$	$20 + W + F \times i,$ $\{i = 0,1,2,3\}$
Local-area Data Channel $\rightarrow$ Wide-area Data Channel	$18 + F \times i,$ $\{i = 1,2,3\}$	$17 + F \times i,$ $\{i = 1,2,3\}$
Local-area Data Channel $\rightarrow$ PPC/Reserved Symbols	---	$1199 - P$

6   All slots in the TPC OFDM symbols use as input a 1000-bit fixed pattern, with each bit set
7   to zero. These bits shall be processed according to the steps illustrated in Figure
8   5.2.1.2.9.1.2-1.

9   5.2.1.2.9.1.5.1 Slot Allocation

10 The TPC OFDM symbol shall be allocated all 8 slots with indices 0 through 7.

11 5.2.1.2.9.1.5.2 Filling of Slot Buffer

12 The buffer for each allocated slot shall be completely filled with a fixed pattern consisting of
13 1000 bits, with each bit set to '0'.

1 5.2.1.2.9.1.5.3 Slot Scrambling

2 The bits of each allocated TPC slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3.
3 The scrambled slot buffer is denoted by SB.

4 5.2.1.2.9.1.5.4 Modulation Symbol Mapping

5 Each group of two consecutive bits from the ith scrambled slot buffer, SB(i, 2k) and SB(i, 2k
6 + 1), i=0,1,2,...7, k = 0,1,...499, which are labeled as s_0 and s_1 respectively, shall be
7 mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table
8 5.2.1.2.9.1.1.3-1 with D = $\frac{1}{\sqrt{2}}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for
9 the QPSK modulation.

10 5.2.1.2.9.1.5.5 Slot to Interlace Mapping

11 The mapping of slots to interlaces for the TPC OFDM symbol shall be as specified in
12 5.2.1.2.10.

13 5.2.1.2.9.1.5.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

14 The 500 modulation symbols in each allocated slot shall be sequentially assigned to 500
15 interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$
16) shall be mapped to the ith sub-carrier of that interlace.

17 5.2.1.2.9.1.5.7 OFDM Common Operation

18 The modulated TPC sub-carriers shall undergo common operations as specified in
19 5.2.1.2.11.

20 5.2.1.2.9.1.6 Positioning Pilot Channel /Reserved Symbols

21 The Positioning Pilot Channel (PPC) may appear at the end of a superframe. When present
22 it has a variable duration of 6, 10 or 14 OFDM symbols. When the PPC is absent, there are
23 two Reserved OFDM symbols at the end of the superframe. The presence or absence of the
24 PPC and its duration are signaled over the OIS Channel.

25 5.2.1.2.9.1.6.1 Positioning Pilot Channel

26 The PPC structure including the information transmitted and the waveform generation is
27 TBD.

28 The FLO device may use the PPC either autonomously or in conjunction with the GPS
29 signal to determine its geographical location.

30 5.2.1.2.9.1.6.2 Reserved OFDM Symbols

31 When the PPC is absent, there are two Reserved OFDM symbols at the end of the
32 superframe.

All slots in the Reserved OFDM Symbols use as input a 1000-bit fixed pattern, with each bit set to zero. These bits shall be processed according to the steps illustrated in Figure 5.2.1.2.9.1.2-1.

5.2.1.2.9.1.6.2.1 Slot Allocation

The Reserved OFDM symbol shall be allocated all 8 slots with indices 0 through 7.

5.2.1.2.9.1.6.2.2 Filling of Slot Buffer

The buffer for each allocated slot shall be completely filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'.

5.2.1.2.9.1.6.2.3 Slot Scrambling

The bits of each allocated Reserved OFDM symbol slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

5.2.1.2.9.1.6.2.4 Modulation Symbol Mapping

Each group of two consecutive bits from the ith scrambled slot buffer, SB(i,2k) and SB(i,2k + 1), i=0,1,2,...7, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table 5.2.1.2.9.1.1.3-1 with D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

5.2.1.2.9.1.6.2.5 Slot to Interlace Mapping

The mapping of slots to interlaces for the Reserved OFDM symbols shall be as specified in 5.2.1.2.10.

5.2.1.2.9.1.6.2.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

The 500 modulation symbols in each allocated slot shall be sequentially assigned to 500 interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$) shall be mapped to the ith sub-carrier of that interlace.

5.2.1.2.9.1.6.2.7 OFDM Common Operation

The modulated Reserved OFDM Symbol sub-carriers shall undergo common operations as specified in 5.2.1.2.11.

5.2.1.2.9.2 Wide-area OIS Channel

This channel is used to convey overhead information about the active MLC's associated with the Wide-area Data Channel, such as their scheduled transmission times and slot allocations, in the current superframe. The Wide-area OIS Channel spans 5 OFDM symbol intervals in each superframe (see Figure 5.2.1.2.3-2).

The Physical layer packet for the Wide-area OIS Channel shall be processed according to the steps illustrated in Figure 5.2.1.2.9.2-1.
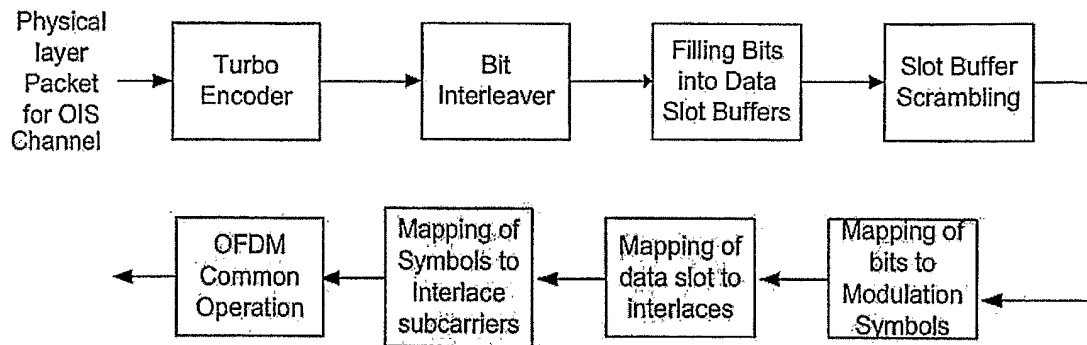
Figure 5.2.1.2.9.2-1 OIS Physical Layer Packet Processing in the Transmitter

5.2.1.2.9.2.1 Encoding

The Wide-area OIS Channel Physical layer packets shall be encoded with code rate R = 1/5. The encoder shall discard the 6-bit TAIL field of the incoming Physical layer packet and encode the remaining bits with a parallel turbo encoder as specified in 5.2.1.2.9.2.1.1. The turbo encoder shall add an internally generated tail of 6/R (=30) output code bits, so that the total number of turbo encoded bits at the output is 1/R times the number of bits in the input Physical layer packet.

Figure 5.2.1.2.9.2.1-1 illustrates the encoding scheme for the Wide-area OIS Channel. The Wide-area OIS Channel encoder parameters shall be as specified in Table 5.2.1.2.9.2.1-1.
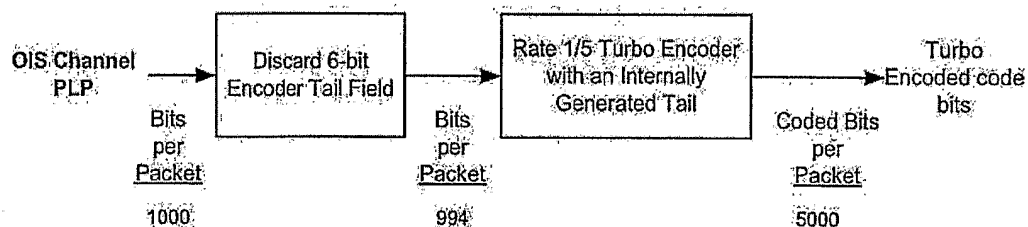
Figure 5.2.1.2.9.2.1-1 Wide-area/Local-area OIS Channel Encoder

Table 5.2.1.2.9.2.1-1 Parameters of the Wide-area/Local-area OIS Channel Encoder

Bits	Turbo Encoder Input Bits N_{turbo}	Code Rate	Turbo Encoder Output bits
1000	994	1/5	5000

5.2.1.2.9.2.1.1 Turbo Encoder

The turbo encoder employs two systematic, recursive, convolutional encoders connected in parallel, with an interleaver, the turbo interleaver, preceding the second recursive convolutional encoder. The two recursive convolutional codes are called the constituent

1   codes of the turbo code. The outputs of the constituent encoders are punctured and
2   repeated to achieve the desired number of turbo encoded output bits.

3   A common constituent code shall be used for turbo codes of rates 1/5, 1/3, 1/2, and 2/3.
4   The transfer function for the constituent code shall be

$$G(D) = \begin{bmatrix} 1 & \dfrac{n_0(D)}{d(D)} & \dfrac{n_1(D)}{d(D)} \end{bmatrix}$$

6   where $d(D) = 1 + D^2 + D^3$, $n_0(D) = 1 + D + D^3$, and $n_1(D) = 1 + D + D^2 + D^3$.

7   The turbo encoder shall generate an output symbol sequence that is identical to the one
8   generated by the encoder shown in Figure 5.2.1.2.9.2.1.1-1. Initially, the states of the
9   constituent encoders registers in this figure are set to zero. Then, the constituent encoders
10   are clocked with the switches in the position noted.

11   The encoded data output bits are generated by clocking the constituent encoders N_{turbo}
12   times with the switches in the up positions and puncturing the output as specified in Table
13   5.2.1.2.9.2.1.1-1. Within a puncturing pattern, a '0' means that the bit shall be deleted and
14   a '1' means that the bit shall be passed. The constituent encoder outputs for each bit
15   period shall be passed in the sequence X, Y_0, Y_1, X', Y'_0, Y'_1 with the X output first. Bit
16   repetition is not used in generating the encoded data output bits.

17   The constituent encoder output symbol puncturing for the tail period shall be as specified
18   in Table 5.2.1.2.9.2.1.1-2. Within a puncturing pattern, a '0' means that the symbol shall
19   be deleted and a '1' means that a symbol shall be passed.

20   For rate 1/5 turbo codes, the tail output code bits for each of the first three tail periods
21   shall be punctured and repeated to achieve the sequence $XXY_0Y_1Y_1$, and the tail output
22   code bits for each of the last three tail bit periods shall be punctured and repeated to
23   achieve the sequence $X'X'Y'_0Y'_1Y'_1$.

40

Clocked once for each of the N_{turbo} data bit periods with the switch up; then, clocked once for each of the three Constituent Encoder 1 tail bit periods with the switch down; then, not clocked for the three Constituent Encoder 2 tail bit periods.

Clocked once for each of the N_{turbo} data bit periods with the switch up; then, not clocked for the three Constituent Encoder 1 tail bit periods; then, clocked once for each of the three Constituent Encoder 2 tail bit periods with the switch down.

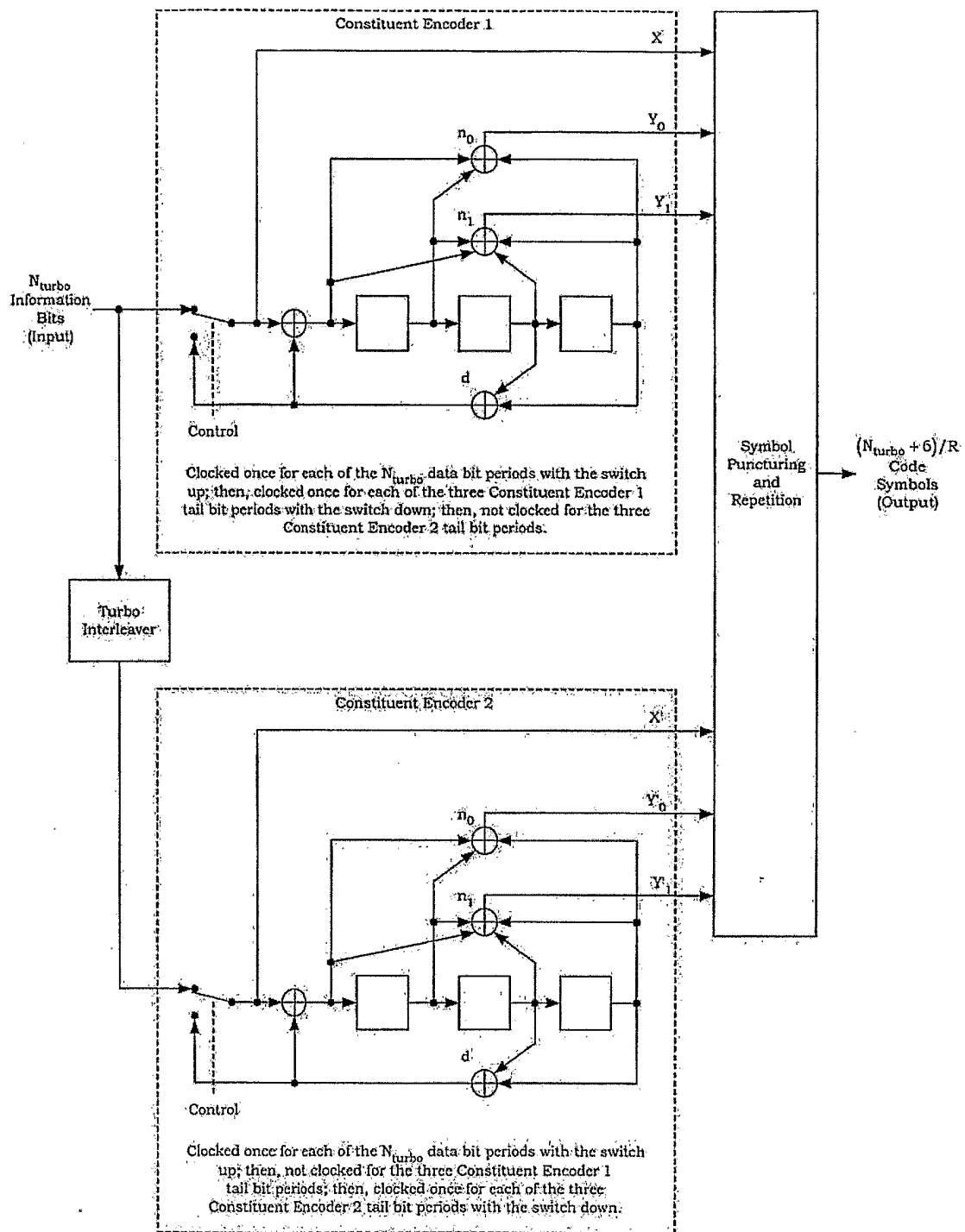Figure 5.2.1.2.9.2.1.1-1 Turbo Encoder

Table 5.2.1.2.9.2.1.1-1 Puncturing Patterns for the Data Bit Periods for the OIS Channel

Output	Code Rate
	1/5
X	1
Y_0	1
Y_1	1
X'	0
Y'_0	1
Y'_1	1

Note: The puncturing table is to be read
from top to bottom.

Table 5.2.1.2.9.2.1.1-2 Puncturing Patterns for the Tail Bit Periods for the OIS Channel

Output	Code Rate
	1/5
X	111 000
Y_0	111 000
Y_1	111 000
X'	000 111
Y'_0	000 111
Y'_1	000 111

Note: For rate-1/5 turbo codes, the puncturing table is to be read
first from top to bottom repeating X, X', Y_1, and Y'_1 and then
from left to right.

5.2.1.2.9.2.1.2 Turbo Interleaver

The turbo interleaver, which is part of the turbo encoder, shall block interleave the turbo encoder input data that is fed to the Constituent Encoder 2.

The turbo interleaver shall be functionally equivalent to an approach where the entire sequence of turbo interleaver input bits are written sequentially into an array at a sequence of addresses and then the entire sequence is read out from a sequence of addresses that are defined by the procedure described below.

1 Let the sequence of input addresses be from 0 to $N_{turbo} - 1$. Then, the sequence of

2 interleaver output addresses shall be equivalent to those generated by the procedure

3 illustrated in Figure 5.2.1.2.9.2.1.2-1 and described below.[36]

4 1. Determine the turbo interleaver parameter, n, where n is the smallest integer such

5   that $N_{turbo} \leq 2^{n+5}$. Table 5.2.1.2.9.2.1.2-1 gives this parameter for the 1000-bit

6   physical layer packet.

7 2. Initialize an (n + 5)-bit counter to 0.

8 3. Extract the n most significant bits (MSBs) from the counter and add one to form a

9   new value. Then, discard all except the n least significant bits (LSBs) of this value.

10 4. Obtain the n-bit output of the table lookup defined in Table 5.2.1.2.9.2.1.2-2 with a

11   read address equal to the five LSBs of the counter. Note that this table depends on

12   the value of n.

13 5. Multiply the values obtained in Steps 3 and 4, and discard all except the n LSBs.

14 6. Bit-reverse the five LSBs of the counter.

15 7. Form a tentative output address that has its MSBs equal to the value obtained in

16   Step 6 and its LSBs equal to the value obtained in Step 5.

17 8. Accept the tentative output address as an output address if it is less than N_{turbo};

18   otherwise, discard it.

19 9. Increment the counter and repeat Steps 3 through 8 until all N_{turbo} interleaver

20   output addresses are obtained.

21
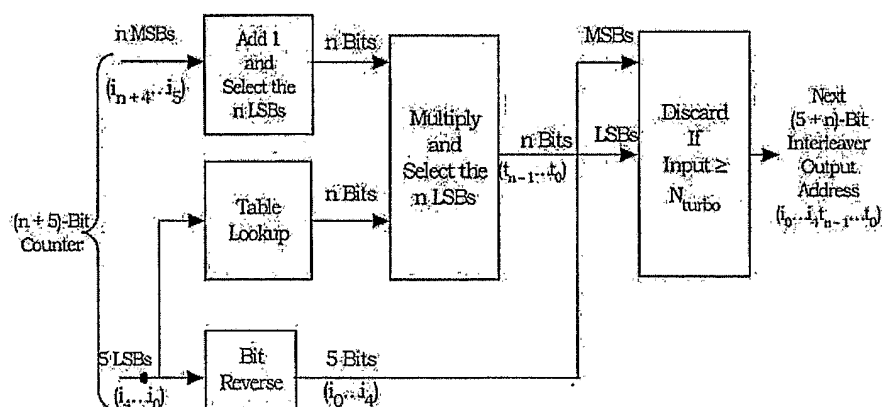
22 Figure 5.2.1.2.9.2.1.2-1 Turbo Interleaver Output Address Calculation Procedure

[36] This procedure is equivalent to one where the counter values are written into a 2^5-row by 2^n-column array by rows, the rows are shuffled according to a bit-reversal rule, the elements within each row are permuted according to a row-specific linear congruential sequence, and tentative output addresses are read out by column. The linear congruential sequence rule is $x(i + 1) = (x(i) + c) \bmod 2^n$, where $x(0) = c$ and c is a row-specific value from a table lookup.

Table 5.2.1.2.9.2.1.2-1 Turbo Interleaver Parameter

Physical Layer Packet Size	Turbo Interleaver Block Size N_{turbo}	Turbo Interleaver Parameter n
1,000	994	5

Table 5.2.1.2.9.2.1.2-2 Turbo Interleaver Lookup Table Definition

Table Index	$n = 5$ Entries	Table Index	$n = 5$ Entries
0	27	16	21
1	3	17	19
2	1	18	1
3	15	19	3
4	13	20	29
5	17	21	17
6	23	22	25
7	13	23	29
8	9	24	9
9	3	25	13
10	15	26	23
11	3	27	13
12	13	28	13
13	1	29	1
14	13	30	13
15	29	31	13

5.2.1.2.9.2.2 Bit Interleaving

For the OIS Channel and the Data Channel, the bit interleaving is a form of block interleaving. The code bits of a turbo encoded packet are interleaved in such a pattern that adjacent code bits are mapped into different constellation symbols.

The Bit Interleaver shall reorder the turbo encoded bits as per the following procedure:

    a. For N bits to be interleaved, the bit interleaver matrix M shall be a 4 columns by N/4 rows block interleaver. The N input bits shall be written into the interleaving array column-by-column sequentially. Label the rows of the matrix M by index j, where j = 0 through N/4 −1 and row 0 is the first row.

    b. For every row j, with even index (j mod 2 =0), the elements in the 2nd and the 3rd column shall be interchanged.

44

c. For every row with odd index (j mod 2 !=0), the elements in the 1st and the 4th column shall be interchanged.

d. Denote the resulting matrix by $\overline{M}$. The contents of $\overline{M}$ shall be read out row-wise, from left to right.

Figure 5.2.1.2.9.2.2-1 illustrates the output of the bit-interleaver for the hypothetical case of N = 20.
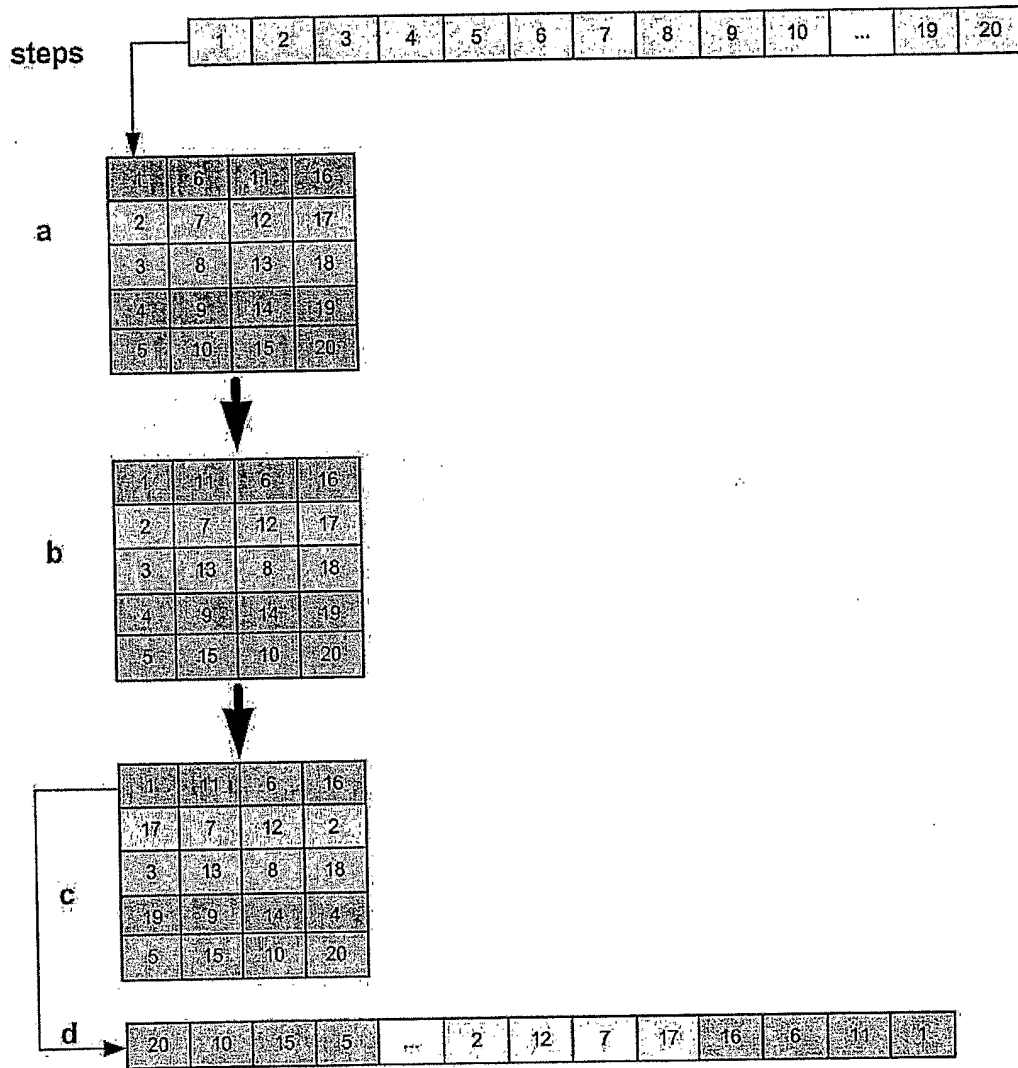
Figure 5.2.1.2.9.2.2-1 Bit Interleaver Operation Example for N = 20

5.2.1.2.9.2.3 Data Slot Allocation

For the Wide-area OIS Channel, 7 data slots shall be allocated per OFDM symbol for the transmission of OIS Channel turbo encoded packets. The Wide-area OIS Channel shall use transmit mode 5. Therefore, it requires 5 data slots to accommodate the content of a single turbo encoded packet. Some Wide-area OIS Channel turbo encoded packets may span two consecutive OFDM symbols. The data slot allocations are made at the MAC layer (see 4.8).

1   5.2.1.2.9.2.4 Filling of Data Slot Buffer

2   The bit-interleaved code bits of a Wide-area OIS Channel turbo encoded packet shall be
3   written sequentially into 5 consecutive data slot buffers in either one or two consecutive
4   OFDM symbols as illustrated in Figure 5.2.1.2.9.2.4-1. These data slot buffers correspond
5   to slot indices 1 through 7. The data slot buffer size shall be 1000 bits[37]. The 7 Wide-area
6   OIS Channel turbo encoded packets (TEP) shall occupy consecutive slots over 5
7   consecutive OFDM symbols in the Wide-area OIS Channel (see Figure 5.2.1.2.3-2).

data slot 7	TEP 2	TEP 3	TEP 5	TEP 6	TEP 7
data slot 6	TEP 2	TEP 3	TEP 4	TEP 6	TEP 7
data slot 5	TEP 1	TEP 3	TEP 4	TEP 6	TEP 7
data slot 4	TEP 1	TEP 3	TEP 4	TEP 5	TEP 7
data slot 3	TEP 1	TEP 2	TEP 4	TEP 5	TEP 7
data slot 2	TEP 1	TEP 2	TEP 4	TEP 5	TEP 6
data slot 1	TEP 1	TEP 2	TEP 3	TEP 5	TEP 6
	OFDM Symbol index 5	OFDM Symbol index 6	OFDM Symbol index 7	OFDM Symbol index 8	OFDM Symbol index 9

8

9   Figure 5.2.1.2.9.2.4-1 Wide-area OIS Channel Turbo Encoded Packet Mapping to Data
10   Slot Buffers

11   5.2.1.2.9.2.5 Slot Scrambling

12   The bits of each allocated slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The
13   scrambled slot buffer is denoted by SB.

14   5.2.1.2.9.2.6 Mapping of Bits to Modulation Symbols

15   Each group of two consecutive bits from the ith scrambled slot buffer, SB(i, 2k) and SB(2k
16   + 1), i= 1, 2,...7, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be

---

[37] The data slot buffer size is 1000 bits for QPSK and 2000 bits for 16-QAM and layered modulation.

1 mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table
2 5.2.1.2.9.1.1.3-1 with D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for
3 the QPSK modulation.

4 **5.2.1.2.9.2.7 Slot to Interlace Mapping**
5 The mapping of slots to interlaces for the Wide-area OIS Channel OFDM symbols shall be
6 as specified in 5.2.1.2.10.

7 **5.2.1.2.9.2.8 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers**
8 The 500 modulation symbols in each allocated slot shall be sequentially assigned to 500
9 interlace sub-carriers as per the following procedure:
10   a. Create an empty Sub-carrier Index Vector (SCIV).
11   b. Let i be an index variable in the range ($i \in \{0, 511\}$). Initialize i to 0.
12   c. Represent i by its 9-bit value i_b.
13   d. Bit reverse i_b and denote the resulting value as i_{br}. If $i_{br} <500$, then append i_{br} to the
14   SCIV.
15   e. If $i<511$, then increment i by 1 and go to step c.
16   f. Map the symbol with index, j ($j \in \{0, 499\}$), in a data slot to the interlace sub-carrier
17   with index SCIV[38][j] assigned to that data slot.

18 **5.2.1.2.9.2.9 OFDM Common Operation**
19 The modulated Wide-area OIS Channel sub-carriers shall undergo common operations as
20 specified in 5.2.1.2.11.

21 **5.2.1.2.9.3 Local-area OIS Channel**

22 This channel is used to convey overhead information about the active MLCs associated
23 with the Local-area Data Channel, such as their scheduled transmission times and slot
24 allocations, in the current superframe. The Local-area OIS channel spans 5 OFDM symbol
25 intervals in each superframe (see Figure 5.2.1.2.3-2).

26 The Physical layer packet for the Local-area OIS Channel shall be processed according to
27 the steps illustrated in Figure 5.2.1.2.9.2-1.

28 **5.2.1.2.9.3.1 Encoding**

29 The Local-area OIS Channel Physical layer packets shall be encoded with code rate R =
30 1/5. The encoding procedure shall be identical to that for the Wide-area OIS Channel
31 Physical layer packets as specified in 5.2.1.2.9.2.1.

32 **5.2.1.2.9.3.2 Bit Interleaving**

33 The Local-area OIS Channel turbo encoded packet shall be bit interleaved as specified in
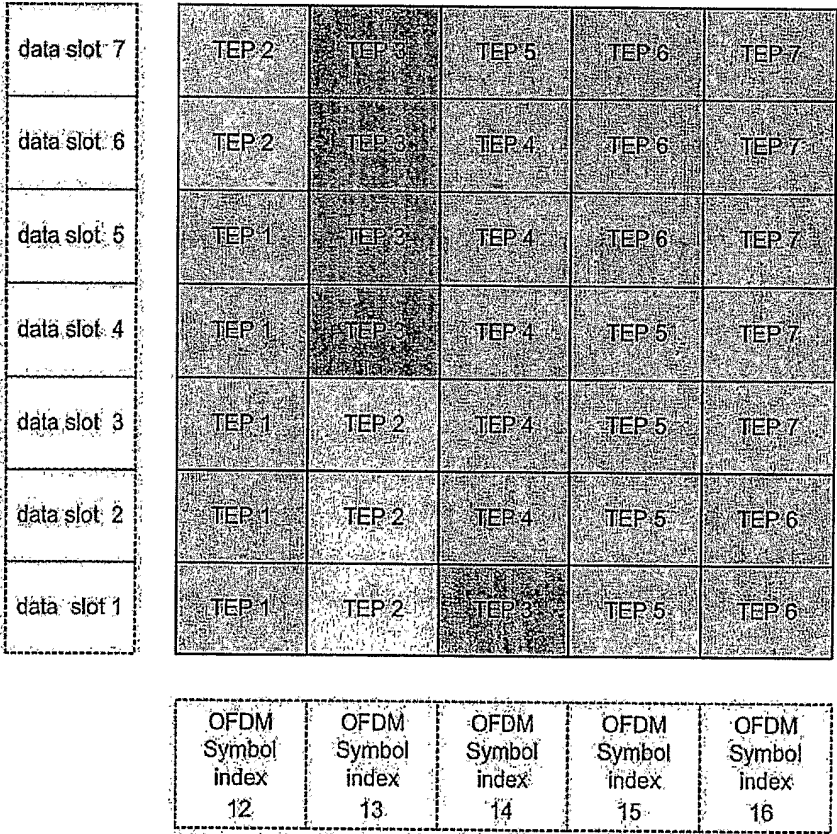34 5.2.1.2.9.2.2.

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[38] SCIV needs to be computed only once and can be used for all data slots.

1   5.2.1.2.9.3.3 Data Slot Allocation

2   For the Local-area OIS Channel, 7 data slots shall be allocated per OFDM symbol for the
3   transmission of turbo encoded packets. The Local-area OIS Channel shall use transmit
4   mode 5. Therefore, it requires 5 data slots to accommodate the content of a single turbo
5   encoded packet. Some Local-area OIS turbo-packets may span two consecutive OFDM
6   symbols. The data slot allocations are made at the MAC layer (see 4.8).

7   5.2.1.2.9.3.4 Filling of Data Slot Buffers

8   The bit-interleaved code bits of a Local-area OIS Channel turbo encoded packet shall be
9   written sequentially into 5 consecutive data slot buffers in either one or two consecutive
10   OFDM symbols as illustrated in Figure 5.2.1.2.9.3.4-1. These data slot buffers correspond
11   to slot indices 1 through 7. The data slot buffer size shall be 1000 bits. The 7 Local-area
12   OIS Channel turbo encoded packets (TEP) shall occupy consecutive slots over 5
13   consecutive OFDM symbols in the Local-area OIS Channel (see Figure 5.2.1.2.9.3.4-1).

	OFDM Symbol index 12	OFDM Symbol index 13	OFDM Symbol index 14	OFDM Symbol index 15	OFDM Symbol index 16
data slot 7	TEP 2	TEP 3	TEP 5	TEP 6	TEP 7
data slot 6	TEP 2	TEP 3	TEP 4	TEP 6	TEP 7
data slot 5	TEP 1	TEP 3	TEP 4	TEP 6	TEP 7
data slot 4	TEP 1	TEP 3	TEP 4	TEP 5	TEP 7
data slot 3	TEP 1	TEP 2	TEP 4	TEP 5	TEP 7
data slot 2	TEP 1	TEP 2	TEP 4	TEP 5	TEP 6
data slot 1	TEP 1	TEP 2	TEP 3	TEP 5	TEP 6

14

15   **Figure 5.2.1.2.9.3.4-1 Local-area OIS Turbo Encoded Packet Mapping to Data Slot**
16   **Buffers**

17   5.2.1.2.9.3.5 Slot Scrambling

18   The bits of each allocated slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The
19   scrambled slot buffer is denoted by SB.

1   5.2.1.2.9.3.6 Mapping of bits to Modulation Symbols

2   Each group of two consecutive bits from the ith scrambled slot buffer, SB(i, 2k) and SB(i,
3   2k + 1), i=1,2,...7, k = 0,1,...499, which are labeled as s_0 and s_1 respectively, shall be
4   mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table
5   5.2.1.2.9.1.1.3-1 with D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for
6   the QPSK modulation.

7   5.2.1.2.9.3.7 Slot to Interlace Mapping

8   The mapping of slots to interlaces for the Local-area OIS Channel OFDM symbols shall be
9   as specified in 5.2.1.2.10.

10   5.2.1.2.9.3.8 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

11   This procedure shall be identical to that for the Wide-area OIS Channel as specified in
12   5.2.1.2.9.2.8.

13   5.2.1.2.9.3.9 OFDM Common Operation

14   The modulated Local-area OIS Channel sub-carriers shall undergo common operations as
15   specified in 5.2.1.2.11.

16   5.2.1.2.9.4 Wide-area FDM Pilot Channel

17   The Wide-area FDM Pilot Channel is transmitted in conjunction with the Wide-area Data
18   Channel or the Wide-area OIS Channel. The Wide-area FDM Pilot Channel carries a fixed
19   bit pattern that may be used for Wide-area Channel estimation and other functions by the
20   FLO device.

21   For the Wide-area FDM Pilot Channel a single slot shall be allocated during every OFDM
22   symbol that carries either the Wide-area Data Channel or the Wide-area OIS Channel.

23   The allocated slot shall use a 1000-bit fixed pattern as input. These bits shall be set to
24   zero. These bits shall be processed according to the steps illustrated in Figure
25   5.2.1.2.9.1.2-1.

26   5.2.1.2.9.4.1 Slot Allocation

27   The Wide-area FDM Pilot Channel shall be allocated the slot with index 0 during every
28   OFDM symbol that carries either the Wide-area Data Channel or the Wide-area OIS
29   Channel.

30   5.2.1.2.9.4.2 Filling of Slot Buffer

31   The buffer for the slot allocated to the Wide-area FDM Pilot Channel shall be completely
32   filled with a fixed pattern consisting of 1000-bits, with each bit set to '0'.

33   5.2.1.2.9.4.3 Slot Scrambling

34   The bits of the Wide-area FDM Pilot Channel slot buffer shall be scrambled as specified in
35   5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

1   5.2.1.2.9.4.4 Modulation Symbol Mapping

2   Each group of two consecutive bits of the ith scrambled slot buffer, SB(i ,2k) and SB(i,2k+1),

3   i = 0, k= 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be mapped into a

4   complex modulation symbol MS= (m_I, m_Q) as specified in Table 5.2.1.2.9.1.1.3-1 with

5    $D = 1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

6   5.2.1.2.9.4.5 Slot to Interlace Mapping

7   The mapping of the Wide-area FDM Pilot Channel slots to interlaces shall be as specified in

8   5.2.1.2.10.

9   5.2.1.2.9.4.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

10   The 500 modulation symbols in the allocated slot shall be sequentially assigned to 500

11   interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)

12   shall be mapped to the ith sub-carrier of that interlace.

13   5.2.1.2.9.4.7 OFDM Common Operation

14   The modulated Wide-area FDM Pilot Channel sub-carriers shall undergo common

15   operations as specified in 5.2.1.2.11.

16   5.2.1.2.9.5 Local-area FDM Pilot Channel

17   The Local-area FDM Pilot Channel is transmitted in conjunction with the Local-area Data

18   Channel or the Local-area OIS Channel. The Local-area FDM Pilot Channel carries a fixed

19   bit pattern that may be used for Local-area channel estimation and other functions by the

20   FLO device.

21   For the Local-area FDM Pilot Channel a single slot shall be allocated during every OFDM

22   symbol that carries either the Local-area Data Channel or the Local-area OIS Channel.

23   The allocated slot shall use a 1000-bit fixed pattern as input. These bits shall be set to

24   zero. These bits shall be processed according to the steps illustrated in Figure

25   5.2.1.2.9.1.2-1

26   5.2.1.2.9.5.1 Slot Allocation

27   The Local-area FDM Pilot Channel shall be allocated the slot with index 0 during every

28   OFDM symbol that carries either the Local-area Data Channel or the Local-area OIS

29   Channel.

30   5.2.1.2.9.5.2 Filling of Pilot Slot Buffer

31   The buffer for the slot allocated to the Local-area FDM Pilot Channel shall be completely

32   filled with a fixed pattern consisting of 1000-bits with each bit set to '0'.

33   5.2.1.2.9.5.3 Slot Buffer Scrambling

34   The bits of the Local-area FDM Pilot slot buffer shall be scrambled as specified in

35   5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

1 5.2.1.2.9.5.4 Modulation Symbols Mapping

2 Each group of two consecutive bits of the ith scrambled slot buffer, SB(i,2k) and SB(i, 2k+1),
3 i =0, k= 0,1,...499 which are labeled as s_0 and s_1, respectively, shall be mapped into a
4 complex modulation symbol MS= (m_I, m_Q) as specified in Table 5.2.1.2.9.1.1.3-1 with
5 D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

6 5.2.1.2.9.5.5 Slot to Interlace Mapping

7 The mapping of the Wide-area FDM Pilot Channel slots to interlaces shall be as specified in
8 5.2.1.2.10.

9 5.2.1.2.9.5.6 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

10 The 500 modulation symbols in the allocated slot shall be sequentially assigned to 500
11 interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)
12 shall be mapped to the ith sub-carrier of that interlace.

13 5.2.1.2.9.5.7 OFDM Common Operation

14 The modulated Local-area FDM Pilot Channel sub-carriers shall undergo common
15 operations as specified in 5.2.1.2.11.

16 5.2.1.2.9.6 Wide-area Data Channel

17 The Wide-area Data Channel is used to carry Physical layer packets meant for Wide-area
18 multicast. The Physical layer packets for the Wide-area Data Channel can be associated
19 with any one of the active MLCs transmitted in the Wide-area.

20 5.2.1.2.9.6.1 Wide-area Data Channel Processing for Allocated Slots

21 The Physical layer packet for the Wide-area Data Channel shall be processed according to
22 the steps illustrated in Figure 5.2.1.2.9.6.1-1.

23 For regular modulation (QPSK and 16-QAM), the Physical layer packet is turbo-encoded
24 and bit interleaved before being stored in the Data slot buffer(s). For layered modulation,
25 the base-component Physical layer packet and the enhancement-component Physical layer
26 packet are turbo-encoded and bit interleaved independently before being multiplexed in to
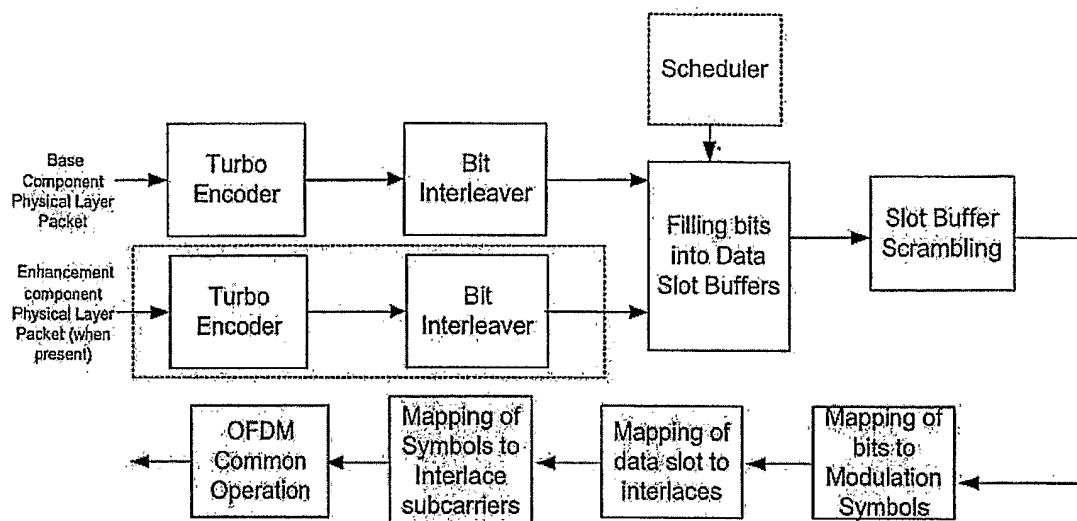27 the Data slot buffer(s).

51

Figure 5.2.1.2.9.6.1-1 Data Channel Physical Layer Packet Processing in the Transmitter

5.2.1.2.9.6.1.1 Encoding

The Wide-area Data Channel Physical layer packets shall be encoded with code rate R = 1/2, 1/3, or 2/3. The encoder shall discard the 6-bit TAIL field of the incoming Physical layer packet and encode the remaining bits with a parallel turbo encoder as specified in 5.2.1.2.9.2.1.1. The turbo encoder shall add an internally generated tail of 6/R (=12, 18 or 9) output code bits, so that the total number of turbo encoded bits at the output is 1/R times the number of bits in the input Physical layer packet.

Figure 5.2.1.2.9.6.1.1-1 illustrates the encoding scheme for the Wide-area Data Channel. The Wide-area Data Channel encoder parameters shall be as specified in Table 5.2.1.2.9.6.1.1-1.
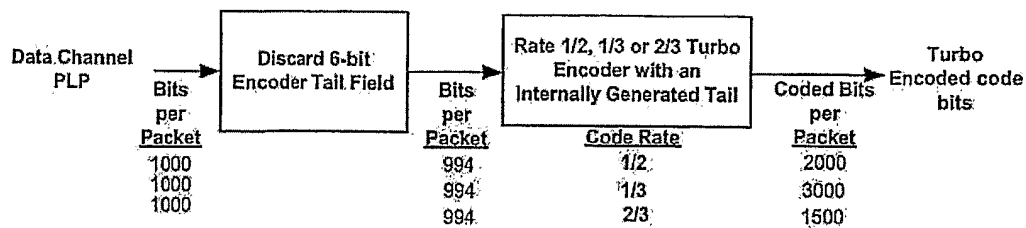
52

Figure 5.2.1.2.9.6.1.1-1 Data Channel Encoder

Table 5.2.1.2.9.6.1.1-1 Parameters of the Data Channel Encoder

Bits	Turbo Encoder Input Bits N_{turbo}	Code Rate	Turbo Encoder Output bits
1000	994	1/2	2000
1000	994	1/3	3000
1000	994	2/3	1500

5.2.1.2.9.6.1.1.1 Turbo Encoder

The turbo encoder used for Wide-area Data Channel Physical layer packets shall be as specified in 5.2.1.2.9.2.1.1.

The encoded data output bits are generated by clocking the constituent encoders N_{turbo} times with the switches in the up positions and puncturing the output as specified in Table 5.2.1.2.9.6.1.1.1-1. Within a puncturing pattern, a '0' means that the bit shall be deleted and a '1' means that the bit shall be passed. The constituent encoder outputs for each bit period shall be passed in the sequence X, Y_0, Y_1, X', Y'_0, Y'_1 with the X output first. Bit repetition is not used in generating the encoded data output symbols.

The constituent encoder output symbol puncturing for the tail period shall be as specified in Table 5.2.1.2.9.6.1.1.1-2. Within a puncturing pattern, a '0' means that the symbol shall be deleted and a '1' means that a symbol shall be passed.

For rate 1/2 turbo codes, the tail output code bits for each of the first three tail bit periods shall be XY_0, and the tail output code bits for each of the last three tail bit periods shall be $X'Y'_0$.

For rate 1/3 turbo codes, the tail output code bits for each of the first three tail bit periods shall be XXY_0, and the tail output code bits for each of the last three tail bit periods shall be $X' X'Y'_0$.

For rate 2/3 turbo codes, the tail output code bits for the first three tail bit periods shall be XY_0, X and XY_0 respectively. The tail output code bits for the last three tail bit periods shall be X', $X'Y'_0$ and X', respectively.

Table 5.2.1.2.9.6.1.1.1-1 Puncturing Patterns for the Data Bit Periods

Output	Code Rate		
	1/2	1/3	2/3
X	11	11	1111
Y_0	10	11	1000
Y_1	00	00	0000
X'	00	00	0000
Y'_0	01	11	0001
Y'_1	00	00	0000

Note: The puncturing table is to be read
from top to bottom.

Table 5.2.1.2.9.6.1.1.1-2 Puncturing Patterns for the Tail Bit Periods

Output	Code Rate		
	1/2	1/3	2/3
X	111 000	111 000	111 000
Y_0	111 000	111 000	101 000
Y_1	000 000	000 000	000 000
X'	000 111	000 111	000 111
Y'_0	000 111	000 111	000 010
Y'_1	000 000	000 000	000 000

Note: For rate-1/2 turbo codes, the puncturing table is to be read
first from top to bottom and then from left to right. For Rate 1/3
turbo code, the puncturing table is to be read from top to bottom
repeating X and X', and then from left to right. For rate-2/3 turbo
codes, the puncturing table is to be read first from top to bottom
and then from left to right.

5.2.1.2.9.6.1.1.2 Turbo Interleaver

The turbo interleaver for the Wide-area Data Channel shall be as specified in
5.2.1.2.9.2.1.2.

5.2.1.2.9.6.1.2 Bit Interleaving

The Wide-area Data Channel turbo encoded packets shall be bit interleaved as specified in
5.2.1.2.9.2.2.

54

1   5.2.1.2.9.6.1.3 Data Slot Allocation

2   For the Wide-area Data Channel, up to 7 data slots may be allocated per OFDM symbol for
3   the transmission of multiple turbo encoded packets associated with one or more MLCs. For
4   certain modes (2, 4, 8 and 11, see Table 5.2.1.2.8-1) a turbo encoded packet occupies a
5   fraction of a slot. However, slots are allocated to MLCs in a manner that avoids multiple
6   MLCs sharing slots within the same OFDM symbol.

7   5.2.1.2.9.6.1.4 Filling of Data Slot Buffers

8   The bit-interleaved code bits of a Wide-area Data Channel turbo encoded packet shall be
9   written into one or more data slot buffers. These data slot buffers correspond to slot indices
10 1 through 7.

11 The data slot buffer size shall be 1000 bits for QPSK and 2000 bits for 16-QAM and layered
12 modulation.

13 For QPSK and 16-QAM modulation, the bit-interleaved code bits shall be sequentially
14 written into the slot buffer(s).

15 For layered modulation, the bit-interleaved code bits corresponding to the base and the
16 enhancement components shall be interleaved as illustrated in Figure 5.2.1.2.9.6.1.4-1,
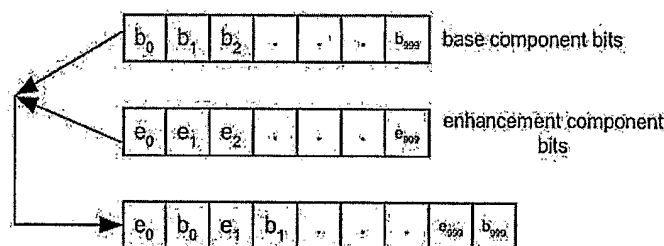17 prior to filling the slot buffer(s).

18

20 **Figure 5.2.1.2.9.6.1.4-1 Interleaving of Base and Enhancement component bits for**
21 **Filling the Slot Buffer for Layered Modulation**

22 Figure 5.2.1.2.9.6.1.4-2 illustrates the case where a single turbo encoded packet spans
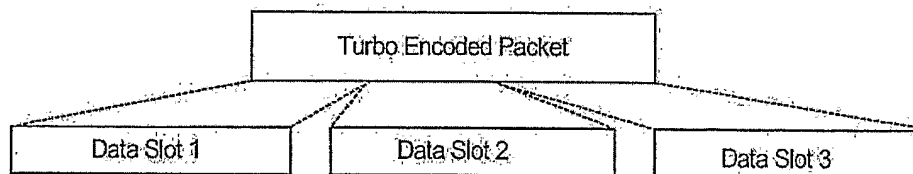23 three data slot buffers.

25 **Figure 5.2.1.2.9.6.1.4-2 A Data Channel Turbo Encoded Packet occupying three Data**
26 **Slot Buffers**

27 Figure 5.2.1.2.9.6.1.4-3 illustrates the case where a base component turbo encoded packet
28 with code rate 1/3 is multiplexed with an enhancement component turbo packet (with the
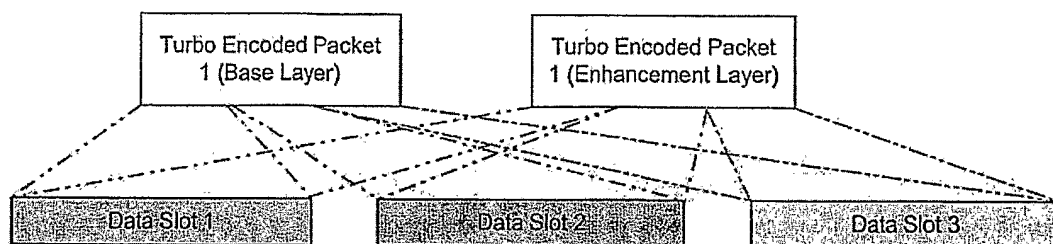29 same code rate) to occupy 3 data slot buffers.

Figure 5.2.1.2.9.6.1.4-3 Multiplexing of Base and Enhancement Component Turbo
Encoded packets occupying three Data Slot Buffers

Figure 5.2.1.2.9.6.1.4-4 illustrates the case where a Data Channel turbo encoded packet
occupies a fraction of a data slot and four turbo encoded packets are required to fill up an
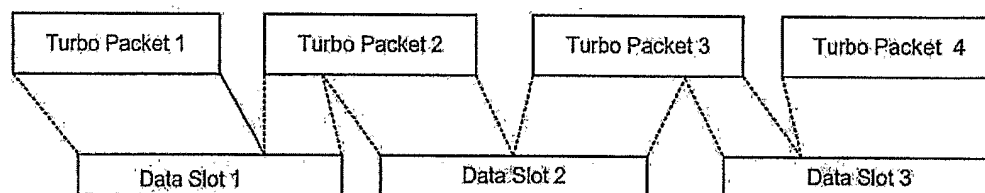integer number of data slots.

Figure 5.2.1.2.9.6.1.4-4 4 Data Channel Turbo Encoded Packet Occupying 3 Data Slot
Buffers

The three slots in the figure may span one OFDM symbol or multiple consecutive OFDM
symbols. In either case, the data slot allocation over an OFDM symbol for an MLC shall
have consecutive slot indices.

Figure 5.2.1.2.9.6.1.4-5 illustrates a snapshot of slot allocations to five different MLCs over
three consecutive OFDM symbols in a frame. In the figure, TEP n,m denotes n^{th} turbo
encoded packet for the mth MLC. In that figure,

* MLC 1 uses transmit mode 0 and requires three slots for each turbo encoded
  packet. It uses 3 consecutive OFDM symbols to send one turbo encoded packet.

* MLC 2 uses transmit mode 1 and utilizes 2 slots to transmit a single turbo encoded
  packet. It uses OFDM symbols n and n+1, to send two turbo encoded packets.

* MLC 3 uses transmit mode 2 and requires 1.5 slots for transmitting one turbo
  encoded packet. It uses three consecutive OFDM symbols to transmit 6 turbo
  encoded packets.

* MLC 4 uses transmit mode 1 and requires 2 slots to transmit a single turbo
  encoded packet. It uses 2 consecutive OFDM symbols to send two turbo encoded
  packets.

* MLC 5 uses transmit mode 3 and requires 1 slot to transmit a turbo encoded
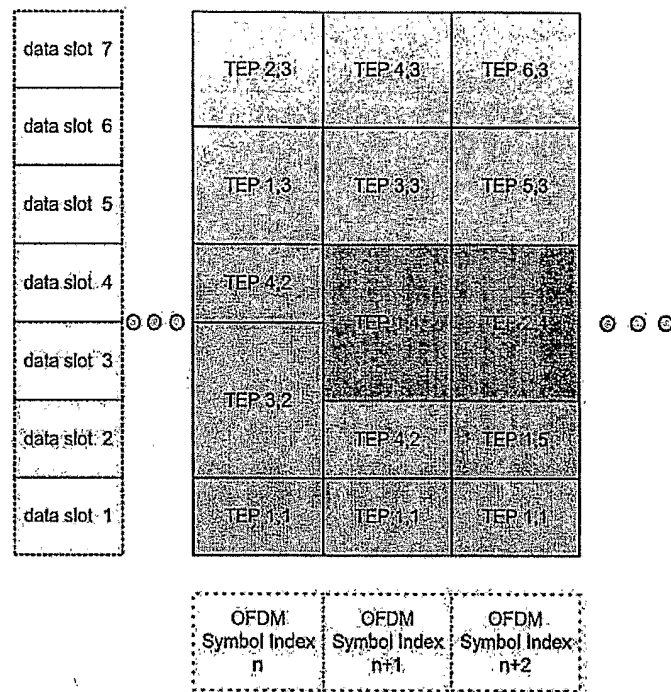 packet. It uses one OFDM symbol to send a turbo encoded packet.

Figure 5.2.1.2.9.6.1.4-5 Slot Allocation to Multiple MLCs over 3 consecutive OFDM Symbols in a Frame

5.2.1.2.9.6.1.5 Slot Scrambling

The bits of each allocated slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

5.2.1.2.9.6.1.6 Mapping of Bits to Modulation Symbols

For the Wide-area Data Channel, depending on the transmit mode, either QPSK, 16-QAM or Layered Modulation may be used.

5.2.1.2.9.6.1.6.1 QPSK Modulation

Each group of two consecutive bits from the ith scrambled slot buffer, SB(i,2k) and SB(i,2k + 1), i=1,2...7, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table 5.2.1.2.9.1.1.3-1 with D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

5.2.1.2.9.6.1.6.2 16-QAM Modulation

Each group of four consecutive bits from the ith scrambled data slot buffer, SB(i,4k), SB(i,4k+1), SB(i, 4k+2) and SB(i,4k+3), i=1,2,...7, k = 0,1,...499 shall be grouped and mapped to a 16-QAM complex modulation symbol S(k)= $(m_I(k), m_Q(k))$, k = 0,1,...499 as specified in Table 5.2.1.2.9.6.1.6.2-1 with A = $1/\sqrt{10}$. Figure 5.2.1.2.9.6.1.6.2-1 shows the

1   signal constellation of the 16-QAM modulator, where s_0=SB(i,4k), s_1=SB(i,4k+1),
2   s_2=SB(i,4k+2), and s_3 = SB(i,4k + 3).

3   **Table 5.2.1.2.9.6.1.6.2-1 16-QAM Modulation Table**

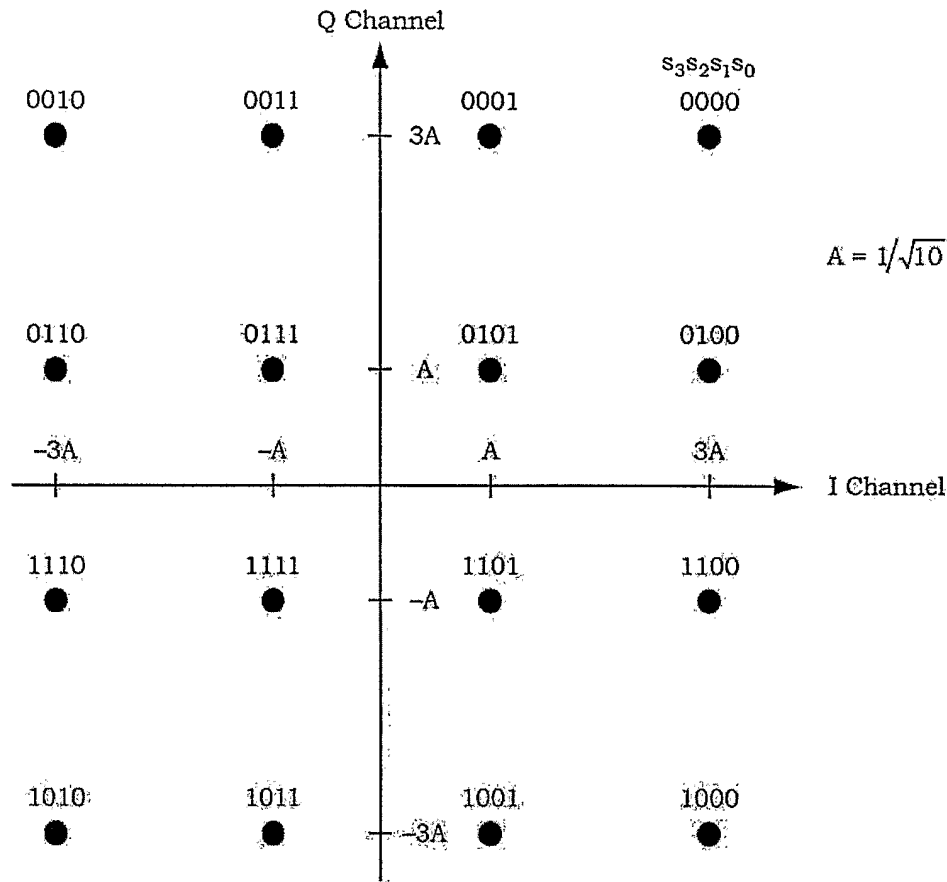| Interleaved Bits				Modulation Symbols	
s_3 SB(i,4k + 3)	s_2 SB(i,4k + 2)	s_1 SB(i,4k + 1)	s_0 SB(i,4k)	$m_Q(k)$	$m_I(k)$
0	0	0	0	3A	3A
0	0	0	1	3A	A
0	0	1	1	3A	−A
0	0	1	0	3A	−3A
0	1	0	0	A	3A
0	1	0	1	A	A
0	1	1	1	A	−A
0	1	1	0	A	−3A
1	1	0	0	−A	3A
1	1	0	1	−A	A
1	1	1	1	−A	−A
1	1	1	0	−A	−3A
1	0	0	0	−3A	3A
1	0	0	1	−3A	A
1	0	1	1	−3A	−A
1	0	1	0	−3A	−3A

4

58

Figure 5.2.1.2.9.6.1.6.2-1 Signal Constellation for 16-QAM Modulation

5.2.1.2.9.6.1.6.3 Layered Modulation with Base and Enhancement Components

Each group of four consecutive bits from the ith scrambled data slot buffer, SB(i,4k), SB(i,4k+1), SB(i,4k+2) and SB(i,4k+3), i=1,2,...7, k = 0,1,...499 shall be grouped and mapped to a layered modulation complex symbol S(k)= $(m_I(k), m_Q(k))$, k = 0,1,...499 as specified in Table 5.2.1.2.9.6.1.6.3-1. If r denotes the energy ratio between the base component and the enhancement component, then α and β shall be given by:

$$\alpha = \sqrt{\frac{r}{2(1+r)}} \text{ and } \beta = \sqrt{\frac{1}{2(1+r)}} \text{ (see Table 5.2.1.2.6-1).}$$

Figure 5.2.1.2.9.6.1.6.3-1 shows the signal constellation for the layered modulation, where s_0=SB(i,4k), s_1=SB(i,4k+1), s_2=SB(i,4k+2), and s_3 = SB(i,4k + 3). It should be noted that the procedure for filling the slot buffer(s) ensures (see Figure 5.2.1.2.9.6.1.4-1) that bits s_0 and s_2 correspond to the enhancement component and bits s_1 and s_3 correspond to the base component.

59

Table 5.2.1.2.9.6.1.6.3-1 Layered Modulation Table

Interleaved Bits				Modulation Symbols	
s_3 SB(i,4k + 3)	s_2 SB(i,4k + 2)	s_1 SB(i,4k + 1)	s_0 SB(i,4k)	$m_Q(k)$	$m_I(k)$
0	0	0	0	$\alpha+\beta$	$\alpha+\beta$
0	0	0	1	$\alpha+\beta$	$\alpha-\beta$
0	0	1	1	$\alpha+\beta$	$-\alpha+\beta$
0	0	1	0	$\alpha+\beta$	$-\alpha-\beta$
0	1	0	0	$\alpha-\beta$	$\alpha+\beta$
0	1	0	1	$\alpha-\beta$	$\alpha-\beta$
0	1	1	1	$\alpha-\beta$	$-\alpha+\beta$
0	1	1	0	$\alpha-\beta$	$-\alpha-\beta$
1	1	0	0	$-\alpha+\beta$	$\alpha+\beta$
1	1	0	1	$-\alpha+\beta$	$\alpha-\beta$
1	1	1	1	$-\alpha+\beta$	$-\alpha+\beta$
1	1	1	0	$-\alpha+\beta$	$-\alpha-\beta$
1	0	0	0	$-\alpha-\beta$	$\alpha+\beta$
1	0	0	1	$-\alpha-\beta$	$\alpha-\beta$
1	0	1	1	$-\alpha-\beta$	$-\alpha+\beta$
1	0	1	0	$-\alpha-\beta$	$-\alpha-\beta$

Note: $\alpha = \sqrt{\dfrac{r}{2(1+r)}}$, $\beta = \sqrt{\dfrac{1}{2(1+r)}}$, where r is the ratio of the base component energy to the enhancement component energy.
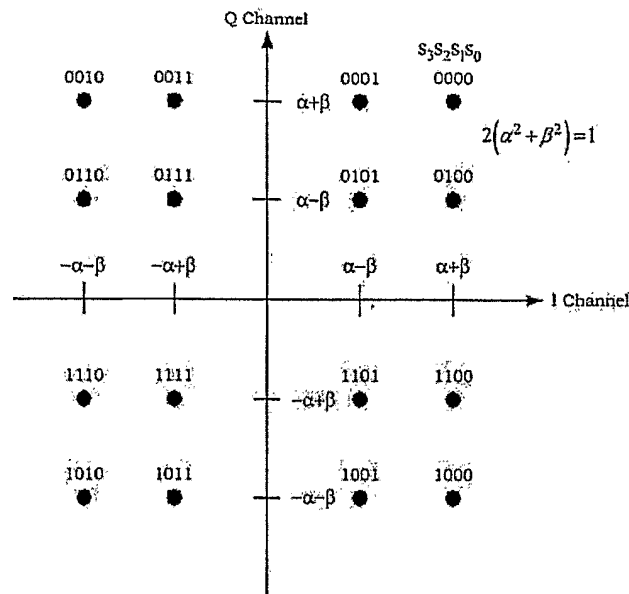
Figure 5.2.1.2.9.6.1.6.3-1 Signal Constellation for Layered Modulation

5.2.1.2.9.6.1.6.4 Layered Modulation with Base Component Only

The 2nd and 4th bits from each group of four consecutive bits from the ith scrambled slot buffer, SB(i, 4k+1) and SB(i, 4k + 3), i = 1,2,...7, k = 0,1,...499, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol MS= (m_I, m_Q) as specified in Table 5.2.1.2.9.1.1.3-1 with D = $1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

5.2.1.2.9.6.1.7 Slot to Interlace Mapping

The mapping of slots to interlaces for the Wide-area Data Channel OFDM symbols shall be as specified in 5.2.1.2.10.

5.2.1.2.9.6.1.8 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

The 500 modulation symbols in each allocated slot shall be sequentially assigned to 500 interlace sub-carriers using the procedure specified in 5.2.1.2.9.2.8.

5.2.1.2.9.6.1.9 OFDM Common Operation

The modulated Wide-area Data Channel sub-carriers shall undergo common operation specified in 5.2.1.2.11.

5.2.1.2.9.6.2 Wide-area Data Channel Processing for Unallocated Slots

The unallocated slots in the Wide-area Data Channel use as input a 1000-bit fixed pattern, with each bit set to zero. These bits shall be processed according to the steps illustrated in Figure 5.2.1.2.9.1.2-1.

5.2.1.2.9.6.2.1 Filling of Slot Buffer

The buffer for each unallocated slot of the Wide-area Data Channel shall be completely filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'.

5.2.1.2.9.6.2.2 Slot Scrambling

The bits of each unallocated slot buffer in the Wide-area Data Channel shall be scrambled as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

5.2.1.2.9.6.2.3 Modulation Symbol Mapping

Each group of two consecutive bits from the ith scrambled slot buffer, $SB(i,2k)$ and $SB(i,2k + 1)$, $i=1,2,...7$, $k = 0,1,...499$, which are labeled as s_0 and s_1, respectively, shall be mapped into a complex modulation symbol $MS = (m_I, m_Q)$ as specified in Table 5.2.1.2.9.1.1.3-1 with $D = 1/\sqrt{2}$. Figure 5.2.1.2.9.1.1.3-1 shows the signal constellation for the QPSK modulation.

5.2.1.2.9.6.2.4 Slot to Interlace Mapping

The mapping of slots to interlaces for the unallocated slots in the Wide-area Data Channel OFDM symbol shall be as specified in 5.2.1.2.10

5.2.1.2.9.6.2.5 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

The 500 modulation symbols in the slot buffer shall be sequentially assigned to 500 interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$) shall be mapped to the ith sub-carrier of that interlace.

5.2.1.2.9.6.2.6 OFDM Common Operation

This modulated Wide-area Data Channel OFDM symbol sub-carriers shall undergo common operations as specified in 5.2.1.2.11.

5.2.1.2.9.7 Local-area Data Channel

The Local-area Data Channel is used to carry Physical layer packets meant for Local-area multicast. The Physical layer packets for the Local-area Data Channel can be associated with any one of the active MLCs transmitted in the Local-area.

5.2.1.2.9.7.1 Local-area Data Channel Processing for Allocated Slots

The Physical layer packet for the Local-area Data Channel shall be processed according to the steps illustrated in Figure 5.2.1.2.9.6.1-1.

For regular modulation (QPSK and 16-QAM), the physical layer packet is turbo-encoded and bit interleaved before being stored in the Data slot buffer(s). For layered modulation, the base-component Physical layer packet and the enhancement-component Physical layer packet are turbo-encoded and bit interleaved independently before being multiplexed in to the Data slot buffer(s).

1   5.2.1.2.9.7.1.1 Encoding

2   The Local-area Data Channel Physical layer packets shall be encoded with code rates R =
3   1/3, ½, or 2/3. The encoding procedure shall be identical to that for the Wide-area Data
4   Channel as specified in 5.2.1.2.9.6.1.1.

5   5.2.1.2.9.7.1.2 Bit Interleaving

6   The Local-area Data Channel turbo encoded packet shall be bit interleaved as specified in
7   5.2.1.2.9.2.2.

8   5.2.1.2.9.7.1.3 Data Slot Allocation

9   For the Local-area Data Channel, the slot allocation shall be as specified in 5.2.1.2.9.6.1.3.

10   5.2.1.2.9.7.1.4 Filling of Data Slot Buffers

11   The procedure for filling the slot buffer for the Local-area Data Channel shall be as
12   specified in 5.2.1.2.9.6.1.4.

13   5.2.1.2.9.7.1.5 Slot Scrambling

14   The bits of each allocated slot buffer shall be scrambled as specified in 5.2.1.2.9.1.2.3. The
15   scrambled slot buffer is denoted by SB.

16   5.2.1.2.9.7.1.6 Mapping of Slot Bits to Modulation Symbols

17   For the Local-area Data Channel, depending on the transmit mode QPSK, 16-QAM or
18   Layered Modulation may be used.

19   5.2.1.2.9.7.1.6.1 QPSK Modulation

20   Each group of two consecutive bits from the scrambled slot buffer shall be mapped in to a
21   QPSK modulation symbol as specified in 5.2.1.2.9.6.1.6.1.

22   5.2.1.2.9.7.1.6.2 16-QAM Modulation

23   Each group of four consecutive bits from the scrambled slot buffer shall be mapped in to a
24   16-QAM modulation symbol as specified in 5.2.1.2.9.6.1.6.2.

25   5.2.1.2.9.7.1.6.3 Layered Modulation with Base and Enhancement Components

26   Each group of four consecutive bits from the scrambled slot buffer shall be mapped in to a
27   layered modulation symbol as specified in 5.2.1.2.9.6.1.6.3.

28   5.2.1.2.9.7.1.6.4 Layered Modulation with Base Component Only

29   The 2nd and 4th bits from each group of four consecutive bits from the scrambled slot buffer
30   shall be mapped into a QPSK modulation symbol as specified in 5.2.1.2.9.6.1.6.4.

31   5.2.1.2.9.7.1.7 Slot to Interlace Mapping
32   The mapping of slots to interlaces for Local-area Data Channel OFDM symbols shall be as
33   specified in 5.2.1.2.10.

1   5.2.1.2.9.7.1.8 Mapping of Slot Modulation Symbols to Interlace Sub-carriers

2   The 500 modulation symbols in each allocated slot shall be sequentially assigned to 500
3   interlace sub-carriers using the procedure specified in 5.2.1.2.9.2.8.

4   5.2.1.2.9.7.1.9 OFDM Common Operation

5   The modulated Wide-area Data Channel sub-carriers shall undergo common operations as
6   specified in 5.2.1.2.11.

7   5.2.1.2.9.7.2 Local-area Data Channel Processing for Unallocated Slots

8   The unallocated slots in the Local-area Data Channel use as input a 1000-bit fixed pattern,
9   with each bit set to zero. These bits shall be processed according to the steps illustrated in
10 Figure 5.2.1.2.9.1.2-1.

11 5.2.1.2.9.7.2.1 Filling of Slot Buffers

12 The buffer for each unallocated slot of the Local-area Data Channel shall be completely
13 filled with a fixed pattern consisting of 1000 bits, with each bit set to '0'.

14 5.2.1.2.9.7.2.2 Slot Scrambling

15 The bits of each unallocated slot buffer in the Wide-area Data Channel shall be scrambled
16 as specified in 5.2.1.2.9.1.2.3. The scrambled slot buffer is denoted by SB.

17 5.2.1.2.9.7.2.3 Modulation Symbol Mapping

18 Each group of two consecutive bits from the scrambled slot buffer shall be mapped in to a
19 QPSK modulation symbol as specified in 5.2.1.2.9.6.2.3.

20 5.2.1.2.9.7.2.4 Slot to Interlace Mapping

21 The mapping of slots to interlaces for the unallocated slots in the Local-area Data Channel
22 OFDM symbol shall be as specified in 5.2.1.2.10

23 5.2.1.2.9.7.2.5 Mapping of Slot Buffer Modulation Symbols to Interlace Sub-carriers

24 The 500 modulation symbols in the slot buffer shall be sequentially assigned to 500
25 interlace sub-carriers as follows: the ith complex modulation symbol (where $i \in \{0,1,...499\}$)
26 shall be mapped to the ith sub-carrier of that interlace.

27 5.2.1.2.9.7.2.6 OFDM Common Operation

28 This modulated Local-area Data Channel OFDM symbol sub-carriers shall undergo
29 common operations as specified in 5.2.1.2.11.

30 5.2.1.2.10 Mapping of Slots to Interlaces

31 The slot to interlace mapping varies from one OFDM symbol to the next as specified in this
32 section.

33 There are 8 slots in every OFDM symbol.

64

1   The FDM Pilot Channel shall utilize slot 0. Slot 0 shall be assigned interlace $I_p[j]$ for OFDM
2   symbol index j in a superframe as follows:

3   • if (j mod 2 = 0), then $I_p[j]$ = 2.

4   • Otherwise, $I_p[j]$ = 6

5   The interlace assignment procedure for slot 0 ensures that the FDM Pilot Channel is
6   assigned interlace 2 and 6 for even and odd OFDM symbol indices respectively. The
7   remaining 7 interlaces in each OFDM symbol are assigned to slots 1 through 7. This is
8   illustrated in Figure 5.2.1.2.10-1, where P and D denote the interlaces assigned to the slots
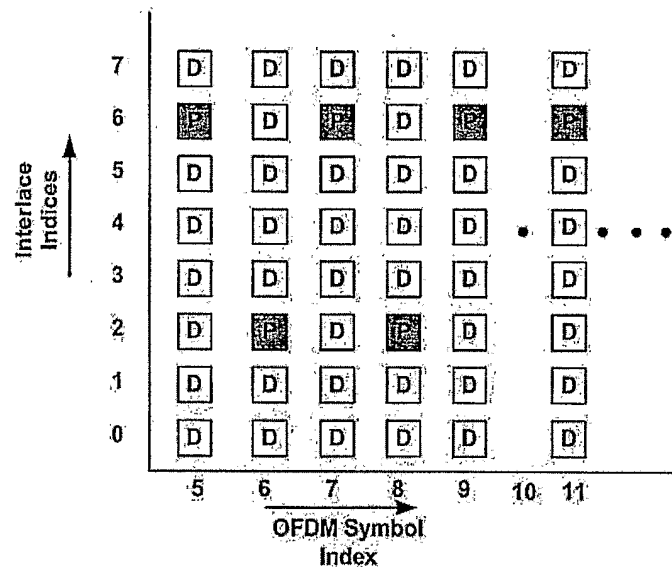9   occupied by the FDM Pilot Channel and the Data Channel, respectively.

10
11   Figure 5.2.1.2.10-1 Interlace Allocations to FDM Pilots

12   The slot to interlace mapping for slots 1 though 7 shall be as follows:

13   1. Let i be the 3-bit value of the interlace index i ($i \in \{0,7\}$). Denote the bit-reversed
14   value of i as i_{br}.

15   2. Let I_j denote the jth interlace as defined in 5.2.1.2.2.4. Permute the interlace
16   sequence $\{I_0 I_1 I_2 I_3 I_4 I_5 I_6 I_7\}$ by replacing the index i ($i \in \{0,7\}$) in I_i with i_{br} to generate
17   the permuted sequence, $PS=\{I_0 I_4 I_2 I_6 I_1 I_5 I_3 I_7\}$.

18   3. Club interlaces[39] I_2 and I_6 in the PS to generate shortened interlace sequence, SIS =
19           $\{I_0 I_4 I_2/I_6 I_1 I_5 I_3 I_7\}$.

20   4. For the OFDM symbol with index j ($j \in \{1,1199\}$)[40] in a superframe, perform a right
21   hand cyclic shift[41] on SIS in step 3, by a value equal to ($2 \times j$) mod 7 to generate the
22   permuted shortened interlace sequence PSIS(j).

---

39 Since interlaces 2 and interlace 6 are used alternatively for the pilot, the remaining seven
interlaces are used for assignment to data slots.

1   5. If (j mod 2 = 0), then choose interlace I₆ in the PSIS(j). Otherwise, choose I₂ in the
2   PSIS[j].

3   6. For the jᵗʰ OFDM symbol interval in a superframe, the kᵗʰ data slot (for
4   k ∈ {1,...7}) shall be assigned the interlace PSIS(j)[k-1].

5   Figure 5.2.1.2.10-2 illustrates the interlace assignment to all 8 slots over 15 consecutive
6   OFDM symbol intervals. The mapping pattern from slots to interlaces repeats after 14
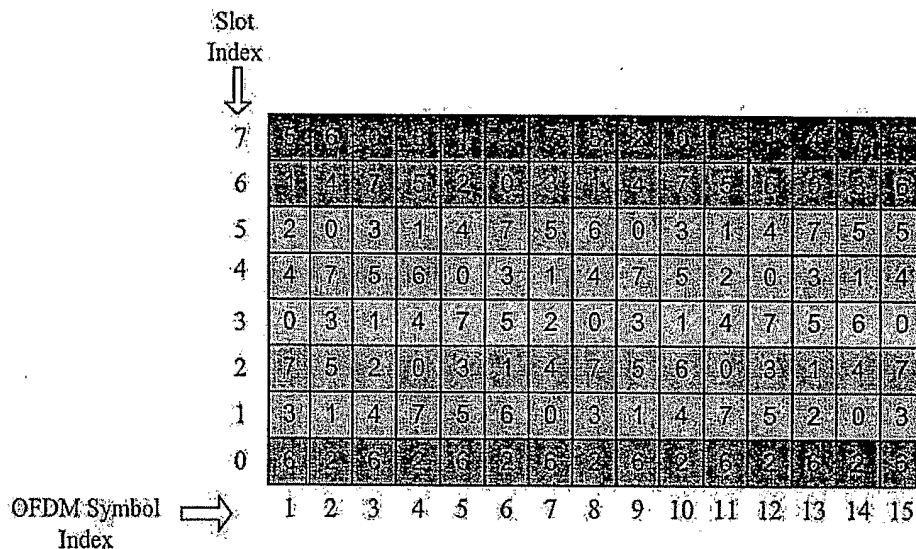7   consecutive OFDM symbol intervals[42],

Figure 5.2.1.2.10-2 Interlace Allocations to Slots

10 5.2.1.2.11 OFDM Common Operation

11 This block transforms the complex modulation symbols $X_{k,m}$, associated with sub-carrier
12 index k for OFDM symbol interval m, into the RF transmitted signal. The operations are
13 illustrated in Figure 5.2.1.2.11-1.

---

[40] A super-frame spans 1200 OFDM symbol intervals. Slot to interlace mapping for OFDM symbol index 0 is not used.

[41] Right hand cyclic shift of the sequence s = {1 2 3 4 5} by 2 yields the sequence s(2) = {4 5 1 2 3}.

[42] The figure shows that all interlaces get assigned next to the Pilot interlace about the same fraction of time, and the channel estimation performance for all interlaces is about the same.
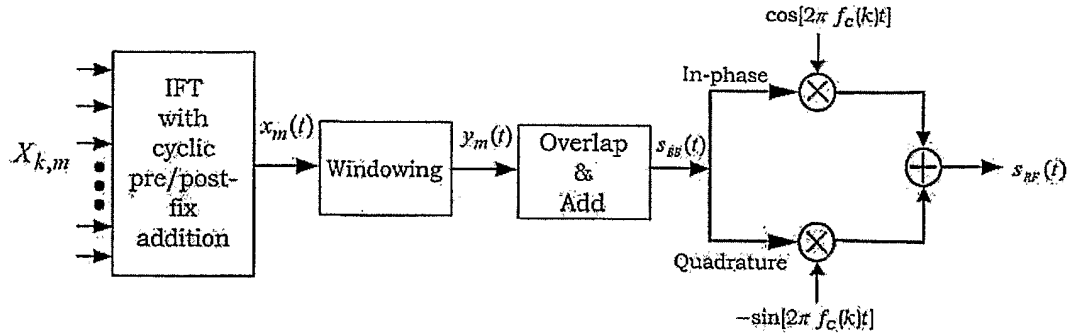
66

Figure 5.2.1.2.11-1 OFDM Common Operation

5.2.1.2.11.1 IFT Operation

The complex modulation symbols $X_{k,m}, k = 0,1,...,4095,$ associated with the mth OFDM symbol shall be related to the continuous-time signal $x_m(t)$ by the inverse Fourier Transform (IFT) equation. Specifically,

$$x_m(t) = \frac{1}{N} \sum_{k=0}^{N-1} X_{k,m}\, e^{j2\pi(\Delta f)_{SC}(k-\frac{N}{2})(t-T_{WGI}-T_{FGI})} ,\text{ for } 0 \le t \le T_s'.$$

In the above equation, $(\Delta f)_{SC}$ is the sub-carrier spacing (see 5.2.1.2.2.2), while T_{WGI}, T_{FGI} and T_s' are defined in 5.2.1.2.3.

5.2.1.2.11.2 Windowing

The signal $x_m(t)$ shall be multiplied by the window function $w(t)$, where

$$w(t) = \begin{cases} 0.5 + 0.5\cos(\pi + \pi\, t/T_{WGI}) & 0 \le t \le T_{WGI} \\ 1 & T_{WGI} < t \le (T_{WGI} + T_{FGI} + T_U) \\ 0.5 + 0.5\cos(\pi + \pi\,(T_s'-t)/T_{WGI}) & (T_{WGI} + T_{FGI} + T_U) \le t \le (2\,T_{WGI} + T_{FGI} + T_U) \end{cases}$$

The windowed signal is denoted by $y_m(t)$, where

$$y_m(t) = x_m(t)\, w(t).$$

In the above, T_U and T_s are as defined in 5.2.1.2.3.

5.2.1.2.11.3 Overlap and Add

The base-band signal $s_{BB}(t)$ shall be generated by overlapping the windowed, continuous-time signals from successive OFDM symbols by T_{WGI}. This is illustrated in Figure 5.2.1.2.11.3-1. Specifically, $s_{BB}(t)$ is given by

$$s_{BB}(t) = \sum_{m=-\infty}^{\infty} y_m(t - mT_s)$$

67
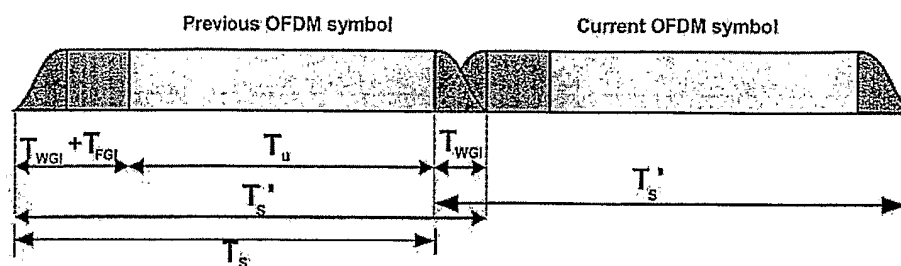
Figure 5.2.1.2.11.3-1 Overlap of Windowed OFDM Symbols

5.2.1.2.11.4 Carrier Modulation

The in-phase and quadrature base-band signals shall be up-converted to RF frequency and summed to generate the RF waveform $s_{RF}(t)$. In Figure 5.2.1.2.11-1, $f_c(k)$ is the centre frequency of the kth FLO RF channel (see Table 5.2.1.1.1-1).

5.2.1.3 Synchronization and Timing

To be provided.

5.2.1.3.1 Timing Reference Source

To be provided.

5.2.1.3.2 FLO network transmission time

To be provided.

68

CLAIMS

1.   A method for interleaving, comprising:

inter-interleave subcarriers of an interlace; and

intra-interleave the interlaces.

2.   The method of claim 1, wherein the number of subcarriers is 500.

3.   The method of claim 2, wherein the number of interlaces is eight.

4.   The method of claim 1, wherein the inter-interleave subcarriers of an interlace involves mapping symbols of a constellation symbol sequence into corresponding subcarriers in a sequential linear fashion according to an assigned slot index using an interlace table.

5.   A processor configured to:

interleave subcarriers of an interlace; and

interleave the interlaces.

6.   A processor, comprising:

means for interleaving subcarriers of an interlace; and

means for interleaving the interlaces.

7.   A readable media embodying a method for interleaving, comprising:

interleaving subcarriers of an interlace; and
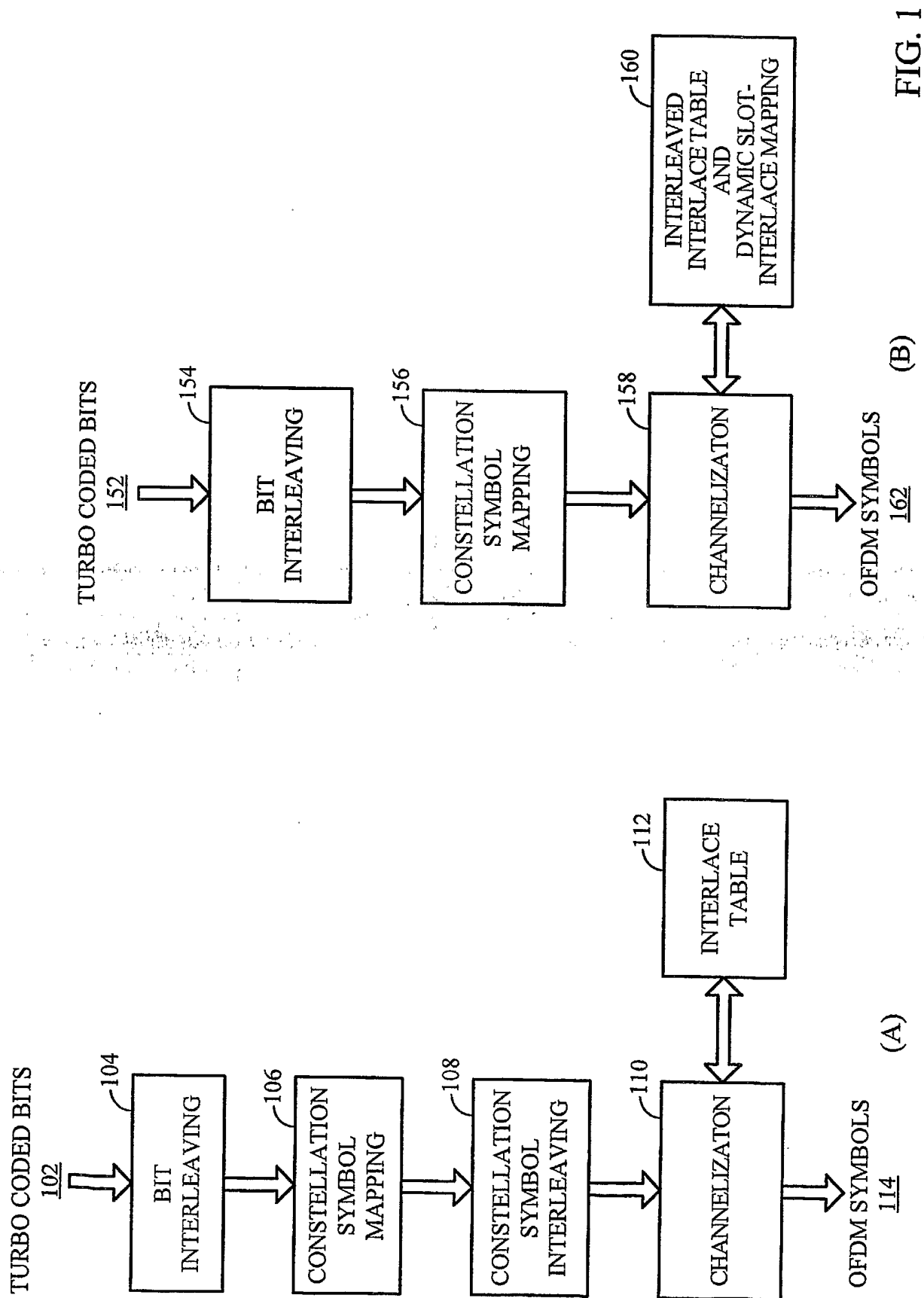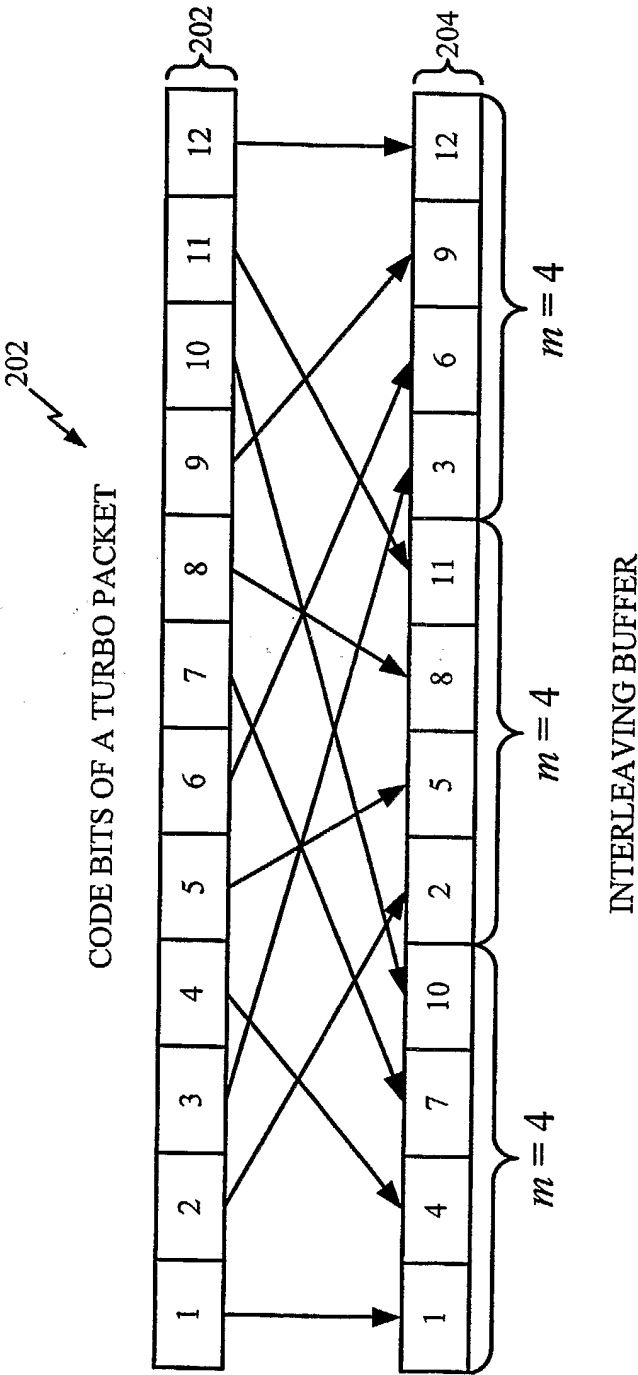
interleaving the interlaces.

FIG. 1

FIG. 2A

FIG. 2B

FIG. 3

⋮

Slot Index \ OFDM Symbol Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
7	7	[7]	7	[7]	7	[7]	7	[7]	7	[7]	7	[7]	7	[7]	7	[7]	7
6	[3]	3	[3]	3	[3]	3	[3]	3	[3]	3	[3]	3	[3]	3	[3]	3	[3]
5	5	[5]	5	[5]	5	[5]	5	[5]	5	[5]	5	[5]	5	[5]	5	[5]	5
4	[1]	1	[1]	1	[1]	1	[1]	1	[1]	1	[1]	1	[1]	1	[1]	1	[1]
3	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6	2/6
2	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4	4
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	2	6	2	6	2	6	2	6	2	6	2	6	2	6	2	6	2

402 ⟶ SLOT INDEX

406 ⟶ RESERVED FOR SCHEDULER

408 ⟶ RESERVED FOR PILOT

404 OFDM SYMBOL INDEX

FIG. 4

FIG. 5

502 SLOT INDEX

506 RESERVED FOR SCHEDULER

508 RESERVED FOR PILOT

504 OFDM SYMBOL INDEX

⋮

Slot Index \ OFDM Symbol Index	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
7	7	[5]	2/6	0	[3]	1	4	[7]	5	2/6	0	3	[1]	4	7	[5]	2/6
6	[3]	1	4	[7]	5	2/6	0	3	[1]	4	7	[5]	2/6	0	[3]	1	4
5	5	2/6	0	3	[1]	4	7	[5]	2/6	0	[3]	1	4	[7]	5	2/6	0
4	[1]	4	7	[5]	2/6	0	[3]	1	4	[7]	5	2/6	0	3	[1]	4	7
3	2/6	0	[3]	1	4	[7]	5	2/6	0	3	[1]	4	7	[5]	2/6	0	[3]
2	4	[7]	5	2/6	0	3	[1]	4	7	[5]	2/6	0	[3]	1	4	[7]	5
1	0	3	[1]	4	7	[5]	2/6	0	[3]	1	4	[7]	5	2/6	0	3	[1]
0	2	6	2	6	2	6	2	6	2	6	2	6	2	6	2	6	2

602 → SLOT INDEX

606 → RESERVED FOR SCHEDULER (slot index 7–1)

608 → RESERVED FOR PILOT (slot index 0)

604 → OFDM SYMBOL INDEX

FIG. 6

FIG. 7