United States Patent

Hinrichs

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[54] ELECTRONIC COMBINATION DOOR AND IGNITION LOCK

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[52] **U.S. Cl.** .....**307/40**, 317/134, 180/114, 340/64, 307/10 AT, 307/247

[51] **Int. Cl.**.....**H02j 3/14**

[58] **Field of Search** .....317/134; 180/114, 112, 99; 340/63, 64, 147, 164, 164 A, 167, 274; 307/10 AT, 40, 218, 239, 247

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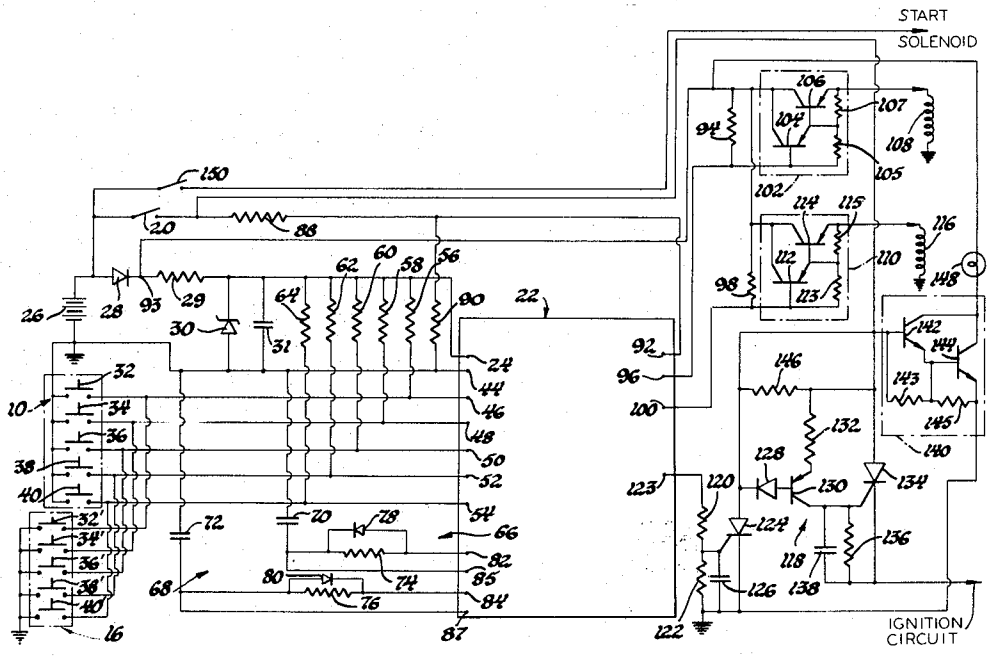
[57] **ABSTRACT**

A circuit is disclosed for unlocking the door and energizing the ignition circuit of a motor vehicle in response to manual insertion of a predetermined 5-digit code selected from a choice of four digits. The circuit includes a four stage solid state register, a six stage counter and logic gates which are interconnected to energize a door unlocking solenoid in response to insertion of the code in the proper sequence from a pushbutton keyboard unit located on the door of the vehicle. A five stage counter and additional logic means is provided which responds to actuation of any of the four digits out of sequence or to actuation of any digit not forming a part of the code to reset the two counters and the register. Upon entry into the vehicle and closure of the ignition switch, the last stage in the door unlocking logic is disabled and a parallel connected logic stage is enabled. The operator must then reinsert the code from a dash mounted pushbutton keyboard in the proper sequence to arm the ignition circuit.

3 Claims, 4 Drawing Figures



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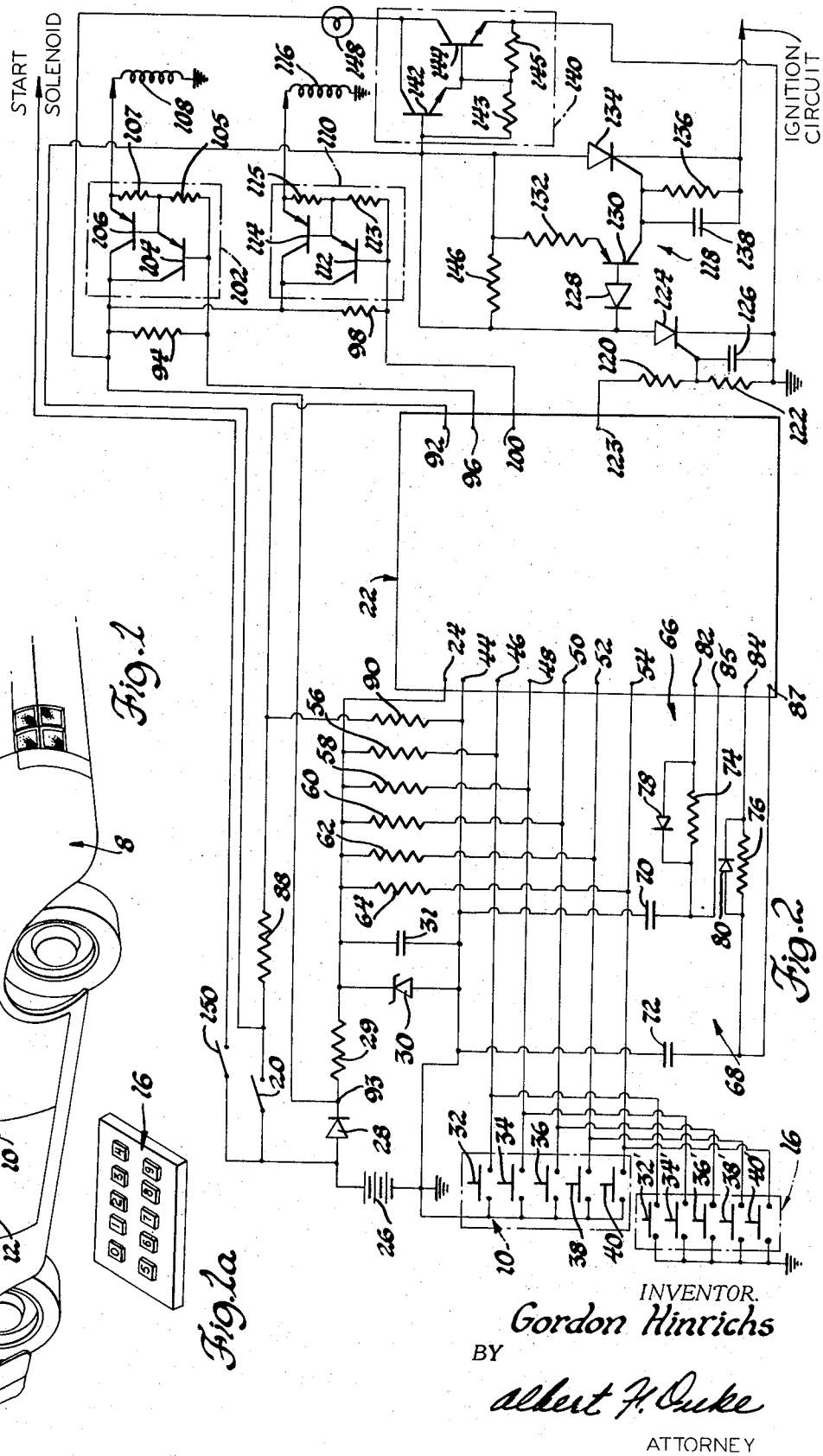

Fig. 1

Fig. 1a

Fig. 2

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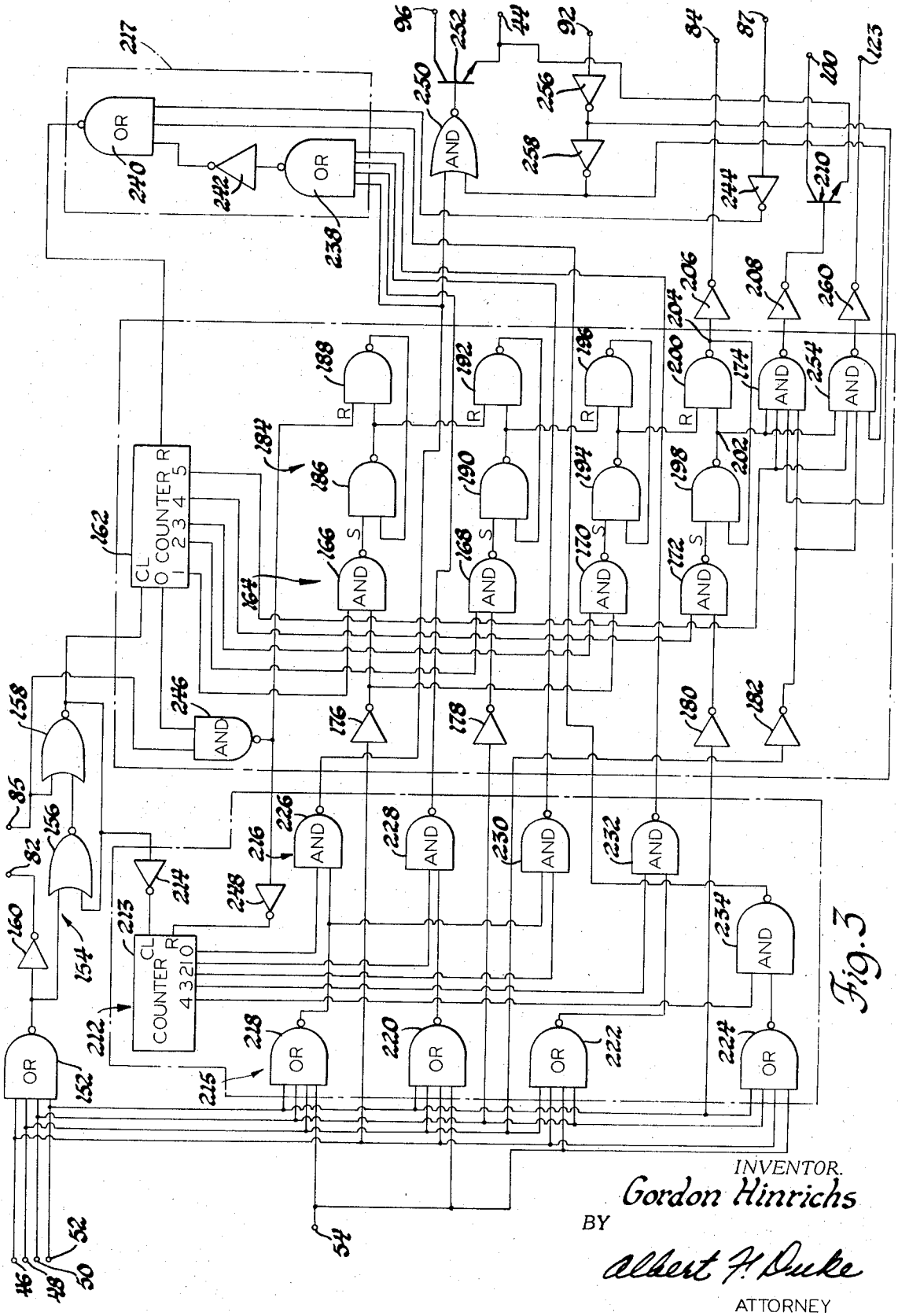

Fig. 3

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ELECTRONIC COMBINATION DOOR AND IGNITION LOCK

This invention relates to motor vehicle anti-theft apparatus and more particularly to an electronic combination door and ignition lock requiring proper insertion of a predetermined code containing repeating symbols in order to obtain entry to the vehicle and reinsertion of the code subsequent to entry in order to start the vehicle.

It is an object of the present invention to provide an improved electronic combination lock circuit which is capable of producing an output signal in response to insertion of a predetermined code containing repeating symbols and which is automatically reset in response to insertion of a sequence of symbols which is not in exact correspondence with the predetermined code.

It is another object of the present invention to provide an improved electronic combination door and ignition lock circuit for a motor vehicle which requires insertion of a predetermined code containing repeating symbols from a keyboard unit mounted on the exterior of the vehicle in order to obtain entry to the vehicle and requires reinsertion of the predetermined code from a pushbutton unit mounted within the vehicle in order to energize the ignition system of the vehicle.

It is another object of the present invention to provide an improved electronic combination lock circuit including means for overcoming the adverse effects of contact bounce associated with the input units for inserting the code.

In accordance with the present invention a door unlocking solenoid is energizable from circuitry responsive to insertion of a predetermined code containing x symbols selected from a choice of y symbols where in the specific example described $x = 5$ and $y = 4$. The code thus includes a repeating symbol. Each stage of a four stage register is sequentially set under the control of the first four of a first group of five gates which in turn are controlled from a pushbutton unit mounted on the exterior of the vehicle. The five gates are enabled sequentially from a first counter which is stepped from a monostable multivibrator which in turn is triggered by actuation of one of the pushbuttons in the pushbutton unit. The monostable multivibrator insures that the counter is stepped only once for each pushbutton actuated notwithstanding repeated contact closure due to contact bounce associated with pushbutton actuation. The fifth gate is also responsive to the output of the last stage of the register and controls the energization of the unlocking solenoid. A second counter, which is stepped from the multivibrator in responsive to release of the pushbutton actuated, sequentially enables a second group of five gates which are operative to reset the first and second counters and the register if any pushbutton is actuated out of sequence or if any pushbutton not forming a part of the code is actuated. A second pushbutton unit mounted on the interior of the vehicle provides a parallel input to the circuitry. Upon closure of the ignition switch and reinsertion of the proper code, the ignition circuit is energized and the vehicle may be started.

Other objects and features of the present invention will become apparent from the following detailed description which should be read in conjunction with the drawings in which:

FIG. 1 shows a portion of a motor vehicle provided with pushbutton units mounted on the exterior and interior of the vehicle;

FIG. 1*a* shows the interiorly mounted unit in more detail;

FIG. 2 is a schematic diagram of the present invention with portions thereof in block form;

FIG. 3 is a detailed schematic of the block portions of the diagram shown in FIG. 1.

Referring now to the drawings and initially to FIGS. 1 and 1*a*, a motor vehicle **8** is shown as having a pushbutton unit **10** mounted on the left front door **12** adjacent the door handle **14**. A second pushbutton unit **16** is shown as mounted on the dash **18** of the motor vehicle **8** adjacent the ignition switch (not shown). Each pushbutton unit **10** and **16** comprises two rows of five pushbuttons numbered 0–9.

The circuitry to be described in connection with FIGS. **2** and **3** is based on the premise that the code consists of five symbols or digits selected from a choice of four symbols thus requiring that at least one of the symbols be repeated. The particular code used for illustrative purposes is 13142.

In FIG. **2** a control circuit generally designated **22** is shown as having an input terminal **24** connected with a source of DC potential **26** through a diode **28** and a voltage dropping resistor **29**. The source **26** is preferably the vehicle battery and will hereinafter be referred to as such. A zener diode **30** and a parallel connected capacitor **31** regulate and filter the voltage appearing at the input terminal **24** of the control circuit **22**. The pushbutton unit **10** is shown as comprising four switches **32**, **34**, **36** and **38** which correspond to the pushbuttons bearing the numerals 1, 2, 3 and 4 respectively. The remaining pushbuttons 0 and 5–9 are schematically represented as a single pushbutton switch **40**. The switches **32** through **40** have one side connected to a ground terminal **44** and the other side connected to terminals **46** through **54** respectively of the control circuit **22** and are connected to the input terminal **24** through the resistors **56** through **64** respectively. The dash mounted pushboard unit **16** is identical to the door mounted pushbutton unit **10** and has its individual switches designated 32′–40′ connected in parallel with the switches **32–40** of the door mounted pushbutton unit **10**.

Time delay networks generally designated **66** and **68** are connected between terminals **82** and **84** respectively of control circuit **22** and ground. The network **66** comprises a capacitor **70** connected in series with parallel connected resistor **74** and diode **78**. The network **68** comprises a capacitor **72** connected in series with parallel connected resistor **76** and diode **80**. Terminal **85** and **87** of circuit **22** are connected respectively to junctions between capacitor **70**, resistor **74** and capacitor **72**, resistor **76**. The purpose of the time delay networks **66** and **68** will be fully described therein after in the detailed discussion of control circuit **22**.

An ignition switch **20** has one side connected to the positive terminal of the battery **26** and the other side connected to ground through a voltage dividing network comprising resistors **88** and **90**. The junction between the voltage dividing resistors **88** and **90** is connected to a terminal **92** of the control circuit **22**.

The junction between the diode **28** and the resistor **30** designated **93** is connected through a resistor **94** to a terminal **96** of the control circuit **22** and through a resistor **98** to a terminal **100** of the control circuit **22**. A drive circuit **102** comprising transistors **104, 106** and resistors **105, 107** is connected across the junctions **93** and terminal **96** for controlling energization of a door lock solenoid **108**. A drive circuit **110** is connected across the junction **93** and terminal **100** and comprises transistors **112, 114** and resistors **113, 115** for controlling energization of a door unlock solenoid **116**.

An ignition control circuit generally designated **118** is interposed between the ignition switch **20** and the ignition circuit of the vehicle (not shown) and includes voltage dividing resistors **120** and **122** connected between ground and an output terminal **123** of the control circuit **22**. An SCR **124** has its cathode connected to ground, its gate connected to ground through a capacitor **126** and its anode connected through a diode **128** to the base electrode of a transistor **130**. The emitter of transistor **130** is connected through a resistor **132** to the ignition switch **20** while its collector is connected to the gate electrode of an SCR **134**. The anode electrode of the SCR **134** is connected with the ignition switch **20** while the cathode electrode of SCR **134** is connected to the ignition circuit of the vehicle. Parallel connected resistor **136** and capacitor **138** are connected between the gate and cathode of the SCR **134**. A drive circuit **140** comprising transistors **142, 144** and resistors **143, 145** has an input connected through a resistor **146** to the ignition switch **20** and is adapted to connect a lamp **148** across the battery **26** in response to closure of the ignition switch **20**. The lamp **148** illuminates the pushbutton unit **16** mounted on the dash **18** of the vehicle **8**.

A start switch generally designated **150** is connected from the battery **26** to the start solenoid (not shown) as indicated in FIG. **2**. The ignition switch **20** and the start switch **150** are shown as separate switches but it will be appreciated that these two switches may be combined in the usual fashion.

Referring now to FIG. **3**, the control circuit **22** is shown in detail. The input terminals **46, 48, 50** and **52** of control circuit **22** are connected to a NAND gate **152** which triggers a monostable multivibrator generally designated **154**. The multivibrator **154** comprises NOR gates **156, 158** and an inverter **160** as well as the time delay network **66** (FIG. **1**). The output of the gate **152** is connected through the inverter **160** to the terminal **82** and from there through the diode **78** and capacitor **70** of network **66** to ground. The output of the gate **152** is also one input to the gate **156**, the other input being from the output of the gate **158**. The output of the gate **156** is one input to the gate **158** while the other input is connected to the terminal **85** and from there to the junction between the capacitor **70** and the diode **78** of network **66**. All inputs to the gate **152** are normally a logic "1" and thus the output of the gate **152** is normally a logic "0." Accordingly, the capacitor **70** is normally charged from the logic "1" output of the inverter **160** through the diode **78**. The gate **152** performs a logical OR function producing a logic "1" output when any of the switches **32** through **38** are closed to place a logic "0" at the input of gate **152**. When any of the switches **32** through **38** are actuated the output of the gate **152** and the input to the gate **156** switches from a logic "0" to a logic "1." The output of the gate **156** and hence one input to the gate **158** switches to a logic "0." Also the output of the inverter **160** switches to a logic "0" and the capacitor **70** begins to discharge through the resistor **74** and the inverter **160**. When the capacitor **70** discharges below the threshold level of the gate **158** the output of the gate **158** switches to a logic "1." Upon release of the pushbutton actuated the capacitor **72** immediately charges from the inverter **160** through the diode **78** switching the output of the gate **158** back to a logic "0." The delay provided by the multivibrator **154** between actuation of one of the switches **32–38** and a change in the state of the multivibrator **154** eliminates the possibility of contact bounce of the switches **32–38** producing several output pulses from actuation of a single pushbutton. This feature is of particular importance where, as in the present invention, a digit of the code is repeated.

The output of the multivibrator **154** is connected with the clock input of a counter **162** having respective output terminals designated **0–5**. The outputs of the counter **162** are decoded and in the reset condition the output at the **0** terminal is a logic "1," while the output at the terminals **1–5** are a logic "0." Each clock pulse from the multivibrator **154** after reset of the counter **162** produces a logic "1" at the respective terminal **1–5**.

First logic means generally designated **164** comprises a plurality of AND function performing gates corresponding in number to the number of symbols in the code and in the example given, comprises five NAND gates designated **166, 168, 170, 172** and **174**. The gates **162** and **174** have one input connected respectively with the output terminals **1–5** of the counter **162**. The switch **32** actuable by the pushbutton bearing the numeral 1 is connected with the second input of the gates **166** and **170** through an inverter **176**. The switch **36** actuable by the pushbutton bearing the numeral 3 is connected as a second input to the gate **168** through an inverter **178**. The switch **38** actuable by the pushbutton bearing the numeral 4 is connected as a second input to the gate **172** through an inverter **180**. The switch **34** actuable by the pushbutton bearing the numeral 2 is connected as a second input to the gate **174** through an inverter **182**.

The gates **166–172** control a register generally designated **184**. The register **184** comprises a plurality of stages corresponding in number to one less than the number of symbols in the code; in this instance **4**. Each stage is a set-reset flip-flop comprising two NAND gates **186, 188; 190, 192; 194, 196**; and **198,200** respectively. The output of the gates **166–172** are connected with the set terminals S of each stage while the output of each stage is connected with the reset terminal R of the following stage.

The output of the last stage designated **202** which is normally a logic "0" is connected as a third input to gate **174**. The output of the gate **200** designated **204** is normally a logic "1" and is connected through an inverter **206** to the terminal **84** which is connected to the time delay network **68** comprising resistor **76**, diode **80** and capacitor **72**. The output of the gate **174** is connected through an inverter **208** to the base electrode of

a transistor **210** having its emitter grounded through the terminal **44** of control circuit **22** and its collector connected to the terminal **100** of control circuit **22** and thence to the drive circuit **110** for the unlocking solenoid **116**.

Reset circuit means generally designated **212** comprises a counter **213** having five output terminals designated **0–4** respectively, second, third, and fourth logic means generally designated **215**, **216** and **217** respectively. The counter **213** is clocked from the output of the multivibrator **154** through an inverter **214**. The second logic means **215** includes a plurality of OR function performing gates corresponding in number to the number of different symbols used in the code and in the example given comprises four NAND gates **218**, **220**, **222** and **224**. The gates **218** through **224** are respectively connected to all the pushbutton switches **32** through **40** excluding the switches actuable by the pushbuttons bearing the numerals 1, 3, 4 and 2 respectively. That is to say the gate **218** is connected to all switches except the switch **32**; the gate **220** is connected to all switches except the switch **36**; the gate **222** is connected to all switches except the switch **38** and the gate **224** is connected to all switches except the switch **34**. The third logic means **216** comprises a plurality of AND function performing gates corresponding in number to the number of symbols in the code and in the example given comprises five NAND gates **226**, **228**, **230**, **232** and **234**. One input to the gates **226–234** is connected with the respective output terminal **0–4** of the counter **213**. The other inputs to the gates **226** and **230** are from the output of the gate **218** while the other input to the gates **228**, **232**, and **234** are from the outputs of the gates **220**, **222** and **224** respectively. Since the gates **226** through **234** are enabled sequentially by the counter **213** a logic "0" output will be obtained from one of the gates **226–234** if any of the pushbuttons other than those bearing the numerals 1, 2, 3 or 4 are actuated or if any of those four pushbuttons are actuated out of proper sequence. The fourth logic means **217** performs an OR function and comprises NAND gates **238** and **240** and an inverter **242**. The inputs to the gate **238** are from the outputs of the gates **226** through **232** respectively. The output of the gate **238** is inverted by the inverter **242** and provides one input to the gate **240**, the other inputs being received from the output of the gate **234** and from the capacitor **72** through the terminal **87** and an inverter **244**. The output of the gate **240** is connected with the reset terminal of the counter **162** which resets the **0** terminal on the counter **162** to a logic "1" and the **1–5** terminals to a logic "0." The **0** terminal of the counter **162** is connected as one input to a NAND gate **246** which performs an AND function. The other input to the gate **246** is connected to the capacitor **70** through the terminal **85**. The output of the gate **246** is connected through an inverter **248** to the reset terminal on the counter **213** which resets the output terminal **0** to a logic "1" and the output terminals **1**, **2**, **3** and **4** to a logic "0." The output of the gate **246** is also fed to the reset terminal R in the first stage of the register **184**. Resetting the first stage of the register causes each succeeding stage to be reset producing a logic "0" at the output terminal **202**.

The output of the gate **226** of the reset circuit means **212** is also fed through a NOR gate **250** to the base of a transistor **252** having its emitter grounded through terminal **44** of the control circuit **22** and its collector connected to the terminal **96** of the control circuit **22** which as shown in FIG. **1** is connected with the drive circuit **102** of the lock solenoid **108**. The gate **250** has a second input connected to the ignition switch **20** through the the terminal **92** of the control circuit **22** and inverters **256** and **258** and performs a logical AND function. That is to say, the gate **250** is enabled only when a logic "0" input is obtained from gate **226** and the ignition switch **20** is open. When the ignition switch is closed a logic "1" appears at one input and disables the gate **250**.

Fifth logic means including a NAND gate **254** is connected in parallel with the gate **174** having inputs connected with the output terminal **202** of the register **184**; with the fifth output terminal of the counter **162**; and with the switch **34** actuable by the pushbutton bearing the numeral 2 through the inverter **182**. The gate **174** is connected to the ignition switch **20** from the terminal **92** of the control circuit **22** through the inverter **256** while the gate **254** is connected to the ignition switch **20** through the inverter **256** and the inverter **258**. When the ignition switch **20** is opened a logic "0" appears at the gate **254** disabling this gate while a logic "1" appears at the input to the gate **174**. When the ignition switch is closed the gate **174** is disabled and a logic "1" appears at the input to the gate **254**. The gate **254** is connected through an inverter **260** to the terminal **123** of the control circuit **22** and from there to the ignition control circuit **118**.

The operation of the circuit will now be described with reference to FIGS. **1–3**. Assuming that the vehicle is locked and all circuitry in a reset state the output of the counter **162** will be 100000 at the **0–5** terminals respectively and the output of the counter **123** will be 10000 at the **0–4** terminals respectively. The unlocking sequence is as follows assuming the code of 13142. Pressing pushbutton No. 1 of the unit **10** actuates switch **32** and grounds input terminals **46** of control circuit **22** producing a logic "1" at the output of gate **152** thus triggering the multivibrator **154**. After a time interval based on the discharge rate of capacitor **70** the output of the multivibrator **154** at gate **158** switches from a logic "0" to a logic "1" clocking the counter **162**, placing a logic "1" on the **1** terminal and consequently at one input of the gate **166**. Closure of the switch **32** also produces a logic "1" output at the inverter **176** and consequently at the other input to the gate **166**. The two logic "1" inputs to the gate **166** produce a logic "0" output which is fed to the gate **186** to set the first stage of the register **184**. When pushbutton No. 1 is released the capacitor **70** charges from the logic "1" output of the inverter **160** through the diode **78** and the output of the gate **158** returns to a logic "0" which clocks the counter **213** through the inverter **214** placing a logic "1" on the **1** output terminal of the counter **213**. In addition, when pushbutton No. 1 is released the output of the gate **166** returns to a logic "1" and the output of the gate **186** returns to a logic "0" placing a logic "1" on the output of the gate **192** and consequently the input of the gate **190** of the second stage of the register **184**. If any pushbutton

other than pushbutton No. 1 is depressed a logic "0" input is applied to gate **218** producing a logic "1" input to gate **226** which combined with the logic "1" input from the **0** output terminal of the counter **213** produces a logic "0" input to the gates **238** and **250**. The logic "0" input to the gate **250** combined with the logic "0" input from the open ignition switch **20** switches the output of the gate **250** to a logic "1" and renders the transistor **252** conductive to energize the door locking solenoid **108**. The logic "0" input to the gate **238** resets the counter **162** through the inverter **242** and gate **240**. Resetting the counter **162** produces a logic "1" input to the gate **246**. Upon release of pushbutton No. 1, the logic "1" input to the gate **246** is combined with the logic "1" input from the capacitor **70** to produce a logic "0" which resets the register **184** and also resets the counter **213** through the inverter **248**.

If now the operator depresses and releases pushbutton No. 3 a similar sequence of events occurs as previously mentioned in connection with depression of pushbutton No. 1 insofar as operation of the counters **162** and **213**, and the register **184** is concerned. If any pushbutton other than pushbutton No. 3 is depressed the gate **228** will be enabled from the gate **220** and the **1** output terminal of the counter **213** resetting the counters **162** and **213** and the register **184**. A similar sequence of events occurs upon depression and release of pushbuttons Nos. 1 and 4. Likewise if any pushbutton other than pushbuttons Nos. 1 and 4 are depressed the counters **162, 213** and the register **184** are reset.

Upon depression of pushbutton No. 4 the output of gate **200** at terminal **204** switches to a logic "0" which is inverted to a logic "1" by inverter **206** charging the capacitor **72** through the resistor **76** from the terminal **84**. Also the output of register **184** at junction **202** switches to a logic "1" and thus when the operator depresses the pushbutton No. 2 the output of the gate **174** switches to a logic "0" which is inverted to a logic "1" by the inverter **208** to render the transistor **210** conductive thereby energizing the unlock solenoid **116** through the drive circuit **110** connected with the junction **100**. The time constant of the timing circuit **68** comprising the resistor **76** and capacitor **72** is sufficiently long to permit the operator to press the last pushbutton unlocking the vehicle door. After a time interval determined by the value of the resistor **76** and capacitor **72** and the threshold of gate **240** the counter **162** and consequently the counter **203** and register **184** are reset.

When the operator enters the vehicle and closes the ignition switch **20** a logic "1" appears at the terminal **92** producing a logic "0" at the output of the inverter **256** disabling the gate **174**. Also a logic "1" appears at the output of the inverter **258** enabling the gate **254** and disabling the gate **250**. Furthermore, closure of the ignition switch **20** renders the drive circuit **140** conductive thus energizing the lamps **148** on the pushbutton unit **16**. The operator now inserts the same combination 13142 and upon actuation of pushbutton numeral 2 the output of the gate **254** switches to a logic "0" which is inverted to a logic "1" by the inverter **260** thus triggering the SCR **124** rendering the transistor **130** conductive to fire the SCR **134** and connect the battery **26** to the ignition circuit. The vehicle may now be started by closing the start switch **150**. In addition, when the SCR **124** conducts the drive circuit **140** is grounded deenergizing to lamp **148**.

A predetermined interval of time after pushbutton numeral **4** is depressed the time delay circuit comprising resistor **76** and capacitor **72** is operative to reset the register **184** and counters **162** and **213**. When the register **184** is reset a logic "0" appears at the output of the inverter **206** and the capacitor **72** discharges through the diode **80**. With the counter **213** in a reset condition a logic "1" appears at one input to the gate **226** and consequently, upon opening the ignition switch **20** and leaving the vehicle the driver may lock the vehicle doors by depressing any of the pushbuttons other than pushbutton No. 1 thereby causing the output of the gate **226** to switch to a logic "0" and the output of the gate **250** to switch to a logic "1," rendering the transistor **252** to conduct and energizing the lock solenoid **108** through the drive circuit **102**.

I claim:

1. A circuit for producing a control signal in response to a predetermined x symbol code selected from a choice of y symbols comprising;

y parallel connected manually actuable switch means, each switch means bearing indicia corresponding to respective ones of said y symbols;

first and second resettable electronic counter means having at least x output terminals;

triggerable switch means having an input connected with each of said y switch means and an output connected with each of said first and second counter means for clocking said first and second counter means in response respectively, to actuation and release of any of said y switch means;

first logic means including x gates performing an AND logic function, each gate having a first input connected with respective output terminals of said first counter means and a second input connected with at least one of said y switch means;

resettable electronic register means having $x-1$ stages, $x-1$ of the gates of said first logic means having an output connected with respective stages of said register means, the output of said register means being connected as a third input to the xth gate of said first logic means, the output of the xth gate of said first logic means producing said control signal when said switch means are actuated in a sequence corresponding to said code;

second logic means including at least y gates performing an OR logic function, each gate having inputs connected respectively with each one of different groups consisting of $y-1$ of said y switch means;

third logic means including x gates performing an AND logic function, each gate having a first input connected with respective output terminals of said second counter means and a second input connected with the output of at least one of the gates of said second logic means;

fourth logic means connected with the output of each of the gates of said third logic means for resetting said first counter means when any of said y switch means are actuated in a sequence differing from said code;

and logic means responsive to reset of said first counter means and release of said y switch means

for resetting said second counter means and said register.

2. In a motor vehicle provided with a source of DC potential, electrically operated door unlocking means and an ignition circuit, a circuit for controlling said door unlocking means and said ignition circuit in response to a predetermined x symbol code selected from a choice of y symbols comprising;

y parallel connected manually actuable switch means, each switch means bearing indicia corresponding to respective ones of said y symbols;

first and second resettable electronic counter means having at least x output terminals;

triggerable monostable multivibrator means having an input connected with each of said y switch means and an output connected with each of said first and second counter means for clocking said first counter means in response to actuation of any of said y switch means and for clocking said second counter means in response to release of any of said y switch means;

first logic means including x gates performing an AND logic function, each gate having a first input connected with respective output terminals of said first counter means and a second input connected with at least one of said y switch means;

resettable electronic register means having $x-1$ stages, $x-1$ of the gates of said first logic means having an output connected with respective stages of said register means, the output of said register means being connected as a third input to the xth gate of said first logic means, the output of the xth gate of said first logic means connected with said electrically operated door unlocking means whereby said door unlocking means are operated when said y switch means are actuated in a sequence corresponding to said code;

second logic means including at least y gates performing an OR logic function, each gate having inputs connected respectively with each one of different groups consisting of $y-1$ of said y switch means;

third logic means including x gates performing an AND logic function, each gate having a first input connected with respective output terminals of said second counter means and a second input connected with the output of at least one of the gates of said second logic means;

fourth logic means having inputs connected with the outputs of respective ones of the gates of said third logic means for resetting said first counter means when any of said y switch means are actuated in a sequence different from said code;

logic means responsive to reset of said first counter means and release of said Y switch means for resetting said second counter means and said register;

time delay means responsive to one state of the last stage of said register means for resetting said first counter means a predetermined interval of time after the last stage of said register means switches to said one state;

fifth logic means comprising a gate performing an AND logic function and connected in parallel with the xth gate of said first logic means;

operator controlled switching means for disabling said x^{th} gate of said first logic means and for enabling said fifth logic means;

said fifth logic means producing a control signal when said switch means are actuated in a sequence corresponding to said code;

normally non-conductive electronic switching means connected in said ignition circuit, said electronic switch means being rendered conductive in response to said control signal of said fifth logic means.

3. In a motor vehicle provided with a source of DC potential, electrically operated door locking and unlocking means and an ignition circuit including an ignition switch connected to said source;

a circuit for energizing said door unlocking means and for energizing said ignition circuit in response to a predetermined x symbol code selected from a choice of y symbols;

y parallel connected manually actuable switch means, each switch means bearing indicia corresponding to respective ones of said y symbols;

first resettable electronic counter means having a reset terminal, a clock terminal, a first output terminal and x additional output terminals;

monostable multivibrator means having an input connected with each of said y switch means and triggerable from a stable state to a semi-stable state a predetermined interval of time after actuation of any one of said y switch means and returning to its stable state upon deactuation of said one of said y switch means, the output of said multivibrator means being connected to the clock terminal of said first counter for clocking said first counter means, each time said multivibrator means is triggered to its semi-stable state;

second resettable electronic counter means having a clock terminal, a reset terminal, and at least x output terminals;

inverter means connecting the output of said multivibrator means to the clock terminal of said second counter means whereby said second counter means is clocked when said multivibrator means returns to its stable state;

first logic means including x gates performing an AND logic function, each gate having a first input connected with the respective x additional output terminals of said first counter means and a second input connected with at least one of said y switch means;

resettable electronic register means having $x-1$ stages, $x-1$ at the gates of said first logic means having an output connected with respective stages of said register means, the output of said register means being connected as a third input to the xth gate of said first logic means, the output of the xth gate of said first logic means connected with said electrically operated door unlocking means whereby said door unlocking means are operated when said switch means are actuated in a sequence corresponding to said code;

second logic means including at least y gates performing an OR logic function, each gate having inputs connected respectively with each one of different groups consisting of $y-1$ of said y switch means;

third logic means including x gates performing an AND logic function, each gate having a first input connected with respective output terminals of said second counter means and a second input connected with the output of at least one of the gates of said second logic means;

fourth logic means having inputs connected with the outputs of respective ones of the gates of said third logic means for resetting said first counter means thereby producing an enabling output at said first output terminal of said first counter means;

means connected with said multivibrator means and said first output terminal for resetting said second counter and said register means when said multivibrator returns to its stable state and an enabling output appears at said first terminal of said first counter means;

time delay means responsive to one state of the last stage of said register means for resetting said first counter means a predetermined interval of time after the last stage of said register means switches to said one state;

fifth logic means comprising a gate performing an AND logic function and connected in parallel with the xth gate of said first logic means, means for disabling said x^{th} gate of said first logic means and for enabling said fifth logic means in response to closure of said ignition switch;

electronic switching means connecting said ignition circuit in series with said ignition switch and responsive to the output of said fifth logic means for energizing said ignition circuit when said y switch means are actuated in a sequence corresponding to said code;

sixth logic means performing an AND logic function and responsive to the output of one of said gates of said third logic means and to opening of said ignition switch for energizing said door locking means.

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