



(51) International Patent Classification:
H03M 13/13 (2006.01)

(21) International Application Number:

PCT/CN2019/071677

(22) International Filing Date:

14 January 2019 (14.01.2019)

(25) Filing Language:

English

(26) Publication Language:

English

(71) Applicants (*for CN only*): **NOKIA SHANGHAI BELL CO., LTD.** [CN/CN]; No. 388, Ningqiao Road, Pudong Jinqiao, Shanghai 201206 (CN). **NOKIA SOLUTIONS AND NETWORKS OY** [FI/FI]; Karaportti 3, 02610 Espoo, (FI).

(71) Applicant (*for all designated States except CN*): **NOKIA TECHNOLOGIES OY** [FI/FI]; Karaportti 3, 02610 Espoo, (FI).

(72) Inventors: **CHEN, Yu**; No.388 Ningqiao Road, Pudong Jinqiao, Shanghai 201206 (CN). **CHEN, Jie**; 1960 Lucent Lane, Naperville, Illinois 60563-159 (US). **ZHU, Kai**; No.388 Ningqiao Road, Pudong Jinqiao, Shanghai 201206 (CN). **LADDU, Keeth Saliya Jayasinghe**; 68/3/1, Sama Uyana, Kottawa Road, Piliyandala (LK).

(74) Agent: **KING & WOOD MALLESONS**; 20th Floor, East Tower, World Financial Centre, No.1 Dongsanhuan Zhonglu, Chaoyang District, Beijing 100020 (CN).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,

(54) Title: POLAR ENCODING

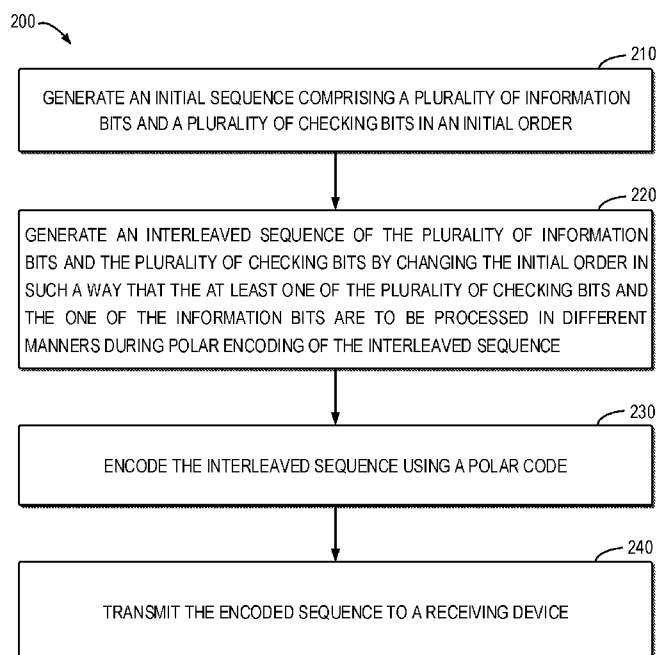


Fig. 2

(57) Abstract: Embodiments of the present disclosure provide a method, device and computer readable medium for performing polar encoding. In example embodiments, the method comprises generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order. At least one of the plurality of checking bits is a duplication of one of the information bits. The method further comprises generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence. The method further comprises encoding the interleaved sequence using a polar code. The method further comprises transmitting the encoded sequence to a receiving device.

DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

POLAR ENCODING

FIELD

[0001] Embodiments of the present disclosure generally relate to wireless communication, and in particular, to a method, device and computer readable medium for performing polar
5 encoding.

BACKGROUND

[0002] Polar code is used as New Radio (NR) enhanced Mobile Broadband (eMBB) control channel coding solution. It is studied that the polar code has benefits of low complexity, low latency and no error floor effect. Thus, it may also be used in Ultra Reliable & Low Latency
10 Communication (URLLC) and massive Machine Type Communication (mMTC).

[0003] In information theory, the polar code is a linear block error correcting code. The code construction is based on a multiple recursive concatenation of a short kernel code which transforms the physical channel into virtual outer channels. When the number of recursions becomes large, the virtual channels tend to either have high reliability or low reliability (in
15 other words, they polarize), and data bits are allocated to the most reliable channels.

SUMMARY

[0004] In general, example embodiments of the present disclosure provide a method, device and computer readable medium for performing polar encoding.

[0005] In a first aspect, there is provided a method for communication. The method
20 comprises generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order. At least one of the plurality of checking bits is a duplication of one of the information bits. The method further comprises generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits
25 and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence. The method further comprises encoding the interleaved sequence using a polar code. The method further comprises transmitting the encoded sequence to a receiving device.

[0006] In a second aspect, there is provided a method for communication. The method
30 comprises generating an initial sequence comprising a plurality of information bits and a

plurality of checking bits in an initial order; inserting at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device; generating an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking bits; encoding the interleaved sequence using a polar code; and transmitting the encoded sequence to the receiving device.

[0007] In a third aspect, there is provided a method for communication. The method comprises generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value; generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order; encoding the interleaved sequence using a polar code; and transmitting the encoded sequence to a receiving device.

[0008] In a fourth aspect, there is provided an electric device. The electric device comprises at least one processor and at least one memory including computer program code. The at least one memory and the computer program code are configured to, with the at least one processor, cause the electric device to: generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits being a duplication of one of the information bits; generate an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence; encode the interleaved sequence using a polar code; and transmit the encoded sequence to a receiving device.

[0009] In a fifth aspect, there is provided an electric device. The electric device comprises at least one processor and at least one memory including computer program code. The at least one memory and the computer program code are configured to, with the at least one processor, cause the electric device to: generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order; insert at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device; generate an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking

bits; encode the interleaved sequence using a polar code; and transmit the encoded sequence to the receiving device.

[0010] In a sixth aspect, there is provided an electric device. The electric device comprises at least one processor and at least one memory including computer program code. The at least one memory and the computer program code are configured to, with the at least one processor, cause the electric device to: generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value; generate an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order; encode the interleaved sequence using a polar code; and transmit the encoded sequence to a receiving device.

[0011] In a seventh aspect, there is provided a computer readable medium having instructions stored thereon. The instructions, when executed on at least one processor of a device, cause the device to carry out the method according to the first aspect.

[0012] In an eighth aspect, there is provided a computer readable medium having instructions stored thereon. The instructions, when executed on at least one processor of a device, cause the device to carry out the method according to the second aspect.

[0013] In a ninth aspect, there is provided a computer readable medium having instructions stored thereon. The instructions, when executed on at least one processor of a device, cause the device to carry out the method according to the third aspect.

[0014] It is to be understood that the summary section is not intended to identify key or essential features of embodiments of the present disclosure, nor is it intended to be used to limit the scope of the present disclosure. Other features of the present disclosure will become easily comprehensible through the following description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Through the more detailed description of some embodiments of the present disclosure in the accompanying drawings, the above and other objects, features and advantages of the present disclosure will become more apparent, wherein:

[0016] Fig. 1 is a schematic diagram of a communication environment in which embodiments of the present disclosure can be implemented;

[0017] Fig. 2 shows a flowchart of an example method in accordance with some

embodiments of the present disclosure;

[0018] Fig. 3 is a schematic diagram illustrating an example of an interleaved sequence in accordance with some embodiments of the present disclosure;

5 [0019] Fig. 4 shows a flowchart of an example method in accordance with some other embodiments of the present disclosure;

[0020] Fig. 5 is a schematic diagram illustrating an example of an interleaved sequence in accordance with some other embodiments of the present disclosure;

10 [0021] Fig. 6A is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels in accordance with some other embodiments of the present disclosure;

[0022] Fig. 6B is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels in accordance with still other embodiments of the present disclosure;

15 [0023] Fig. 7 shows a flowchart of an example method in accordance with still other embodiments of the present disclosure;

[0024] Fig. 8 shows a flowchart of an example method in accordance with yet other embodiments of the present disclosure;

20 [0025] Fig. 9 is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels in accordance with yet other embodiments of the present disclosure;

[0026] Fig. 10 shows a flowchart of an example method in accordance with some other embodiments of the present disclosure;

[0027] Fig. 11 is a schematic diagram of an example polar decoding structure;

25 [0028] Fig. 12 is a graph illustrating simulation results for performance evaluation in accordance with some embodiments of the present disclosure; and

[0029] Fig. 13 is a simplified block diagram of a device that is suitable for implementing embodiments of the present disclosure.

[0030] Throughout the drawings, the same or similar reference numerals represent the same or similar elements.

DETAILED DESCRIPTION OF EMBODIMENTS

[0031] Principle of the present disclosure will now be described with reference to some example embodiments. It is to be understood that these embodiments are described only for the purpose of illustration and help those skilled in the art to understand and implement the present disclosure, without suggesting any limitations as to the scope of the disclosure. The disclosure described herein can be implemented in various manners other than the ones described below.

[0032] In the following description and claims, unless defined otherwise, all technical and scientific terms used herein have the same meaning as commonly understood by one of ordinary skills in the art to which this disclosure belongs.

[0033] As used herein, the term “network device” or “base station” (BS) refers to a device which is capable of providing or hosting a cell or coverage where terminal devices can communicate. Examples of a network device include, but not limited to, a Node B (NodeB or NB), an Evolved NodeB (eNodeB or eNB), a next generation NodeB (gNB), a Remote Radio Unit (RRU), a radio head (RH), a remote radio head (RRH), a low power node such as a femto node, a pico node, and the like. For the purpose of discussion, in the following, some embodiments will be described with reference to eNB or gNB as examples of the network device.

[0034] As used herein, the term “terminal device” refers to any device having wireless or wired communication capabilities. Examples of the terminal device include, but not limited to, user equipment (UE), personal computers, desktops, mobile phones, cellular phones, smart phones, personal digital assistants (PDAs), portable computers, image capture devices such as digital cameras, gaming devices, music storage and playback appliances, or Internet appliances enabling wireless or wired Internet access and browsing and the like. For the purpose of discussion, in the following, some embodiments will be described with reference to UEs as examples of terminal devices and the terms “terminal device” and “user equipment” (UE) may be used interchangeably in the context of the present disclosure.

[0035] The term “circuitry” used herein may refer to one or more or all of the following: (a) hardware-only circuit implementations (such as implementations in only analog and/or digital circuitry) and (b) combinations of hardware circuits and software, such as (as applicable): (i) a combination of analog and/or digital hardware circuit(s) with software/firmware and (ii) any portions of hardware processor(s) with software (including digital signal processor(s)),

software, and memory(ies) that work together to cause an apparatus, such as a mobile phone or server, to perform various functions) and (c) hardware circuit(s) and or processor(s), such as a microprocessor(s) or a portion of a microprocessor(s), that requires software (for example,, firmware) for operation, but the software may not be present when it is not needed

5 for operation.”

[0036] This definition of circuitry applies to all uses of this term in this application, including in any claims. As a further example, as used in this application, the term circuitry also covers an implementation of merely a hardware circuit or processor (or multiple processors) or portion of a hardware circuit or processor and its (or their) accompanying
10 software and/or firmware. The term circuitry also covers, for example and if applicable to the particular claim element, a baseband integrated circuit or processor integrated circuit for a mobile device or a similar integrated circuit in server, a cellular network device, or other computing or network device.

[0037] As used herein, the singular forms “a”, “an” and “the” are intended to include the
15 plural forms as well, unless the context clearly indicates otherwise. The term “includes” and its variants are to be read as open terms that mean “includes, but is not limited to.” The term “based on” is to be read as “based at least in part on.” The term “one embodiment” and “an embodiment” are to be read as “at least one embodiment.” The term “another embodiment” is to be read as “at least one other embodiment.” The terms “first,” “second,” and the like
20 may refer to different or same objects. Other definitions, explicit and implicit, may be included below.

[0038] In some examples, values, procedures, or apparatus are referred to as “best,” “lowest,” “highest,” “minimum,” “maximum,” or the like. It will be appreciated that such descriptions are intended to indicate that a selection among many used functional alternatives can be made,
25 and such selections need not be better, smaller, higher, or otherwise preferable to other selections.

[0039] Fig. 1 is a schematic diagram of a communication environment 100 in which embodiments of the present disclosure can be implemented. The communication environment 100 may comprise a network device 110, which provides wireless connections
30 for a plurality of terminal devices 120, 130 within its coverage. The terminal devices 120 and 130 may communicate with the network device 110 via a wireless transmission channel 115 or 125 and/or communicate with each other via a transmission channel 135.

[0040] It is to be understood that the number of network devices and the number of terminal devices as shown in Fig. 1 are only for the purpose of illustration without suggesting any limitations. The communication environment 100 may include any suitable number of network devices and terminal devices adapted for implementing embodiments of the present disclosure. In addition, it would be appreciated that there may be various wireless communications as well as wireline communications (if needed) among these network devices and the terminal devices.

[0041] The communications in the communication environment 100 may conform to any suitable standards including, but not limited to, Global System for Mobile Communications (GSM), Extended Coverage Global System for Mobile Internet of Things (EC-GSM-IoT), Long Term Evolution (LTE), LTE-Evolution, LTE-Advanced (LTE-A), Wideband Code Division Multiple Access (WCDMA), Code Division Multiple Access (CDMA), GSM EDGE Radio Access Network (GERAN), and the like.

[0042] Furthermore, the communications in the communication environment 100 may be performed according to any generation communication protocols either currently known or to be developed in the future. Examples of the communication protocols include, but not limited to, the first generation (1G), the second generation (2G), 2.5G, 2.75G, the third generation (3G), the fourth generation (4G), 4.5G, the fifth generation (5G) communication protocols.

[0043] By way of illustrative example, the various example implementations or techniques described herein may be applied to various terminal devices, such as machine type communication (MTC) terminal devices, enhanced machine type communication (eMTC) terminal devices, Internet of Things (IoT) terminal devices, and/or narrowband IoT terminal devices.

[0044] In an example implementation, a terminal device or UE may be a UE/terminal device with URLLC applications. A cell (or cells) may include a number of terminal devices connected to the cell, including terminal devices of different types or different categories, for example, including the categories of MTC, NB-IoT, URLLC, or other UE category.

[0045] The various example implementations may be applied to a wide variety of wireless technologies or wireless networks, such as LTE, LTE-A, 5G, cmWave, and/or mmWave band networks, IoT, MTC, eMTC, URLLC, and the like, or any other wireless network or wireless technology. These example networks or technologies are provided only as illustrative

examples, and the various example implementations may be applied to any wireless technology/wireless network.

[0046] As mentioned above, the polar code may be used as control channel coding solution for URLLC. False alarm rate for error detection is critical for downlink control channel that needs blind decoding. Compared with LTE, URLLC requires a lower false alarm rate for error detection, such as $1e-5$. Two conventional solutions for reducing the false alarm rate are proposed.

[0047] In one of the two conventional solutions, more Cyclic Redundancy Check (CRC) bits are employed, which means a larger CRC polynomial should be used. Because the current CRC attachment was optimized for early termination by having an interleaver after CRC generation, the larger CRC polynomial should be carefully designed in order to have the backward compatibility.

[0048] In another conventional solution, unused bits in downlink control information (DCI) message are employed for checking. However, there exist two problems with this solution: the false alarm rate cannot fulfil the requirement even if there is no repetition, and not all of the current eight DCI formats contain the unused bits.

[0049] In order to at least in part solve above and other potential problems, embodiments of the present disclosure provide a solution for polar encoding. According to embodiments of the present disclosure, at least one new checking bit is introduced and the at least one new checking bit is a duplication of one of a plurality of information bits. The at least one new checking bit is inserted into the plurality of information bits in such a way that the at least one new checking bit and the one of the information bits are to be processed in different manners during polar encoding. With the embodiments of the present disclosure, because the at least one new checking bit and the one of the information bits are to be processed in different manners during polar encoding, the probability that errors occur in the at least one new checking bit and the one of the information bits may be reduced. Thus, checking effectiveness may be improved. In the following, some embodiments according to the present disclosure will be detailed with reference to Figs. 2-12.

[0050] Fig. 2 shows a flowchart of an example method 200 in accordance with some embodiments of the present disclosure. In context of the present disclosure, for ease of discussion and without loss of generality, the network device 110 in the communication environment 100 may be described as a transmitting device and the terminal device 120 in the

communication environment 100 may be described as a receiving device. It is to be appreciated that, in some other communication scenarios, the terminal device 120 may be a transmitting device and the network device 110 may be a receiving device.

5 [0051] In general, the transmitting device 110 may transmit information to the receiving device 120 for communication. For example, the transmitted information may be data information, control information, or the like. Before the transmission, the transmitting device 110 may perform encoding (such as channel encoding) on the information using a polar code, so as to improve quality of the transmission. Correspondingly, the receiving device 120 may receive the encoded information and obtain the information by decoding the
10 encoded information using the polar code.

[0052] At block 210, the transmitting device 110 generates an initial sequence, for example, based on control information to be transmitted to the receiving device 120. The initial sequence includes a plurality of information bits and a plurality of checking bits in an initial order. Among the plurality of checking bits, at least one checking bit is a duplication of one
15 of the information bits. For example, each of the at least one checking bit may be a duplication of an information bit that is adjacent to the checking bit. In context of the present disclosure, the checking bit that is a duplication of an information bit is also referred to as a new checking bit, and other checking bits in the plurality of checking bits are also referred to as existing checking bits.

20 [0053] In some embodiments, the at least one new checking bit is a bit in a downlink control information (DCI) message. In some embodiments, the existing checking bits may be any type of error detection code, such as CRC bits. For ease of discussion and without loss of generality, the existing checking bits will be described taking CRC bits for example. It is to be appreciated that the existing checking bits may be other type of error detection code if
25 other error detection scheme is employed by the transmitting device 110 and the receiving device 120.

[0054] In some embodiments, the number of the at least one new checking bit may be determined based on an expected false alarm rate and the number of the existing checking bits. For example, where the expected false alarm rate is 2^{-27} and the number of the existing
30 checking bits is 2^{-24} , the number of the at least one new checking bit may be determined as three.

[0055] At block 220, the transmitting device 110 generates an interleaved sequence of the

plurality of information bits and the plurality of checking bits by changing the initial order. The change to the initial order is performed in such a way that the at least one new checking bit and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence. In context of the present disclosure, the interleaved sequence to be encoded using the polar code may also be referred to as an information block or a block.

[0056] In some embodiments, during polar encoding of the interleaved sequence, the transmitting device 110 may perform an exclusive “or” output of the at least one new checking bit, and perform an original output of the one of the information bits. Alternatively, during polar encoding of the interleaved sequence, the transmitting device 110 may perform an exclusive “or” output of the one of the information bits, and perform an original output of the at least one new checking bit. It should be understood that performing the exclusive “or” output and performing the original output are just examples of different manners of processing, without suggesting any limitation as to the scope of the disclosure. Because the at least one new checking bit and the one of the information bits are to be processed in different manners during polar encoding, the probability that errors occur in the at least one new checking bit and the one of the information bits may be reduced. Thus, checking effectiveness may be improved.

[0057] Generally, after changing the initial order of the initial sequence, the plurality of checking bits may be not uniformly distributed in the interleaved sequence, as shown in Fig. 3, for example.

[0058] Fig. 3 is a schematic diagram illustrating an example of an interleaved sequence 300 in accordance with some embodiments of the present disclosure. As shown, the interleaved sequence 300 comprises information bits 311 and checking bits 312. A first sequence 314 of information bits, a second sequence 315 of information bits, and a third sequence 316 of information bits may be referred to as a first Distributed CRC (DCRC) section, a second (DCRC) section and a third (DCRC) section, as defined in 3GPP TS 38.211. It can be seen from Fig. 3 that the checking bits 312 are not uniformly distributed in the interleaved sequence 300, which may reduce the checking effectiveness.

[0059] In order to improve the checking effectiveness, in some embodiments of the present disclosure, the transmitting device 110 changes the initial order of the initial sequence to uniformly distribute the plurality of checking bits so as to generate the interleaved sequence.

In other words, the plurality of checking bits are uniformly distributed in the interleaved sequence. This means that for any two sections in the interleaved sequence, a difference between a ratio of the checking bits to the information bits in one of the two sections and a ratio of the checking bits to the information bits in the other of the two sections is below a threshold difference. One of such embodiments will be described below with reference to Fig. 4.

[0060] Fig. 4 shows a flowchart of an example method 400 of generating an interleaved sequence in accordance with some other embodiments of the present disclosure. The method 400 can be implemented at the transmitting device 110 as shown in Fig. 1. For the purpose of discussion, the method 400 will be described from the perspective of the transmitting device 110 with reference to Figs. 1 and 3. For example, the method 400 may be an example implementation of the block 220 as shown in Fig. 2. It is to be understood that the method 400 may include additional blocks not shown and/or may omit some blocks as shown, and the scope of the present disclosure is not limited in this regard.

[0061] At block 410, the transmitting device 110 sets an index x of a DCRC section be one. At block 415, the transmitting device 110 distributes N checking bits uniformly in the first DCRC section 314, where N represents the number of the new checking bits as described above.

[0062] At block 420, the transmitting device 110 calculates a first average number of information bits between two checking bits in DCRC section x and a second average number of information bits between two checking bits in DCRC section $x+1$.

[0063] At block 425, the transmitting device 110 determines whether the first average number of information bits in DCRC section x is less than the second average number of information bits in DCRC section $x+1$. If it is determined that the first average number is not less than the second average number, the transmitting device 110 increases the index x by one at block 430.

[0064] At block 435, the transmitting device 110 determines whether a value of the index x is less than or equal to a total number of the DCRC sections. For example, in the example as shown in Fig. 3, the total number of the DCRC sections is equal to three. If the value of the index x is equal to one, the transmitting device 110 may determine that the value of the index x is less than the total number of the DCRC sections.

[0065] If it is determined at block 435 that the value of the index x is less than or equal to

the total number of the DCRC sections, the transmitting device 110 determines whether there is any checking bit that needs to be moved to the next DCRC section at block 440.

[0066] If it is determined at block 440 that no checking bit needs to be moved to the next DCRC section, the transmitting device 110 arranges, on f node and g node respectively, the checking bit and the information bit that are to be processed in different manners during polar encoding. For the purpose of arranging the checking bit and the information bit on f node and g node respectively, the transmitting device 110 may move one of the checking and information bits left or right by at most one bit if the checking and information bits are both arranged on f nodes or g nodes.

[0067] On the other hand, if it is determined at block 425 that the first average number is not less than the second average number, the transmitting device 110 moves, at block 450, one checking bit in DCRC section x to DCRC section x+1 and uniformly distributes the checking bits in DCRC section x. Then, the method 400 returns to block 420.

[0068] In addition, if it is determined at block 435 that the value of the index x is greater than the total number of the DCRC sections, the transmitting device 110 increases the index x by one at block 455. Then, the method 400 returns to block 420.

[0069] Moreover, if it is determined at block 440 that no checking bit needs to be moved to the next DCRC section, the transmitting device 110 sets the index x of DCRC section be one at block 460. Then, the method 400 returns to block 420.

[0070] With the method 400, the plurality of checking bits are uniformly distributed in the interleaved sequence, as shown in Fig. 5, for example. Fig. 5 is a schematic diagram illustrating an example of an interleaved sequence 500 in accordance with some other embodiments of the present disclosure. Compared with the example as shown in Fig. 3, in the example as shown in Fig. 5, existing checking bits 511 and new checking bits 512 are uniformly distributed in the interleaved sequence 500, thereby improving the checking effectiveness. It should be noted that a sequence 313 of checking bits are not moved because sub-channels onto which the checking bits 313 would be mapped have higher reliability.

[0071] Referring back to Fig. 2, at block 230, the transmitting device 110 encodes the interleaved sequence using a polar code. During the polar encoding, various encoding algorithms may be utilized, including existing polar encoding algorithms and possibly other polar encoding algorithms that will be developed in future.

[0072] At block 240, the transmitting device 110 transmits the encoded sequence to the

receiving device 120.

[0073] In general, polar coding has a property that at a specific break point, an index of the first sub-channel onto which an information bit or a checking bit is mapped will be changed to its half. For example, if an index of the first sub-channel is 256 for a specific size of an information block, the index of the first sub-channel will be changed to 128 even if only one additional bit is added to the information block. Typically, the receiving device 120 will start decoding from the first sub-channel. If the index of the first sub-channel decreases greatly, the decoding delay will be increased significantly, which will be described with reference to Figs. 6A and 6B.

[0074] Fig. 6A is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels of a channel 600 in accordance with some other embodiments of the present disclosure, and Fig. 6B is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels of a channel 605 in accordance with still other embodiments of the present disclosure.

[0075] As shown in Fig. 6A, the channel 600 comprises sub-channels 611 and sub-channels 612. Existing checking bits or information bits in an information block are mapped onto the sub-channels 611 for polar encoding. Thus, in the context of the present disclosure, sub-channels 611 onto which existing checking bits or information bits are mapped are also referred to as occupied sub-channels of a first type 611. No existing checking bits or information bits are mapped onto the sub-channels 612, but frozen bits are mapped onto the sub-channels 612. Because valued of the frozen bits are known to the receiving device 120, the receiving device 120 will exclude the encoded frozen bits from decoding. Thus, in the context of the present disclosure, sub-channels 612 onto which frozen bits are mapped are also referred to as blank sub-channels of a first type 612.

[0076] As shown in Fig. 6A, a starting occupied sub-channel of the first type 611 is adjacent to the blank sub-channels of the first type 612. Upon receiving the encoded information block, the receiving device 120 will start decoding from the starting occupied sub-channel of the first type 611. On the starting occupied sub-channel of the first type 611, an information bit or a checking bit is mapped.

[0077] If one additional bit is added to the information block, a position of the starting occupied sub-channel may be changed. As shown in Fig. 6B, the position of the starting occupied sub-channel is changed so that it is positioned between the blank sub-channels of the

first type 612. The starting occupied sub-channel that is positioned between the blank sub-channels of the first type 612 may be referred to as an occupied sub-channel of a second type 613. Upon receiving the encoded information block, the receiving device 120 will start decoding from the occupied sub-channel of the second type 613. In other words, it will take
5 the receiving device 120 more time to decode the encoded information block. That is, the decoding delay is increased significantly.

[0078] In order to reduce the decoding delay, in some embodiments, the transmitting device 110 may insert at least one dummy bit before checking bits and information bits, which will be described below with reference to Fig. 7.

10 **[0079]** Fig. 7 shows a flowchart of an example method 700 in accordance with some embodiments of the present disclosure. For example, the method 700 can be implemented at the network device 110 as shown in Fig. 1. It is to be understood that the method 700 may include additional blocks not shown and/or may omit some blocks as shown, and the scope of the present disclosure is not limited in this regard. In context of the present disclosure, for
15 ease of discussion and without loss of generality, the network device 110 in the communication environment 100 may be described as a transmitting device and the terminal device 120 in the communication environment 100 may be described as a receiving device. It is to be appreciated that, in some other communication scenarios, the terminal device 120 may be a transmitting device and the network device 110 may be a receiving device.

20 **[0080]** At block 710, the transmitting device 110 generates an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order.

[0081] At block 720, the transmitting device 110 inserts at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device.

25 **[0082]** At block 730, the transmitting device 110 generates an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking bits.

[0083] At block 740, the transmitting device 110 encodes the interleaved sequence using a polar code.

30 **[0084]** At block 750, the transmitting device 110 transmits the encoded sequence to the receiving device 120.

[0085] In some embodiments, the at least one dummy bit is determined based on an identity of the receiving device 120.

[0086] Because a value of each dummy bit is known to the receiving device 120, the receiving device 120 will bypass the at least one dummy bit and start encoding of information or checking bits after the at least one dummy bit. In other words, the receiving device 120 will exclude the at least one dummy bit from decoding. Thus, the speed of decoding is accelerated and the decoding delay is reduced.

[0087] Fig. 8 shows a flowchart of an example method 800 of inserting at least one dummy bit in accordance with still other embodiments of the present disclosure. The method 800 can be implemented at the transmitting device 110 as shown in Fig. 1. For the purpose of discussion, the method 800 will be described from the perspective of the transmitting device 110 with reference to Fig. 1. For example, the method 800 may be an example implementation of the method 700 as shown in Fig. 7. It is to be understood that the method 800 may include additional blocks not shown and/or may omit some blocks as shown, and the scope of the present disclosure is not limited in this regard.

[0088] As shown, at block 810, the transmitting device 110 generates a first additional sequence by combining a sequence of frozen bits with the interleaved sequence. For example, in the example as shown in Fig. 6B, the first additional sequence may be the sequence comprising the bits mapped on the sub-channels 611, 612 and 613.

[0089] At block 820, the transmitting device 110 determines the number of a subset of the frozen bits between a starting bit and a first bit in the first additional sequence. For example, in the example as shown in Fig. 6B, the starting bit may be the bit that is mapped onto the sub-channel 613, the first bit may be the bit that is mapped onto the sub-channel 611 subsequent to the sub-channel 613, and the subset of the frozen bits may be the frozen bits that are mapped onto the sub-channels 612 between the sub-channel 613 and the sub-channel 611.

[0090] At block 830, the transmitting device 110 determines whether the number of the subset of the frozen bits exceeds a threshold number. In some embodiments, the threshold number may be determined as $2^{\lceil \log_2(P)-1 \rceil}$, where P represents an index of the sub-channel onto which the starting bit in the first additional sequence. For example, in the example as shown in Fig. 6B, P represents an index of the sub-channel 613. It should be understood that $2^{\lceil \log_2(P)-1 \rceil}$ is just an example of the threshold number, without

suggesting any limitations as to the scope of the disclosure. Depending on the specific application scenario, the threshold number may be determined as any appropriate value.

[0091] If it is determined at block 830 that the number of the subset of the frozen bits exceeds the threshold number, the transmitting device 110 marks the starting bit x as “D” (also referred to as bit “D”) at block 840. On the other hand, if it is determined at block 830 that the number of the subset of the frozen bits exceeds the threshold number, the transmitting device 110 may perform any appropriate act at block 890.

[0092] At block 850, the transmitting device 110 inserts a dummy bit marked as “Y” (also referred to as bit “Y”). At block 860, the transmitting device 110 interleaves the dummy bit, checking bits and information bits.

[0093] At block 870, the transmitting device 110 determines whether the bit “Y” is positioned before the bit “D”. If it is determined at block 870 that the bit “Y” is not positioned before the bit “D”, the transmitting device 110 exchanges positions of the bit “D” and the bit “Y” at block 880. On the other hand, if it is determined at block 870 that the bit “Y” is positioned before the bit “D”, the transmitting device 110 may perform any appropriate act at block 890.

[0094] It should be understood that the method 800 may be performed repeatedly if more dummy bits will be inserted.

[0095] Fig. 9 is a schematic diagram illustrating an example mapping of an interleaved sequence onto sub-channels of a channel 900 in accordance with yet other embodiments of the present disclosure. Compared the example as shown in Fig. 9 with the example as shown in Fig. 6B, a dummy bit is mapped onto a sub-channel 614 (also referred to as a blank sub-channel of a second type 614). The starting checking or information bit as shown in Fig. 6B is mapped onto a sub-channel 613 (also referred to as an occupied sub-channel of a second type 613). In this way, upon receiving the encoded information block, the receiving device 120 will bypass the sub-channel 614 and start encoding from the sub-channel 611 subsequent to the sub-channel 614. That is, the speed of decoding is accelerated and the decoding delay is reduced.

[0096] Fig. 10 shows a flowchart of an example method 1000 of generating an interleaved sequence in accordance with some other embodiments of the present disclosure. The method 1000 can be implemented at the transmitting device 110 as shown in Fig. 1. For the purpose of discussion, the method 1000 will be described from the perspective of the

transmitting device 110 with reference to Fig.1. It is to be understood that the method 1000 may include additional blocks not shown and/or may omit some blocks as shown, and the scope of the present disclosure is not limited in this regard.

[0097] At block 1010, the transmitting device 110 generates an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order. At least one of the plurality of checking bits having a predefined value.

[0098] In some embodiments, the predefined value may be zero or one.

[0099] At block 1020, the transmitting device 110 generates an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order.

[00100] At block 1030, the transmitting device 110 encodes the interleaved sequence using a polar code.

[00101] At block 1040, the transmitting device 110 transmits the encoded sequence to the receiving device 120.

[00102] In some embodiments, the at least one of the plurality of checking bits is a bit in a downlink control information message.

[00103] In some embodiments, the plurality of checking bits are uniformly distributed in the interleaved sequence.

[00104] In the following, decoding operations performed at the receiving device 120 will be described with reference to Fig. 11. Fig. 11 is a schematic diagram of an example polar decoding structure 1100. As shown, the example polar decoding structure 1100 comprises f nodes 1111 to 1114 and g nodes 1121 to 1124.

[00105] In some embodiments, computations performed at the f nodes 1111 to 1114 may be represented by the following Equation (1), and computations performed at the g nodes 1121 to 1124 may be represented by the following Equation (2):

$$f(a, b) = \text{sign}(a)\text{sign}(b)\min(|a|, |b|) \quad (1)$$

$$g(a, b) = (-1)^u + b \quad (2)$$

where a and b represent input parameters for the f nodes 1111 to 1114 and the g nodes 1121 to 1124, and u represents a decoded information bit or a decoded checking bit.

[00106] For leave nodes in a code tree for polar decoding, the f nodes 1111 to 1114 are the nodes with odd indexes and the g nodes 1121 to 1124 are the nodes with even indexes. The

leave nodes are indexed in such a way that the first node is decoded first in a successive cancelation decoder.

[00107] As described above, during polar encoding, the transmitting device 110 may arrange, on f node and g node respectively, an information bit and a checking bit that is a duplication of the information bit so that they are processed in different manners. Corresponding, during polar decoding, the receiving device 120 may arrange the encoded information bit on one of the f nodes 911 and 912, and arrange the encoded checking bit on one of the g nodes 921 and 922. Because the computations performed at the f nodes 911 to 914 and the computations performed at the g nodes 921 to 924 are not strongly correlated with each other, checking effectiveness may be improved.

[00108] Fig. 12 is a graph 1200 illustrating simulation results for performance evaluation in accordance with some embodiments of the present disclosure. In the simulation, an example solution according to embodiments of the present disclosure is compared with a conventional encoding/decoding solution. In Fig. 12, a curve 1210 refers to a conventional encoding/decoding solution and a curve 1220 refers to the example solution according to embodiments of the present disclosure. In Fig. 12, the horizontal axis refers to SNR and the vertical axis refers to BLER.

[00109] In the simulation, a block size $K=6$ and 6 CRC bits are considered, where there are two new checking bits are introduced. Thus, there are 8 information bits. The two new checking bits are set as bit 8 and bit 6, which are copied from information bit 5 and information bit 4 respectively. A list size of 16 is used. These checking bits are used for tree pruning in case of no repetition is performed. As can be seen from Fig. 12, there is about 0.3dB gain to be achieved. It is also observed that for larger list size, the gain is higher, and this especially useful for URLLC as URLLC may use larger list size to achieve better performance.

[00110] In some embodiments, an apparatus for performing the method 200 (for example, the network device 110 or the terminal devices 120, 130) may comprise respective means for performing the corresponding steps in the method 200. These means may be implemented in any suitable manners. For example, it can be implemented by circuitry or software modules.

[00111] In some embodiments, the apparatus comprises: means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an

initial order, at least one of the plurality of checking bits being a duplication of one of the information bits; means for generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence; means for encoding the interleaved sequence using a polar code; and means for transmitting the encoded sequence to a receiving device.

[00112] In some embodiments, the at least one of the plurality of checking bits is a bit in a downlink control information message.

[00113] In some embodiments, means for generating the interleaved sequence comprises means for changing the initial order to uniformly distribute the plurality of checking bits to generate the interleaved sequence.

[00114] In some embodiments, an apparatus for performing the method 700 (for example, the network device 110 or the terminal devices 120, 130) may comprise respective means for performing the corresponding steps in the method 700. These means may be implemented in any suitable manners. For example, it can be implemented by circuitry or software modules.

[00115] In some embodiments, the apparatus comprises: means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order; means for inserting at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device; means for generating an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking bits; means for encoding the interleaved sequence using a polar code; and means for transmitting the encoded sequence to the receiving device.

[00116] In some embodiments, the at least one dummy bit is determined based on an identity of the receiving device.

[00117] In some embodiments, an apparatus for performing the method 1000 (for example, the network device 110 or the terminal devices 120, 130) may comprise respective means for performing the corresponding steps in the method 1000. These means may be implemented in any suitable manners. For example, it can be implemented by circuitry or software

modules.

[00118] In some embodiments, the apparatus comprises: means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value; means for
5 generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order; means for encoding the interleaved sequence using a polar code; and means for transmitting the encoded sequence to a receiving device.

[00119] In some embodiments, the at least one of the plurality of checking bits is a bit in a downlink control information message.

10 [00120] In some embodiments, the plurality of checking bits are uniformly distributed in the interleaved sequence.

[00121] Fig. 13 is a simplified block diagram of a device 1300 that is suitable for implementing embodiments of the present disclosure. The device 1300 can be considered as a further example embodiment of the network device 110 and the terminal devices 120, 130 as
15 shown in Fig. 1. Accordingly, the device 1300 can be implemented at or as at least a part of the network device 110 or the terminal devices 120, 130.

[00122] As shown, the device 1300 includes a processor 1310, a memory 1320 coupled to the processor 1310, a suitable transmitter (TX) and receiver (RX) 1340 coupled to the processor 1310, and a communication interface coupled to the TX/RX 1340. The memory 1320 stores
20 at least a part of a program 1330. The TX/RX 1340 is for bidirectional communications. The TX/RX 1340 has at least one antenna to facilitate communication, though in practice an Access Node mentioned in this application may have several ones. The communication interface may represent any interface that is necessary for communication with other network elements, such as X2 interface for bidirectional communications between eNBs, S1 interface
25 for communication between a Mobility Management Entity (MME)/Serving Gateway (S-GW) and the eNB, Un interface for communication between the eNB and a relay node (RN), or Uu interface for communication between the eNB and a terminal device.

[00123] The program 1330 is assumed to include program instructions that, when executed by the associated processor 1310, enable the device 1300 to operate in accordance with the
30 embodiments of the present disclosure, as discussed herein with reference to Figs. 2 to 10. The embodiments herein may be implemented by computer software executable by the processor 1310 of the device 1300, or by hardware, or by a combination of software and

hardware. The processor 1310 may be configured to implement various embodiments of the present disclosure. Furthermore, a combination of the processor 1310 and memory 1320 may form processing means 1350 adapted to implement various embodiments of the present disclosure.

5 [00124] The memory 1320 may be of any type suitable to the local technical network and may be implemented using any suitable data storage technology, such as a non-transitory computer readable storage medium, semiconductor based memory devices, magnetic memory devices and systems, optical memory devices and systems, fixed memory and removable memory, as non-limiting examples. While only one memory 1320 is shown in the device
10 1300, there may be several physically distinct memory modules in the device 1300. The processor 1310 may be of any type suitable to the local technical network, and may include one or more of general purpose computers, special purpose computers, microprocessors, digital signal processors (DSPs) and processors based on multicore processor architecture, as non-limiting examples. The device 1300 may have multiple processors, such as an
15 application specific integrated circuit chip that is slaved in time to a clock which synchronizes the main processor.

[00125] The components included in the apparatuses and/or devices of the present disclosure may be implemented in various manners, including software, hardware, firmware, or any combination thereof. In one embodiment, one or more units may be implemented using
20 software and/or firmware, for example, machine-executable instructions stored on the storage medium. In addition to or instead of machine-executable instructions, parts or all of the units in the apparatuses and/or devices may be implemented, at least in part, by one or more hardware logic components. For example, and without limitation, illustrative types of hardware logic components that can be used include Field-programmable Gate Arrays
25 (FPGAs), Application-specific Integrated Circuits (ASICs), Application-specific Standard Products (ASSPs), System-on-a-chip systems (SOCs), Complex Programmable Logic Devices (CPLDs), and the like.

[00126] Generally, various embodiments of the present disclosure may be implemented in hardware or special purpose circuits, software, logic or any combination thereof. Some
30 aspects may be implemented in hardware, while other aspects may be implemented in firmware or software which may be executed by a controller, microprocessor or other computing device. While various aspects of embodiments of the present disclosure are illustrated and described as block diagrams, flowcharts, or using some other pictorial

representation, it will be appreciated that the blocks, apparatus, systems, techniques or methods described herein may be implemented in, as non-limiting examples, hardware, software, firmware, special purpose circuits or logic, general purpose hardware or controller or other computing devices, or some combination thereof.

5 [00127] The present disclosure also provides at least one computer program product tangibly stored on a non-transitory computer readable storage medium. The computer program product includes computer-executable instructions, such as those included in program modules, being executed in a device on a target real or virtual processor, to carry out the process or method as described above with reference to any of Figs. 2, 4 and 7. Generally,
10 program modules include routines, programs, libraries, objects, classes, components, data structures, or the like that perform particular tasks or implement particular abstract data types. The functionality of the program modules may be combined or split between program modules as desired in various embodiments. Machine-executable instructions for program modules may be executed within a local or distributed device. In a distributed device,
15 program modules may be located in both local and remote storage media.

[00128] Program code for carrying out methods of the present disclosure may be written in any combination of one or more programming languages. These program codes may be provided to a processor or controller of a general purpose computer, special purpose computer, or other programmable data processing apparatus, such that the program codes, when
20 executed by the processor or controller, cause the functions/operations specified in the flowcharts and/or block diagrams to be implemented. The program code may execute entirely on a machine, partly on the machine, as a stand-alone software package, partly on the machine and partly on a remote machine or entirely on the remote machine or server.

[00129] The above program code may be embodied on a machine readable medium, which
25 may be any tangible medium that may contain, or store a program for use by or in connection with an instruction execution system, apparatus, or device. The machine readable medium may be a machine readable signal medium or a machine readable storage medium. A machine readable medium may include but not limited to an electronic, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any suitable
30 combination of the foregoing. More specific examples of the machine readable storage medium would include an electrical connection having one or more wires, a portable computer diskette, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), an optical fiber, a

portable compact disc read-only memory (CD-ROM), an optical storage device, a magnetic storage device, or any suitable combination of the foregoing.

[00130] Further, while operations are depicted in a particular order, this should not be understood as requiring that such operations be performed in the particular order shown or in sequential order, or that all illustrated operations be performed, to achieve desirable results. In certain circumstances, multitasking and parallel processing may be advantageous. Likewise, while several specific embodiment details are contained in the above discussions, these should not be construed as limitations on the scope of the present disclosure, but rather as descriptions of features that may be specific to particular embodiments. Certain features that are described in the context of separate embodiments may also be implemented in combination in a single embodiment. Conversely, various features that are described in the context of a single embodiment may also be implemented in multiple embodiments separately or in any suitable sub-combination.

[00131] Although the present disclosure has been described in language specific to structural features and/or methodological acts, it is to be understood that the present disclosure defined in the appended claims is not necessarily limited to the specific features or acts described above. Rather, the specific features and acts described above are disclosed as example forms of implementing the claims.

WHAT IS CLAIMED IS:

1. An electronic device, comprising:

at least one processor; and

at least one memory including computer program code;

5 the at least one memory and the computer program code configured to, with the at least one processor, cause the electronic device to:

generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits being a duplication of one of the information bits;

10 generate an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence;

encode the interleaved sequence using a polar code; and

15 transmit the encoded sequence to a receiving device.

2. The electronic device of Claim 1, wherein the at least one of the plurality of checking bits is a bit in a downlink control information message.

20 3. The electronic device of Claim 1, wherein the plurality of checking bits are uniformly distributed in the interleaved sequence.

4. An electronic device, comprising:

at least one processor; and

25 at least one memory including computer program code;

the at least one memory and the computer program code configured to, with the at least one processor, cause the electronic device to:

generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order;

30 insert at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device;

generate an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way

that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking bits;

encode the interleaved sequence using a polar code; and
transmit the encoded sequence to the receiving device.

5

5. The electronic device of Claim 4, wherein the at least one dummy bit is determined based on an identity of the receiving device.

6. An electronic device, comprising:

10

at least one processor; and

at least one memory including computer program code;

the at least one memory and the computer program code configured to, with the at least one processor, cause the electronic device to:

15 generate an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value;

generate an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order;

encode the interleaved sequence using a polar code; and

20

transmit the encoded sequence to a receiving device.

7. The electronic device of Claim 6, wherein the at least one of the plurality of checking bits is a bit in a downlink control information message.

25

8. The electronic device of Claim 6, wherein the plurality of checking bits are uniformly distributed in the interleaved sequence.

9. A method for communications, comprising:

30 generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits being a duplication of one of the information bits;

generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different

manners during polar encoding of the interleaved sequence;
encoding the interleaved sequence using a polar code; and
transmitting the encoded sequence to a receiving device.

5 10. The method of Claim 9, wherein the at least one of the plurality of checking bits is
a bit in a downlink control information message.

11. The method of Claim 9, wherein the plurality of checking bits are uniformly
distributed in the interleaved sequence.

10

12. A method for communications, comprising:

generating an initial sequence comprising a plurality of information bits and a plurality
of checking bits in an initial order;

15 inserting at least one dummy bit into the initial sequence, a value of each dummy bit
known to a receiving device;

generating an interleaved sequence of the plurality of information bits, the plurality of
checking bits and the at least one dummy bit by changing the initial order in such a way that
the at least one dummy bit are arranged before the plurality of information bits and the
plurality of checking bits;

20 encoding the interleaved sequence using a polar code; and
transmitting the encoded sequence to the receiving device.

13. The method of Claim 12, wherein the at least one dummy bit is determined based
on an identity of the receiving device.

25

14. A method for communications, comprising:

generating an initial sequence comprising a plurality of information bits and a plurality
of checking bits in an initial order, at least one of the plurality of checking bits having a
predefined value;

30 generating an interleaved sequence of the plurality of information bits and the plurality
of checking bits by changing the initial order;

encoding the interleaved sequence using a polar code; and
transmitting the encoded sequence to a receiving device.

15. The method of Claim 14, wherein the at least one of the plurality of checking bits is a bit in a downlink control information message.

16. The method of Claim 14, wherein the plurality of checking bits are uniformly
5 distributed in the interleaved sequence.

17. A computer readable medium having instructions stored thereon, the instructions, when executed on at least one processor of a device, causing the device to perform at least the following:

10 generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits being a duplication of one of the information bits;

generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the
15 plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence;

encoding the interleaved sequence using a polar code; and
transmitting the encoded sequence to a receiving device.

20 18. A computer readable medium having instructions stored thereon, the instructions, when executed on at least one processor of a device, causing the device to perform at least the following:

generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order;

25 inserting at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device;

generating an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such a way that the at least one dummy bit are arranged before the plurality of information bits and the
30 plurality of checking bits;

encoding the interleaved sequence using a polar code; and
transmitting the encoded sequence to the receiving device.

19. A computer readable medium having instructions stored thereon, the instructions,

when executed on at least one processor of a device, causing the device to perform at least the following:

generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value;

generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order;

encoding the interleaved sequence using a polar code; and

transmitting the encoded sequence to a receiving device.

20. An apparatus for communications, comprising:

means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits being a duplication of one of the information bits;

means for generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order in such a way that the at least one of the plurality of checking bits and the one of the information bits are to be processed in different manners during polar encoding of the interleaved sequence;

means for encoding the interleaved sequence using a polar code; and

means for transmitting the encoded sequence to a receiving device.

21. The apparatus of Claim 20, wherein the at least one of the plurality of checking bits is a bit in a downlink control information message.

22. The apparatus of Claim 20, wherein the plurality of checking bits are uniformly distributed in the interleaved sequence.

23. An apparatus for communications, comprising:

means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order;

means for inserting at least one dummy bit into the initial sequence, a value of each dummy bit known to a receiving device;

means for generating an interleaved sequence of the plurality of information bits, the plurality of checking bits and the at least one dummy bit by changing the initial order in such

a way that the at least one dummy bit are arranged before the plurality of information bits and the plurality of checking bits;

means for encoding the interleaved sequence using a polar code; and

means for transmitting the encoded sequence to the receiving device.

5

24. The apparatus of Claim 23, wherein the at least one dummy bit is determined based on an identity of the receiving device.

25. An apparatus for communications, comprising:

10

means for generating an initial sequence comprising a plurality of information bits and a plurality of checking bits in an initial order, at least one of the plurality of checking bits having a predefined value;

means for generating an interleaved sequence of the plurality of information bits and the plurality of checking bits by changing the initial order;

15

means for encoding the interleaved sequence using a polar code; and

means for transmitting the encoded sequence to a receiving device.

26. The apparatus of Claim 25, wherein the at least one of the plurality of checking bits is a bit in a downlink control information message.

20

27. The apparatus of Claim 25, wherein the plurality of checking bits are uniformly distributed in the interleaved sequence.

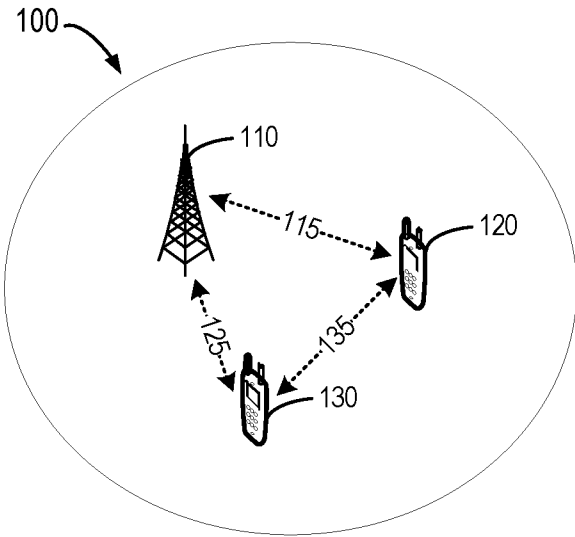


Fig. 1

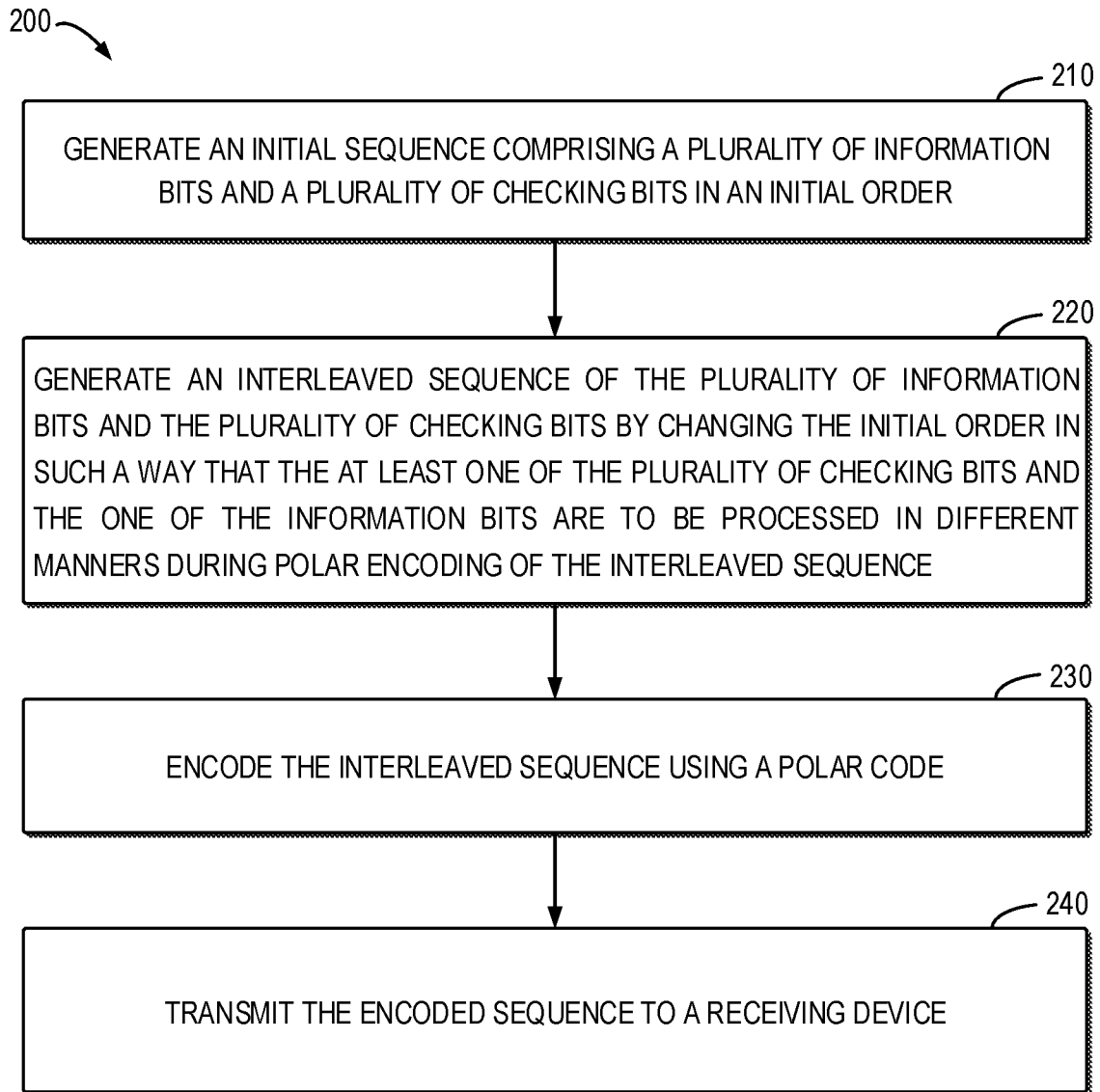


Fig. 2

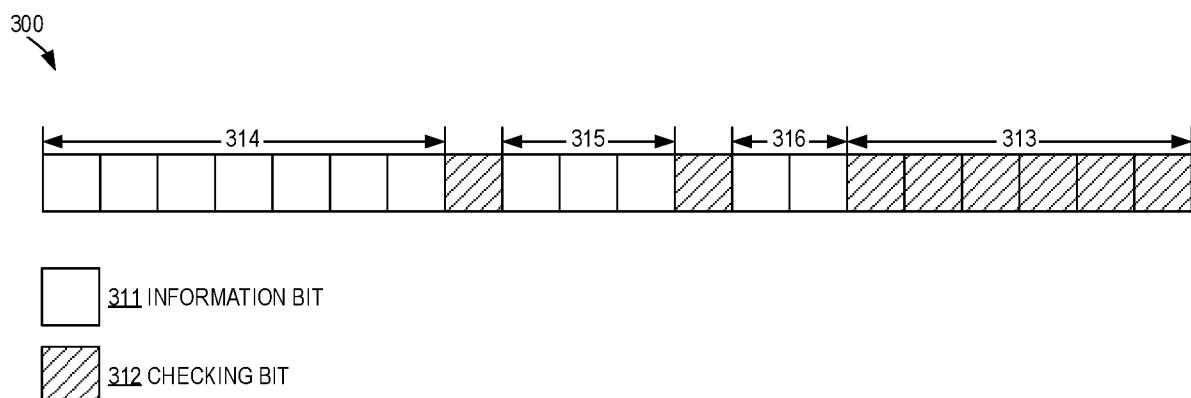


Fig. 3

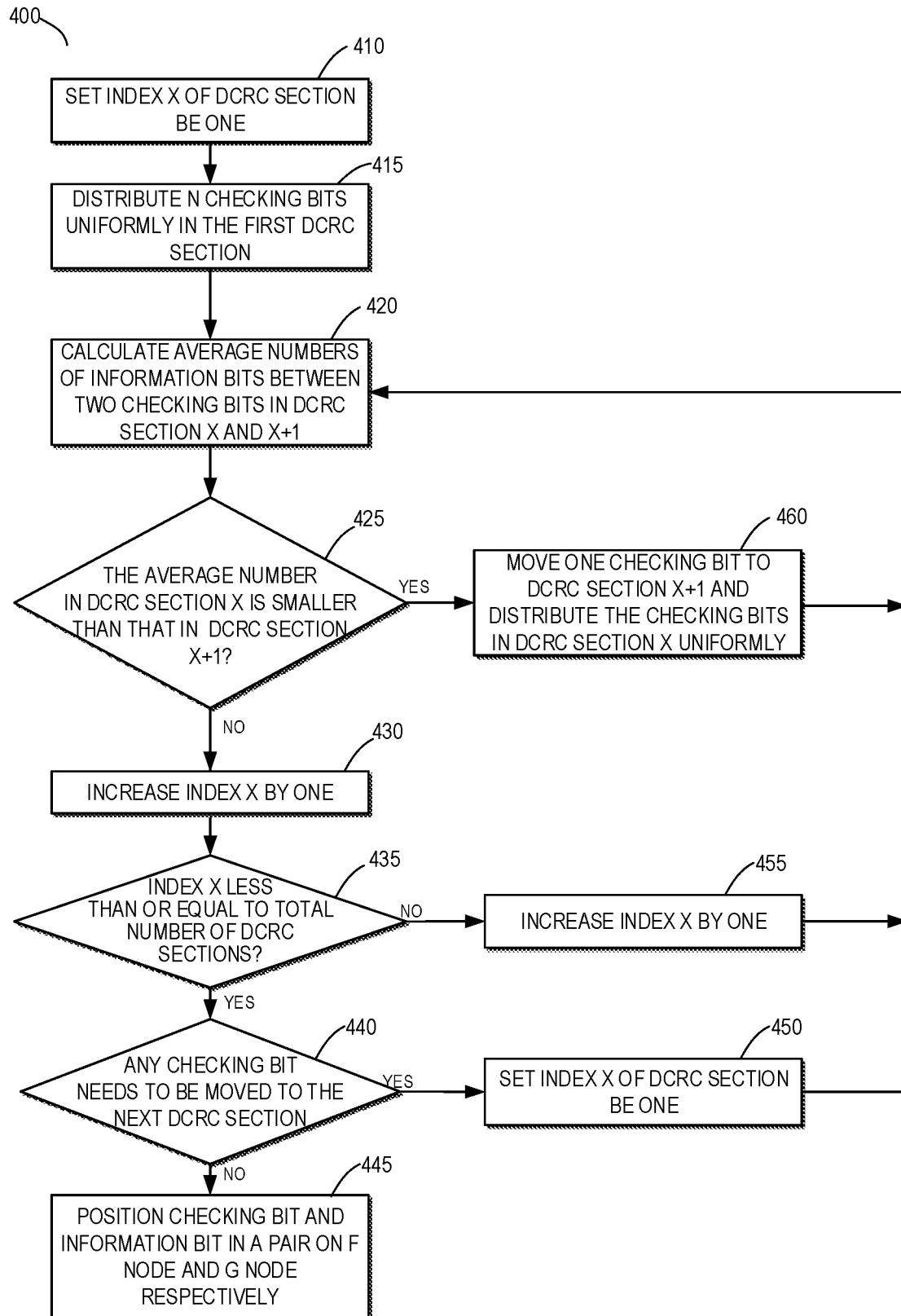


Fig. 4

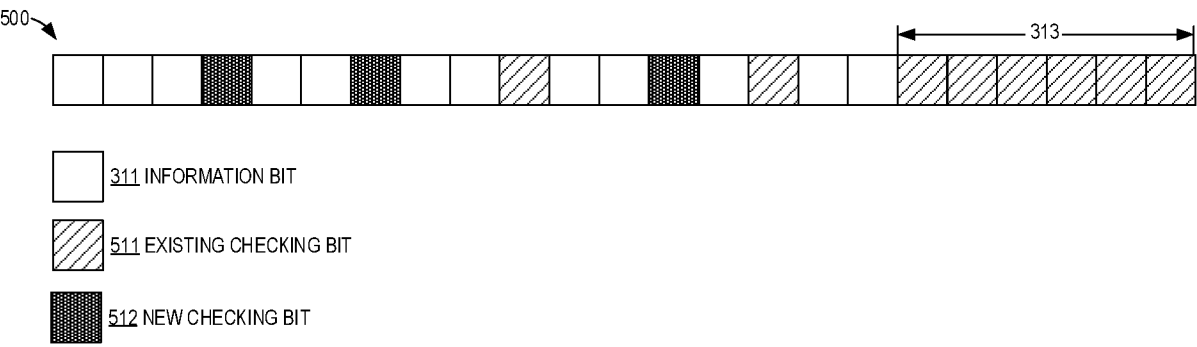


Fig. 5

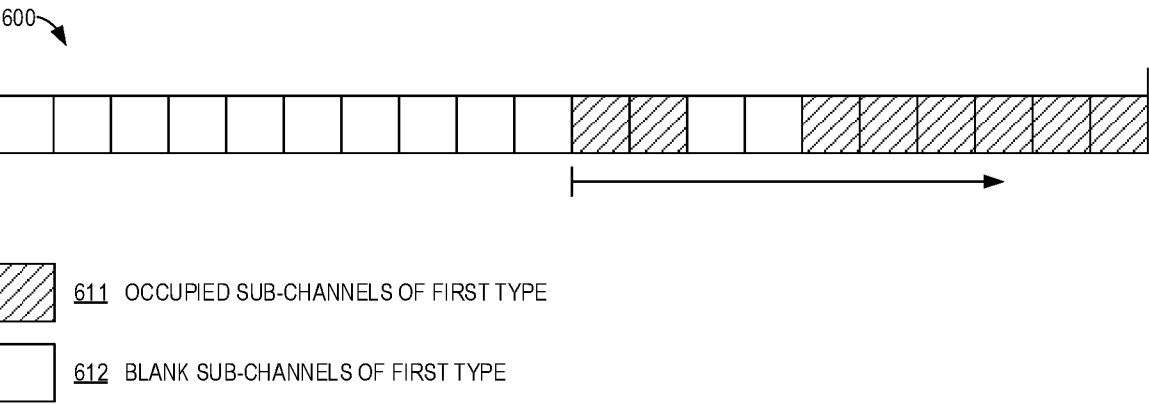


Fig. 6A

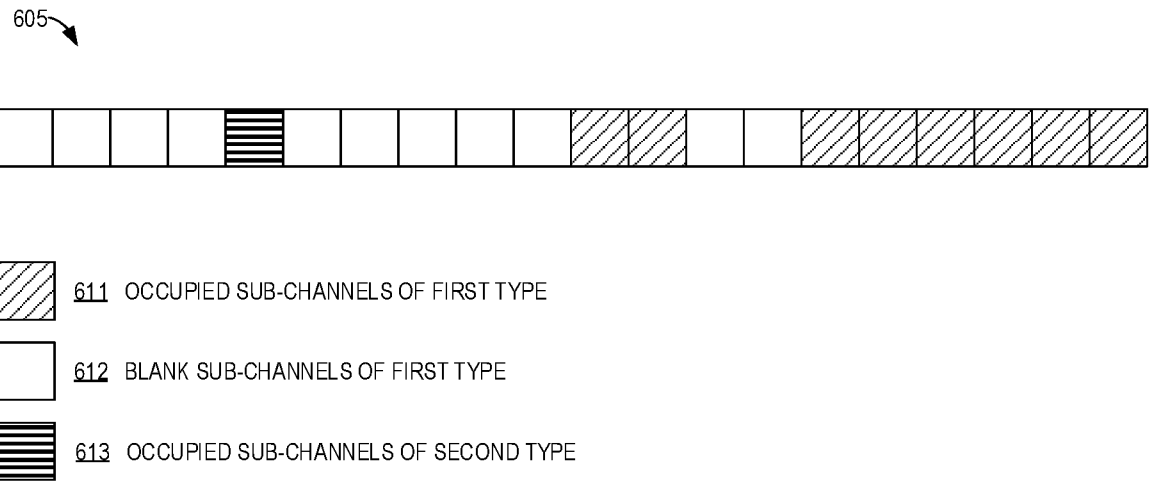


Fig. 6B

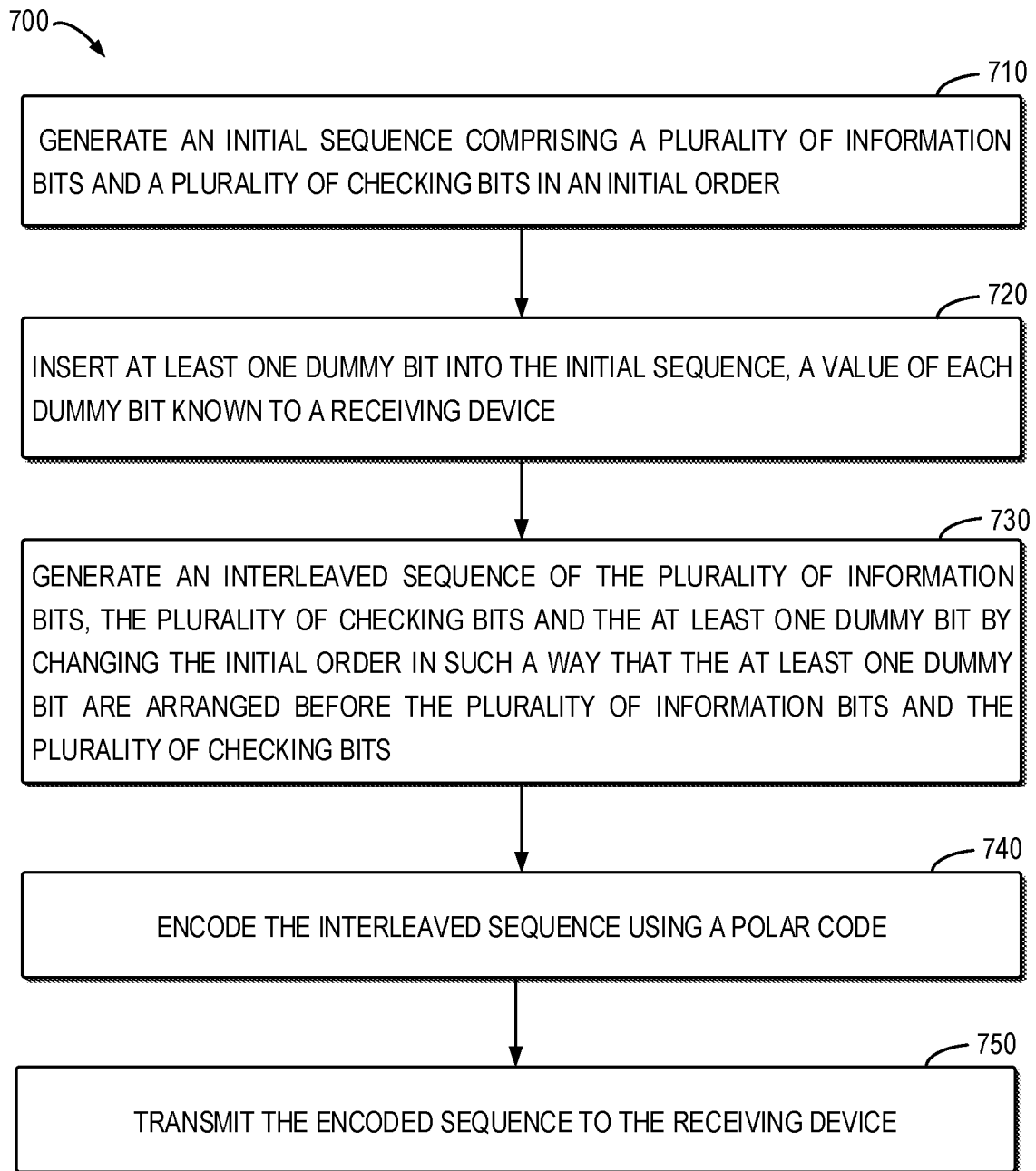


Fig. 7

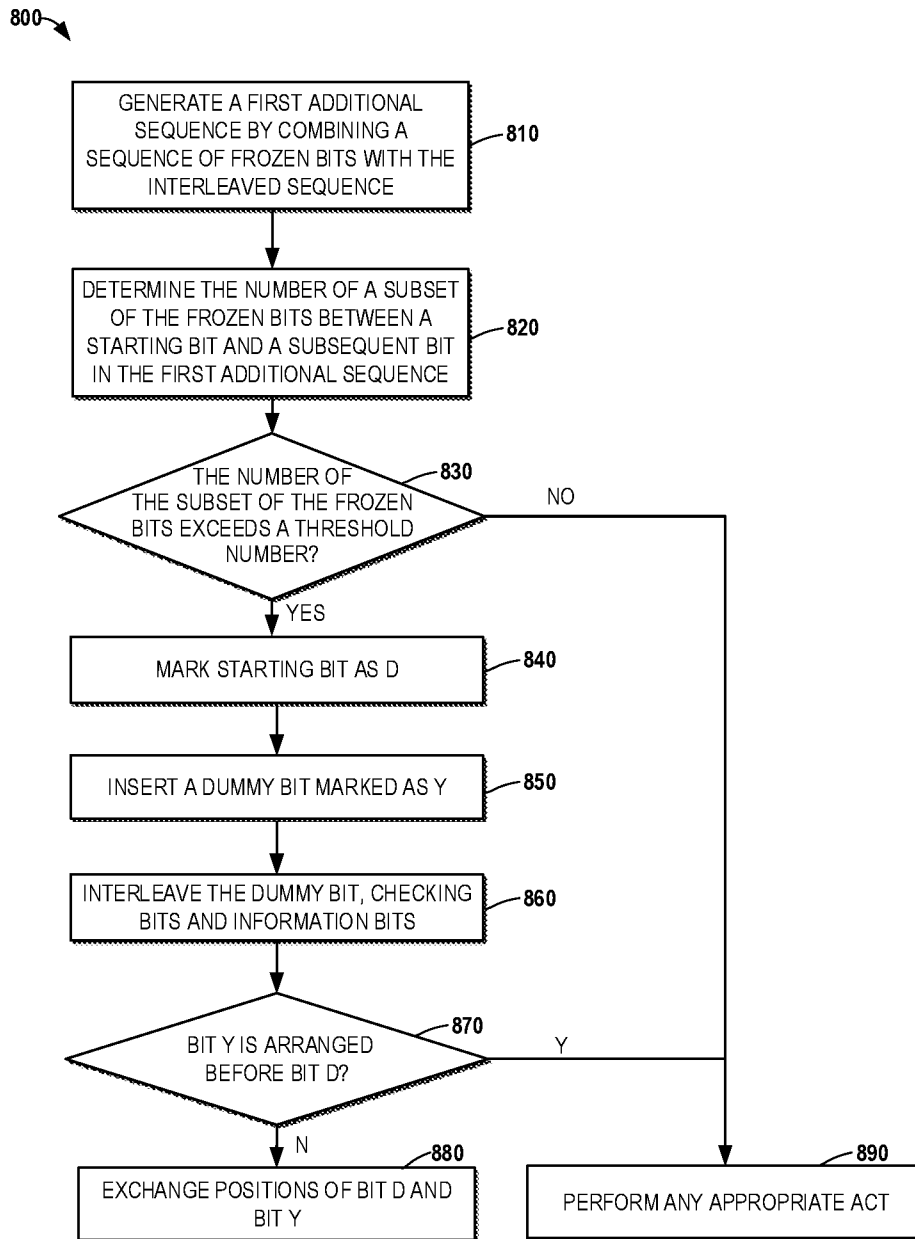


Fig. 8

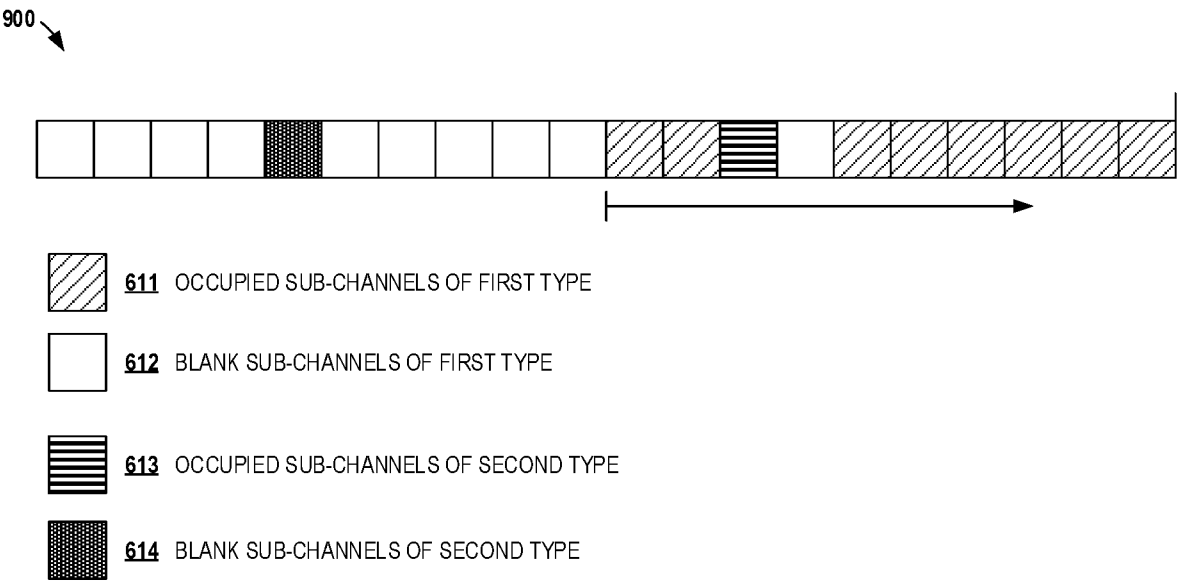


Fig. 9

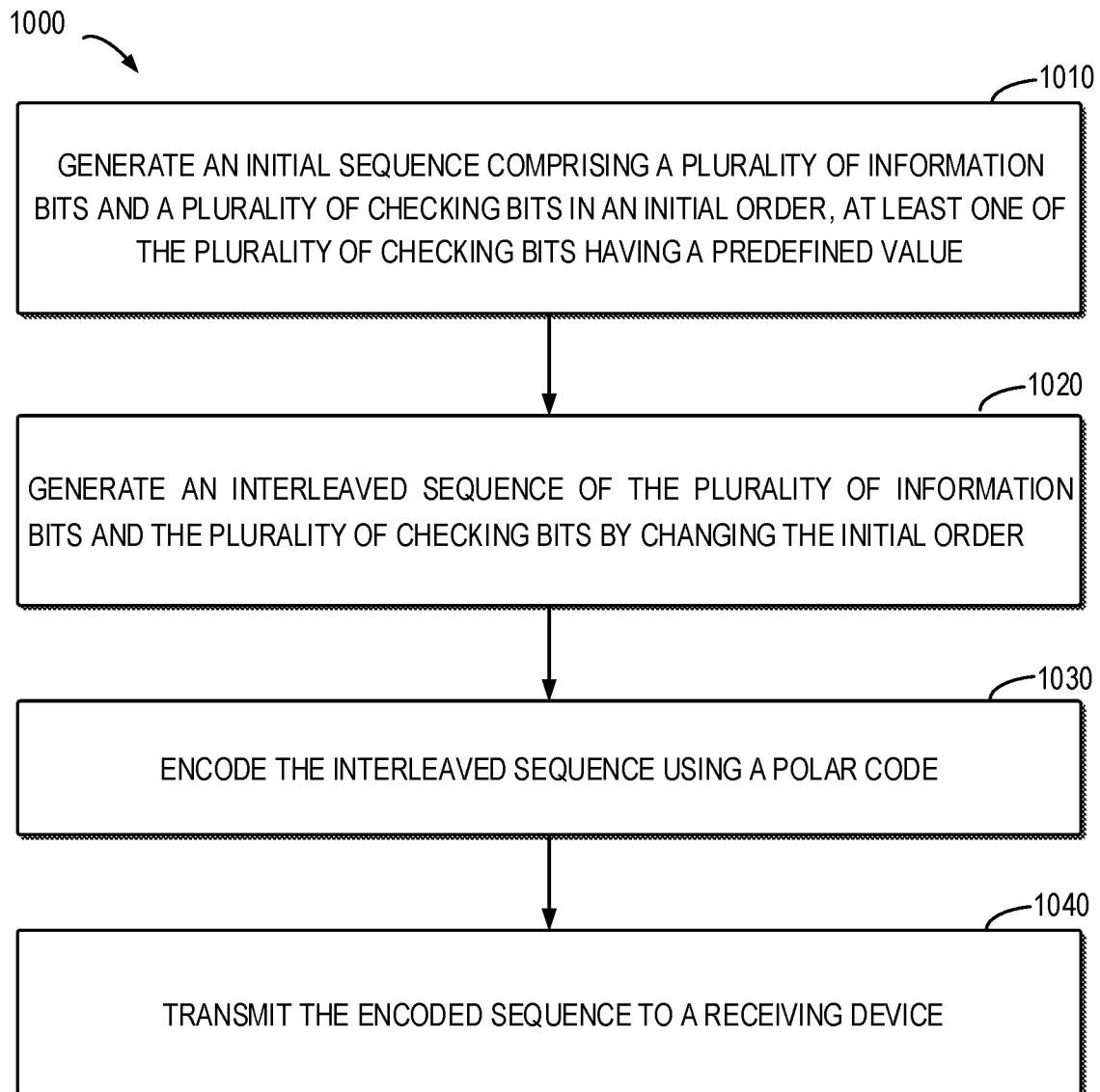


Fig. 10

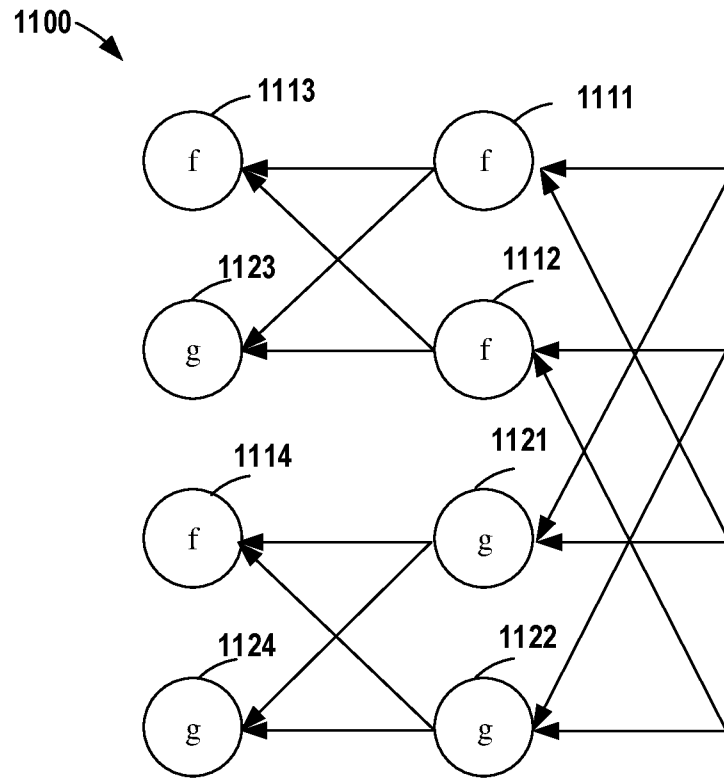


Fig. 11

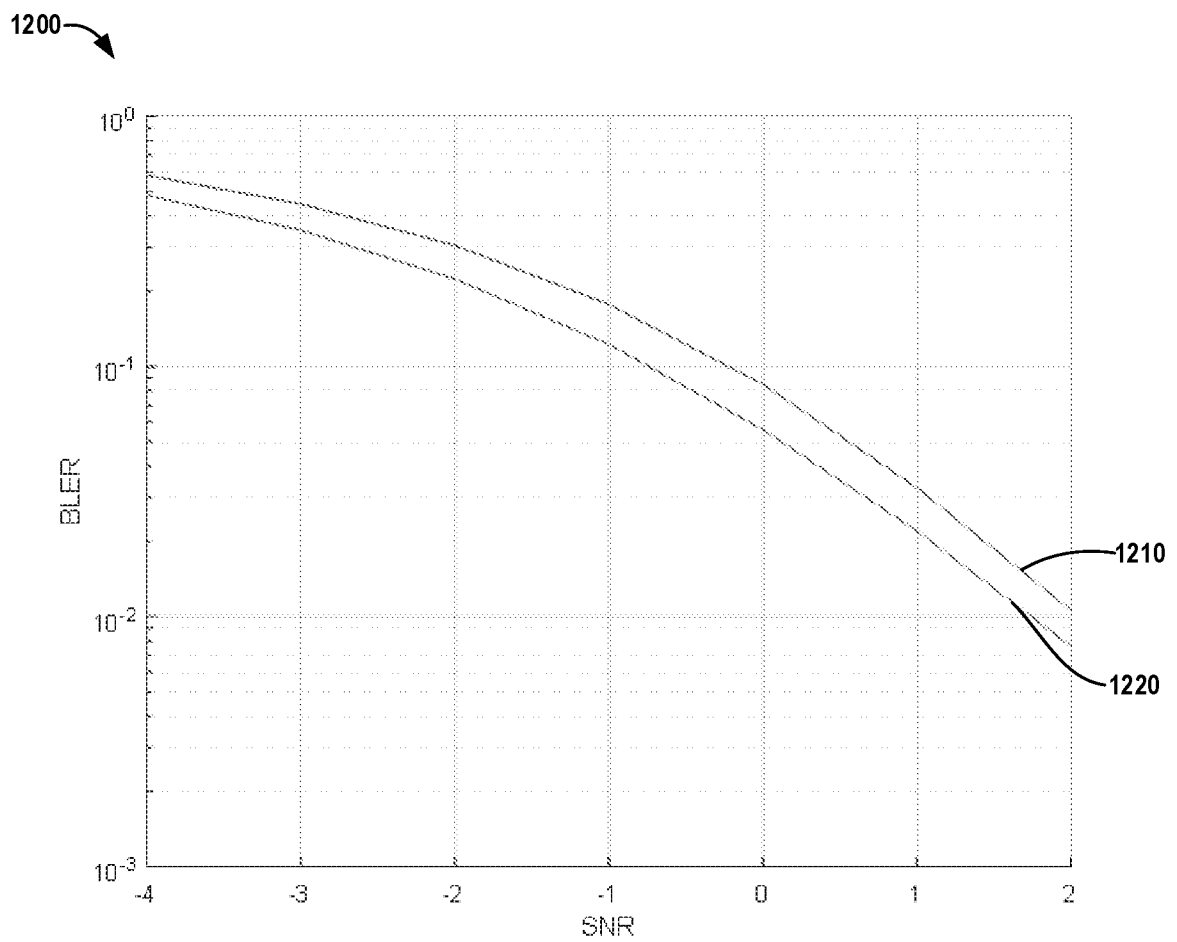


Fig. 12

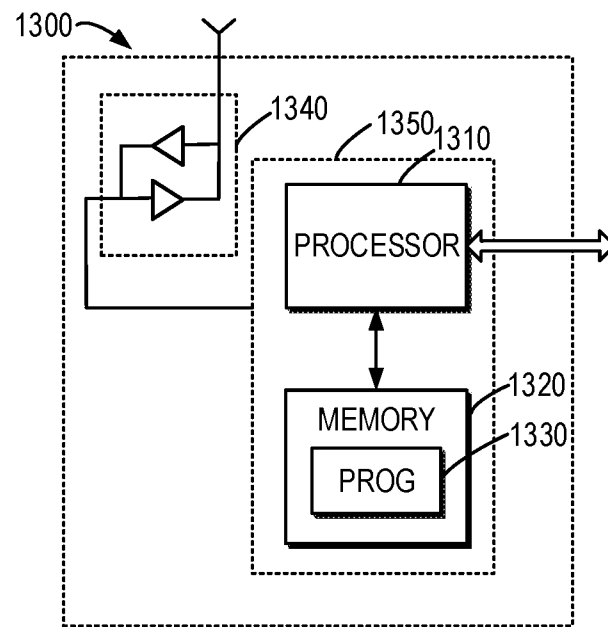


Fig. 13

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/071677

A. CLASSIFICATION OF SUBJECT MATTER		
H03M 13/13(2006.01)i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
H03M; H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
CNPAT;CNKI;WPI;EPODOC;3GPP;polar, dci, crc, checking bits, info+ bits, duplication, copy, dummy, frozen, front, beginning, fixed value, predefined value		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	NOKIA et al. "3GPP TSG RAN WG1 Meeting #89 R1-1708833" <i>Design details of distributed CRC</i> , 19 May 2017 (2017-05-19), section 2, figure 1	4-8, 12-16, 18-19, 23-27
Y	QUALCOMM INCORPORATED. "3GPP TSG RAN WG1 Meeting #91 R1-1721428" <i>DCI CRC Initialization and Masking</i> , 01 December 2017 (2017-12-01), section 3, figures 2-3	4-5, 12-13, 18, 23-24
Y	MEDIATEK INC. "3GPP TSG RAN WG1 Meeting #87 R1-1612121" <i>On 2-stage Downlink Control Information for NR</i> , 18 November 2016 (2016-11-18), sections 2.2-2.3	6-8, 14-16, 19, 25-27
A	NOKIA et al. "3GPP TSG RAN WG1 Meeting #89 R1-1708833" <i>Design details of distributed CRC</i> , 19 May 2017 (2017-05-19), section 2, figure 1	1-3, 9-11, 17, 20-22
A	US 2014173376 A1 (SUNGKYUNKWAN UNIVERSITY RESEARCH & BUSINESS FOUNDATION ET AL.) 19 June 2014 (2014-06-19) the whole document	1-27
☒ Further documents are listed in the continuation of Box C. ☒ See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
17 September 2019		26 September 2019
Name and mailing address of the ISA/CN		Authorized officer
National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088 China		ZHANG, Caixa
Facsimile No. (86-10)62019451		Telephone No. 86-(10)-53961804

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2019/071677

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2018199317 A1 (MEDIATEK INC.) 12 July 2018 (2018-07-12) the whole document	1-27

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2019/071677

Patent document cited in search report			Publication date (day/month/year)	Patent family member(s)			Publication date (day/month/year)
US	2014173376	A1	19 June 2014	US	2017187396	A1	29 June 2017
				WO	2014092502	A1	19 June 2014
				KR	20140077492	A	24 June 2014
US	2018199317	A1	12 July 2018	CN	109314952	A	05 February 2019
				WO	2018130151	A1	19 July 2018