



(12) **EUROPEAN PATENT APPLICATION**
published in accordance with Art. 153(4) EPC

(43) Date of publication:
05.07.2023 Bulletin 2023/27

(51) International Patent Classification (IPC):
H03F 1/02 (2006.01) H03F 1/42 (2006.01)
H03F 3/21 (2006.01)

(21) Application number: **22871171.9**

(86) International application number:
PCT/CN2022/108110

(22) Date of filing: **27.07.2022**

(87) International publication number:
WO 2023/045544 (30.03.2023 Gazette 2023/13)

(84) Designated Contracting States:
AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HR HU IE IS IT LI LT LU LV MC MK MT NL NO PL PT RO RS SE SI SK SM TR
Designated Extension States:
BA ME
Designated Validation States:
KH MA MD TN

(72) Inventors:
• **CAI, Liyuan**
Shenzhen, Guangdong 518052 (CN)
• **XUAN, Kai**
Shenzhen, Guangdong 518052 (CN)
• **GUO, Jiashuai**
Shenzhen, Guangdong 518052 (CN)

(30) Priority: **23.09.2021 CN 202111118024**

(74) Representative: **Bayramoglu et al.**
Mira Office
Kanuni Sultan Süleyman Boulevard 5387
Street Beytepe, floor 12, no:50
06800 Cankaya, Ankara (TR)

(71) Applicant: **Lansus Technologies Inc.**
Shenzhen, Guangdong 518052 (CN)

(54) **BROADBAND DOHERTY POWER AMPLIFIER AND IMPLEMENTATION METHOD**

(57) The present disclosure provides a broadband Doherty power amplifier, including a power divider, a carrier power amplifier circuit, a peak power amplifier circuit, and a load modulation network. The carrier power amplifier circuit includes a carrier input matching circuit, a carrier power amplifier, and a carrier output matching circuit. The peak power amplifier circuit includes a peak input matching circuit, a peak power amplifier and a peak output matching circuit. A resistance value of a system load is Z_L . An output impedance of the carrier output matching circuit is Z_m and meets $Z_m = Z_L(n+1)$. An output impedance of the peak output matching circuit is Z_p and meets $Z_p = Z_L(n+1)/n$. The load modulation network is configured to set an impedance of a combination point to be Z_Q , whose resistance value is Z_L . A method of implementing a broadband Doherty power amplifier is further provided. Technical solutions of the present disclosure allow a load modulation network structure to remove a quarter-wave impedance transformation line after combination point, thereby realizing a simple circuit structure and a high operating bandwidth.

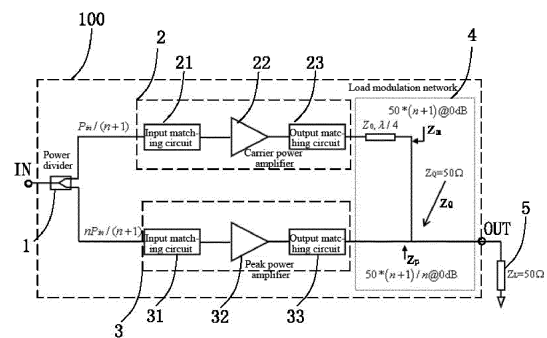


FIG. 2

Description

TECHNICAL FIELD

[0001] The present disclosure relates to the technical field of circuits, and in particular to a broadband Doherty power amplifier and an implementation method for a broadband Doherty power amplifier.

BACKGROUND

[0002] Currently, with the development of wireless communication technology, especially the widely use of fifth generation communication technology, radio frequency power amplifiers are more and more important in a mobile phone communication system since performance of the radio frequency power amplifiers greatly affects working states of the wireless communication system. As the communication technology advances, a modulation signal shows characteristics of a high peak-to-average ratio. The emergence of the fifth generation communication technology puts forward higher requirements on bandwidths of power amplifiers. Therefore, the radio frequency power amplifiers used in the fifth generation communication technology are generally a high-efficiency broadband Doherty power amplifier.

[0003] In the related art, the broadband Doherty power amplifier typically includes a power divider, a carrier power amplifier circuit, a peak power amplifier circuit, and a load modulation network. The carrier power amplifier circuit includes a carrier input matching circuit, a carrier power amplifier, and a carrier output matching circuit sequentially connected in series. The peak power amplifier circuit includes a peak input matching circuit, a peak power amplifier, and a peak output matching circuit sequentially connected in series. Referring to FIG. 1, FIG. 1 illustrates the broadband Doherty power amplifier in the related art. An input terminal of the carrier power amplifier circuit, an input terminal of the peak power amplifier circuit, and the load modulation network each uses a quarter-wave impedance transformation line.

[0004] However, impedance transformation lines in the related art limit operating bandwidths of the power amplifiers, so that the power amplifiers each only has a narrow operating bandwidth, which fails to provide large bandwidth for the fifth generation communication system. Therefore, in the related art, a quarter-wave impedance transformation ratio is reduced, and an equivalent impedance transformer circuit is used to replace a quarter wavelength for impedance transformation, or a load modulation structure having no transmission line is used to remove the quarter-wave impedance transformation line. These two solutions in the related art widen the bandwidth to a certain extent, but increase complexity of the power amplifier circuit.

[0005] Therefore, it is necessary to provide a novel broadband Doherty power amplifier and an implementation method to solve the foregoing problems.

SUMMARY

[0006] In view of shortcomings in the related art, the present disclosure provides a broadband Doherty power amplifier and an implementation method for a broadband Doherty power amplifier, which allows a load modulation network structure to remove a quarter-wave impedance transformation line after combination point, thereby realizing a simple circuit structure and a high operating bandwidth.

[0007] In order to solve the foregoing problems, in a first aspect, one embodiment of the present disclosure provides a broadband Doherty power amplifier, including a power divider, a carrier power amplifier circuit, a peak power amplifier circuit, and a load modulation network. An input terminal of the power divider serves as an input terminal of the broadband Doherty power amplifier, two output terminals of the power divider are respectively connected to an input terminal of the carrier power amplifier circuit and an input terminal of the peak power amplifier circuit, an output terminal of the carrier power amplifier circuit is connected to a first input terminal of the load modulation network, an output terminal of the peak power amplifier circuit is connected to a second input terminal of the load modulation network, and an output terminal of the load modulation network serves as an output terminal of the broadband Doherty power amplifier for connecting to a system load.

[0008] The carrier power amplifier circuit includes a carrier input matching circuit, a carrier power amplifier, and a carrier output matching circuit sequentially connected in series. An input terminal of the carrier input matching circuit is connected to the output terminal of the power divider, and an output terminal of the carrier output matching circuit is connected to the first input terminal of the load modulation network.

[0009] The peak power amplifier circuit includes a peak input matching circuit, a peak power amplifier, and a peak output matching circuit sequentially connected in series. An input terminal of the peak input matching circuit is connected to the output terminal of the power divider, and an output terminal of the peak output matching circuit is connected to the second input terminal of the load modulation network.

[0010] A resistance value of the system load is Z_L .

[0011] The power divider is configured to respectively allocate power to the carrier power amplifier circuit and the peak power amplifier circuit according to a power division ratio of 1:n.

[0012] The carrier input matching circuit is configured to match a terminal impedance of the input terminal of the carrier input matching circuit to an input impedance of the carrier power amplifier, the carrier output matching circuit is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier. An output impedance of the carrier output matching circuit is Z_m , and a following formula is satisfied:

$$Z_m = Z_L(n+1);$$

and n is a positive number.

[0013] The peak input matching circuit is configured to match a terminal impedance of the input terminal of the peak input matching circuit to an input impedance of the peak power amplifier, the peak output matching circuit is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier. An output impedance of the peak output matching circuit is Z_p , and a following formula is satisfied:

$$Z_p = Z_L(n+1)/n.$$

[0014] The load modulation network is configured to perform power combination on an output signal of the carrier output matching circuit and an output signal of the peak input matching circuit, and is configured to set an impedance Z_Q of a power amplifier combination point, where a resistance value of the impedance Z_Q is Z_L .

[0015] Optionally, the resistance value Z_L of the system load is 50 ohms.

[0016] Optionally, the power division ratio is 1:1.5, a resistance value of Z_m is 125 ohms, a resistance value of Z_p is 83.3 ohms, and the resistance value of the impedance Z_Q is 50 ohms.

[0017] Optionally, the carrier power amplifier circuit is a class AB power amplifier.

[0018] Optionally, the carrier power amplifier circuit is implemented by a transistor.

[0019] Optionally, the peak power amplifier circuit is a class C power amplifier.

[0020] Optionally, the peak power amplifier circuit is implemented by a transistor.

[0021] Optionally, the power divider is an in-phase power divider or a phase quadrature power divider.

[0022] Optionally, the carrier input matching circuit and the peak input matching circuit each includes a corresponding phase compensation circuit.

[0023] In a second aspect, one embodiment of the present disclosure further provides an implementation method for a broadband Doherty power amplifier. The broadband Doherty power amplifier includes a power divider, a carrier power amplifier circuit, a peak power amplifier circuit, and a load modulation network. An input terminal of the power divider serves as an input terminal of the broadband Doherty power amplifier, two output terminals of the power divider are respectively connected to an input terminal of the carrier power amplifier circuit and an input terminal of the peak power amplifier circuit, an output terminal of the carrier power amplifier circuit is connected to a first input terminal of the load modulation network, an output terminal of the peak power amplifier

circuit is connected to a second input terminal of the load modulation network, and an output terminal of the load modulation network serves as an output terminal of the broadband Doherty power amplifier for connecting to a system load.

[0024] The carrier power amplifier circuit includes a carrier input matching circuit, a carrier power amplifier, and a carrier output matching circuit sequentially connected in series. An input terminal of the carrier input matching circuit is connected to the output terminal of the power divider, and an output terminal of the carrier output matching circuit is connected to the first input terminal of the load modulation network.

[0025] The peak power amplifier circuit includes a peak input matching circuit, a peak power amplifier, and a peak output matching circuit sequentially connected in series. An input terminal of the peak input matching circuit is connected to the output terminal of the power divider, and an output terminal of the peak output matching circuit is connected to the second input terminal of the load modulation network. The method implementation includes the following steps:

S1. debugging the power divider to allocate power to the carrier power amplifier circuit and the peak power amplifier circuit according to a power division ratio of 1:n;

S2. debugging the carrier input matching circuit to match a terminal impedance of the input terminal of the carrier input matching circuit to an input impedance of the carrier power amplifier, and debugging the carrier output matching circuit to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier, where an output impedance of the carrier output matching circuit is Z_m , the resistance value of the system load is Z_L , and a following formula being satisfied:

$$Z_m = Z_L(n+1);$$

where n is a positive number;

S3. debugging the peak input matching circuit to match a terminal impedance of an input terminal of the peak input matching circuit to an input impedance of the peak power amplifier, and debugging the peak output matching circuit to match a resistance value of the system load to an output impedance of the carrier power amplifier, where an output impedance of the peak output matching circuit is Z_p , and a following formula being satisfied:

$$Z_p = Z_L(n+1)/n;$$

and

S4. debugging the load modulation network to perform power combination on an output signal of the carrier output matching circuit and an output signal of the peak input matching circuit, and setting an impedance Z_Q of a power amplifier circuit, where a resistance value of Z_Q is Z_L .

[0026] Compared with the related art, according to the broadband Doherty power amplifier and the implementation method for the broadband Doherty power amplifier provided by the present disclosure, the carrier input matching circuit matches the terminal impedance of its input terminal to the input impedance of the carrier power amplifier, and the peak input matching circuit matches the terminal impedance of its input terminal to the input impedance of the peak power amplifier. Moreover, the load modulation network performs power combination on the output signal of the carrier output matching circuit and the output signal of the peak input matching circuit, and the impedance of the power amplifier combination point is set to be equal to the resistance value of the system load, so that the load modulation network structure can remove the quarter-wave impedance transformation line after the combination point, which allows the broadband Doherty power amplifier to have a simple circuit structure and a high operating bandwidth.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The present disclosure is described below with reference to accompanying drawings. In conjunction with the accompanying drawings, the foregoing or other aspects of the present disclosure is made clearer and more readily understood. In the drawings:

FIG. 1 is a structural schematic diagram of an application circuit of an asymmetric Doherty power amplifier in the related technology.

FIG. 2 is a structural schematic diagram of an application circuit of a broadband Doherty power amplifier according to the present disclosure.

FIG. 3 is a structural schematic diagram of an application circuit of one embodiment of a broadband Doherty power amplifier according to the present disclosure.

FIG. 4 is a schematic flowchart of an implementation method for a broadband Doherty power amplifier according to one embodiment of the present disclosure.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0028] Specific embodiments of the present disclosure are described in details below with reference to the accompanying drawings.

[0029] The specific embodiments described herein are specific implementations of the present disclosure, and are used to illustrate concepts of the present disclosure,

which are explanatory and exemplary, and should not be interpreted as limiting implementations and scopes of the present disclosure. In addition to the embodiments described herein, based on contents disclosed in the claims and specifications of the present disclosure, those skilled in the art can adopt other technical solutions. Any substitution or modification made to the embodiments described herein is within the protection scope of the present disclosure.

[0030] The present disclosure provides a broadband Doherty power amplifier 100.

[0031] Referring to FIG. 2, FIG. 2 is a structural schematic diagram of an application circuit of a broadband Doherty power amplifier according to the present disclosure.

[0032] In circuit applications, the broadband Doherty power amplifier 100 is connected to a system load 5. The system load 5 has a resistance value Z_L . In this embodiment, the resistance value Z_L of the system load 5 is 50 ohms.

[0033] Specifically, the broadband Doherty power amplifier 100 includes a power divider 1, a carrier power amplifier circuit 2, a peak power amplifier circuit 3, and a load modulation network 4.

[0034] The power divider 1 is configured to respectively allocate power to the carrier power amplifier circuit 2 and the peak power amplifier circuit 3 according to a power division ratio of 1:n. The power divider 1 determines a specific power division ratio according to the requirement of a modulation signal of the broadband Doherty power amplifier 100. In one embodiment, the power divider 1 is an in-phase power divider or a phase quadrature power divider.

[0035] The carrier power amplifier circuit 2 is a class AB power amplifier. In one embodiment, the carrier power amplifier circuit 2 is implemented by a transistor. Specifically, the carrier power amplifier circuit 2 includes a carrier input matching circuit 21, a carrier power amplifier 22, and a carrier output matching circuit 23 sequentially connected in series.

[0036] The carrier input matching circuit 21 is configured to match a terminal impedance of its input terminal to an input impedance of the carrier power amplifier 22.

[0037] The carrier output matching circuit 23 is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier 22. An output impedance of the carrier output matching circuit 23 is Z_m , and a following formula is satisfied:

$$Z_m = Z_L(n+1);$$

[0038] Specifically, n is a positive number.

[0039] In one embodiment, a corresponding phase compensation circuit is disposed in the carrier input matching circuit 21.

[0040] The peak power amplifier circuit 3 is a class C power amplifier. In one embodiment, the peak power am-

plifier circuit 3 is implemented by a transistor. The peak power amplifier circuit 3 includes a peak input matching circuit 31, a peak power amplifier 32, and a peak output matching circuit 33 sequentially connected in series.

[0041] The peak input matching circuit 31 is configured to match a terminal impedance of its input terminal to an input impedance of the peak power amplifier 32.

[0042] The peak output matching circuit 33 is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier 32. An output impedance of the peak output matching circuit 33 is Z_p , and a following formula is satisfied:

$$Z_p = Z_L(n+1)/n.$$

[0043] In one embodiment, a corresponding phase compensation circuit is disposed in the peak input matching circuit 31.

[0044] The load modulation network 4 is configured to perform power combination on an output signal of the carrier output matching circuit 23 and an output signal of the peak input matching circuit 31, and is configured to set an impedance Z_Q of the power amplifier combination point. The resistance value of Z_Q is Z_L .

[0045] Specifically, the circuit connection relationship is described below.

[0046] An input terminal of the power divider 1 is served as an input terminal IN of the broadband Doherty power amplifier 100. Two output terminals of the power divider 1 are respectively connected to an input terminal of the carrier power amplifier circuit 2 and an input terminal of the peak power amplifier circuit 3.

[0047] An output terminal of the carrier power amplifier circuit 2 is connected to a first input terminal of the load modulation network 4. Specifically, the input terminal of the carrier input matching circuit 21 is connected to one output terminal of the power divider 1, and the output terminal of the carrier output matching circuit 23 is connected to the first input terminal of the load modulation network 4.

[0048] An output terminal of the peak power amplifier circuit 3 is connected to a second input terminal of the load modulation network 4. Specifically, the input terminal of the peak input matching circuit 31 is connected to the other output terminal of the power divider 1, and the output terminal of the peak output matching circuit 33 is connected to the second input terminal of the load modulation network 4.

[0049] An output terminal of the load modulation network 4 is served as an output terminal OUT of the broadband Doherty power amplifier 100 for connecting to the system load 5.

[0050] It should be noted that the power divider 1, the carrier power amplifier circuit 2, the peak power amplifier circuit 3, and the load modulation network 4 described herein are common circuits or modules used in the art. In addition, their indicators and parameters can be ad-

justed according to actual applications, which is not detailed herein.

[0051] The working principle of the broadband Doherty power amplifier 100 is described below.

[0052] In the case of a saturated power, the output impedance of the carrier power amplifier 22 is set to be Z_0 . Z_0 is a characteristic impedance of the transmission line used in the broadband Doherty power amplifier 100. According to the power division ratio of 1:n of the power divider 1, it can be known, from the power formula $P=U^2/R$, that the ratio of the output impedance of the carrier power amplifier 22 to the output impedance of the peak power amplifier 32 is n:1. Therefore, the output impedance of the peak power amplifier 32 is

$$Z_Q = \frac{Z_m * Z_p}{Z_m + Z_p} = \frac{Z_0}{n+1}.$$

In this case, the impedance of the power amplifier combination point is $Z_Q = Z_0/n$. This impedance is matched to the load $Z_L = 50\Omega$ through the quarter-wave impedance transformation line, and the impedance of the impedance transformation line is

$$Z_T = \sqrt{Z_Q Z_L} = \frac{Z_0}{\sqrt{n+1}}.$$

If it is to remove the quarter-wave impedance transformation line after the combination point, the impedance value of the power amplifier combination point needs to be equal to the impedance value of the system load 5, namely 50 ohms. Therefore, the impedance of the power amplifier combination point is determined to be $Z_Q = Z_0/(n+1) = 50$ ohms, where $Z_0 = 50(n+1)$. According to the working principle of the asymmetric Doherty power amplifier, in the case of the saturated power, the output impedance of the carrier power amplifier circuit is $Z_m = Z_0 = 50(n+1)$, and the output impedance of the peak power amplifier 32 is $Z_p = Z_0/n = 50(n+1)/n$. Therefore, in the case that the output impedance of the carrier power amplifier 22 and the output impedance of the peak power amplifier 32 satisfy the

$$Z_Q = \frac{Z_m * Z_p}{Z_m + Z_p} = \frac{Z_0}{n+1} = 50\Omega$$

foregoing formulas,

The impedance value of the power amplifier combination point is equal to the impedance value of the system load 5, so that the quarter-wave impedance transformation line can be removed, which widens the operating bandwidth of the broadband Doherty power amplifier 100. In addition, the circuit complexity is reduced, thereby reducing the loss. Moreover, the combined amplified signal is directly output to the system load 5 through the output terminal OUT00 of the broadband Doherty power amplifier, so that the broadband Doherty power amplifier 100 is allowed to have a simple circuit structure and a high operating bandwidth.

[0053] In the following, one embodiment is described

as an example. Referring to FIG. 3, FIG. 3 is a schematic structural diagram of an application circuit of an embodiment of a broadband Doherty power amplifier according to the present disclosure. In this embodiment, the power divider 11 of the broadband Doherty power amplifier 101 has a power division ratio of 1:1.5. The output impedance Z_m of the carrier output matching circuit 231 has a resistance value of 125 ohms. The output impedance Z_p of the peak output matching circuit 331 has a resistance value of 83.3 ohms. In the case that the output impedance of the carrier power amplifier 221 and the output impedance of the peak power amplifier 321 meet the foregoing equations, the resistance value of Z_Q is 50 ohms. The broadband Doherty power amplifier 101 directly outputs the combined amplified signal to the system load 51 with the resistance value of 50 ohms through its output terminal OUT. Therefore, the broadband Doherty power amplifier 101 can remove the quarter-wave impedance transformation line, thereby widening the operating bandwidth of the broadband Doherty power amplifier 101. In addition, the circuit complexity is reduced, thereby reducing the loss.

[0054] The present disclosure further provides an implementation method for a broadband Doherty power amplifier. The method is applied to the broadband Doherty power amplifier 100.

[0055] In circuit applications, the broadband Doherty power amplifier 100 is connected to a system load 5. The system load 5 has a resistance value Z_L . In this embodiment, the resistance value Z_L of the system load 5 is 50 ohms.

[0056] Specifically, the broadband Doherty power amplifier 100 includes a power divider 1, a carrier power amplifier circuit 2, a peak power amplifier circuit 3, and a load modulation network 4.

[0057] The power divider 1 is configured to respectively allocate power to the carrier power amplifier circuit 2 and the peak power amplifier circuit 3 according to a power division ratio of 1:n. The power divider 1 determines a specific power division ratio according to the requirement of a modulation signal of the broadband Doherty power amplifier 100. In an embodiment, the power divider 1 is an in-phase power divider or a phase quadrature power divider.

[0058] The carrier power amplifier circuit 2 is a class AB power amplifier. In an embodiment, the carrier power amplifier circuit 2 is implemented by a transistor. Specifically, the carrier power amplifier circuit 2 includes a carrier input matching circuit 21, a carrier power amplifier 22, and a carrier output matching circuit 23 sequentially connected in series.

[0059] The carrier input matching circuit 21 is configured to match a terminal impedance of its input terminal to an input impedance of the carrier power amplifier 22.

[0060] The carrier output matching circuit 23 is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier 22. An output impedance of the carrier output matching circuit

circuit 23 is Z_m , and a following formula is satisfied:

$$Z_m = Z_L(n+1);$$

[0061] Specifically, n is a positive number.

[0062] In one embodiment, a corresponding phase compensation circuit is disposed in the carrier input matching circuit 21.

[0063] The peak power amplifier circuit 3 is a class C power amplifier. In one embodiment, the peak power amplifier circuit 3 is implemented by a transistor. The peak power amplifier circuit 3 includes a peak input matching circuit 31, a peak power amplifier 32, and a peak output matching circuit 33 sequentially connected in series.

[0064] The peak input matching circuit 31 is configured to match a terminal impedance of its input terminal to an input impedance of the peak power amplifier 32.

[0065] The peak output matching circuit 33 is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier 32. An output impedance of the peak output matching circuit 33 is Z_p , and a following formula is satisfied:

$$Z_p = Z_L(n+1)/n.$$

[0066] In one embodiment, a corresponding phase compensation circuit is disposed in the peak input matching circuit 31.

[0067] The load modulation network 4 is configured to perform power combination on an output signal of the carrier output matching circuit 23 and an output signal of the peak input matching circuit 31, and is configured to set an impedance Z_Q of the power amplifier combination point. The resistance value of Z_Q is Z_L .

[0068] Specifically, the circuit connection relationship is described below.

[0069] An input terminal of the power divider 1 is served as an input terminal IN of the broadband Doherty power amplifier. Two output terminals of the power divider 1 are connected to an input terminal of the carrier power amplifier circuit 2 and an input terminal of the peak power amplifier circuit 3 respectively.

[0070] An output terminal of the carrier power amplifier circuit 2 is connected to a first input terminal of the load modulation network 4. Specifically, the input terminal of the carrier input matching circuit 21 is connected to one output terminal of the power divider 1, and the output terminal of the carrier output matching circuit 23 is connected to the first input terminal of the load modulation network 4.

[0071] An output terminal of the peak power amplifier circuit 3 is connected to a second input terminal of the load modulation network 4. Specifically, the input terminal of the peak input matching circuit 31 is connected to the other output terminal of the power divider 1, and the output terminal of the peak output matching circuit 33 is

connected to the second input terminal of the load modulation network 4.

[0072] An output terminal of the load modulation network 4 is served as an output terminal OUT of the broadband Doherty power amplifier for connecting to the system load 5.

[0073] Referring to FIG. 4, FIG. 4 is a schematic flow-chart of an implementation method for a broadband Doherty power amplifier according to an embodiment of the present disclosure.

[0074] The method includes the following steps:

S1. debugging the power divider 1 to respectively allocate power to the carrier power amplifier circuit 2 and the peak power amplifier circuit 3 according to a power division ratio of 1:n.

S2. debugging the carrier input matching circuit 21 to match a terminal impedance of its input terminal to an input impedance of the carrier power amplifier 22, and debugging the carrier output matching circuit 23 to match the resistance value of the system load to an output impedance of the carrier power amplifier 22. The output impedance of the carrier output matching circuit 23 is Z_m , the resistance value of the system load 5 is Z_L , and a following formula is satisfied:

$$Z_m = Z_L(n+1),$$

and n is a positive number.

S3. debugging the peak input matching circuit 31 to match a terminal impedance of its input terminal to an input impedance of the peak power amplifier 32, and debugging the peak output matching circuit 33 to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier 32. The output impedance of the peak output matching circuit 33 is Z_p , and a following formula is satisfied:

$$Z_p = Z_L(n+1)/n.$$

S4. debugging the load modulation network 4 to perform power combination on an output signal of the carrier output matching circuit 23 and an output signal of the peak input matching circuit 31, and setting an impedance Z_Q of the power amplifier combination point. The resistance value of Z_Q is Z_L .

[0075] To sum up, through the steps of the foregoing method, the broadband Doherty power amplifier 100 is allowed to have a simple circuit structure and a high operating bandwidth.

[0076] Compared with the related art, according to the broadband Doherty power amplifier and the method of implementing the broadband Doherty power amplifier provided by the present disclosure, the carrier input matching circuit matches the terminal impedance of its input terminal to the input impedance of the carrier power amplifier, and the peak input matching circuit matches the terminal impedance of its input terminal to the input impedance of the peak power amplifier. Moreover, the load modulation network performs power combination on the output signal of the carrier output matching circuit and the output signal of the peak input matching circuit, and the impedance of the power amplifier combination point is set to be equal to the resistance value of the system load, so that the load modulation network structure can remove the quarter-wave impedance transformation line after the combination point, which allows the broadband Doherty power amplifier to have a simple circuit structure and a high operating bandwidth.

[0077] It should be noted that the embodiments described above with reference to the accompanying drawings are only used to illustrate the scope of the present disclosure and not to limit the scope of the present disclosure. Those of ordinary skill in the art should understand that modifications or equivalent substitutions to the present disclosure without departing from the spirit and scope of the present disclosure should be covered within the scope of the present disclosure. In addition, unless the context otherwise requires, words that appear in the singular include the plural, and vice versa. In addition, unless specifically stated, all or part of any embodiment may be used in conjunction with all or part of any other embodiment.

Claims

1. A broadband Doherty power amplifier, comprising:

a power divider;
a carrier power amplifier circuit;
a peak power amplifier circuit; and
a load modulation network;
wherein an input terminal of the power divider serves as an input terminal of the broadband Doherty power amplifier; two output terminals of the power divider are respectively connected to an input terminal of the carrier power amplifier circuit and an input terminal of the peak power amplifier circuit; an output terminal of the carrier power amplifier circuit is connected to a first input terminal of the load modulation network; an output terminal of the peak power amplifier circuit is connected to a second input terminal of the load modulation network; and an output terminal of the load modulation network serves as an output terminal of the broadband Doherty power amplifier, for connecting to a system load;

the carrier power amplifier circuit comprises a carrier input matching circuit, a carrier power amplifier, and a carrier output matching circuit sequentially connected in series; an input terminal of the carrier input matching circuit is connected to the output terminal of the power divider, and an output terminal of the carrier output matching circuit is connected to the first input terminal of the load modulation network; the peak power amplifier circuit comprises a peak input matching circuit, a peak power amplifier, and a peak output matching circuit sequentially connected in series; an input terminal of the peak input matching circuit is connected to the output terminal of the power divider, and an output terminal of the peak output matching circuit is connected to the second input terminal of the load modulation network; a resistance value of the system load is Z_L ; the power divider is configured to respectively allocate power to the carrier power amplifier circuit and the peak power amplifier circuit according to a power division ratio of 1:n; the carrier input matching circuit is configured to match a terminal impedance of the input terminal of the carrier input matching circuit to an input impedance of the carrier power amplifier, and the carrier output matching circuit is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier; an output impedance of the carrier output matching circuit is Z_m , and a following formula is satisfied:

$$Z_m = Z_L(n+1);$$

wherein n is a positive number; the peak input matching circuit is configured to match a terminal impedance of the input terminal of the peak input matching circuit to an input impedance of the peak power amplifier, and the peak output matching circuit is configured to match the resistance value Z_L of the system load to an output impedance of the carrier power amplifier; an output impedance of the peak output matching circuit is Z_p , and a following formula is satisfied:

$$Z_p = Z_L(n+1)/n;$$

and

the load modulation network is configured to perform power combination on an output signal of the carrier output matching circuit and an output signal of the peak input matching circuit, and is configured to set an impedance Z_Q of a power

amplifier combination point, wherein a resistance value of the impedance Z_Q is Z_L .

2. The broadband Doherty power amplifier according to claim 1, wherein the resistance value Z_L of the system load is 50 ohms.
3. The broadband Doherty power amplifier according to claim 2, wherein the power division ratio is 1:1.5, a resistance value of Z_m is 125 ohms, a resistance value of Z_p is 83.3 ohms, and the resistance value of the impedance Z_Q is 50 ohms.
4. The broadband Doherty power amplifier according to claim 1, wherein the carrier power amplifier circuit is a class AB power amplifier.
5. The broadband Doherty power amplifier according to claim 4, wherein the carrier power amplifier circuit is implemented by a transistor.
6. The broadband Doherty power amplifier according to claim 1, wherein the peak power amplifier circuit is a class C power amplifier.
7. The broadband Doherty power amplifier according to claim 4, wherein the peak power amplifier circuit is implemented by a transistor.
8. The broadband Doherty power amplifier according to claim 1, wherein the power divider is an in-phase power divider or a phase quadrature power divider.
9. The broadband Doherty power amplifier according to claim 1, wherein the carrier input matching circuit and the peak input matching circuit each comprises a corresponding phase compensation circuit.
10. An implementation method for a broadband Doherty power amplifier, wherein the broadband Doherty power amplifier comprises:
 - a power divider;
 - a carrier power amplifier circuit;
 - a peak power amplifier circuit; and
 - a load modulation network;
 an input terminal of the power divider serves as an input terminal of the broadband Doherty power amplifier; two output terminals of the power divider are respectively connected to an input terminal of the carrier power amplifier circuit and an input terminal of the peak power amplifier circuit; an output terminal of the carrier power amplifier circuit is connected to a first input terminal of the load modulation network; an output terminal of the peak power amplifier circuit is connected to a second input terminal of the load modulation network; and an output terminal of

the load modulation network serves as an output terminal of the broadband Doherty power amplifier for connecting to a system load;
 the carrier power amplifier circuit comprises the carrier input matching circuit, the carrier power amplifier, and the carrier output matching circuit sequentially connected in series; the input terminal of the carrier input matching circuit is connected to a first one of the two output terminals of the power divider, and an output terminal of the carrier output matching circuit is connected to the first input terminal of the load modulation network; and
 the peak power amplifier circuit comprises the peak input matching circuit, the peak power amplifier, and the peak output matching circuit sequentially connected in series; the input terminal of the peak input matching circuit is connected to a second one of the two output terminals of the power divider, and an output terminal of the peak output matching circuit is connected to the second input terminal of the load modulation network;
 wherein the implementation method for the broadband Doherty power amplifier comprises:

S1. debugging the power divider to allocate power to the carrier power amplifier circuit and the peak power amplifier circuit according to a power division ratio of 1:n;
 S2. debugging the carrier input matching circuit to match a terminal impedance of the input terminal of the carrier input matching circuit to an input impedance of the carrier power amplifier, and debugging the carrier output matching circuit to match a resistance value of a system load to an output impedance of the carrier power amplifier, where an output impedance of the carrier output matching circuit is Z_m , the resistance value of the system load is Z_L , and a following formula is satisfied:

$$Z_m = Z_L(n+1);$$

wherein n is a positive number;
 S3. debugging the peak input matching circuit to match a terminal impedance of the input terminal of the peak input matching circuit to an input impedance of the peak power amplifier, and debugging the peak output matching circuit to match the resistance value Z_L of the system load to the output impedance of the carrier power amplifier, where an output impedance of the peak output matching circuit is Z_p , and a following formula being satisfied:

$$Z_p = Z_L(n+1)/n;$$

and

S4. debugging the load modulation network to perform power combination on an output signal of the carrier output matching circuit and an output signal of the peak input matching circuit, and setting an impedance Z_Q of a power amplifier combination point, where a resistance value of the impedance Z_Q is Z_L .

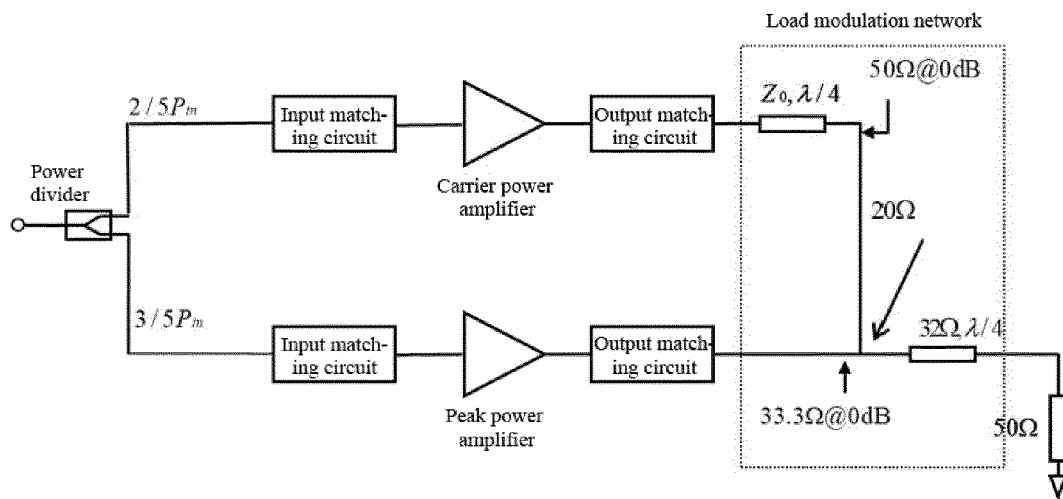


FIG. 1

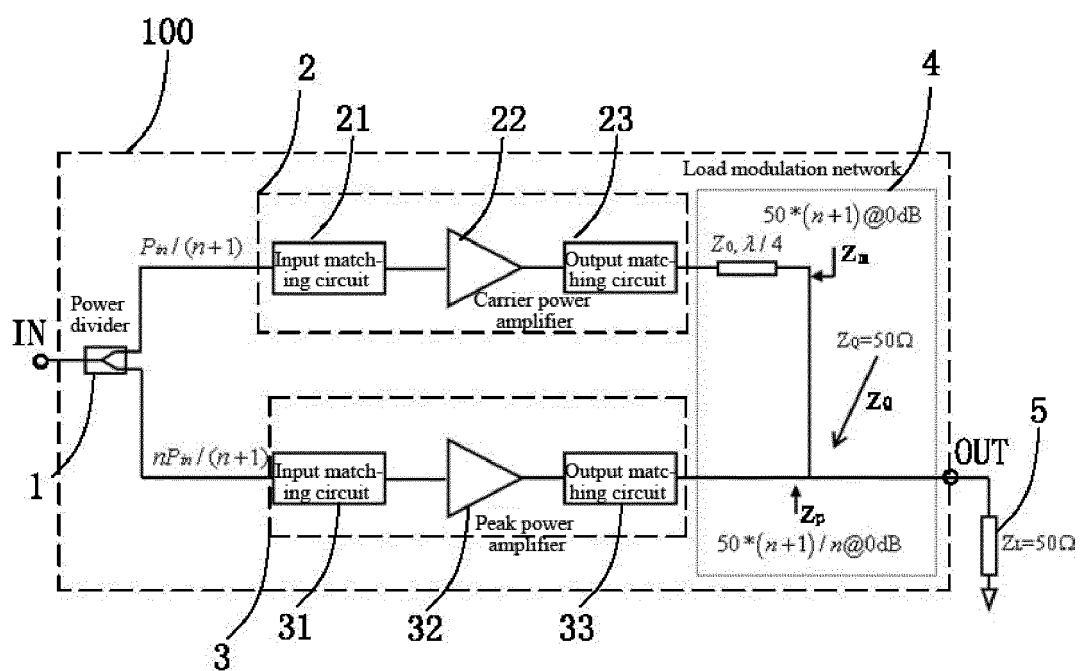


FIG. 2

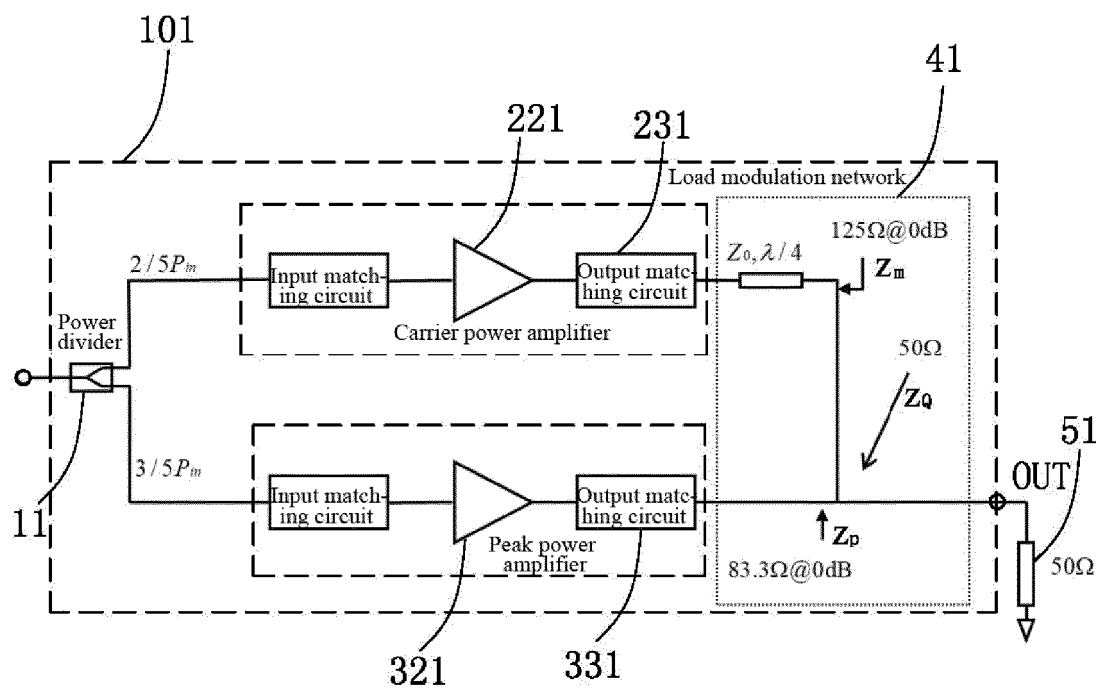


FIG. 3

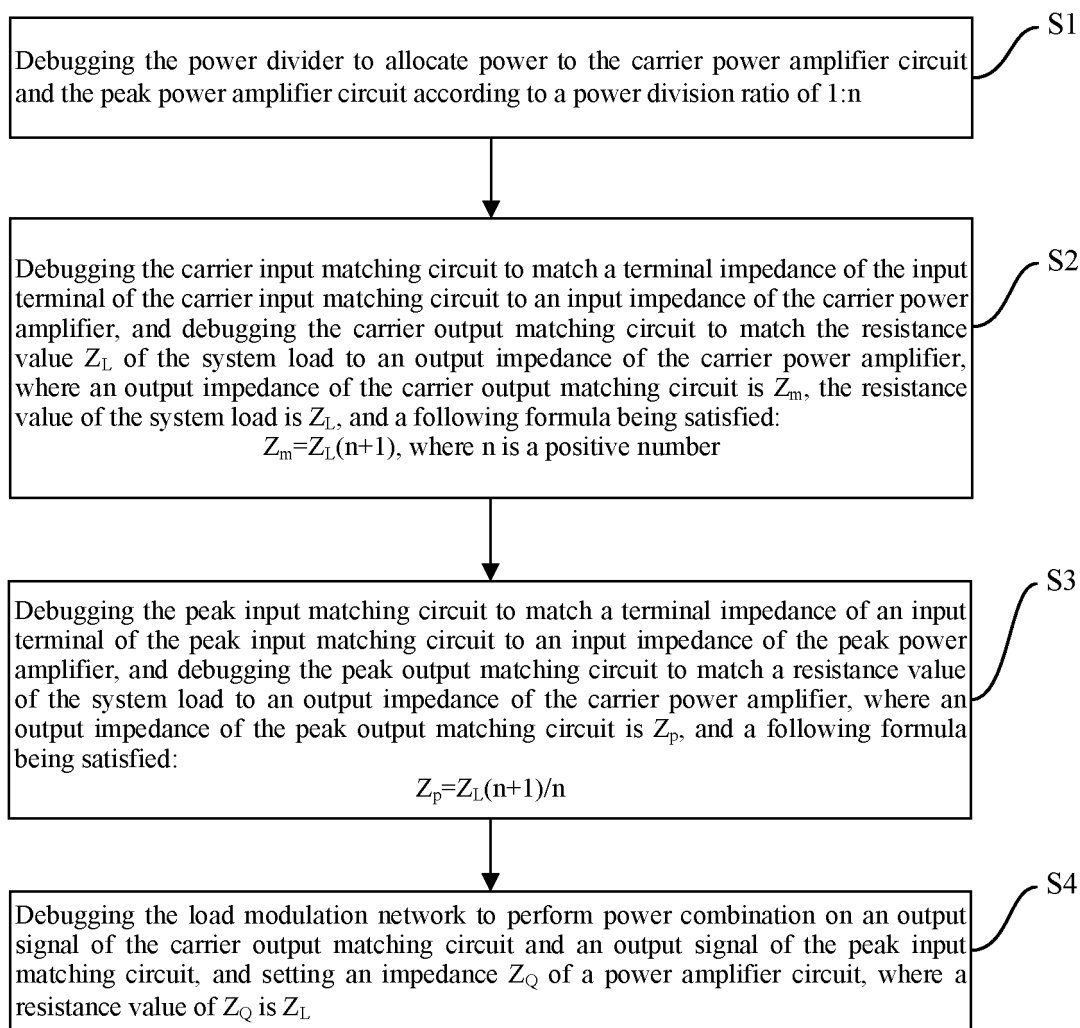


FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.

PCT/CN2022/108110

A. CLASSIFICATION OF SUBJECT MATTER

H03F 1/02(2006.01)i; H03F 1/42(2006.01)i; H03F 3/21(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

CNKI, CNPAT, WPI, EPODOC, IEEE: 功率放大器, 功分器, 载波, 峰值, 负载, 调制, 匹配, 阻抗, Doherty, power amplifier, power divider, carrier, peak, load, capacity, modulat+, match, impedance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
PX	CN 113904628 A (LANSUS TECHNOLOGIES INC.) 07 January 2022 (2022-01-07) description, paragraphs [0042]-[0095]	1-10
X	CN 107508560 A (HANGZHOU DIANZI UNIVERSITY) 22 December 2017 (2017-12-22) description, paragraphs [0045]-[0053], and figure 3	1-10
A	CN 109660212 A (JIANGSU UNIVERSITY) 19 April 2019 (2019-04-19) entire document	1-10
A	EP 2887541 A1 (TELEFONAKTIEBOLAGET L M ERICSSON (PUBL)) 24 June 2015 (2015-06-24) entire document	1-10

☐ Further documents are listed in the continuation of Box C.
☒ See patent family annex.

* Special categories of cited documents:

“A” document defining the general state of the art which is not considered to be of particular relevance

“E” earlier application or patent but published on or after the international filing date

“L” document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

“O” document referring to an oral disclosure, use, exhibition or other means

“P” document published prior to the international filing date but later than the priority date claimed

“T” later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

“X” document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

“Y” document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

“&” document member of the same patent family

Date of the actual completion of the international search

15 September 2022

Date of mailing of the international search report

27 September 2022

Name and mailing address of the ISA/CN

**China National Intellectual Property Administration (ISA/
CN)**
**No. 6, Xitucheng Road, Jimenqiao, Haidian District, Beijing
100088, China**

Facsimile No. (86-10)62019451

Authorized officer

Telephone No.

Form PCT/ISA/210 (second sheet) (January 2015)

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.

PCT/CN2022/108110

Patent document cited in search report			Publication date (day/month/year)		Patent family member(s)			Publication date (day/month/year)	
CN	113904628	A	07 January 2022		None				
CN	107508560	A	22 December 2017		None				
CN	109660212	A	19 April 2019		None				
EP	2887541	A1	24 June 2015		US	2015180428	A1	25 June 2015	

Form PCT/ISA/210 (patent family annex) (January 2015)