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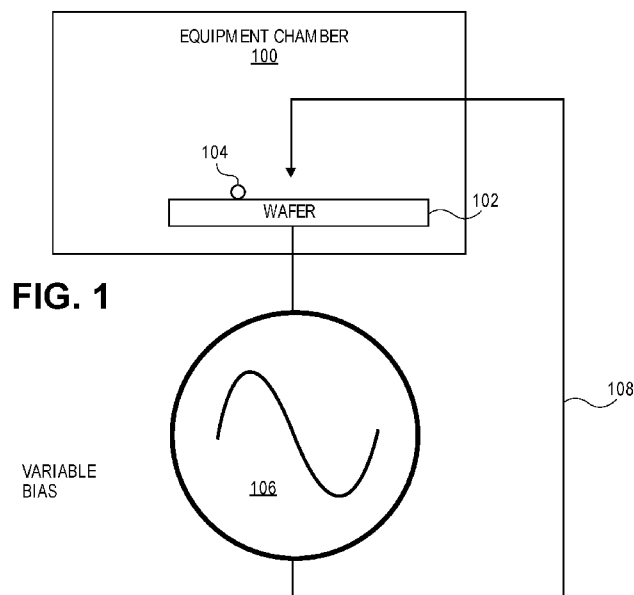


FIG. 2

(57) Abstract: Equipment and processes for enhanced defect removal through substrate and media charge modulation are described. In an example, a system for defect removal through substrate and media charge modulation is provided. In another example, a method for defect removal through substrate and media charge modulation is provided.



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ENHANCED DEFECT REMOVAL THROUGH SUBSTRATE AND MEDIA CHARGE MODULATION**CROSS-REFERENCE TO RELATED APPLICATIONS**

[0001] This application claims the benefit of U.S. Provisional Application No.

5 62/329,929, filed on April 29, 2016, the entire contents of which are hereby incorporated by reference herein.

TECHNICAL FIELD

[0002] Embodiments of the invention are in the field of semiconductor processing and, in
10 particular, equipment and processes for enhanced defect removal through substrate and media charge modulation.

BACKGROUND

[0003] For the past several decades, the scaling of features in integrated circuits has been
15 a driving force behind an ever-growing semiconductor industry. Scaling to smaller and smaller features enables increased densities of functional units on the limited real estate of semiconductor chips.

[0004] As transistor size decreases, the impact of issues associated with particle
contamination of a semiconductor wafer surface during processing increases. State of the art
20 approaches for contamination or particle removal still include the RCA clean. The RCA clean is a standard set of wafer cleaning operations which need to be performed before high-temperature processing operations (e.g., oxidation, diffusion, CVD) of silicon wafers in semiconductor manufacturing. The basic procedure involves the following chemical processes performed in
sequence: (1) removal of the organic contaminants (organic clean + particle clean), (2) removal
25 of thin oxide layer (oxide strip, optional), (3) removal of ionic contamination (ionic clean). However, improvements are needed in the field of particle and defect removal during semiconductor wafer processing.

BRIEF DESCRIPTION OF THE DRAWINGS

30 [0005] Figure 1 is a schematic illustrating an equipment chamber, in accordance with an embodiment of the present invention.

[0006] Figure 2 is a schematic illustrating a system for defect removal through substrate and media charge modulation, the system including the equipment chamber of Figure 1, in accordance with an embodiment of the present invention.

35 [0007] Figure 3 is a plot of interaction force (in Newtons) as a function of separation

distance (in meters) for interaction forces with ideal surfaces, in accordance with an embodiment, of the present invention.

[0008] Figure 4 is a plot of interaction force (in Newtons) as a function of separation distance (in meters) for interaction forces with irregular particles, in accordance with an embodiment, of the present invention.

[0009] Figure 5 is a schematic illustrating the distribution of ions around a charged particle, in accordance with an embodiment of the present invention.

[0010] Figure 6 illustrates a schematic showing stages (A) and (B) in a method of enhanced defect removal involving radiation-enhanced charge modulation, in accordance with an embodiment of the present invention.

[0011] Figure 7 is a schematic illustrating electrophoresis as a motion of dispersed particles relative to a fluid under the influence of a spatially uniform electric field, in accordance with an embodiment of the present invention.

[0012] Figure 8 illustrates a system for performing enhanced defect removal through electrophoresis and associated schematic showing exemplary electrophoresis parameters, in accordance with an embodiment of the present invention.

[0013] Figure 9 illustrates a system including a chuck assembly, in accordance with an embodiment of the present invention.

[0014] Figure 10 illustrates a bipolar chuck having a wafer with induced charge thereon, in accordance with an embodiment of the present invention.

[0015] Figure 11 is a schematic of an assembly for ex situ enhanced defect removal from a substrate, in accordance with an embodiment of the present invention.

[0016] Figure 12 is a schematic of an assembly for wet processing for enhanced defect removal from a substrate, in accordance with an embodiment of the present invention.

[0017] Figure 13 is a schematic of an assembly for ex situ enhanced defect removal from a substrate, in accordance with an embodiment of the present invention.

[0018] Figure 14 is a schematic of an assembly for in situ ionization of a substrate, in accordance with an embodiment of the present invention.

[0019] Figure 15 is a schematic of a vacuum chamber, in accordance with an embodiment of the present invention.

[0020] Figure 16 illustrates an assembly for in situ enhanced defect removal from a substrate, in accordance with an embodiment of the present invention.

[0021] Figure 17 illustrates another assembly for in situ enhanced defect removal from a substrate, in accordance with another embodiment of the present invention.

[0022] Figure 18 illustrates an assembly for implementing a focused magnetic field

approach in conjunction with an ultrasonic shockwave or gas nozzle approach, in accordance with an embodiment of the present invention.

[0023] Figure 19 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention.

[0024] Figure 20A illustrates a cross-sectional view of a non-planar semiconductor device having fins, in accordance with an embodiment of the present invention.

[0025] Figure 20B illustrates a plan view taken along the a-a' axis of the semiconductor device of Figure 20A, in accordance with an embodiment of the present invention.

[0026] Figure 21 illustrates a computing device in accordance with one implementation of the invention.

[0027] Figure 22 illustrates a block diagram of an exemplary computer system, in accordance with an embodiment of the present invention.

[0028] Figure 23 is an interposer implementing one or more embodiments of the invention.

[0029] Figure 24 is a computing device built in accordance with an embodiment of the invention.

DESCRIPTION OF THE EMBODIMENTS

[0030] Equipment and processes for enhanced defect removal through substrate and media charge modulation are described. In the following description, numerous specific details are set forth, such as specific tooling, integration and material regimes, in order to provide a thorough understanding of embodiments of the present invention. It will be apparent to one skilled in the art that embodiments of the present invention may be practiced without these specific details. In other instances, well-known features, such as semiconductor device operations, are not described in detail in order to not unnecessarily obscure embodiments of the present invention. Furthermore, it is to be appreciated that the various embodiments shown in the Figures are illustrative representations and are not necessarily drawn to scale. In some cases, various operations will be described as multiple discrete operations, in turn, in a manner that is most helpful in understanding the present invention, however, the order of description should not be construed to imply that these operations are necessarily order dependent. In particular, these operations need not be performed in the order of presentation.

[0031] Certain terminology may also be used in the following description for the purpose of reference only, and thus are not intended to be limiting. For example, terms such as “upper”, “lower”, “above”, and “below” refer to directions in the drawings to which reference is made.

Terms such as “front”, “back”, “rear”, and “side” describe the orientation and/or location of portions of the component within a consistent but arbitrary frame of reference which is made clear by reference to the text and the associated drawings describing the component under discussion. Such terminology may include the words specifically mentioned above, derivatives thereof, and words of similar import.

[0032] One or more embodiments described herein are directed to defect removal through substrate and media charge modulation. Applications may include one or more of defect reduction, particle removal, or yield improvement. Embodiments may be included in computer system architecture features and interfaces made in high volumes. Embodiments may encompass architectures, devices (e.g., transistors) and associated manufacturing processes.

[0033] Embodiments described herein may be implemented to improve particle removal efficiency without damaging delicate structures on a wafer surface. To provide context, state of the art solutions use chemical and/or physical energy. As pattern dimensions decrease, physical energy is limited by pattern damage. One or more embodiments described herein changes (weakens) the attractive force between wafer and particle. This will increase the window between pattern damage and attractive force, allowing low energy removal methods to more efficiently remove particles from the wafer surface.

[0034] One or more embodiments involves Coulomb’s law as the underlying principle. In an embodiments, an attractive force is replaced with a repulsive one, by changing the charge on the wafer. A weaker attractive force or a repulsive force enables lower energy and improves particle removal efficiency. The charge placed on the wafer may be variable in order to weaken the bonds between particles of different charges.

[0035] To provide further context, state of the art solutions do not reduce the attractive force between the particle and the wafer surface. Instead, various forms of physical or chemical energy are implemented to separate the particle from the wafer. Furthermore, many applications do not allow chemical etching (undercutting) due to adverse impact of materials on the wafer. Additionally, many structures may be damaged by the physical energy required to overcome the attractive force between the particle and the wafer substrate. Embodiments described herein may be implemented to weaken the attractive force between the particle and wafer substrate, improving the efficiency (removal rate) of methods that will not damage or essentially not damage the underlying substrate. Thus, one or more embodiments may be referred to as enhanced defect removal since defect removal is aided through charge modulation. The enhanced defect removal may be part of an actual cleans process or as a pre-treatment to an actual cleans process.

[0036] Figure 1 is a schematic illustrating an equipment chamber, in accordance with an

embodiment of the present invention. Referring to Figure 1, an equipment chamber 100 has a wafer 102 housed therein. A particle 104 is on the surface of the wafer 102, effectively contaminating the wafer 102.

[0037] Figure 2 is a schematic illustrating a system for defect removal through substrate and media charge modulation, the system including the equipment chamber of Figure 1, in accordance with an embodiment of the present invention. Referring to Figure 2, a variable bias 106 is coupled via pathway 108 with the chamber of Figure 1.

[0038] Using Figures 1 and 2 as a foundation, in a first exemplary embodiment, a system for enhancing defect removal from a wafer or substrate includes a vacuum processing chamber 100. A wafer or substrate processing region 102 is located within the vacuum processing chamber 100. A module 106 is coupled 108 to the vacuum processing chamber 100. The module 106 is for effecting charge modulation at the wafer or substrate processing region 102. In one embodiment, a chuck (not shown) is immediately below the wafer or substrate processing region, as is described in greater detail below.

[0039] Using Figures 1 and 2 as a foundation, in a second exemplary embodiment, a system for enhancing defect removal from a wafer or substrate includes a wet processing chamber 100. A wafer or substrate processing region 102 is located within the wet processing chamber 100. A module 106 is coupled 108 to the wet processing chamber 100. The module 106 is for effecting charge modulation at the wafer or substrate processing region.

[0040] Embodiments may be implemented for any semiconductor manufacturing facility looking to improve yield without causing pattern damage. This may be primarily an equipment capability. To provide further context, common practice involves cleaning using chemistry to reduce the charge difference between the wafer surface and particles on the surface. In an embodiment, reduction of the difference in charge (attractive force) between the defect and the wafer surface improves the effectiveness of existing technology.

[0041] Initial experimental attempts to clean wafers using an E-Chuck on a Plasma Etcher (No plasma used) yielded the following conclusions: (1) defects were moved/removed from the wafer by changing the charge and various purge/vacuum sequences; (2) improved defect removal would occur with (a) finer control of the charge, (b) improved transport of the defects from the surface of the wafer, and/or (c) characterization of the defects and the charge on these defects.

[0042] In an embodiment, based on Coulomb's law as the underlying principle, the concept involves an approach to change the attractive nature (force) between the substrate and the particle. Improved particle removal efficiency may be achieved. State of the art particle removal methods will likely become insufficient to meet future needs. Developing technology to

remove particulate defects on various substrates of interest are thus described. One or more embodiments are nearly inert to wafer substrates. One or more embodiments involve no or very little etching of pattern/substrate. One or more embodiments involve no or little pattern damage. Some embodiments are specific to wet processing (e.g., wafer drying, waste segregation, environmental effluents, etc.). Some embodiments are specific to dry implementation (e.g., expected for high aspect ratio and/or pattern collapse modules/applications).

[0043] Embodiments may include equipment, chemistry, materials, hardware, software, and process technology to improve particle removal efficiency in an equipment capability by implementing, incorporating, or practicing defect removal through substrate and media charge modulation. Embodiments may be applied in the wet cleans space, dry etch space, or a combination of both to meet cleaning requirements for various process modules.

[0044] Embodiments may include an equipment capability and any related equipment, chemistry, materials, hardware, software, and process technology that improves particle removal efficiency (PRE) by implementing, incorporating, or practicing defect removal through substrate and media charge modulation in a manner that will not impact pattern integrity and will not induce pattern damage. The overall solution may be a wet process, a dry process, or a combination of wet and dry processes.

[0045] In an embodiment, a wet cleans implementation includes an equipment capability including any necessary chemistry, materials, hardware, software, and process technology implemented to improve PRE through immersion, spray, combo, or other techniques. The equipment capability may apply chemical assistance (e.g., very dilute HF, surfactant or surface tension reducing methods, dilute NH₄OH or SC1 etc.). Solutions may include, but are not limited to, wafer drying, waste segregation, environmental effluents etc. However, in one embodiment, the solution maintains reasonable cost per wafer pass.

[0046] In an embodiment, a dry etch implementation includes an equipment capability including any necessary chemistry, materials, hardware, software, and process technology implemented to improve PRE through vacuum, gas stream, solid/sublimating substance in conjunction with gas/combo, or others. If needed, the equipment capability can incorporate chemical assistance, e.g., possibly with gases like O₂ to support improved polymer elimination. Solutions may include, but are not limited to, waste segregation, environmental effluents, etc. However, in one embodiment, the solution maintains reasonable cost per wafer pass. In another embodiment, a combination of wet cleans and dry etch implementations as described above is implemented.

[0047] In an embodiment, concepts described herein may have two basic components:

(1) reducing the attraction/bond strength between the particle and the wafer substrate, and/or (2)

use of existing or novel cleaning methods to eliminate/break the weakened attractive forces between the particle and the wafer and transport the particle away from the wafer.

[0048] In an embodiment, methods described herein may be implemented to weaken the attractive forces between particulate and wafer substrate. One or more embodiments may be implemented to use an e-chuck “like” device to control the charge on the wafer surface. The voltage/surface charge may be changed (e.g., positive/negative, magnitude and transition method between different set points). The wafer may be ground to dissipate charge. The voltage/surface charge may be modulated by recipe control to enable removal of particulate of different charges.

[0049] To provide further context, observations have been made that UV exposure (such as a litho UV cure) can dissipate charge on a wafer. One implementation involves inserting an operation such as described above into the cleaning sequence. In an embodiment, use of a charged “wand” is passed over a wafer (e.g., possibly on an e-chuck like device). The wand may have similar properties as the e-chuck like device described above. In addition, the proximity of the wand to the wafer surface may be controlled. In an embodiment, when used in conjunction with an e-chuck like device, controlling potential can be linked (coordinated) to maximize effectiveness. In an immersion implementation, a wafer clamp mechanism is used as one pole and a “wand” is used as the other. In one embodiment, the initial fluid is selected for its coupling properties. In an embodiment, fluid flow and wafer orientation with respect to such fluid flow is optimized to transport defects away from the wafer.

[0050] In an embodiment, a dry implementation involves charge modulation. In one embodiment, the lesser bound defect is removed and transported from the wafer surface. In one embodiment, a gas stream is implemented to use momentum transfer to break the weakened bond and transport the defect off the wafer surface. In one embodiment, a vacuum system removes the gas stream and particulate from the process chamber. In one embodiment, a charged device is used to attract and retain a particulate.

[0051] In an embodiment, a wet implementation involves charge modulation. In one embodiment, the lesser bound defect is removed and transported from the wafer surface. In one embodiment, transport of particles occurs using common methods to overcome the weekend attractive force: dilute chemistry, lowering the surface tension in the solution with a surfactant, to separate the particle from the wafer and transport it off the wafer surface. In one embodiment, other methods are used in conjunction with the dilute chemistry. For example, a solvent or water based polymer may be implemented to entangle/surround the particle. In one embodiment, the particle is removed with the polymer.

[0052] In another aspect, concepts pertaining to charge modulation can be viewed in the context of forces involved in particle adhesion. Figure 3 is a plot 300 of interaction force (in

Newton's) as a function of separation distance (in meters) for interaction forces with ideal surfaces, in accordance with an embodiment, of the present invention. Plot 300 includes curves for van der Waals interactions, electrostatic interactions and combined DLVO interactions along with different stages in an ideal particle to ideal surface relationship. Figure 4 is a plot 400 of interaction force (in Newton's) as a function of separation distance (in meters) for interaction forces with irregular particles, in accordance with an embodiment, of the present invention. Plot 400 includes curves for van der Waals interactions, electrostatic interactions and combined DLVO interactions along with different stages in an irregular particle to surface relationship.

[0053] In another aspect, considerations for apparatuses for charge modulation and, in particular, apparatuses for enhancing defect removal from surfaces through charge modulation are described below.

[0054] In an embodiment, ionization is used to reduce static charge on surfaces. The effects include one or more of control of charge polarity, potential, duration and feedback of the surface charge. In one embodiment, a corona discharge is implemented for ionization based charge modulation. Figure 5 is a schematic 500 illustrating the distribution of ions around a charged particle, in accordance with an embodiment of the present invention. Referring to Figure 5, a distribution of ions around a charged particle 502 includes condensed counter-ions 504, a stern layer 506, a slipping plane 508, and a double diffuse layer 510. A relative plot in mV as a function of distance from the particle 502 surface is shown for surface potential, stern potential, and zeta potential.

[0055] In an embodiment, a wet processing pretreatment is implemented immediately prior to introducing a wafer to wet cleaning chemicals. In one such embodiment, an ex situ approach involves use of a separate chamber prior to processing in a separate wet chamber. In another such embodiment, an in situ approach involves incorporation of the wet processing pretreatment into a wet chamber.

[0056] In another embodiment, a dry processing pretreatment is implemented immediately prior to introducing a wafer to a dry cleaning treatment. In one such embodiment, an ex situ approach involves use of a separate chamber prior to processing in a separate dry clean chamber. In another such embodiment, an in situ approach involves incorporation of the dry processing pretreatment into a dry clean chamber. In a particular such embodiment, the dry processing pretreatment is incorporated as a selectable part of a cleans recipe.

[0057] In yet another embodiment, radiation such as ultra violet (UV) radiation or soft X-ray radiation is implemented as part of a static surface charge reduction method. UV radiation can reduce the electrostatic potential of surfaces. Gas molecules in close proximity to a wafer substrate generate ions and electrons used to neutralize the wafer substrate charge (e.g., to

provide a non-biased state). Embodiments include select combinations of gas species and chamber pressure (e.g., the radiation may be performed in a vacuum chamber). In an embodiment, a variable wavelength UV source is used. Control of UV intensity and/or pulse duration can be tailored to provide suitable charge modulation for ultimate particle removal. In an embodiment, a variable gas supply is included in such a chamber which allows for control of reactive gas species and flowrate. In an embodiment, particle removal efficiency is improved by reducing the attractive force between the substrate and the wafer.

[0058] In an embodiment, a radiation-enhanced approach is implemented to improve existing wet clean methods, e.g., as an ex situ treatment prior to entering a wet clean chamber. In another embodiment, a radiation-enhanced approach is implemented to improve existing in situ particle removal methods used in a vacuum chamber. In one such embodiment, gas cluster momentum transfer (uncharged) is implemented via a gas nozzle. In a specific embodiment, an enhanced defect removal method involves alternating between charge reduction and particle removal operations until particle removal is complete.

[0059] Figure 6 illustrates a schematic showing stages (A) and (B) in a method of enhancing defect removal involving radiation-enhanced charge modulation, in accordance with an embodiment of the present invention. Referring to Figure 6, at stage (A), a vacuum chamber 602 with a variable wavelength UV source 604 houses a wafer 606 therein. At stage (B), a gas cluster nozzle 608 on a control arm 610 is introduced to the chamber 602 for wafer 606 cleaning.

[0060] In an embodiment, electrophoresis is used to reduce static charge on surfaces. In one embodiment, an in situ wet etch treatment is used to separate a particle from a wafer surface. The electric field may be controlled and modulated to enable enhanced removal of particles with differing polarity and charge. Figure 7 is a schematic 700 illustrating electrophoresis as a motion of dispersed particles relative to a fluid under the influence of a spatially uniform electric field, in accordance with an embodiment of the present invention. An electrostatic force is in an opposite direction to friction forces and electrophoretic retardation forces.

[0061] Figure 8 illustrates a system 800 for performing enhancing defect removal through electrophoresis, in accordance with an embodiment of the present invention. The system 800 includes a bath 802 having a wafer 804 immersed therein. Variable switching power supply 806 is coupled to the bath 802. An associated schematic 850 shows exemplary electrophoresis parameters. It is to be appreciated that ultimate separation of particles can be tailored for particles of differing charge and size.

[0062] In an embodiment, electrophoresis is implemented to enhance wafer defect removal by making the substrate (wafer) act as (either or both) the anode and cathode by varying the polarity of the substrate using a wafer chuck to set the wafer surface potential. The media in

the bath 802 may be optimized to effectively remove the particles from solution. In one such embodiment, separation is achieved by keeping the particles from being attracted to the substrate when the polarity is switched. In an embodiment, ligands used in the bath 802 are tailored to bind to a charged particle, and ultimately keep it separated from a wafer surface. In an embodiment, a flow of the bath 802 solution is implemented to transport removed particles away from the surface/boundary layer of the wafer. Optimal media may differ as substrate polarity of the wafer changes and/or the charge of the particle being removed changes. The variable/switching power supply 806 can be modulated to control the charge of the wafer and media (e.g., by varying polarity and/or magnitude). In an embodiment, the controller 806 is programmable to enable a recipe sequences to run. A feedback system may also be included to use the effluent from a stream of the bath 802 stream to trigger and/or control starting a next operation in the sequence. An alternate side of the circuit may be an electrode immersed in the media and feedback to the power supply.

[0063] In an embodiment, bath 802 is a wet immersion tank. In one such embodiment, the wet immersion tank includes a chuck for holding the wafer as immersed in the media. The electrical potential of the chuck may be controlled by the variable/switching power supply 806. Such a chuck may be configured to transmit the electrical potential to the wafer/substrate 804 while physically holding the wafer 804 in the media. The alternate electrode (to the chuck) may be immersed in the media. In on embodiment, the polarity and potential of the alternate electrode is controlled by the variable/switching power supply 806 as part of the same circuit as the wafer chuck.

[0064] In an embodiment, bath 802 is a wet immersion single wafer spray tool chamber. In one such embodiment, the wet immersion tank includes a chuck for holding the wafer single wafer spray tool chamber includes a chuck for holding the wafer 804. The electrical potential of such a chuck may be controlled by the variable/switching power supply 806. The chuck may be designed to transmit the electrical potential to the wafer/substrate 804 while physically holding the wafer. The alternate electrode (to the chuck) may be physically located above the wafer 804. In one embodiment, the polarity and potential of the alternate electrode is controlled by the variable/switching power supply 806 as part of the same circuit as the wafer chuck. In one embodiment, the media is introduced between the two plates (electrodes), completing the electrical circuit.

[0065] Figure 9 illustrates a system 900 including a chuck assembly, in accordance with an embodiment of the present invention. The system 900 includes a chuck assembly 902 having a chuck 904. A wafer 906 is supported on the chuck 904. An alternate electrode 910 is above the wafer 906. A media 908 is between the alternate electrode 910 and the wafer 906. The

media 908 is where flow removes particulate away from the wafer substrate. The chuck 904 is coupled to variable switching supply 912.

[0066] In an embodiment, electrostatic induction is used to reduce static charge on a surface. In one embodiment, the electrostatic induction is implemented as a dry application and involves use of an electrostatic chuck. In particular, an electrostatic chuck is used to create a potential on the wafer. Features of such an electrostatic chuck approach may involve one or more of variable charge polarity, variable charge magnitude, and recipe-controlled applications. In an embodiment, potential from the electrostatic chuck impacts the attractive force with which particles adhere to the wafer. By controlling and/or varying the polarity and magnitude of the charge, the attractive force of particulate of different composition and/or native charge may be neutralized and/or reduced, improving removal efficiency. In an embodiment, particles with a relatively lowest attractive force are removed by a cleaning function, as described in greater detail below. Such a cleaning function may be repeated with each change in the electrostatic chuck/wafer potential. In an embodiment, particle removal is accomplished using one or more of shockwave from an inert gas flow in a vacuum or physical bombardment (momentum transfer) of a gas cluster. In the latter case, such gas clusters may be accelerated through the use of the charge on the electrostatic chuck.

[0067] Accordingly, electrical/charge attraction may be modulated by an alternatively charged device in close proximity to the wafer substrate/electrostatic chuck. As an example of such a system, Figure 10 illustrates a bipolar chuck 1000 having a wafer 1002 with induced charge thereon, in accordance with an embodiment of the present invention.

[0068] In another embodiment, electrostatic induction is implemented using an “electrostatic wand” to induce a temporary change in the charge of the wafer surface or particulate. Such a wand may be passed over a wafer in close proximity to the surface of the wafer. Features of such an electrostatic wand approach may involve one or more of variable charge polarity, variable charge magnitude, and recipe-controlled applications (e.g., motion, polarity and charge magnitude). In an embodiment, potential from the electrostatic wand impacts the attractive force with which particles adhere to the wafer. By controlling or varying the polarity and magnitude of the charge, the attractive force of particulate of different composition/native charge may be neutralized or reduced, improving removal efficiency. In an embodiment, particles with a relatively lowest attractive force are removed by a cleaning function, as described in greater detail below. Such a cleaning function may be repeated with each change in the electrostatic wand/wafer potential. In an embodiment, particle removal is accomplished using one or more of shockwave from an inert gas flow in a vacuum or physical bombardment (momentum transfer) of a gas cluster. In the latter case, such gas clusters may be

accelerated through the use of the charge on the electrostatic wand. Implementations can be made as in situ or ex situ prior to a wet clean or between wet clean particle removal operations.

[0069] In an embodiment, magnetic force such as electromagnetic force is used to reduce static charge on a surface. In one such embodiment, a magnetic field is used to temporarily
5 change a wafer surface charge or the charge of a particle/defect on the wafer surface. A magnetic field may be focused on a targeted area of the wafer. The field can then be modulated. In one embodiment, particle removal is effected by a focused gas cluster nozzle or a focus shockwave used in conjunction with the magnetic field. In further embodiments, a magnetic force in conjunction with an electrostatic chuck device is used to modulate the surface charge of the
10 wafer.

[0070] In another aspect, considerations for methods of charge modulation and, in particular, methods for enhancing defect removal from surfaces through charge modulation are described below.

[0071] In an embodiment, charge modulation is implemented to reduce attractive force(s)
15 between a wafer and particulate/defects. Without a reduction in attractive force, the force required to remove some particulate may induce collateral damage to the wafer as part of that process. In an embodiment, reducing the attractive force enables state-of-the-art cleaning methods to be extended to remove defects that would otherwise remain. Embodiments described herein may be implemented to enables new cleaning methods that have previously been
20 ineffective since, as implemented, they were not suitable to overcome the attractive forces of particles and a wafer surface.

[0072] To provide context, van der Waals forces include attraction and repulsions between atoms, molecules, and surfaces, as well as other intermolecular forces. Van der Waals forces differ from covalent and ionic bonding in that they are caused by correlations in the
25 fluctuating polarizations of nearby particles (a consequence of quantum dynamics). According to Coulomb's law, the magnitude of the electrostatic force of interaction between two point charges is directly proportional to the scalar multiplication of the magnitudes of charges and inversely proportional to the square of the distance between them. The magnitude of the electrostatic force of interaction between two point charges is directly proportional to the scalar
30 multiplication of the magnitudes of charges and inversely proportional to the square of the distance between them.

[0073] Embodiments described herein may provide an approach to modulate a charge at a wafer substrate surface. Modulation may be effected by one or more of ionization, corona discharge ionization, variable wavelength UV radiation in a vacuum chamber, and
35 electrophoresis techniques for separating particles of differing charge in solution. In an

embodiment, the substrate potential is changed with respect to the particulate using an electrostatic chuck. Other approaches include electrostatic induction or magnetic/electromagnetic techniques.

[0074] Figure 11 is a schematic of an assembly 1100 for ex situ enhanced defect removal from a substrate, in accordance with an embodiment of the present invention. Referring to Figure 11, the ex situ assembly 1100 includes an incoming ion source 1104 and an exhaust port 1106. Substrates 1102 are housed between the incoming ion source 1104 and exhaust port 1106 for pre-cleaning and/or cleaning.

[0075] Figure 12 is a schematic of an assembly 1200 for wet processing for enhancing defect removal from a substrate, in accordance with an embodiment of the present invention. Referring to Figure 12, the assembly 1200 includes or is a wet clean chamber. An ion delivery sparge bar arm 1202 is situated over a wafer 1204 in the wet clean chamber.

[0076] In an embodiment, ionization is used to reduce static charge on wafer surfaces. In one embodiment, ionization is implemented as a dry treatment. In one such embodiment, an ex situ approach is used with ionization performed in a separate chamber prior to a dry clean process. In another embodiment, ionization is implemented as an in situ treatment, e.g., where an ionization procedure is implemented into a dry clean chamber and can be added as part of a cleaning recipe.

[0077] Figure 13 is a schematic of an assembly 1300 for ex situ enhanced defect removal from a substrate, in accordance with an embodiment of the present invention. Referring to Figure 13, the ex situ assembly 1300 includes an incoming ion source 1304 and an exhaust port 1306. Substrates 1302 are housed in a vacuum chamber between the incoming ion source 1304 and exhaust port 1306 for pre-cleaning or cleaning.

[0078] Figure 14 is a schematic of an assembly 1400 for in situ ionization of a substrate, in accordance with an embodiment of the present invention. Referring to Figure 14, the assembly 1400 includes or is a dry clean vacuum chamber. An ion delivery sparge bar arm 1402 is situated over a wafer 1404 in the dry clean vacuum chamber.

[0079] In an embodiment, ionization is achieved using via radiation, such as UV or soft X-ray radiation. Such an approach may be referred to as a static surface charge reduction method. In one embodiment, UV radiation is used to reduce electrostatic potential of a wafer surface. Gas molecules in close proximity to the wafer substrate generate ions and electrons used to neutralize the wafer substrate charge to provide a non-biased state. Particle removal efficiency may be improved by reducing the attractive force between the substrate and the wafer. In a specific embodiment, radiation-based ionization is implemented to improve a state-of-the-art wet clean method. In a particular embodiment, radiation-based ionization is implemented as an ex

situ treatment prior to entering a wet clean chamber. Such a treatment may be used as a pretreatment for either a wet clean or a dry clean chamber. In another particular embodiment, radiation-based ionization is implemented as an in situ treatment in a vacuum chamber. The ionization may be effected using gas cluster momentum transfer via a gas nozzle, where charge reduction and particle removal operations are alternated until particle removal is complete. Referring again to Figure 6, in an embodiment, operation (A) is a pretreatment operations, and operation (B) is a cleaning operation.

[0080] Figure 15 is a schematic of a vacuum chamber 1500, in accordance with an embodiment of the present invention. Referring to Figure 15, the vacuum chamber 1500 is shown as a single wafer 1502 configuration. It is to be appreciated, however, that a batch configuration would include multiple wafers. The vacuum chamber 1500 includes a variable wavelength UV source 1504. In one embodiment, following UV exposure, the wafer 1502 is transferred to a load lock chamber 1506 as an intermediate operation prior to robotic transport to an atmospheric clean chamber 1508. In another embodiment, following UV exposure, the wafer 1502 is transferred directly to an atmospheric clean chamber 1508.

[0081] In another embodiment, electrophoresis is implemented as an in situ wet etch treatment to separate a particle (or particles) from a wafer surface. An electric field may be controlled and modulated to enable enhanced removal of particles with differing polarity and charge, as described above in association with Figure 8. In one such embodiment, enhanced wafer cleaning is effected by making the substrate (wafer) act as an anode and/or cathode by varying the polarity of the substrate using a wafer chuck to set the wafer surface potential. The media is optimized to effectively remove particles from solution once detached from the wafer surface, which avoids re-attraction to the substrate surface when the polarity switched. In an embodiment, the media includes ligands for binding to a released charged particle such that reattachment is further inhibited. In an embodiment, a variable/switching power supply is used to control the charge of the wafer and media. In a particular embodiment, electrophoresis is implemented in a wet immersion tank, as described above. In another particular embodiment, electrophoresis is implemented in a single wafer spray tool, as is also described above, e.g., as the right-hand portion of Figure 9.

[0082] In another embodiment, electrostatic induction is implemented as a treatment to separate a particle (or particles) from a wafer surface. In one embodiment, an electrostatic chuck is used to create a potential on a wafer. The potential impacts the attractive force with which particles adhere to the wafer. By controlling and/or varying the polarity and magnitude of the charge, the attractive force of particulates of different composition/native charge can be neutralized or reduced, improving removal efficiency. Particles with the lowest attractive force

may be removed by a cleaning function. In one embodiment, such a cleaning function is repeated with each change in the electrostatic chuck/wafer potential. Particle removal may be effected using a shockwave from inert gas flow in a vacuum or by physical bombardment (momentum transfer) of a gas cluster. Overall, the approach involves electrical or charge attraction by an alternatively charged device in close proximity to the wafer substrate, e.g., an electrostatic chuck or electrostatic “wand”, as described above in association with Figure 10. In one embodiment, electrostatic induction is used in situ or ex situ prior to a wet clean operation, or in between wet clean particle removal operations.

[0083] In an embodiment involving a wet processing application, an electrostatically charged arm may be used to effect electrostatic induction. For example, Figure 16 illustrates an assembly 1600 for in situ enhanced defect removal from a substrate 1602, in accordance with an embodiment of the present invention. Referring to Figure 16, the in situ example of an assembly 1600 for substrate 1602 treatment includes a wet process scan arm 1604. The scan arm 1604 may be a recipe controlled electrostatically charged arm. The scan arm 1604 may be configured or manipulated to have a particular rotation (angle and/or speed), a particular Z-height (distance from wafer), and a particular charge (polarity, magnitude, frequency).

[0084] In an embodiment involving a vacuum chamber application, a dry clean arm may be used to effect electrostatic induction. For example, Figure 17 illustrates another assembly 1700 for in situ enhanced defect removal from a substrate 1702, in accordance with another embodiment of the present invention. Referring to Figure 17, the in situ example of an assembly 1700 for substrate 1702 treatment includes a dry process scan arm 1704. The scan arm 1704 is configured to deliver a gas shock wave or molecular gas cluster at the wafer surface to provide a physical separation of particles from the wafer. In an embodiment, an electrostatic chuck 1706 is also included in the assembly 1700, as is depicted in Figure 17.

[0085] In another embodiment, a focused magnetic field approach is implemented in conjunction with ultrasonic shockwave or gas nozzle approaches. A magnetic field is used to temporarily change the wafer surface charge or the charge of the particle/defect on the wafer surface. In one embodiment, the magnetic field is focused on a targeted area of the wafer. The field can be modulated, and magnetic field polarity and magnitude can be rapidly modified to change the target particulate of different native charge/surface charge relationships. In an embodiment, particle removal is effected using a focused gas cluster nozzle or a focus shockwave, either of which can be used in conjunction with the magnetic field. In another embodiment, a focused magnetic field approach is implemented in conjunction with an electrostatic chuck device, where the electrostatic device is included to modulate the surface charge of the wafer. In yet another embodiment, a focused magnetic field approach is

implemented in conjunction with an electrostatic chuck device and one or both of an ultrasonic shockwave or gas nozzle approach.

[0086] Figure 18 illustrates an assembly for implementing a focused magnetic field approach in conjunction with an ultrasonic shockwave or gas nozzle approach, in accordance with an embodiment of the present invention. Referring to Figure 18, a magnetic field generator 1800 assembly includes a chamber 1802 coupled with a magnetic field generator 1804. The chamber 1802 includes a support location for a wafer 1806. In an optional embodiment, the support location is or includes an electrostatic chuck 1808. The chamber 1802 also includes a focused magnetic field 1810 and associated particle removal nozzle 1812.

[0087] More generally, referring to all of the above aspects of embodiments of the present invention, equipment or a process for defect removal through substrate and media charge modulation is implemented during fabrication of a metallization layer in a semiconductor device. It is to be appreciated that a metallization layer having lines with line cuts (or plugs) and having associated vias may be fabricated above a substrate and, in one embodiment, may be fabricated above a previous metallization layer. As an example, Figure 19 illustrates a plan view and corresponding cross-sectional view of a previous layer metallization structure, in accordance with an embodiment of the present invention. Referring to Figure 19, a starting structure 1900 includes a pattern of metal lines 1902 and interlayer dielectric (ILD) lines 1904. The starting structure 1900 may be patterned in a grating-like pattern with metal lines spaced at a constant pitch and having a constant width, as is depicted in Figure 19. Although not shown, the lines 1902 may have interruptions (i.e., cuts or plugs) at various locations along the lines. The pattern, for example, may be fabricated by a pitch halving or pitch quartering approach. Some of the lines may be associated with underlying vias, such as line 1902' shown as an example in the cross-sectional view.

[0088] In an embodiment, fabrication of a metallization layer on the previous metallization structure of Figure 19 begins with formation of an interlayer dielectric (ILD) material above the structure 1900. A hardmask material layer may then be formed on the ILD layer. The hardmask material layer may be patterned to form a grating of unidirectional lines orthogonal to the lines 1902 of 1900. In one embodiment, the grating of unidirectional hardmask lines is fabricated using conventional lithography (e.g., photoresist and other associated layers) and may have a line density defined by a pitch-halving, pitch-quartering etc. approach as described above. The grating of hardmask lines leaves exposed a grating region of the underlying ILD layer. It is these exposed portions of the ILD layer that are ultimately patterned for metal line formation, via formation, and plug formation. For example, in an embodiment, via locations are patterned in regions of the exposed ILD. The patterning may involve formation of a

resist layer and patterning of the resist layer to provide via opening locations which may be etched into the ILD regions. The lines of overlying hardmask can be used to confine the vias to only regions of the exposed ILD, with overlap accommodated by the hardmask lines which can effectively be used as an etch stop. Plug (or cut) locations may also be patterned in exposed regions of the ILD, as confined by the overlying hardmask lines, in a separate processing operation. The fabrication of cuts or plugs effectively preserve regions of ILD that will ultimately interrupt metal lines fabricated therein. Metal lines may then be fabricated using a damascene approach, where exposed portions of the ILD (those portions between the hardmask lines and not protected by a plug preservation layer, such as a resist layer patterned during “cutting”) are partially recessed. The recessing may further extend the via locations to open metal lines from the underlying metallization structure. The partially recessed ILD regions are then filled with metal (a process which may also involve filling the via locations), e.g., by plating and CMP processing, to provide metal lines between the overlying hardmask lines. The hardmask lines may ultimately be removed for completion of a metallization structure. It is to be appreciated that the above ordering of line cuts, via formation, and ultimate line formation is provided only as an example.

[0089] In an embodiment, as used throughout the present description, interlayer dielectric (ILD) material is composed of or includes a layer of a dielectric or insulating material. Examples of suitable dielectric materials include, but are not limited to, oxides of silicon (e.g., silicon dioxide (SiO_2)), doped oxides of silicon, fluorinated oxides of silicon, carbon doped oxides of silicon, various low-k dielectric materials known in the arts, and combinations thereof. The interlayer dielectric material may be formed by conventional techniques, such as, for example, chemical vapor deposition (CVD), physical vapor deposition (PVD), or by other deposition methods.

[0090] In an embodiment, as is also used throughout the present description, interconnect material is composed of one or more metal or other conductive structures. A common example is the use of copper lines and structures that may or may not include barrier layers between the copper and surrounding ILD material. As used herein, the term metal includes alloys, stacks, and other combinations of multiple metals. For example, the metal interconnect lines may include barrier layers, stacks of different metals or alloys, etc. The interconnect lines are also sometimes referred to in the arts as traces, wires, lines, metal, or simply interconnect.

[0091] In an embodiment, as is also used throughout the present description, hardmask materials are composed of dielectric materials different from the interlayer dielectric material. In some embodiments, a hardmask layer includes a layer of a nitride of silicon (e.g., silicon nitride) or a layer of an oxide of silicon, or both, or a combination thereof. Other suitable materials may

include carbon-based materials. In another embodiment, a hardmask material includes a metal species. For example, a hardmask or other overlying material may include a layer of a nitride of titanium or another metal (e.g., titanium nitride). Potentially lesser amounts of other materials, such as oxygen, may be included in one or more of these layers. Alternatively, other hardmask layers known in the arts may be used depending upon the particular implementation. The hardmask layers maybe formed by CVD, PVD, or by other deposition methods.

[0092] It is to be appreciated that the layers and materials described in association with Figure 19 are typically formed on or above an underlying semiconductor substrate or structure, such as underlying device layer(s) of an integrated circuit. In an embodiment, an underlying semiconductor substrate represents a general workpiece object used to manufacture integrated circuits. The semiconductor substrate often includes a wafer or other piece of silicon or another semiconductor material. Suitable semiconductor substrates include, but are not limited to, single crystal silicon, polycrystalline silicon and silicon on insulator (SOI), as well as similar substrates formed of other semiconductor materials. The semiconductor substrate, depending on the stage of manufacture, often includes transistors, integrated circuitry, and the like. The substrate may also include semiconductor materials, metals, dielectrics, dopants, and other materials commonly found in semiconductor substrates. Furthermore, the structure depicted in Figure 3 may be fabricated on underlying lower level interconnect layers.

[0093] In another embodiment, equipment or a process for defect removal through substrate and media charge modulation is implemented during fabrication of semiconductor devices, such as PMOS or NMOS devices of an integrated circuit. As an example of a completed device, Figures 20A and 20B illustrate a cross-sectional view and a plan view (taken along the a-a' axis of the cross-sectional view), respectively, of a non-planar semiconductor device having a plurality of fins, in accordance with an embodiment of the present invention.

[0094] Referring to Figure 20A, a semiconductor structure or device 2000 includes a non-planar active region (e.g., a fin structure including protruding fin portion 2004 and sub-fin region 2005) formed from substrate 2002, and within isolation region 2006. A gate line 2008 is disposed over the protruding portions 2004 of the non-planar active region as well as over a portion of the isolation region 2006. As shown, gate line 2008 includes a gate electrode 2050 and a gate dielectric layer 2052. In one embodiment, gate line 2008 may also include a dielectric cap layer 2054. A gate contact 2014, and overlying gate contact via 2016 are also seen from this perspective, along with an overlying metal interconnect 2060, all of which are disposed in inter-layer dielectric stacks or layers 2070. Also seen from the perspective of Figure 20A, the gate contact 2014 is, in one embodiment, disposed over isolation region 2006, but not over the non-planar active regions.

[0095] Referring to Figure 20B, the gate line 2008 is shown as disposed over the protruding fin portions 2004. Source and drain regions 2004A and 2004B of the protruding fin portions 2004 can be seen from this perspective. In one embodiment, the source and drain regions 2004A and 2004B are doped portions of original material of the protruding fin portions 2004. In another embodiment, the material of the protruding fin portions 2004 is removed and replaced with another semiconductor material, e.g., by epitaxial deposition. In either case, the source and drain regions 2004A and 2004B may extend below the height of dielectric layer 2006, i.e., into the sub-fin region 2005.

[0096] In an embodiment, the semiconductor structure or device 2000 is a non-planar device such as, but not limited to, a fin-FET or a tri-gate device. In such an embodiment, a corresponding semiconducting channel region is composed of or is formed in a three-dimensional body. In one such embodiment, the gate electrode stacks of gate lines 2008 surround at least a top surface and a pair of sidewalls of the three-dimensional body.

[0097] Embodiments disclosed herein may be used to manufacture a wide variety of different types of integrated circuits and/or microelectronic devices. Examples of such integrated circuits include, but are not limited to, processors, chipset components, graphics processors, digital signal processors, micro-controllers, and the like. In other embodiments, semiconductor memory may be manufactured. Moreover, the integrated circuits or other microelectronic devices may be used in a wide variety of electronic devices known in the arts. For example, in computer systems (e.g., desktop, laptop, server), cellular phones, personal electronics, etc. The integrated circuits may be coupled with a bus and other components in the systems. For example, a processor may be coupled by one or more buses to a memory, a chipset, etc. Each of the processor, the memory, and the chipset, may potentially be manufactured using the approaches disclosed herein.

[0098] Figure 21 illustrates a computing device 2100 in accordance with one implementation of the invention. The computing device 2100 houses a board 2102. The board 2102 may include a number of components, including but not limited to a processor 2104 and at least one communication chip 2106. The processor 2104 is physically and electrically coupled to the board 2102. In some implementations the at least one communication chip 2106 is also physically and electrically coupled to the board 2102. In further implementations, the communication chip 2106 is part of the processor 2104.

[0099] Depending on its applications, computing device 2100 may include other components that may or may not be physically and electrically coupled to the board 2102. These other components include, but are not limited to, volatile memory (e.g., DRAM), non-volatile memory (e.g., ROM), flash memory, a graphics processor, a digital signal processor, a crypto

processor, a chipset, an antenna, a display, a touchscreen display, a touchscreen controller, a battery, an audio codec, a video codec, a power amplifier, a global positioning system (GPS) device, a compass, an accelerometer, a gyroscope, a speaker, a camera, and a mass storage device (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

5 **[00100]** The communication chip 2106 enables wireless communications for the transfer of data to and from the computing device 2100. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires,
10 although in some embodiments they might not. The communication chip 2106 may implement any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE 802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and
15 beyond. The computing device 2100 may include a plurality of communication chips 2106. For instance, a first communication chip 2106 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 2106 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

20 **[00101]** The processor 2104 of the computing device 2100 includes an integrated circuit die packaged within the processor 2104. In some implementations of the invention, the integrated circuit die of the processor includes one or more structures fabricated using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention. The term “processor” may refer to any
25 device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00102] The communication chip 2106 also includes an integrated circuit die packaged within the communication chip 2106. In accordance with another implementation of
30 embodiments of the invention, the integrated circuit die of the communication chip includes one or more structures fabricated using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention.

[00103] In further implementations, another component housed within the computing
35 device 2100 may contain an integrated circuit die that includes one or more structures fabricated

using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention.

[00104] In various implementations, the computing device 2100 may be a laptop, a netbook, a notebook, an ultrabook, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 2100 may be any other electronic device that processes data.

[00105] Embodiments of the present invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to embodiments of the present invention. In one embodiment, the computer system is coupled with a system for defect removal through substrate and media charge modulation, such as described in association with Figures 1 and 2. A machine-readable medium includes any mechanism for storing or transmitting information in a form readable by a machine (e.g., a computer). For example, a machine-readable (e.g., computer-readable) medium includes a machine (e.g., a computer) readable storage medium (e.g., read only memory ("ROM"), random access memory ("RAM"), magnetic disk storage media, optical storage media, flash memory devices, etc.), a machine (e.g., computer) readable transmission medium (electrical, optical, acoustical or other form of propagated signals (e.g., infrared signals, digital signals, etc.)), etc.

[00106] Figure 22 illustrates a diagrammatic representation of a machine in the exemplary form of a computer system 2200 within which a set of instructions, for causing the machine to perform any one or more of the methodologies described herein (such as end-point detection), may be executed. In alternative embodiments, the machine may be connected (e.g., networked) to other machines in a Local Area Network (LAN), an intranet, an extranet, or the Internet. The machine may operate in the capacity of a server or a client machine in a client-server network environment, or as a peer machine in a peer-to-peer (or distributed) network environment. The machine may be a personal computer (PC), a tablet PC, a set-top box (STB), a Personal Digital Assistant (PDA), a cellular telephone, a web appliance, a server, a network router, switch or bridge, or any machine capable of executing a set of instructions (sequential or otherwise) that specify actions to be taken by that machine. Further, while only a single machine is illustrated, the term "machine" shall also be taken to include any collection of machines (e.g., computers) that individually or jointly execute a set (or multiple sets) of instructions to perform any one or more of the methodologies described herein.

[00107] The exemplary computer system 2200 includes a processor 2202, a main memory 2204 (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM) such as synchronous DRAM (SDRAM) or Rambus DRAM (RDRAM), etc.), a static memory 2206 (e.g., flash memory, static random access memory (SRAM), etc.), and a secondary memory 5 2218 (e.g., a data storage device), which communicate with each other via a bus 2230.

[00108] Processor 2202 represents one or more general-purpose processing devices such as a microprocessor, central processing unit, or the like. More particularly, the processor 2202 may be a complex instruction set computing (CISC) microprocessor, reduced instruction set computing (RISC) microprocessor, very long instruction word (VLIW) microprocessor, 10 processor implementing other instruction sets, or processors implementing a combination of instruction sets. Processor 2202 may also be one or more special-purpose processing devices such as an application specific integrated circuit (ASIC), a field programmable gate array (FPGA), a digital signal processor (DSP), network processor, or the like. Processor 2202 is configured to execute the processing logic 2226 for performing the operations described herein.

15 [00109] The computer system 2200 may further include a network interface device 2208. The computer system 2200 also may include a video display unit 2210 (e.g., a liquid crystal display (LCD), a light emitting diode display (LED), or a cathode ray tube (CRT)), an alphanumeric input device 2212 (e.g., a keyboard), a cursor control device 2214 (e.g., a mouse), and a signal generation device 2216 (e.g., a speaker).

20 [00110] The secondary memory 2218 may include a machine-accessible storage medium (or more specifically a computer-readable storage medium) 2232 on which is stored one or more sets of instructions (e.g., software 2222) embodying any one or more of the methodologies or functions described herein. The software 2222 may also reside, completely or at least partially, within the main memory 2204 and/or within the processor 2202 during execution thereof by the 25 computer system 2200, the main memory 2204 and the processor 2202 also constituting machine-readable storage media. The software 2222 may further be transmitted or received over a network 2220 via the network interface device 2208.

[00111] While the machine-accessible storage medium 2232 is shown in an exemplary embodiment to be a single medium, the term “machine-readable storage medium” should be 30 taken to include a single medium or multiple media (e.g., a centralized or distributed database, and/or associated caches and servers) that store the one or more sets of instructions. The term “machine-readable storage medium” shall also be taken to include any medium that is capable of storing or encoding a set of instructions for execution by the machine and that cause the machine to perform any one or more of the methodologies of the present invention. The term “machine- 35 readable storage medium” shall accordingly be taken to include, but not be limited to, solid-state

memories, and optical and magnetic media.

[00112] Implementations of embodiments of the invention may be formed or carried out on a substrate, such as a semiconductor substrate. In one implementation, the semiconductor substrate may be a crystalline substrate formed using a bulk silicon or a silicon-on-insulator substructure. In other implementations, the semiconductor substrate may be formed using alternate materials, which may or may not be combined with silicon, that include but are not limited to germanium, indium antimonide, lead telluride, indium arsenide, indium phosphide, gallium arsenide, indium gallium arsenide, gallium antimonide, or other combinations of group III-V or group IV materials. Although a few examples of materials from which the substrate may be formed are described here, any material that may serve as a foundation upon which a semiconductor device may be built falls within the spirit and scope of the present invention.

[00113] A plurality of transistors, such as metal-oxide-semiconductor field-effect transistors (MOSFET or simply MOS transistors), may be fabricated on the substrate. In various implementations of the invention, the MOS transistors may be planar transistors, nonplanar transistors, or a combination of both. Nonplanar transistors include FinFET transistors such as double-gate transistors and tri-gate transistors, and wrap-around or all-around gate transistors such as nanoribbon and nanowire transistors. Although the implementations described herein may illustrate only planar transistors, it should be noted that the invention may also be carried out using nonplanar transistors.

[00114] Each MOS transistor includes a gate stack formed of at least two layers, a gate dielectric layer and a gate electrode layer. The gate dielectric layer may include one layer or a stack of layers. The one or more layers may include silicon oxide, silicon dioxide (SiO_2) and/or a high-k dielectric material. The high-k dielectric material may include elements such as hafnium, silicon, oxygen, titanium, tantalum, lanthanum, aluminum, zirconium, barium, strontium, yttrium, lead, scandium, niobium, and zinc. Examples of high-k materials that may be used in the gate dielectric layer include, but are not limited to, hafnium oxide, hafnium silicon oxide, lanthanum oxide, lanthanum aluminum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, titanium oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate. In some embodiments, an annealing process may be carried out on the gate dielectric layer to improve its quality when a high-k material is used.

[00115] The gate electrode layer is formed on the gate dielectric layer and may consist of at least one P-type workfunction metal or N-type workfunction metal, depending on whether the transistor is to be a PMOS or an NMOS transistor. In some implementations, the gate electrode layer may consist of a stack of two or more metal layers, where one or more metal layers are

workfunction metal layers and at least one metal layer is a fill metal layer.

[00116] For a PMOS transistor, metals that may be used for the gate electrode include, but are not limited to, ruthenium, palladium, platinum, cobalt, nickel, and conductive metal oxides, e.g., ruthenium oxide. A P-type metal layer will enable the formation of a PMOS gate electrode with a workfunction that is between about 4.9 eV and about 5.2 eV. For an NMOS transistor, metals that may be used for the gate electrode include, but are not limited to, hafnium, zirconium, titanium, tantalum, aluminum, alloys of these metals, and carbides of these metals such as hafnium carbide, zirconium carbide, titanium carbide, tantalum carbide, and aluminum carbide. An N-type metal layer will enable the formation of an NMOS gate electrode with a workfunction that is between about 3.9 eV and about 4.2 eV.

[00117] In some implementations, the gate electrode may consist of a “U”-shaped structure that includes a bottom portion substantially parallel to the surface of the substrate and two sidewall portions that are substantially perpendicular to the top surface of the substrate. In another implementation, at least one of the metal layers that form the gate electrode may simply be a planar layer that is substantially parallel to the top surface of the substrate and does not include sidewall portions substantially perpendicular to the top surface of the substrate. In further implementations of the invention, the gate electrode may consist of a combination of U-shaped structures and planar, non-U-shaped structures. For example, the gate electrode may consist of one or more U-shaped metal layers formed atop one or more planar, non-U-shaped layers.

[00118] In some implementations of the invention, a pair of sidewall spacers may be formed on opposing sides of the gate stack that bracket the gate stack. The sidewall spacers may be formed from a material such as silicon nitride, silicon oxide, silicon carbide, silicon nitride doped with carbon, and silicon oxynitride. Processes for forming sidewall spacers are well known in the art and generally include deposition and etching process operations. In an alternate implementation, a plurality of spacer pairs may be used, for instance, two pairs, three pairs, or four pairs of sidewall spacers may be formed on opposing sides of the gate stack.

[00119] As is well known in the art, source and drain regions are formed within the substrate adjacent to the gate stack of each MOS transistor. The source and drain regions are generally formed using either an implantation/diffusion process or an etching/deposition process. In the former process, dopants such as boron, aluminum, antimony, phosphorous, or arsenic may be ion-implanted into the substrate to form the source and drain regions. An annealing process that activates the dopants and causes them to diffuse further into the substrate typically follows the ion implantation process. In the latter process, the substrate may first be etched to form recesses at the locations of the source and drain regions. An epitaxial deposition process may then be carried out to fill the recesses with material that is used to fabricate the source and drain

regions. In some implementations, the source and drain regions may be fabricated using a silicon alloy such as silicon germanium or silicon carbide. In some implementations the epitaxially deposited silicon alloy may be doped in situ with dopants such as boron, arsenic, or phosphorous. In further embodiments, the source and drain regions may be formed using one or more alternate semiconductor materials such as germanium or a group III-V material or alloy. And in further embodiments, one or more layers of metal and/or metal alloys may be used to form the source and drain regions.

[00120] One or more interlayer dielectrics (ILD) are deposited over the MOS transistors. The ILD layers may be formed using dielectric materials known for their applicability in integrated circuit structures, such as low-k dielectric materials. Examples of dielectric materials that may be used include, but are not limited to, silicon dioxide (SiO₂), carbon doped oxide (CDO), silicon nitride, organic polymers such as perfluorocyclobutane or polytetrafluoroethylene, fluorosilicate glass (FSG), and organosilicates such as silsesquioxane, siloxane, or organosilicate glass. The ILD layers may include pores or air gaps to further reduce their dielectric constant.

[00121] Figure 23 illustrates an interposer 2300 that includes one or more embodiments of the invention. The interposer 2300 is an intervening substrate used to bridge a first substrate 2302 to a second substrate 2304. The first substrate 2302 may be, for instance, an integrated circuit die. The second substrate 2304 may be, for instance, a memory module, a computer motherboard, or another integrated circuit die. Generally, the purpose of an interposer 2300 is to spread a connection to a wider pitch or to reroute a connection to a different connection. For example, an interposer 2300 may couple an integrated circuit die to a ball grid array (BGA) 2306 that can subsequently be coupled to the second substrate 2304. In some embodiments, the first and second substrates 2302/2304 are attached to opposing sides of the interposer 1600. In other embodiments, the first and second substrates 2302/2304 are attached to the same side of the interposer 2300. And in further embodiments, three or more substrates are interconnected by way of the interposer 2300.

[00122] The interposer 2300 may be formed of an epoxy resin, a fiberglass-reinforced epoxy resin, a ceramic material, or a polymer material such as polyimide. In further implementations, the interposer may be formed of alternate rigid or flexible materials that may include the same materials described above for use in a semiconductor substrate, such as silicon, germanium, and other group III-V and group IV materials.

[00123] The interposer may include metal interconnects 2308 and vias 2310, including but not limited to through-silicon vias (TSVs) 2312. The interposer 2300 may further include embedded devices 2314, including both passive and active devices. Such devices include, but

are not limited to, capacitors, decoupling capacitors, resistors, inductors, fuses, diodes, transformers, sensors, and electrostatic discharge (ESD) devices. More complex devices such as radio-frequency (RF) devices, power amplifiers, power management devices, antennas, arrays, sensors, and MEMS devices may also be formed on the interposer 2300.

5 [00124] In accordance with embodiments of the invention, apparatuses or processes disclosed herein may be used in the fabrication of interposer 2300.

[00125] Figure 24 illustrates a computing device 2400 in accordance with one embodiment of the invention. The computing device 2400 may include a number of components. In one embodiment, these components are attached to one or more motherboards.

10 In an alternate embodiment, these components are fabricated onto a single system-on-a-chip (SoC) die rather than a motherboard. The components in the computing device 2400 include, but are not limited to, an integrated circuit die 2402 and at least one communication chip 2408. In some implementations the communication chip 2408 is fabricated as part of the integrated circuit die 2402. The integrated circuit die 2402 may include a CPU 1704 as well as on-die memory
15 2406, often used as cache memory, that can be provided by technologies such as embedded DRAM (eDRAM) or spin-transfer torque memory (STTM or STTM-RAM).

[00126] Computing device 2400 may include other components that may or may not be physically and electrically coupled to the motherboard or fabricated within an SoC die. These other components include, but are not limited to, volatile memory 2410 (e.g., DRAM), non-
20 volatile memory 2412 (e.g., ROM or flash memory), a graphics processing unit 2414 (GPU), a digital signal processor 2416, a crypto processor 2442 (a specialized processor that executes cryptographic algorithms within hardware), a chipset 2420, an antenna 2422, a display or a touchscreen display 2424, a touchscreen controller 2426, a battery 2429 or other power source, a power amplifier (not shown), a global positioning system (GPS) device 2428, a compass 2430, a
25 motion coprocessor or sensors 2432 (that may include an accelerometer, a gyroscope, and a compass), a speaker 2434, a camera 2436, user input devices 2438 (such as a keyboard, mouse, stylus, and touchpad), and a mass storage device 2440 (such as hard disk drive, compact disk (CD), digital versatile disk (DVD), and so forth).

[00127] The communications chip 2408 enables wireless communications for the transfer
30 of data to and from the computing device 2400. The term “wireless” and its derivatives may be used to describe circuits, devices, systems, methods, techniques, communications channels, etc., that may communicate data through the use of modulated electromagnetic radiation through a non-solid medium. The term does not imply that the associated devices do not contain any wires, although in some embodiments they might not. The communication chip 2408 may implement
35 any of a number of wireless standards or protocols, including but not limited to Wi-Fi (IEEE

802.11 family), WiMAX (IEEE 802.16 family), IEEE 802.20, long term evolution (LTE), Ev-DO, HSPA+, HSDPA+, HSUPA+, EDGE, GSM, GPRS, CDMA, TDMA, DECT, Bluetooth, derivatives thereof, as well as any other wireless protocols that are designated as 3G, 4G, 5G, and beyond. The computing device 2400 may include a plurality of communication chips 2408. For instance, a first communication chip 2408 may be dedicated to shorter range wireless communications such as Wi-Fi and Bluetooth and a second communication chip 2408 may be dedicated to longer range wireless communications such as GPS, EDGE, GPRS, CDMA, WiMAX, LTE, Ev-DO, and others.

[00128] The processor 2404 of the computing device 2400 includes one or more structures fabricated using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention. The term “processor” may refer to any device or portion of a device that processes electronic data from registers and/or memory to transform that electronic data into other electronic data that may be stored in registers and/or memory.

[00129] The communication chip 2408 may also include one or more structures fabricated using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention.

[00130] In further embodiments, another component housed within the computing device 2400 may contain one or more structures fabricated using equipment or a process for defect removal through substrate and media charge modulation, in accordance with implementations of embodiments of the invention.

[00131] In various embodiments, the computing device 2400 may be a laptop computer, a netbook computer, a notebook computer, an ultrabook computer, a smartphone, a tablet, a personal digital assistant (PDA), an ultra mobile PC, a mobile phone, a desktop computer, a server, a printer, a scanner, a monitor, a set-top box, an entertainment control unit, a digital camera, a portable music player, or a digital video recorder. In further implementations, the computing device 2400 may be any other electronic device that processes data.

[00132] The above description of illustrated implementations of embodiments of the invention, including what is described in the Abstract, is not intended to be exhaustive or to limit the invention to the precise forms disclosed. While specific implementations of, and examples for, the invention are described herein for illustrative purposes, various equivalent modifications are possible within the scope of the invention, as those skilled in the relevant art will recognize.

[00133] These modifications may be made to the invention in light of the above detailed description. The terms used in the following claims should not be construed to limit the invention to the specific implementations disclosed in the specification and the claims. Rather,

the scope of the invention is to be determined entirely by the following claims, which are to be construed in accordance with established doctrines of claim interpretation.

[00134] Thus, equipment and processes for enhanced defect removal through substrate and media charge modulation have been described.

5 [00135] Example embodiment 1: A system for enhancing defect removal from a wafer or substrate includes a vacuum processing chamber. A wafer or substrate processing region is located within the vacuum processing chamber. A chuck is immediately below the wafer or substrate processing region. A module is coupled to the vacuum processing chamber, the module for effecting charge modulation at the wafer or substrate processing region.

10 [00136] Example embodiment 2: The system of example embodiment 1, wherein the module is configured to provide a corona discharge at the wafer or substrate processing region.

[00137] Example embodiment 3: The system of example embodiment 1 or 2, wherein the module is configured to provide ultra-violet (UV) or soft X-ray radiation at the wafer or substrate processing region.

15 [00138] Example embodiment 4: The system of example embodiment 1, 2 or 3, wherein the module is configured to reduce static charge at the wafer or substrate processing region through electrophoresis.

[00139] Example embodiment 5: The system of example embodiment 1, 2, 3 or 4, wherein the module includes a variable switching power supply.

20 [00140] Example embodiment 6: The system of example embodiment 1, 2, 3, 4 or 5, wherein the module includes an electrostatic wand.

[00141] Example embodiment 7: The system of example embodiment 1, 2, 3, 4, 5 or 6, wherein the module is configured to provide a modulated magnetic field at the wafer or substrate processing region.

25 [00142] Example embodiment 8: The system of example embodiment 1, 2, 3, 4, 5, 6 or 7, wherein the vacuum processing chamber is a pre-treatment chamber, and the system further includes a second chamber for processing subsequent to processing in the pre-treatment chamber.

[00143] Example embodiment 9: The system of example embodiment 1, 2, 3, 4, 5, 6, 7 or 8, wherein the chuck is a bipolar chuck.

30 [00144] Example embodiment 10: The system of example embodiment 1, 2, 3, 4, 5, 6, 7, 8 or 9, further including a focused gas cluster nozzle directed to the wafer or substrate processing region.

[00145] Example embodiment 11: The system of example embodiment 1, 2, 3, 4, 5, 6, 7, 8, 9 or 10, wherein the vacuum processing chamber is configured to deliver a focus shockwave to
35 the wafer or substrate processing region.

[00146] Example embodiment 12: A system for enhancing defect removal from a wafer or substrate includes a wet processing chamber. A wafer or substrate processing region is located within the wet processing chamber. A module is coupled to the wet processing chamber, the module for effecting charge modulation at the wafer or substrate processing region.

5 [00147] Example embodiment 13: The system of example embodiment 12, wherein the wet processing chamber is configured to perform a dry pretreatment operation prior to performing a wet cleaning operation.

[00148] Example embodiment 14: The system of example embodiment 12 or 13, wherein the module is configured to provide a corona discharge at the wafer or substrate processing
10 region.

[00149] Example embodiment 15: The system of example embodiment 12, 13 or 14, wherein the module is configured to provide ultra-violet (UV) or soft X-ray radiation at the wafer or substrate processing region.

[00150] Example embodiment 16: The system of example embodiment 12, 13, 14 or 15,
15 wherein the module is configured to reduce static charge at the wafer or substrate processing region through electrophoresis.

[00151] Example embodiment 17: The system of example embodiment 12, 13, 14, 15 or 16, wherein the module includes a variable switching power supply.

[00152] Example embodiment 18: The system of example embodiment 12, 13, 14, 15, 16
20 or 17, wherein the module includes an electrostatic wand.

[00153] Example embodiment 19: The system of example embodiment 12, 13, 14, 15, 16, 17 or 18, wherein the module is configured to provide a modulated magnetic field at the wafer or substrate processing region.

[00154] Example embodiment 20: The system of example embodiment 12, 13, 14, 15, 16,
25 17, 18 or 19, wherein the wet processing chamber is a pre-treatment chamber, and the system further includes a second chamber for processing subsequent to processing in the pre-treatment chamber.

[00155] Example embodiment 21: The system of example embodiment 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein the wet processing chamber includes a batch immersion tank for
30 processing a plurality of wafers or substrates at a same time.

[00156] Example embodiment 22: The system of example embodiment 12, 13, 14, 15, 16, 17, 18, 19 or 20, wherein the wet processing chamber includes a single wafer spray tank.

[00157] Example embodiment 23: The system of example embodiment 22, wherein the single wafer spray tank includes a chuck immediately below the wafer or substrate processing
35 region.

[00158] Example embodiment 24: A method for defect removal of a wafer or substrate includes providing a wafer or substrate in a processing chamber. The wafer or substrate has a number of particles attached to a surface of the wafer or substrate. The method also includes reducing the number of particles attached to the surface of the wafer or substrate through charge modulation at the surface of the wafer or substrate.

[00159] Example embodiment 25: The method of example embodiment 24, wherein reducing the number of particles attached to the surface of the wafer or substrate through charge modulation at the surface of the wafer or substrate includes using a charge modulation technique selected from the group consisting of ionization through corona discharge, providing ultra-violet (UV) or soft X-ray radiation, static charge modulation, and magnetic field modulation.

CLAIMS

What is claimed is:

1. A system for enhancing defect removal from a wafer or substrate, the system comprising:
5 a vacuum processing chamber;
a wafer or substrate processing region located within the vacuum processing chamber;
a chuck immediately below the wafer or substrate processing region; and
a module coupled to the vacuum processing chamber, the module for effecting charge
modulation at the wafer or substrate processing region.
10
2. The system of claim 1, wherein the module is configured to provide a corona discharge at the
wafer or substrate processing region.
3. The system of claim 1, wherein the module is configured to provide ultra-violet (UV) or soft
15 X-ray radiation at the wafer or substrate processing region.
4. The system of claim 1, wherein the module is configured to reduce static charge at the wafer
or substrate processing region through electrophoresis.
- 20 5. The system of claim 4, wherein the module comprises a variable switching power supply.
6. The system of claim 1, wherein the module comprises an electrostatic wand.
7. The system of claim 1, wherein the module is configured to provide a modulated magnetic
25 field at the wafer or substrate processing region.
8. The system of claim 1, wherein the vacuum processing chamber is a pre-treatment chamber,
the system further comprising:
a second chamber for processing subsequent to processing in the pre-treatment chamber.
30
9. The system of claim 1, wherein the chuck is a bipolar chuck.
10. The system of claim 1, further comprising:
a focused gas cluster nozzle directed to the wafer or substrate processing region.
35

11. The system of claim 1, wherein the vacuum processing chamber is configured to deliver a focus shockwave to the wafer or substrate processing region.

12. A system for enhancing defect removal from a wafer or substrate, the system comprising:

5 a wet processing chamber;

a wafer or substrate processing region located within the wet processing chamber; and

a module coupled to the wet processing chamber, the module for effecting charge modulation at the wafer or substrate processing region.

10 13. The system of claim 12, wherein the wet processing chamber is configured to perform a dry pretreatment operation prior to performing a wet cleaning operation.

14. The system of claim 12, wherein the module is configured to provide a corona discharge at the wafer or substrate processing region.

15 15. The system of claim 12, wherein the module is configured to provide ultra-violet (UV) or soft X-ray radiation at the wafer or substrate processing region.

16. The system of claim 12, wherein the module is configured to reduce static charge at the wafer or substrate processing region through electrophoresis.

17. The system of claim 16, wherein the module comprises a variable switching power supply.

18. The system of claim 12, wherein the module comprises an electrostatic wand.

19. The system of claim 12, wherein the module is configured to provide a modulated magnetic field at the wafer or substrate processing region.

20. The system of claim 12, wherein the wet processing chamber is a pre-treatment chamber, the system further comprising:

30 a second chamber for processing subsequent to processing in the pre-treatment chamber.

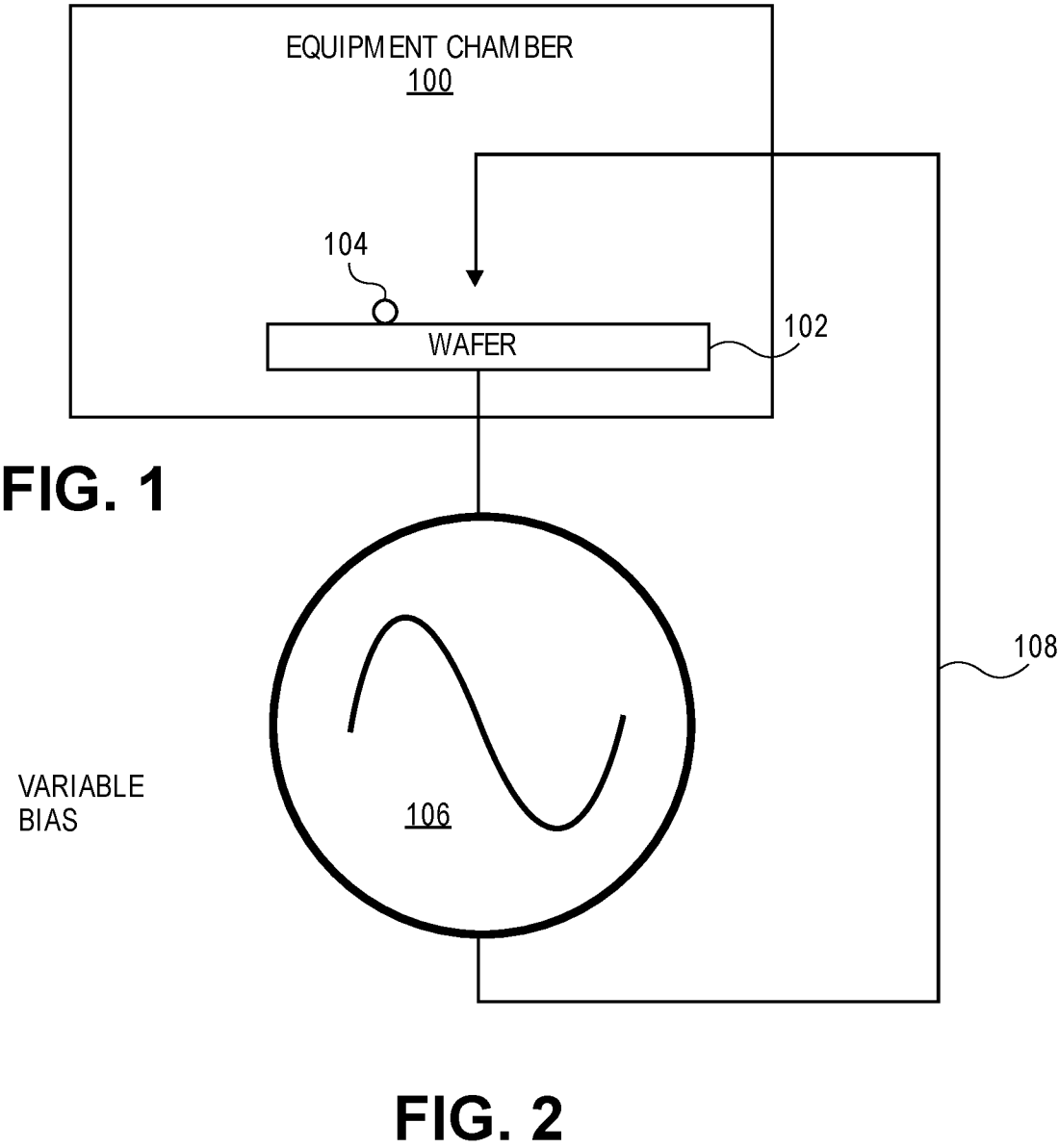
21. The system of claim 12, wherein the wet processing chamber comprises a batch immersion tank for processing a plurality of wafers or substrates at a same time.

22. The system of claim 12, wherein the wet processing chamber comprises a single wafer spray tank.

23. The system of claim 22, wherein the single wafer spray tank comprises a chuck immediately
5 below the wafer or substrate processing region.

24. A method for defect removal of a wafer or substrate, the method comprising:
providing a wafer or substrate in a processing chamber, the wafer or substrate having a
number of particles attached to a surface of the wafer or substrate; and
10 reducing the number of particles attached to the surface of the wafer or substrate through
charge modulation at the surface of the wafer or substrate.

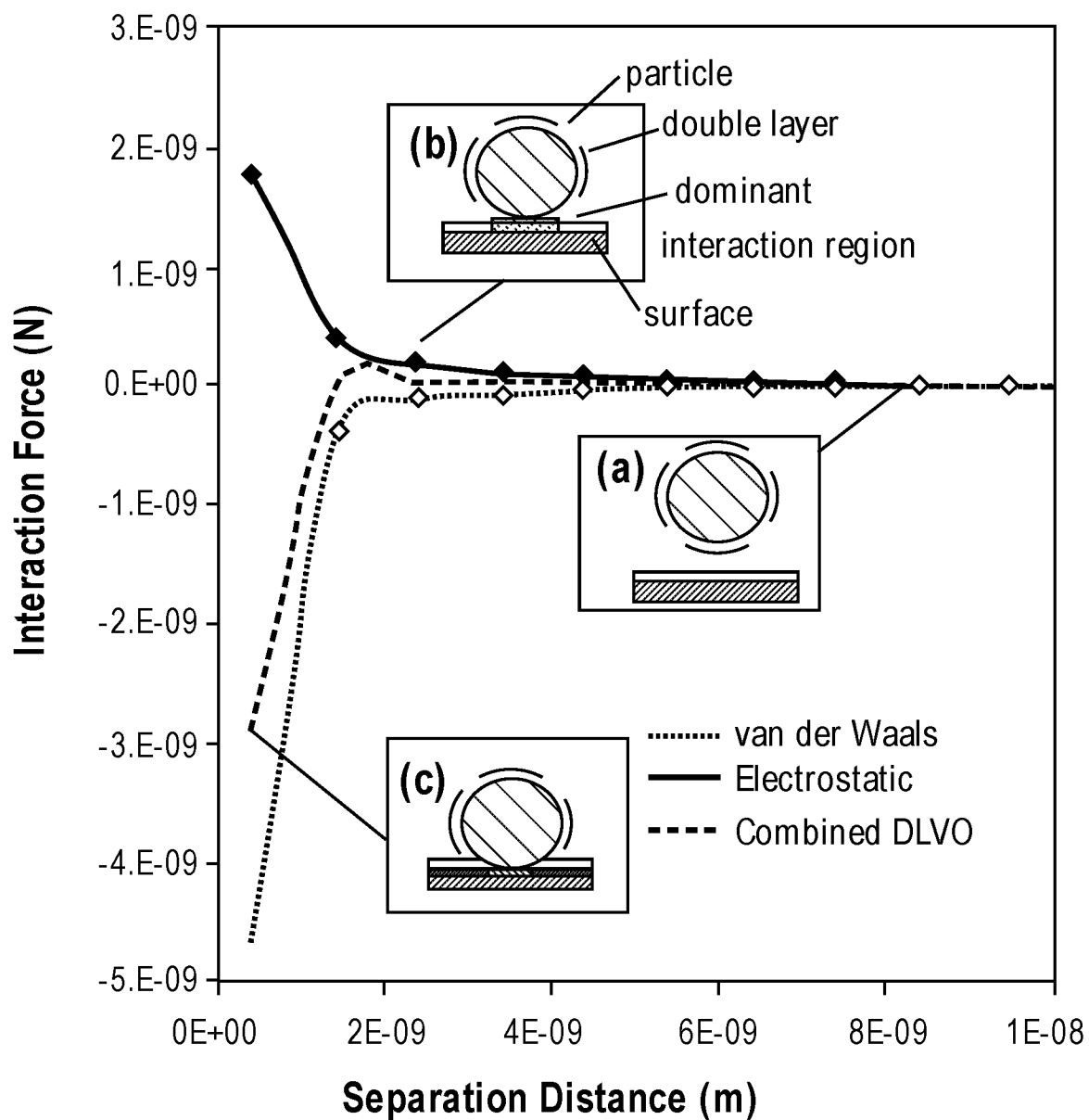
25. The method of claim 24, wherein reducing the number of particles attached to the surface of
the wafer or substrate through charge modulation at the surface of the wafer or substrate
15 comprises using a charge modulation technique selected from the group consisting of ionization
through corona discharge, providing ultra-violet (UV) or soft X-ray radiation, static charge
modulation, and magnetic field modulation.



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300

Interaction Forces: Ideal Surfaces

**FIG. 3**

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400

Interaction Forces: Irregular Particles

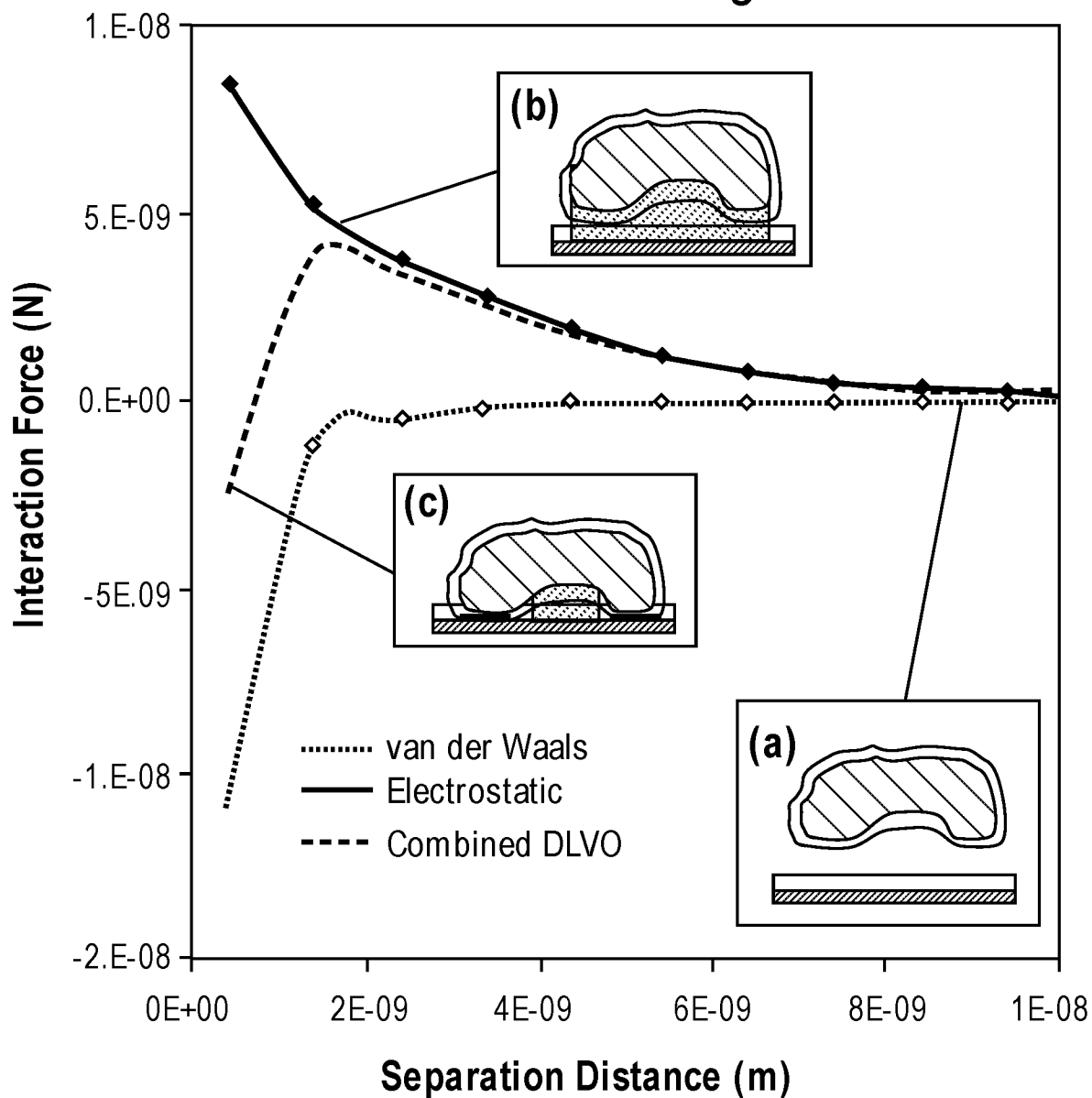
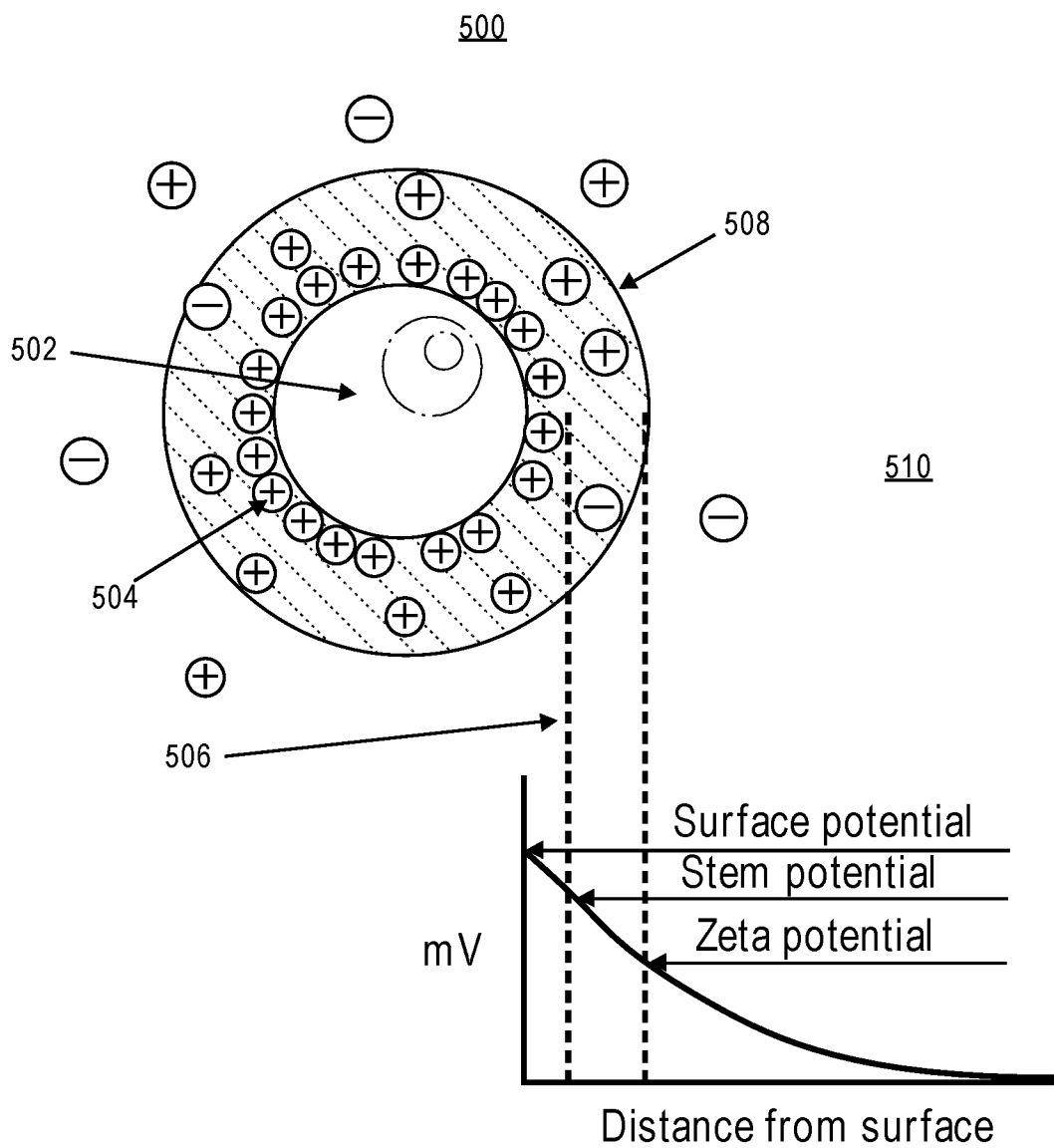


FIG. 4

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**FIG. 5**

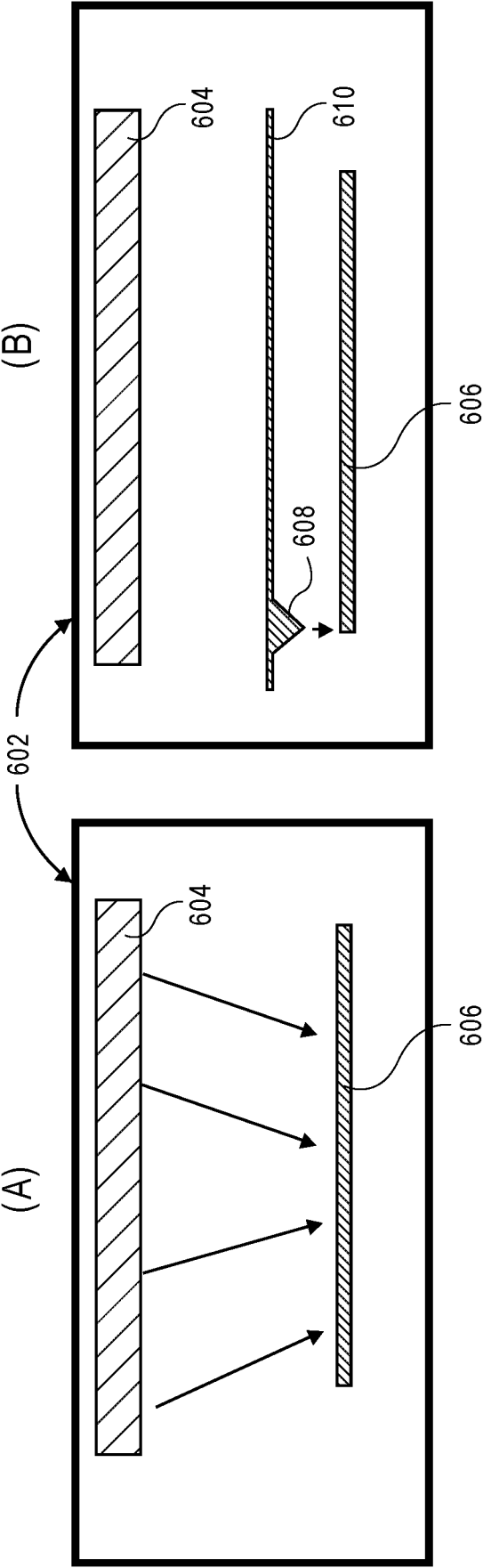


FIG. 6

700

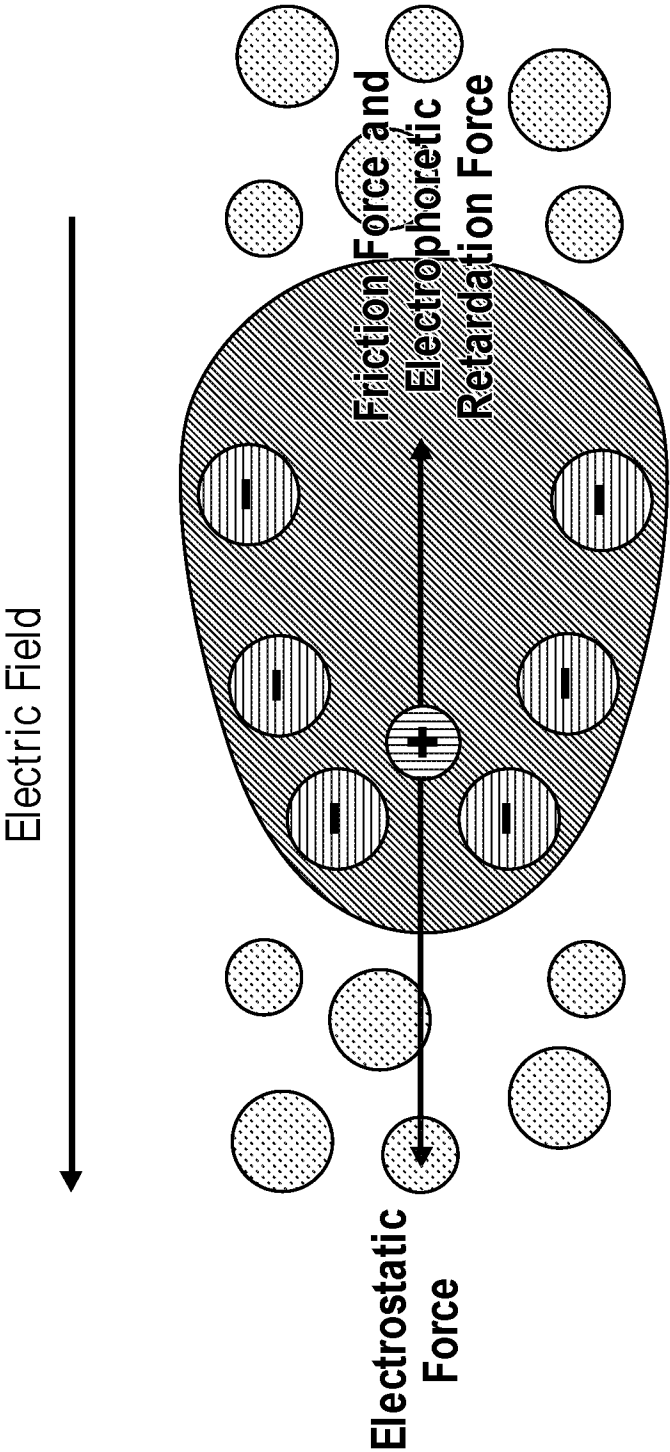


FIG. 7

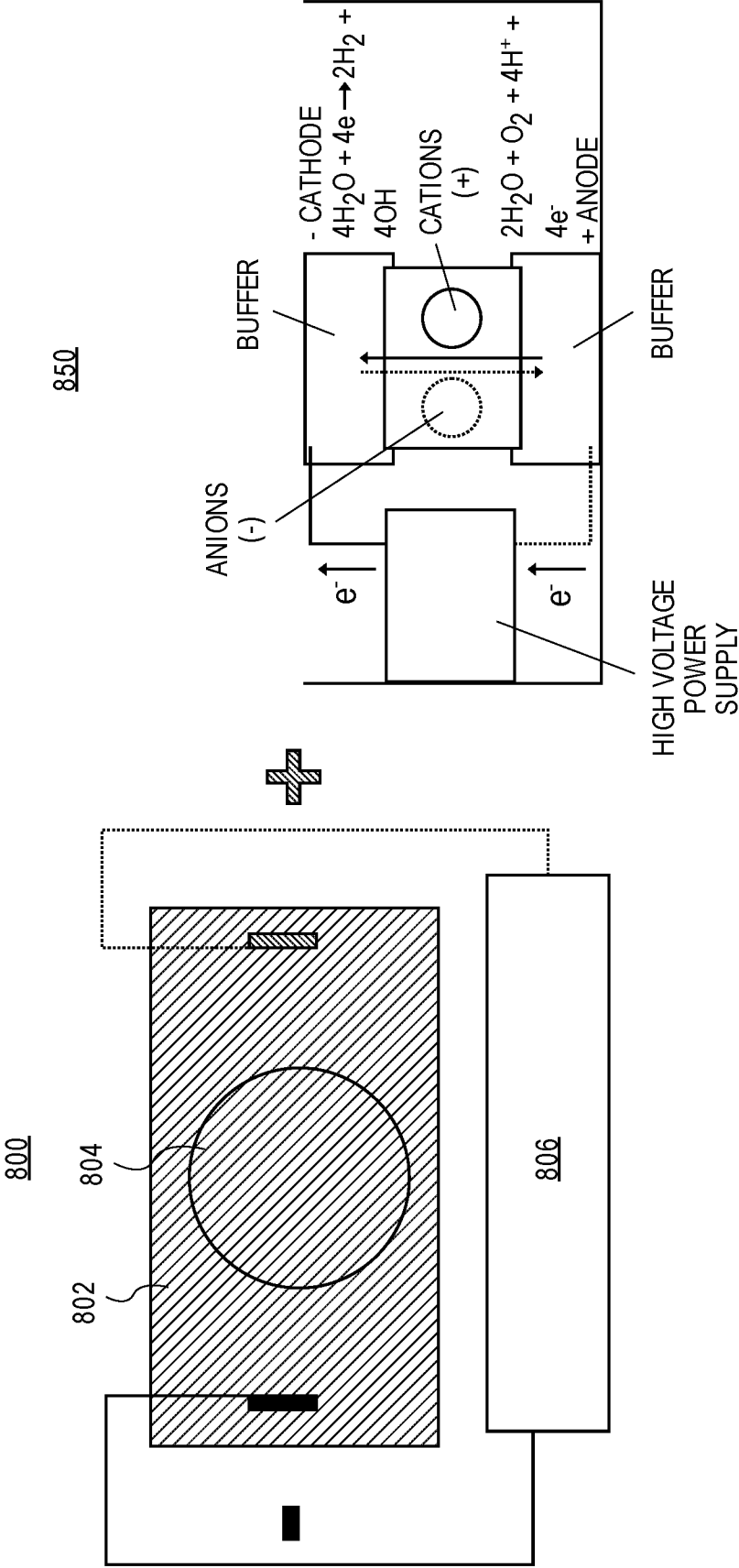


FIG. 8

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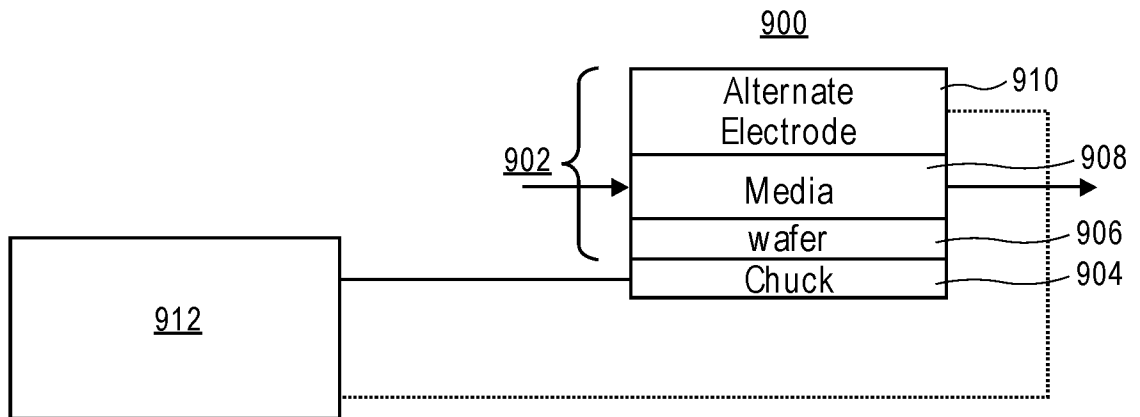


FIG. 9

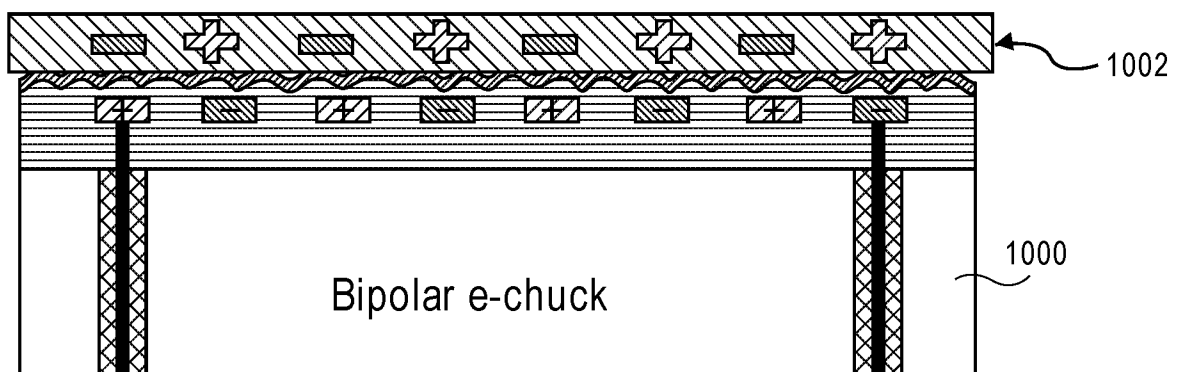


FIG. 10

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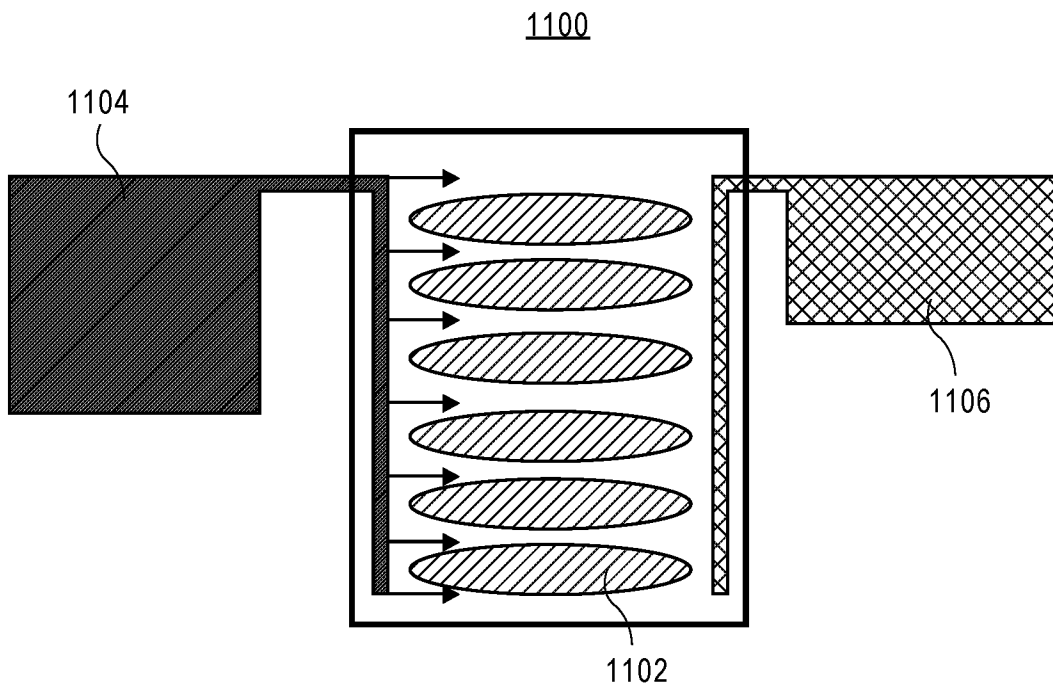


FIG. 11

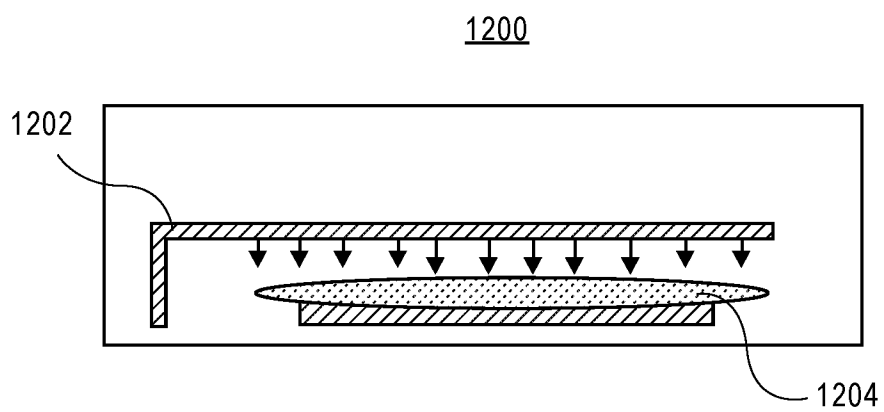


FIG. 12

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1300

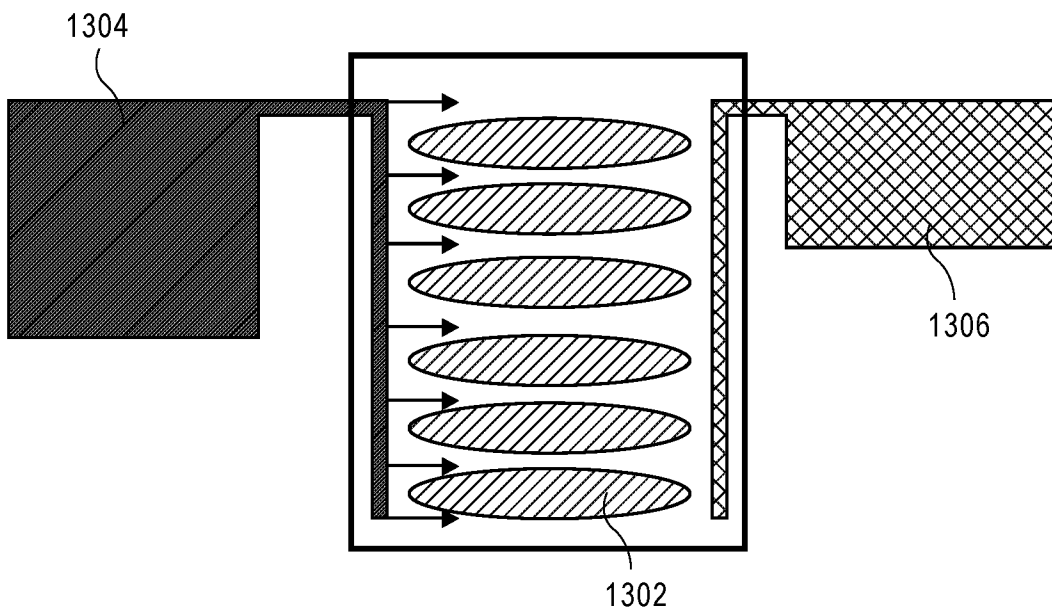


FIG. 13

1400

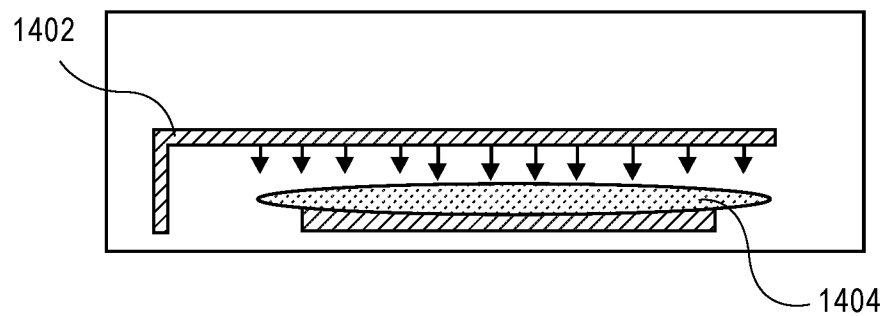


FIG. 14

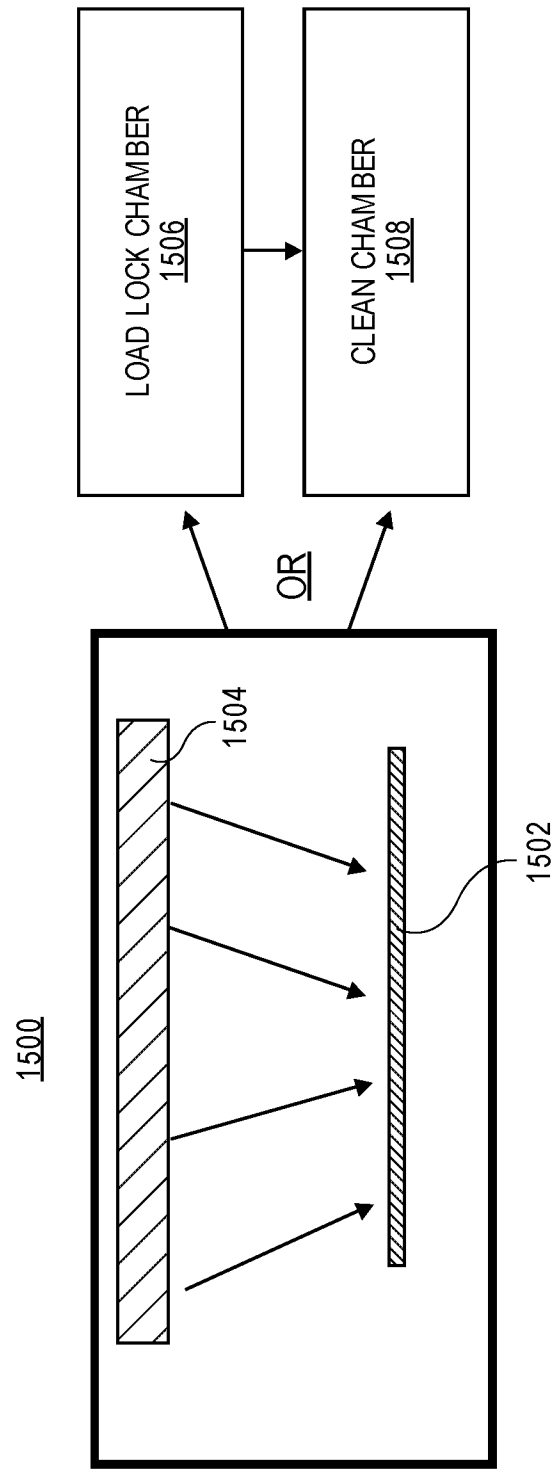


FIG. 15

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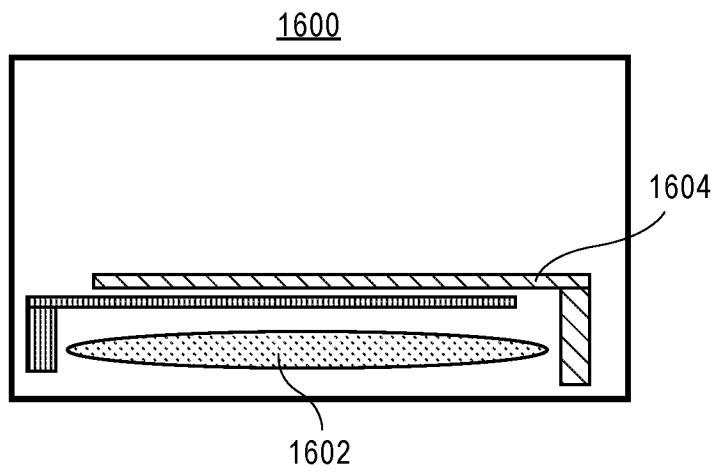


FIG. 16

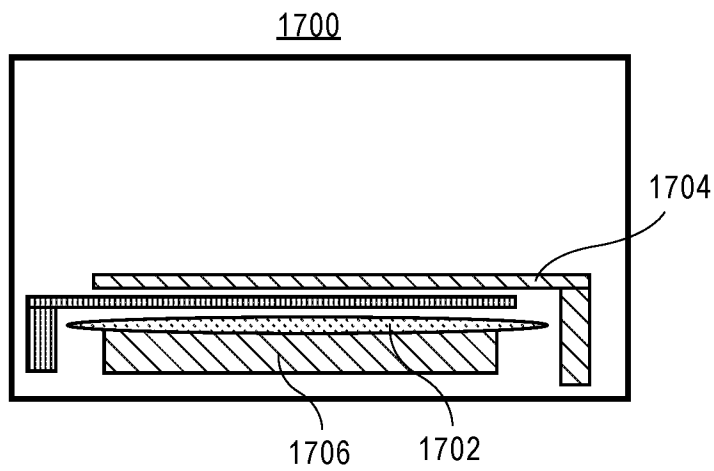


FIG. 17

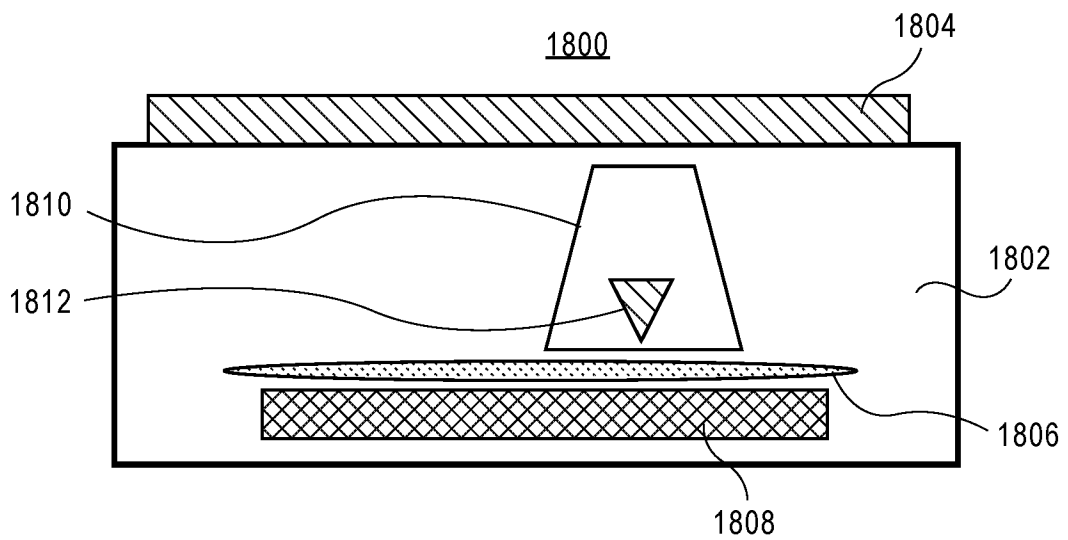


FIG. 18

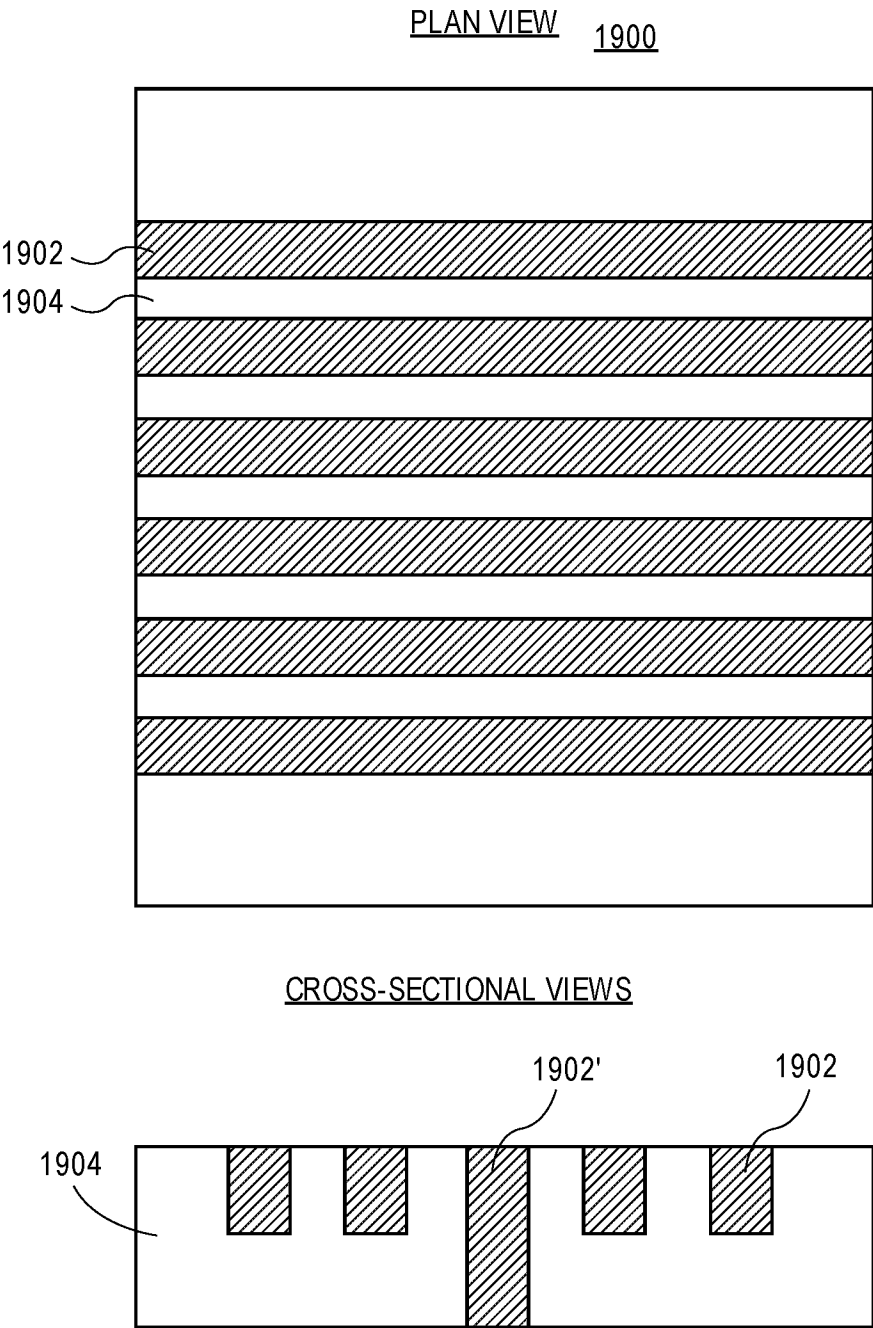


FIG. 19

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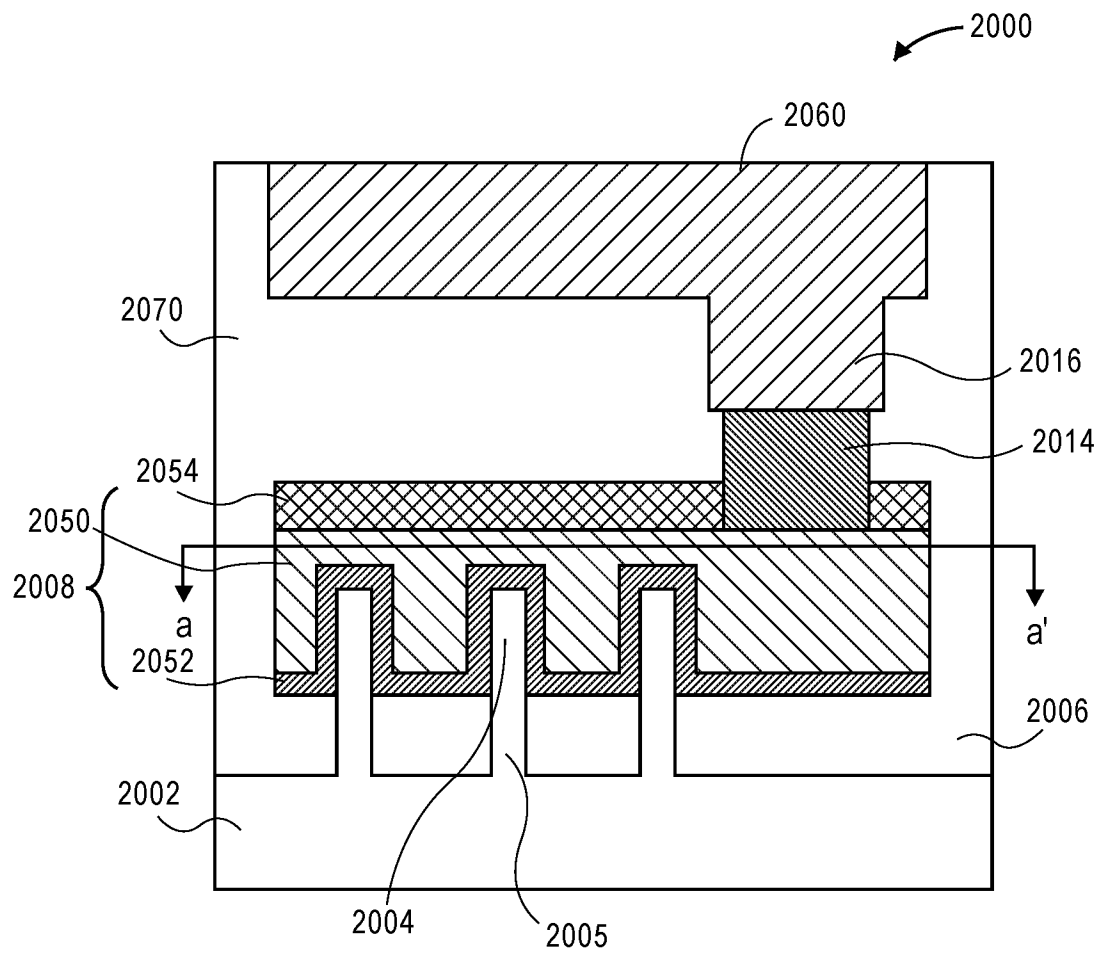


FIG. 20A

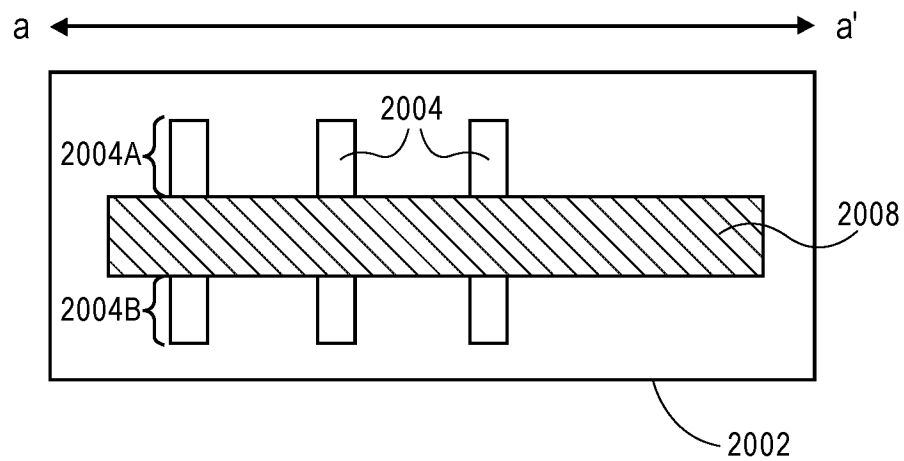


FIG. 20B

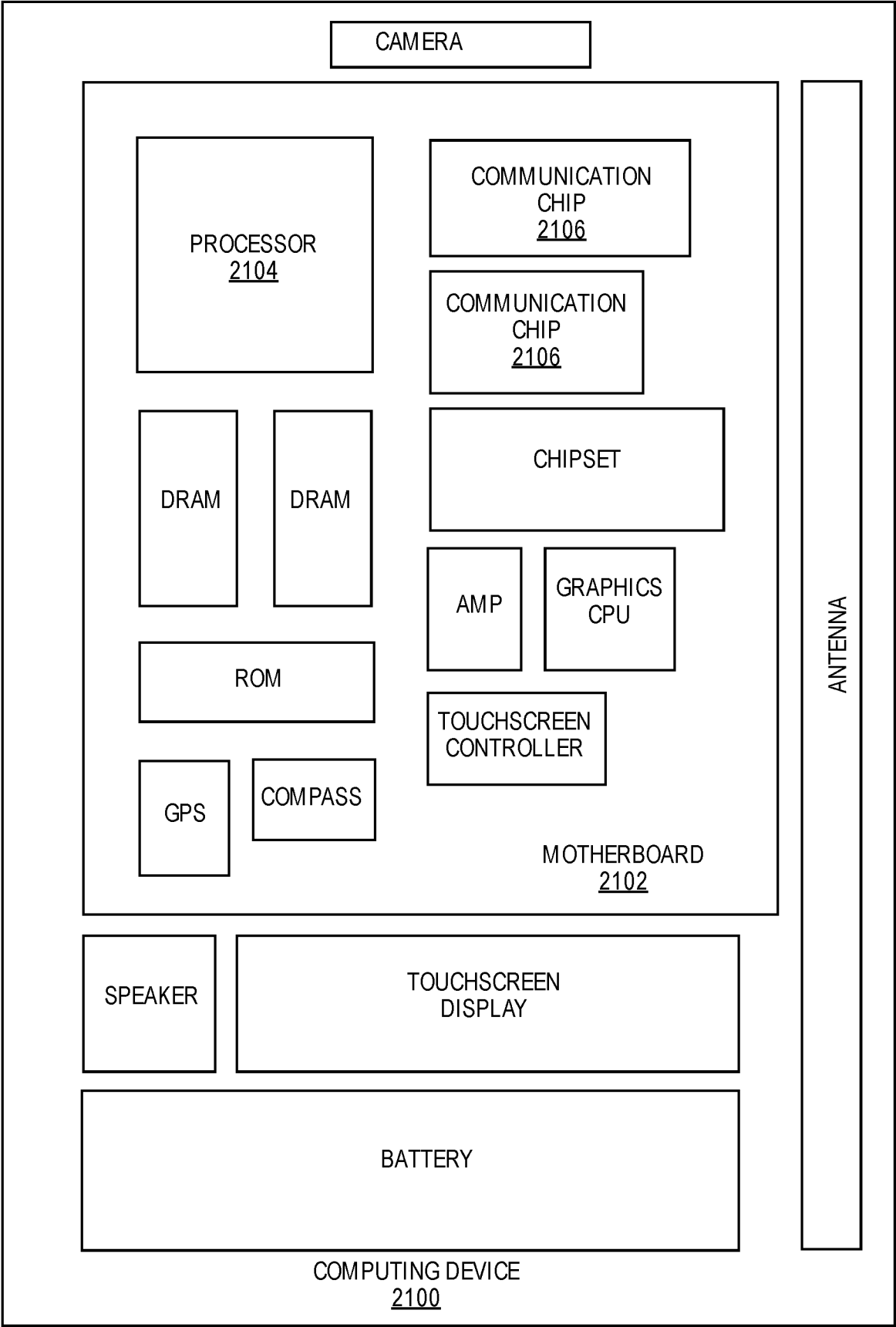
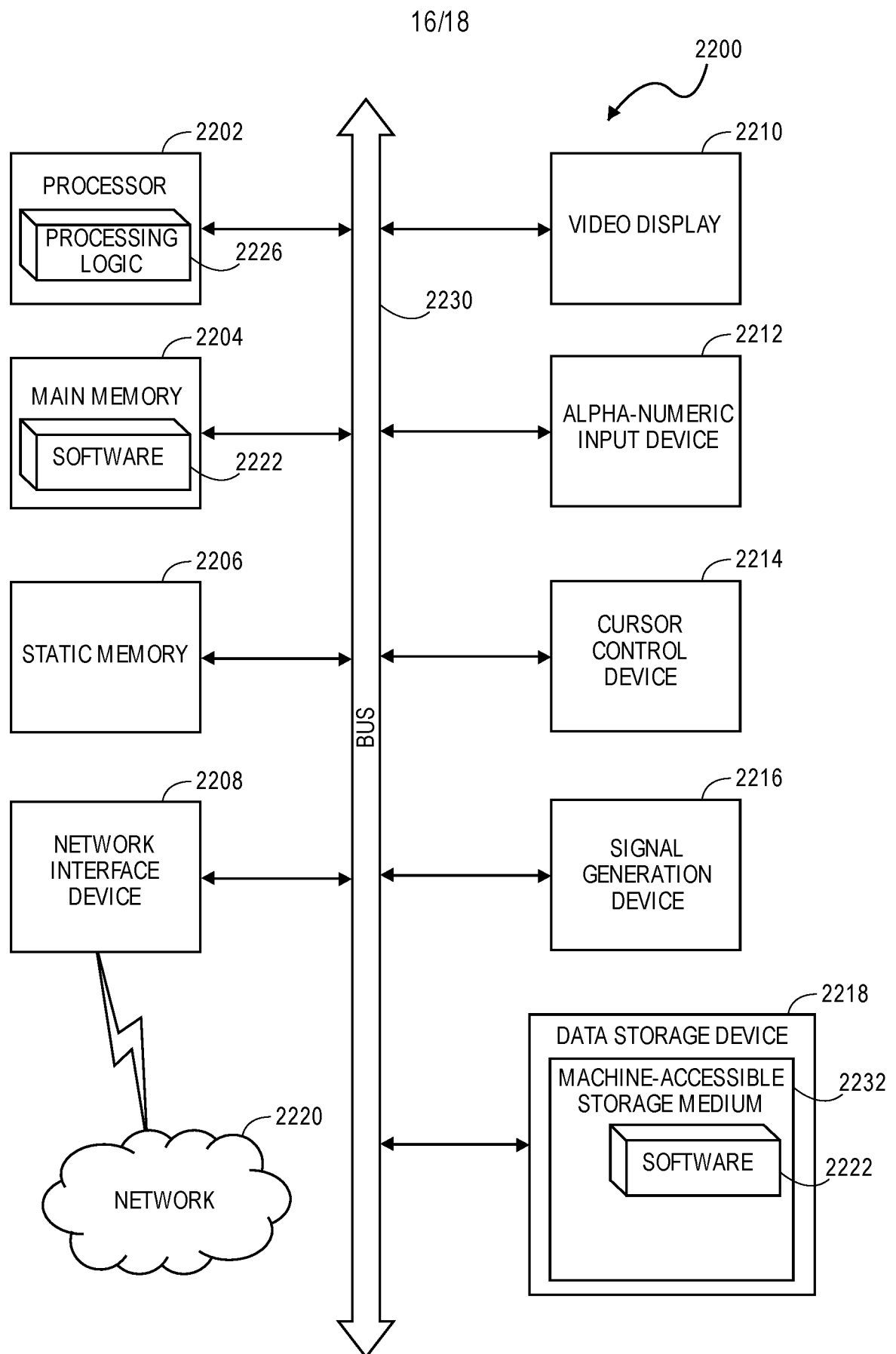


FIG. 21

**FIG. 22**

