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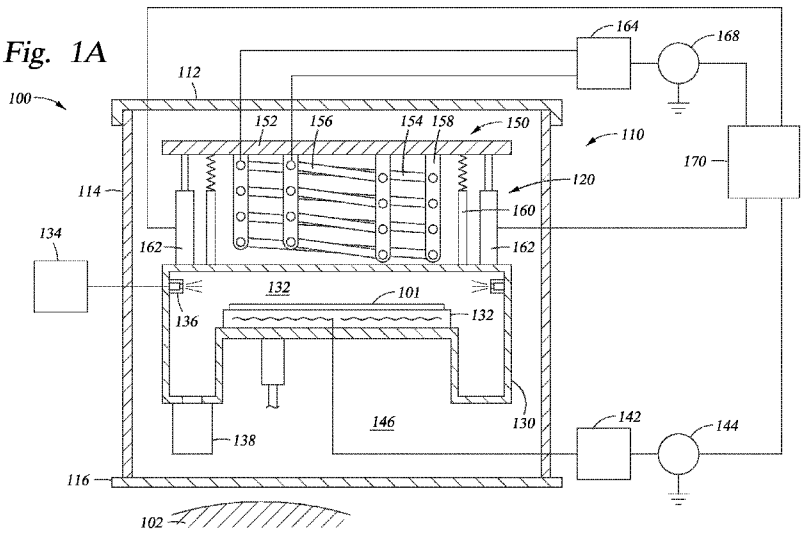
(54) Title: SELF ALIGNED DUAL PATTERNING TECHNIQUE ENHANCEMENT WITH MAGNETIC SHIELDING

Fig. 1A



(57) Abstract: Embodiments of the present disclosure generally provide apparatus and method for improving processing uniformity by reducing external magnetic noises. One embodiment of the present disclosure provides an apparatus for processing semiconductor substrates. The apparatus includes a chamber body defining a vacuum volume for processing one or more substrate therein, and a shield assembly for shielding magnetic flux from the chamber body disposed outside the chamber body, wherein the shield assembly comprises a bottom plate disposed between the chamber body and the ground to shield magnetic flux from the earth.

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SELF ALIGNED DUAL PATTERNING TECHNIQUE ENHANCEMENT WITH MAGNETIC SHIELDING

BACKGROUND

Field

[0001] Embodiments of the present disclosure generally relate to apparatus and methods for processing semiconductor substrates. More particularly, embodiments of the present disclosure relate to apparatus and method for shielding magnetic noises from plasma generated in a semiconductor substrate processing chamber.

Description of the Related Art

[0002] Processing chambers used in semiconductor processing generally have inherent non-uniformities of varying degrees depending on chamber structure and processing conditions. The inherent non-uniformities generally cause skews, which can be compensated by hardware or software adjustment. However, the skew caused by inherent non-uniformity of hardware sometimes overlays with non-uniformity cause by external factors, such as magnetic field of the earth, thermal and or magnetic field of surrounding processing chambers. The overlaid non-uniformities are difficult to compensate or adjust because the external factors may be random and difficult to predict.

[0003] Therefore, there is a need for apparatus and methods for reducing and compensating skews caused by both inherent non-uniformities and external factors.

SUMMARY

[0004] Embodiments of the present disclosure generally provide apparatus and method for improving processing uniformity by reducing external magnetic noises.

[0005] One embodiment of the present disclosure provides an apparatus for processing semiconductor substrates. The apparatus includes a chamber body defining a vacuum volume for processing one or more substrate therein, and a shield assembly for shielding magnetic flux from the chamber body disposed outside the chamber body, wherein the shield assembly comprises a bottom plate disposed between the chamber body and the ground to shield magnetic flux from the earth.

[0006] Another embodiment of the present disclosure provides a method for processing a substrate. The method includes applying a shield between a processing chamber and the ground to shield the processing chamber from magnetic flux generated by the earth, measuring a process rate of a process recipe performed by the processing chamber, and determining a skew in the measured process rate. The method further includes adjusting one or more components of the processing chamber or one or more processing parameters according to the determined skew, and processing one or more substrates in the processing chamber.

[0007] Yet another embodiment of the present disclosure provides a method for processing a substrate. The method includes applying a shield around a processing chamber to shield the processing chamber from magnetic flux and measuring a processing rate of the processing chamber to obtain a skew, and adjusting one or more components of the processing chamber or one or more processing parameters to correct the skew. The method further includes etching a template mask disposed below a patterned mask to form both a narrow feature and a wide feature in the template mask, removing the patterned mask from the narrow feature while substantially retaining the patterned mask on the wide feature, and etching the template mask to thin the exposed narrow feature relative to the wide feature formed in the template mask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0009] Figure 1A is a schematic sectional view of a processing chamber according to one embodiment of the present disclosure.

[0010] Figure 1B is a flow chart of a method according to one embodiment of the present disclosure.

[0011] Figures 2A-2F are schematic sectional view of a substrate being processed according to one embodiment of the present disclosure.

[0012] Figure 3 is a flow chart of a method according to one embodiment of the present disclosure.

[0013] Figure 4 includes schematic plots showing processing results according to embodiments of the present disclosure.

[0014] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures. It is contemplated that elements disclosed in one embodiment may be beneficially utilized on other embodiments without specific recitation.

DETAILED DESCRIPTION

[0015] Embodiments of the present disclosure provide apparatus and methods for improving processing uniformity in a semiconductor processing chamber, such as a plasma processing chamber. According to embodiments of the present disclosure, a shield assembly including a bottom plate positioned between a processing chamber and the ground may be applied to the processing chamber. The bottom plate attenuates or even eliminates magnetic flux from the earth. The shield assembly may also include a top plate and sidewalls. The top plate, sidewalls and bottom plate form an enclosure where the processing chamber is positioned. By enclosing the processing chamber, the shield assembly effectively preventing environment magnetic flux from entering the processing volume of the processing chamber.

[0016] According to one embodiment of the present disclosure, processing rate may be measured and a skew determined while the shield assembly is applied around the processing chamber. With the environment magnetic flux substantially shielded by the shield assembly, the measured skew substantially represents non-uniformities that are inherent to the processing chamber, thus, can be compensated by adjusting one or more components of the processing chamber or adjusting one or

more processing parameters. In one embodiment, one or more coils of an antenna assembly for generating a plasma inside the processing chamber may be adjusted to adjust plasma distribution, thus, compensate the skew. In another embodiment, upon compensation of the skew inherent to the processing chamber, processing uniformity may be improved. The improved uniformity may also enable adjustment of processing parameters, such as plasma bias voltage, to achieve processing effects that cannot be otherwise achieved.

[0017] Figure 1A is a schematic sectional view of a processing chamber 100 according to one embodiment of the present disclosure. The processing chamber 100 includes a chamber body 130, a plasma generator 120, and a shield assembly 110 disposed around the chamber body 130 and the plasma generator 120. The shield assembly 110 surrounds the chamber body 130 and the plasma generator 120 to prevent environmental magnetic flux from affecting processes

[0018] The chamber body 130 defines a processing volume 132. A substrate support 132 is disposed in the processing volume 132 for supporting a substrate 101 to be processed in the processing volume 132. A vacuum pump 138 may be coupled to the chamber body 130 to maintain a vacuum environment in the processing volume 132. A gas source 134 may be coupled to a gas distribution assembly 136. The gas distribution assembly 136 delivers one or more processing gas from the gas source 134 to the processing volume 132.

[0019] The plasma generator 120 generates plasma in the processing volume 132 for processing the substrate 101. In one embodiment, the plasma generator 120 may include an antenna assembly 150 for generating inductively coupled plasma in the processing volume 132. The antenna assembly 150 may include two antennas 154, 156 positioned above the chamber body 130. The antennas 154, 156 may be attached to a frame 152 by brackets 158. The antennas 154, 156 may be connected to a radio frequency (RF) power source 168 via a matching network 164 for plasma generation. In one embodiment, an electrode The antenna assembly 150 may include one or more motors 162 for adjusting the coils 154, 156 relative to the processing volume 132. The one or more motors 162 may also be used to adjust relative position of the coils 154, 156. In one embodiment, the motors

162 may be attached to the frame 152. Optionally, a shield 160 may be positioned around the antennas 154, 156.

[0020] The shield assembly 110 shields the processing volume 132 from external magnetic flux. Particularly, the shield assembly 110 includes one or more components positioned between the chamber body 130 and the ground 102 to shield any magnetic flux from the earth. In one embodiment, the shield assembly 110 may include a top plate 112, sidewalls 114 and a bottom plate 116. The top plate 112, sidewalls 114 and bottom plate 116 define an enclosure 146 to enclose the chamber body 130 therein. In one embodiment, the plasma generator 120 is also enclosed in the shield assembly 110. The bottom plate 114 positioned between the chamber body 130 and the ground 102 effectively attenuates magnetic flux from the earth, which may affect plasma distribution within the processing volume 132. Beside the magnetic flux from the earth, the shield assembly 110 also attenuates other environmental magnetic noises, such as noises from adjacent processing chambers, from entering the processing volume 132.

[0021] The shield assembly 110 may be formed from any material that is capable of attenuate magnetic flux from the environment. In one embodiment, the shield assembly 110 may be formed from a metal having high magnetic permeability and capable of shielding against static or low frequency magnetic fields. For example, the shield assembly 110 may be formed from stainless steel, such as 410 stainless steel, mu-metal, or soft-iron.

[0022] The shield assembly 110 may be formed in any suitable shape to enclose the chamber body 130 and the plasma generator 120 therein and to accommodate surroundings of the processing chamber 100. Sectional view of the sidewalls 114 may be circular or polygonal, such as rectangular or hexagonal.

[0023] The processing chamber further includes a controller 170 for monitoring and controlling the process performed therein. The shield assembly 110 allows the processing chamber 100 to process substrates with minimal affect from the environment. The controller 170 may connect and control the RF power source 168, a bias power source 144 via a matching network, or the motor 162. In one embodiment, the controller 170 may be used to monitor the processing rate across

the substrate with the shield assembly 110 applied around the chamber body 130 and the plasma generation. The controller 170 may include a control program that determines a skew from the monitored process rate, and generates control signals to components of the processing chamber 100 to adjust the process rate and improve uniformity across the substrate.

[0024] Figure 1B is a flow chart of a method 180 according to one embodiment of the present disclosure. The method 180 may be used to compensate a skew inherent to a processing chamber to achieve desired the processing effect, such as improving process uniformity.

[0025] Box 182 of the method 180 includes applying a shield around a processing chamber to shield the processing chamber from external magnetic flux. In one embodiment, the shield includes a plate disposed between the processing chamber and the ground to block any magnetic flux from the earth. The shield may be similar to the shield assembly 110 of the processing chamber 100.

[0026] Box 184 of the method 180 includes measuring a process rate across a substrate while running a process in the processing chamber having the shield applied. Since the shield effectively substantially prevents environmental magnetic noises from entering the processing chamber, non-uniformities in the measured process rate can be contributed substantially to causes inherent to the processing chamber itself, thus, may be addressed by adjusting the processing chamber alone. The measurement of box 184 may be performed in-situ using sensors in the processing chamber, such as the processing chamber 100. Alternatively, the measurement of box 184 may be performed in a metrology station independent from the processing chamber.

[0027] Box 186 of the method 180 includes characterizing the measured process rate. Characterizing the measured process rate may include a calculation to determine one or more characters of the measured process rate so that adjustment can be made to obtain desired process rate based on the one or more characters. In one embodiment, charactering the measured process may be determining a skew that reflects gradients of the non-uniformities in the measured process rate. In one embodiment, the skew may be used to generate signals for adjusting a plasma

generator. Other characters of the measured process rate may be used according to process requirement.

[0028] Box 188 of the method 180 includes adjusting one or more components of the processing chamber or one or more processing parameters according to the one or more characters determined in box 186. The adjustment of box 188 may be used to improve processing results, such as improving uniformity across the substrate being processed, or achieving certain process results, such as edge thin or edge thick. In one embodiment, a plasma generator of the processing chamber may be adjusted according to the direction of the skew in the measured process rate to improve uniformity. For example, the plasma generator 120 in the processing chamber 100 may be adjusted by the controller 170. The plasma generator 120 may be adjusted by various approaches, such as adjusting positions of the antennas 154, 156 relative to the processing volume 132, adjusting relative positions between the antennas 154, 156, adjusting frequency, phase, or amplitude of the RF power source 168, or combinations thereof. In one embodiment, the positions of the antennas 154, 156 may be adjusted by moving the motors 162. Alternatively, other chamber components or processing parameters may be adjusted. For example, a bias power applied to the plasma may be adjusted. In the processing chamber 100, bias voltage applied to the substrate 101 by the bias power source 144 may be adjusted to improve process uniformity. For example, the bias voltage may be increased to allow lower plasma density in the processing volume 132, thus, improving controllability of the process rate across the substrate.

[0029] Box 190 of the method 190 includes processing one or more substrates in the processing chamber after adjustment with improved results. Generally, the same process recipe as performed in box 184 may be run for plurality of substrates for production with improved results. The process recipe may be any suitable ones such as etching, deposition, or epitaxial growth.

[0030] Figures 2A-2F are schematic sectional view of a substrate being processed by a method according to one embodiment of the present disclosure. Particularly, Figures 2A-2F illustrates etching and deposition processes in a selective self-aligned double patterning (SADP). The selective SADP generally includes using a photoresist pattern mask narrow features and wide features and

formed in a single lithography operation to form a template mask by etching, then thinning the template mask by further etching, forming a spacer mask having half the pitch of the narrow feature in the template mask, and then forming features using the spacer mask. Usually, the narrow features are in a central cell region of a substrate, and the wide features are in a periphery edge of the substrate. The improved uniformity provided by apparatus and methods of the present disclosure enables the SADP process to be successful in even smaller critical dimensions. Particularly, embodiments of the present disclosure may be used to reduce pitting occurs in the narrow features formed by SADP process.

[0031] Figure 2A depicts an exemplary partial cross-sectional view of device stack on a substrate 200. The device stack may be an integrated memory circuit device. The substrate 200 includes both a cell region 201 having narrow features and a periphery region 205 having wide features formed by etching a photoresist (PR) mask 235. The substrate 200 includes a spacer layer 210 wherein half picture spacer structures are to be formed. The spacer layer 210 may be any thin film layer suitable for the SADP process. A multi-layer template mask is form over the spacer layer 210. In one embodiment, the template mask may include a carbon hard based mask (CHM) 215 formed on the spacer layer 210, a dielectric anti-reflective coating (DARC) 220 formed over the CHM 215 and a bottom anti-reflective coating (BARC) 225 formed over the DARC 220. The PR mask 235 is over the BARC 225 and patterned by a photo lithography process. The PR mask 235 has narrow features 240 in the cell region 201 and wide features 245 in the periphery region 205. In one embodiment, the critical dimension of the wide features 245 may be about 5 to 10 time greater than the critical dimension of the narrow features 240.

[0032] In Figure 2A, a first etch process has been performed to the substrate 200, and the pattern of the PR mask 235 is transferred to the BARC 225 and the DARC 220. The first etch process may be performed in a processing chamber according to embodiment of the present disclosure having a shield assembly applied and components or parameter adjusted after the shield assembly is applied to improve uniformity.

[0033] In Figure 2B, a second etch process is performed to thin the template mask in the cell region 201 after the PR mask 235 in the cell region 201 is removed

while the PR mask 235 in the periphery region 205 remains. As shown in the dashed lines, the BARC 225 and DARC 220 are removed during the second etch process while the BARC 225 and the DARC 220 in the periphery region 205 simply "thinned". The CHM 215 is etched at the same rate in both the cell region 201 and the periphery region 205. Like the first etch process, the second etch process may be performed in a processing chamber according to embodiment of the present disclosure having a shield assembly applied and components or parameter adjusted after the shield assembly is applied to improve uniformity. The first and second etch process may be performed in the same processing chamber or a different processing chamber.

[0034] In Figure 2C, the second etch process continues after the PR mask 235 in the periphery region 205 is removed and narrow and wide features formed in the CHM 215. The CHM 215 is exposed in the central cell region 201 and covered by the DARC 220 in the periphery region 205.

[0035] In Figure 2D, sidewall spacer mask 250 is formed around the narrow and wide features of the CHM 215. The sidewall spacer mask 250 may be formed by first conformally depositing a spacer mask layer over the CHM 215, then anisotropically etching the conformal spacer mask layer to form the sidewall spacer mask 250.

[0036] In Figure 2E, a third etching process is performed to remove the CHM 215 in the narrow features between the sidewall spacer mask 250. The pitch of the spacer sidewall mask 250 in the central cell region 201 is also most half of the pitch of the narrow features 240 in the PR mask 235, thus effectively doubling the structural density in the central cell region 201.

[0037] In Figure 2F, a fourth etching process is performed to form spacers in the spacer layer 210 using the sidewall spacer mask 250 formed in Figure 2E. The final result has narrow features in the central cell region 201 and wide features in the periphery region 205.

[0038] The etch processes described in Figures 2C-2F may also be performed in a processing chamber according to embodiment of the present disclosure having a shield assembly applied and components or parameter adjusted after the shield

assembly is applied to improve uniformity. The various etch processes may be performed in the same chamber, or combinations of different chambers depending on the tool arrangement and/or process recipe.

[0039] Figure 3 is a flow chart of a method 300 of a SADP method according to one embodiment of the present disclosure. The method 300 may be performed using one or more processing chambers similar to the processing chamber 100 of Figure 1A. The method 300 may be performed in a single processing chamber, or multiple processing chambers.

[0040] Box 310 of the method 300 includes applying a shield around a processing chamber and measuring a processing rate of the processing chamber to obtain a skew. The shield is similar to the shield assembly 110 of the processing chamber 100 that prevents environmental magnetic flux from entering the processing chamber. The shield may include a top plate, sidewalls and a bottom plate to enclose the processing chamber therein. In one embodiment, a processing rate may be measured and a skew determined to non-uniformity after excluding the external magnetic noises from the processing chamber.

[0041] Box 320 of the method 300 includes adjusting one or more components of the processing chamber or processing parameters to correct the skew. Similar to box 188 of the method 180, chamber components, such as antennas in a plasma generator, or processing parameters, such as bias voltage, may be adjusted to correct the skew and improve uniformity.

[0042] Depending on the number of processing chambers used, box 310 and box 320 may be performed for some or all the processing chambers used in the processes to follow.

[0043] Box 330 of the method 300 includes etching one or more layers in a template mask disposed below a patterned mask to form both a narrow feature and a wide feature in the template mask. The narrow feature may be arranged in a central cell region and the wide feature may be arranged a periphery region. Figure 2A schematically illustrates a substrate stack after the etch process described in box 330.

[0044] Box 340 of the method 300 includes removing the patterned mask from the narrow feature while substantially retaining the patterned mask on the wide feature.

[0045] Box 350 of the method 300 includes etching the template mask to thin the exposed narrow feature relative to the wide feature formed in the template mask. Figure 2B schematically illustrates a substrate stack after the etch processes described in box 340 and box 350.

[0046] Box 360 of the method 300 includes removing the patterned mask from the wide feature and etching through all layers of template mask to expose a spacer layers formed below, as shown in Figure 2C.

[0047] Box 370 of the method 300 includes forming sidewall spacers around narrow and wide features in the template mask as shown in Figure 2D.

[0048] Box 380 of the method 300 includes removing the template mask on the narrow feature to form a spacer mask from the sidewall spacers. The pitch of the spacer mask in the central region is almost half of the pitch of the narrow features in the photoresist pattern in box 330. Figure 2E schematically illustrates a substrate stack after the etch process described in box 380.

[0049] Box 390 of the method 300 includes etching the spacer layer disposed under the spacer mask to form spacers of a narrow pitch and a wide pitch as shown in Figure 2F.

[0050] Figure 4 includes schematic plots showing processing results according to embodiments of the present disclosure. Figure 4 includes four contour plots. Plots (a) and (b) are reference data. Plot (a) schematically illustrates a skew of etch rate across a substrate for a tungsten etch in a plasma chamber without a shield. Arrow 402 indicates a direction of the skew. Antennas in the plasma chamber are then adjusted to correct the skew shown in plot (a). The same tungsten process is performed in the plasma chamber again without a shield after the adjustment. Plot (b) schematically illustrates an etch rate across the substrate of the tungsten etch after adjustment.

[0051] Plot (c) schematically illustrates a skew of etch rate across a substrate for the same tungsten etch in the same plasma chamber as in plots (a) and (b) but with a shield. The shield is formed a mu-metal and structurally similar to the shield assembly as described in Figure 1A. Arrow 404 indicates a direction of the skew. The fact that the skews in plots (a) and (c) have different directions indicates the shield does remove some external noises from the plasma chamber. Antennas in the plasma chamber are then adjusted to correct the skew shown in plot (c). The same tungsten process is performed in the plasma chamber again with the shield after the adjustment. Plot (d) schematically illustrates an etch rate across the substrate of the tungsten etch after adjustment with the shield. In plot (d) the range of non-uniformity is 85.10 while in plot (b) the range of non-uniformity is 108.3. Therefore, the etch rate shown in plot (d) is more uniform that the etch rate shown in plot (b), indicating that apparatus and method according to the present disclosure improve uniformity.

[0052] Even though, embodiments of the present disclosure are described in association with inductive coupled plasma chamber used for etching, embodiments of the present disclosure may be used in combination with any processing chambers that use plasma to improve processing uniformities.

[0053] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims

1. An apparatus for processing semiconductor substrates, comprising:

a chamber body defining a vacuum volume for processing one or more substrate therein; and

a shield assembly for shielding magnetic flux from the chamber body disposed outside the chamber body, wherein the shield assembly comprises a bottom plate disposed between the chamber body and the ground to shield magnetic flux from the earth.

2. The apparatus of claim 1, wherein the shield assembly further comprising:

a top plate; and

sidewalls disposed between the top plate and the bottom plate, wherein the top plate, the sidewall and sidewalls form an enclosure, and the chamber body is disposed in the enclosure.

3. The apparatus of claim 2, wherein the shield assembly is formed from stainless steel, mu-metal, or soft iron.

4. The apparatus of claim 2, further comprising a plasma generator disposed inside the shield assembly for generating plasma within the vacuum volume.

5. The apparatus of claim 4, wherein the plasma generator is an antenna assembly disposed outside the chamber body for generating inductively coupled plasma within the vacuum volume.

6. The apparatus of claim 5, wherein the antenna assembly is disposed above the chamber body and below the top plate of the shield assembly.

7. The apparatus of claim 6, wherein the antenna assembly comprises an adjustment mechanism for moving an antenna relative to the chamber body to adjust plasma distribution within the vacuum volume.

8. The apparatus of claim 7, wherein the adjustment mechanism is a motor coupled to the antenna.

9. The apparatus of claim 8, further comprising a system controller coupled to the motor, wherein the system controller sends control signals to the motor to adjust the antenna according to a measurement of a plasma distribution in the vacuum volume.

10. A method for processing a substrate, comprising:

applying a shield between a processing chamber and the ground to shield the processing chamber from magnetic flux generated by the earth;

measuring a process rate of a process recipe performed by the processing chamber;

determining a skew in the measured process rate;

adjusting one or more components of the processing chamber or one or more processing parameters according to the determined skew; and

processing one or more substrates in the processing chamber.

11. The method of claim 10, wherein applying a shield comprises applying a shield assembly having a top plate, sidewalls and a bottom plate that form an enclosure, and the enclosure encloses the processing chamber therein.

12. The method of claim 11, wherein adjusting one or more components comprises adjusting a plasma generator of the processing chamber to adjust a plasma distribution within a vacuum volume of the processing chamber, and the plasma generator is positioned within the shield assembly.

13. The method of claim 12, wherein adjusting the plasma generator comprises adjusting an antenna assembly relative to the vacuum volume of the processing chamber.

14. A method for processing a substrate, comprising

applying a shield around a processing chamber to shield the processing chamber from magnetic flux and measuring a processing rate of the processing chamber to obtain a skew;

adjusting one or more components of the processing chamber or one or more processing parameters to correct the skew;

etching a template mask disposed below a patterned mask to form both a narrow feature and a wide feature in the template mask;

removing the patterned mask from the narrow feature while substantially retaining the patterned mask on the wide feature; and

etching the template mask to thin the exposed narrow feature relative to the wide feature formed in the template mask.

15. The method of claim 14, wherein adjusting one or more components comprises adjust a plasma distribution within a vacuum volume of the processing chamber, and the plasma generator is positioned within the shield and outside the processing chamber.

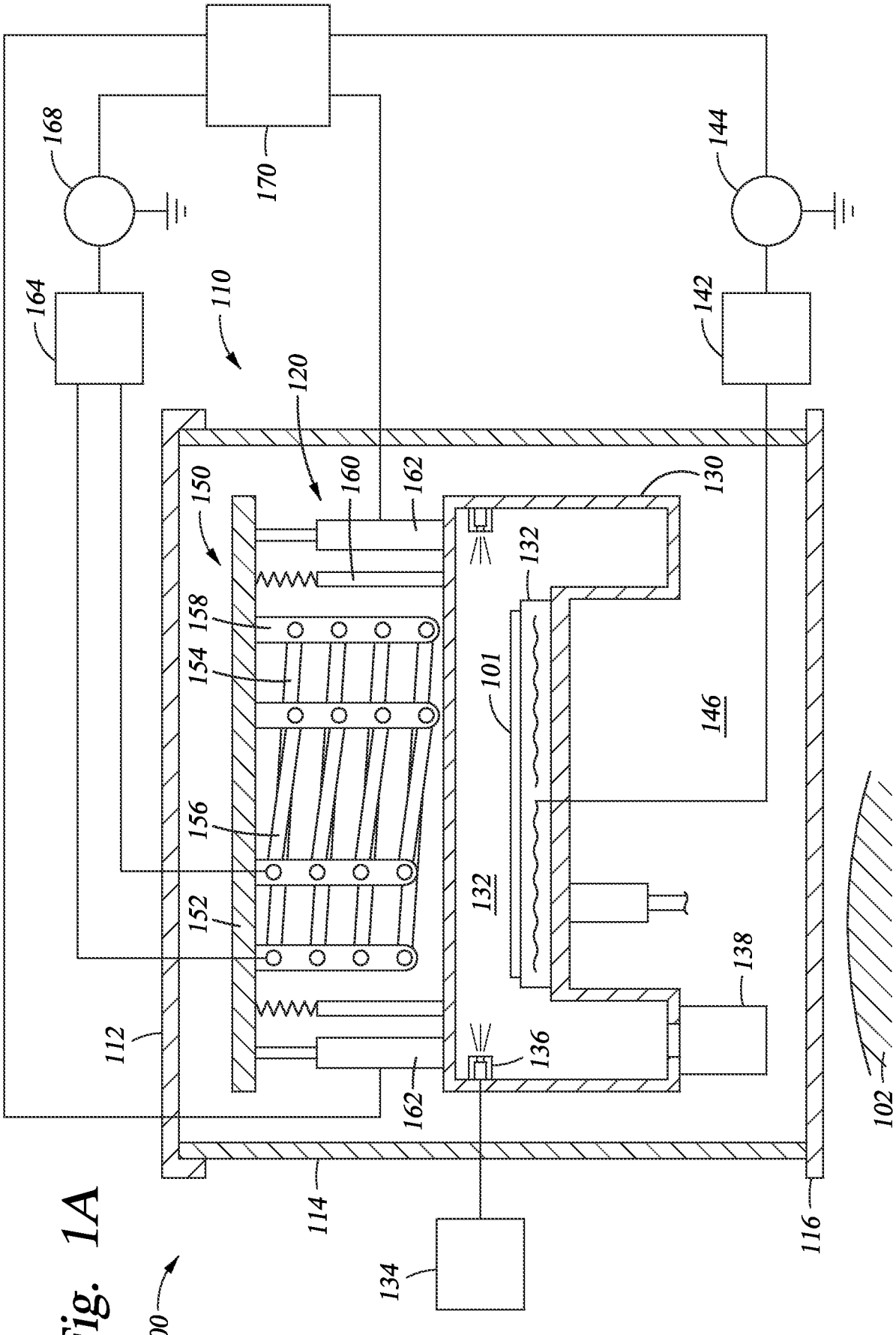
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Fig. 1A

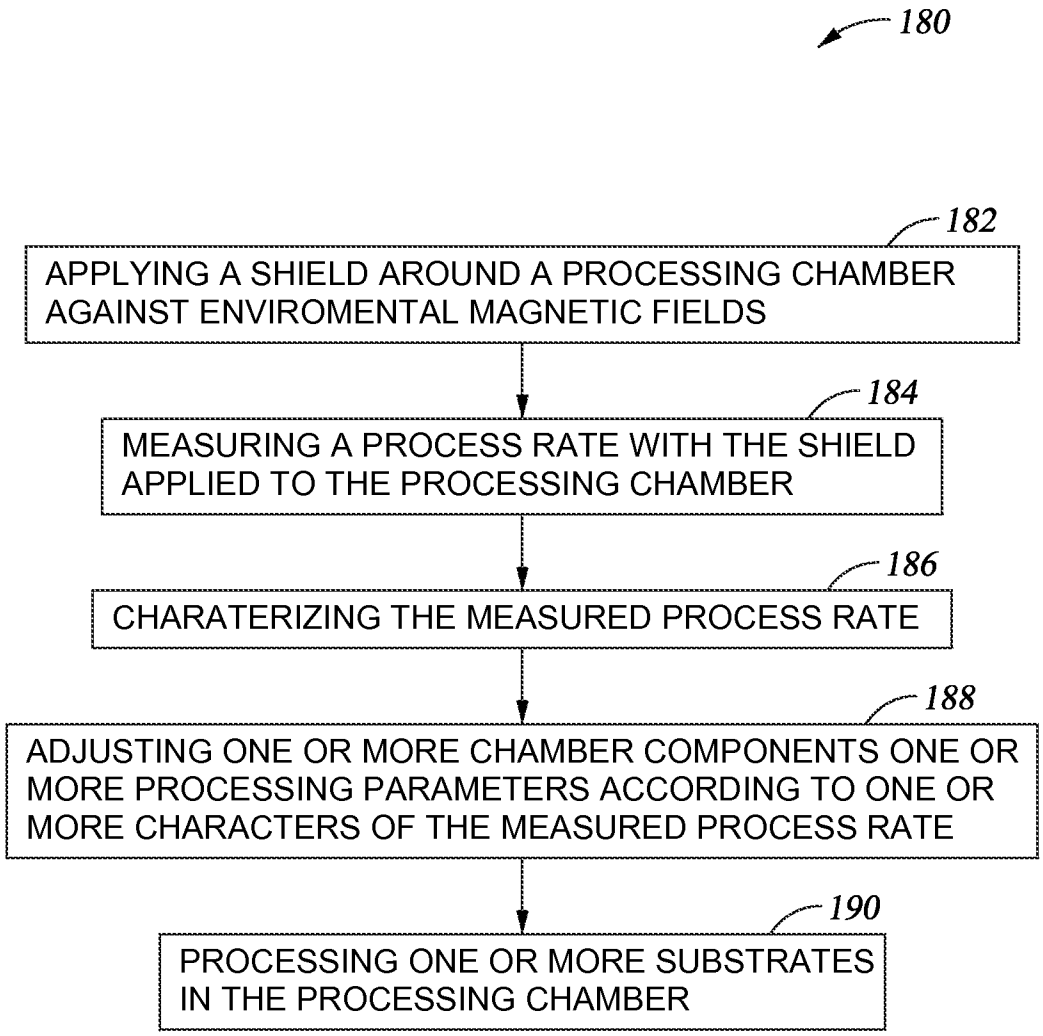
180
182
APPLYING A SHIELD AROUND A PROCESSING CHAMBER AGAINST ENVIROMENTAL MAGNETIC FIELDS
184
MEASURING A PROCESS RATE WITH THE SHIELD APPLIED TO THE PROCESSING CHAMBER
186
CHARATERIZING THE MEASURED PROCESS RATE
188
ADJUSTING ONE OR MORE CHAMBER COMPONENTS ONE OR MORE PROCESSING PARAMETERS ACCORDING TO ONE OR MORE CHARACTERS OF THE MEASURED PROCESS RATE
190
PROCESSING ONE OR MORE SUBSTRATES IN THE PROCESSING CHAMBER

Fig. 1B

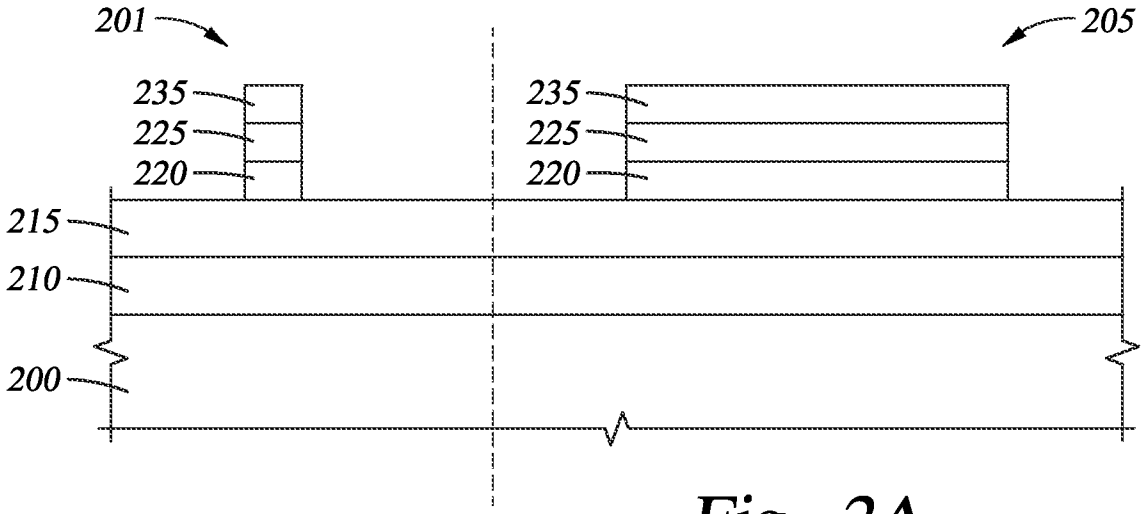

Fig. 2A

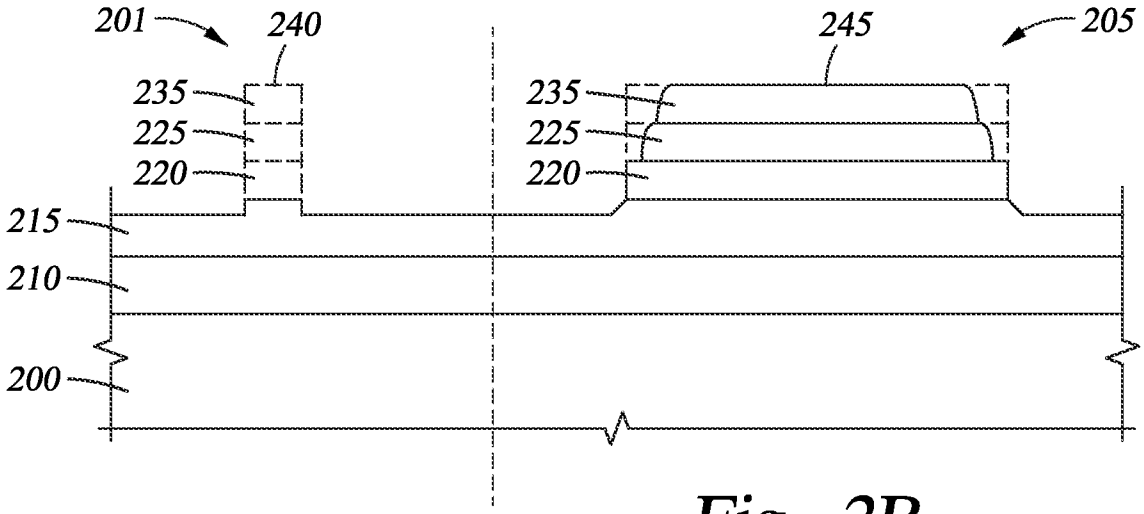

Fig. 2B

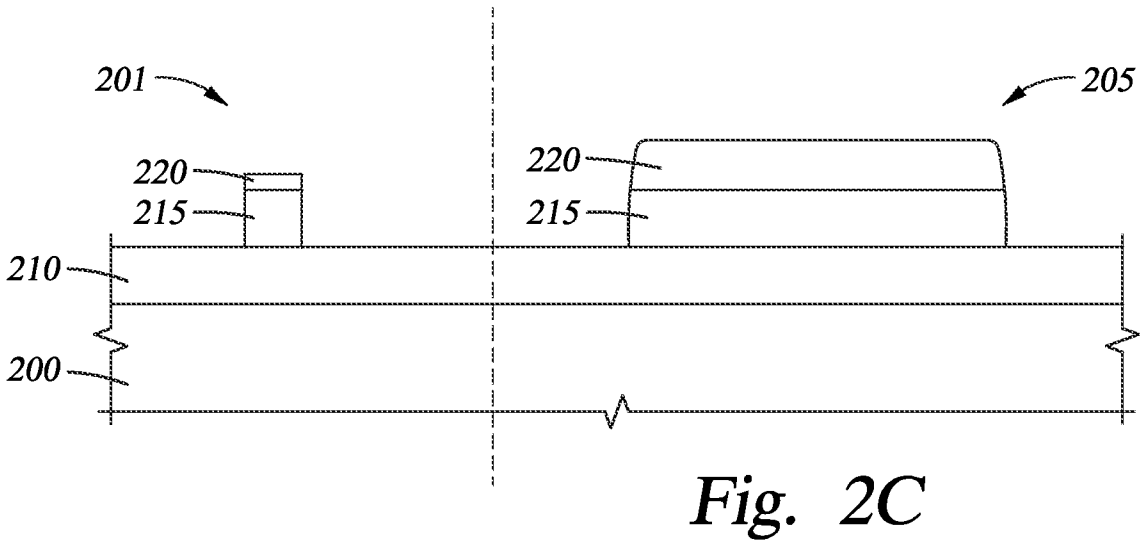

Fig. 2C

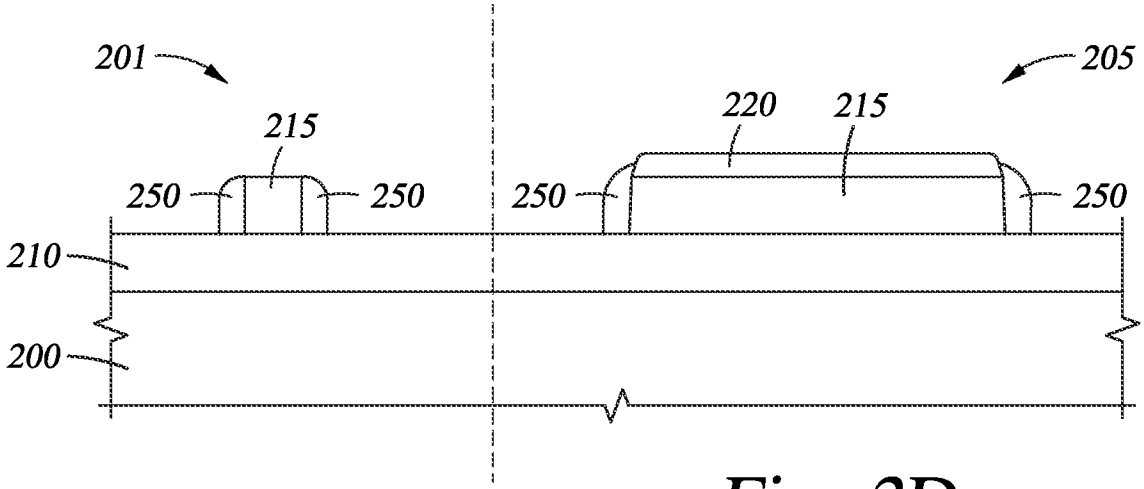

Fig. 2D

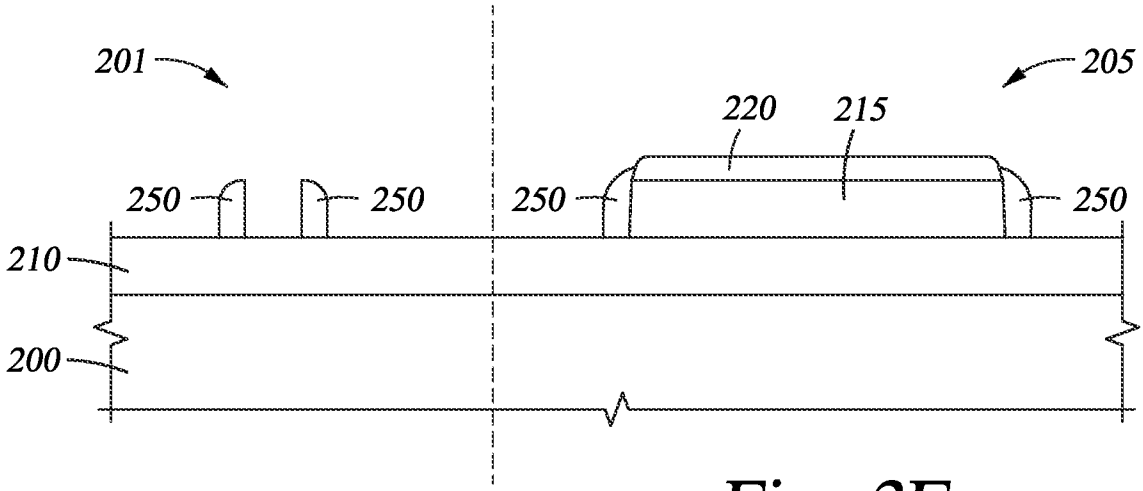

Fig. 2E

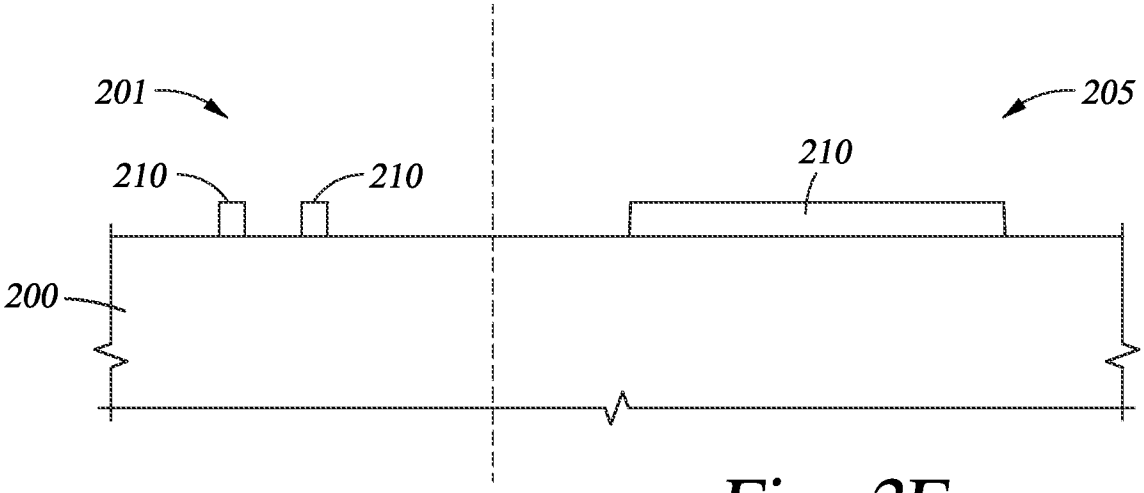

Fig. 2F

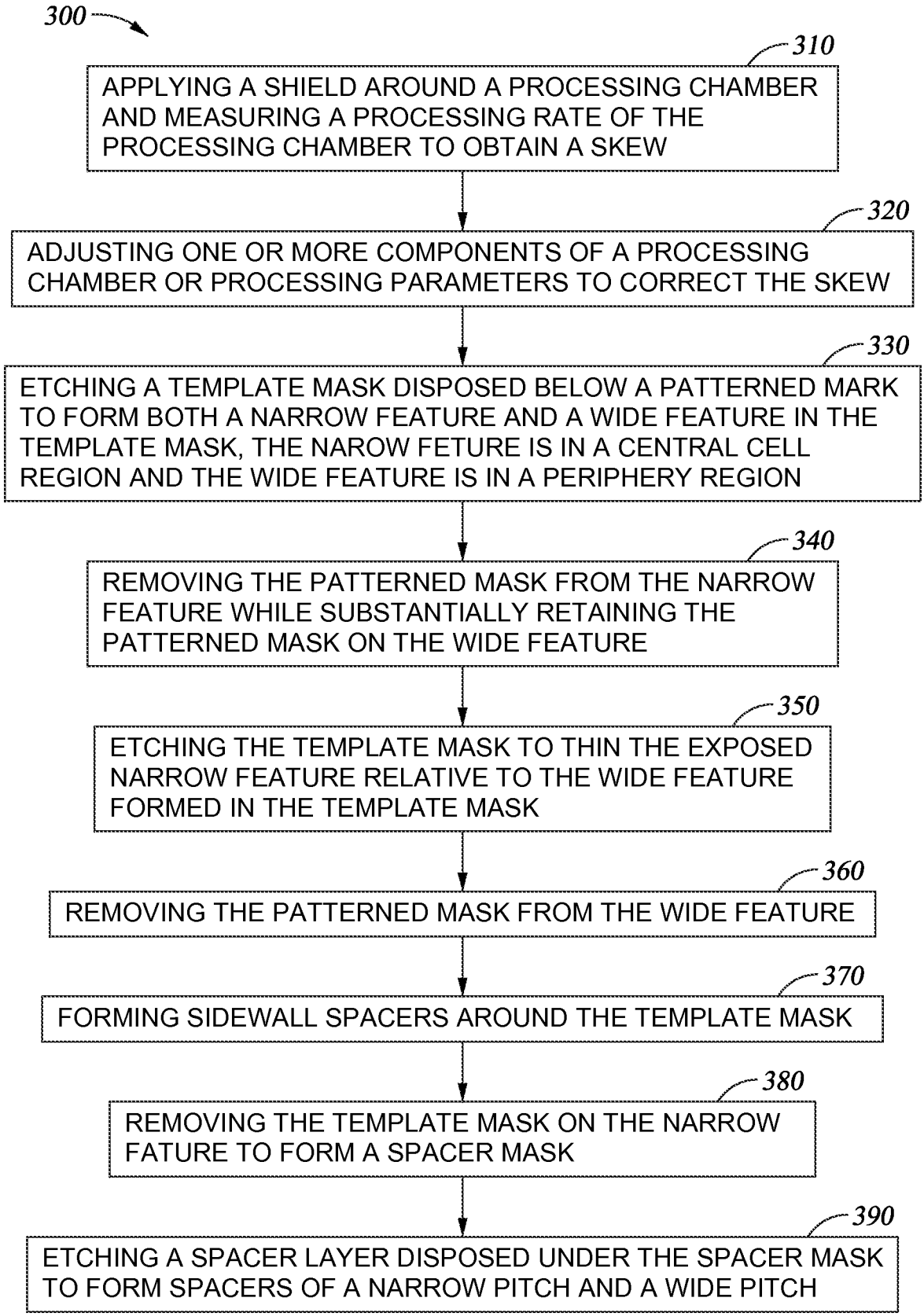
300
310
APPLYING A SHIELD AROUND A PROCESSING CHAMBER AND MEASURING A PROCESSING RATE OF THE PROCESSING CHAMBER TO OBTAIN A SKEW
320
ADJUSTING ONE OR MORE COMPONENTS OF A PROCESSING CHAMBER OR PROCESSING PARAMETERS TO CORRECT THE SKEW
330
ETCHING A TEMPLATE MASK DISPOSED BELOW A PATTERNED MARK TO FORM BOTH A NARROW FEATURE AND A WIDE FEATURE IN THE TEMPLATE MASK, THE NAROW FETURE IS IN A CENTRAL CELL REGION AND THE WIDE FEATURE IS IN A PERIPHERY REGION
340
REMOVING THE PATTERNED MASK FROM THE NARROW FEATURE WHILE SUBSTANTIALLY RETAINING THE PATTERNED MASK ON THE WIDE FEATURE
350
ETCHING THE TEMPLATE MASK TO THIN THE EXPOSED NARROW FEATURE RELATIVE TO THE WIDE FEATURE FORMED IN THE TEMPLATE MASK
360
REMOVING THE PATTERNED MASK FROM THE WIDE FEATURE
370
FORMING SIDEWALL SPACERS AROUND THE TEMPLATE MASK
380
REMOVING THE TEMPLATE MASK ON THE NARROW FATURE TO FORM A SPACER MASK
390
ETCHING A SPACER LAYER DISPOSED UNDER THE SPACER MASK TO FORM SPACERS OF A NARROW PITCH AND A WIDE PITCH

Fig. 3

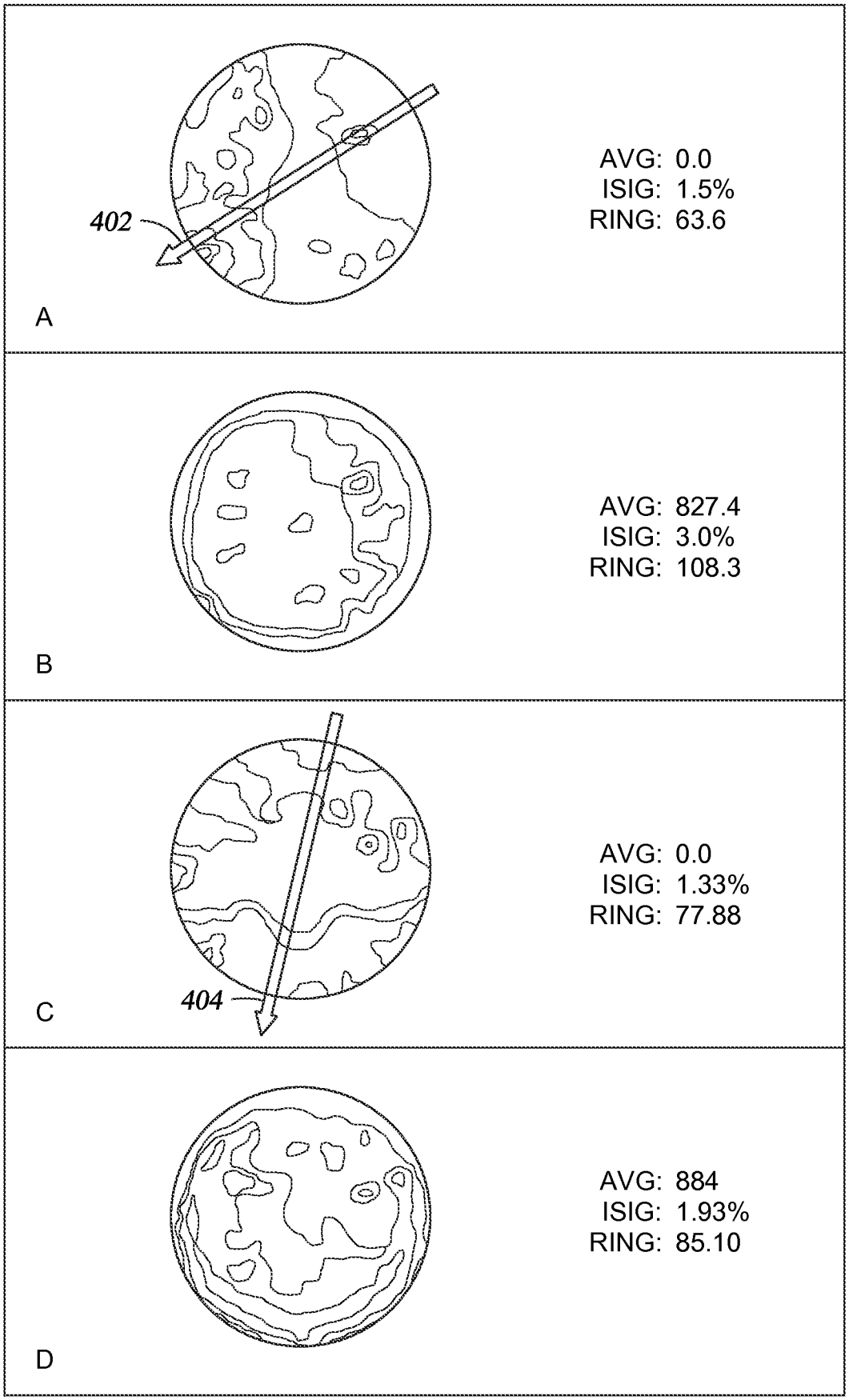
402
AVG: 0.0
ISIG: 1.5%
RING: 63.6
A
AVG: 827.4
ISIG: 3.0%
RING: 108.3
B
404
AVG: 0.0
ISIG: 1.33%
RING: 77.88
C
AVG: 884
ISIG: 1.93%
RING: 85.10
D

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2014/010071

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/02(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/02; H01L 21/311; H01L 21/3065; H05H 1/24; H01L 21/205; H01L 21/31; H01J 37/32; C23C 16/507

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: SADP, chamber, plasma, shield, vaccum, motor, skew

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2004-022988 A (APPLIED MATERIALS, INC.) 22 January 2004 See abstract; paragraphs [0032]-[0041], [0060]-[0061]; claims 1-22 and figures 1-2, 10.	1-4
Y		5-15
Y	US 2009-0159425 A1 (WEI LIU et al.) 25 June 2009 See abstract; paragraphs [0026]-[0055]; claims 1-21 and figures 2-5C.	5-15
Y	US 2010-0075503 A1 (CHRISTOPHER DENNIS BENCHER et al.) 25 March 2010 See abstract; paragraphs [0021]-[0039] and figures 3A-3K.	14-15
A	EP 0820087 A2 (APPLIED MATERIALS, INC.) 21 January 1998 See abstract; column 5, line 28 - column 9, line 36 and figures 1-18.	1-15
A	KR 10-0800401 B1 (EUGENE TECHNOLOGY CO., LTD.) 01 February 2008 See abstract; paragraphs [0028]-[0053]; claims 1-10 and figure 1.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
11 June 2014 (11.06.2014)	**13 June 2014 (13.06.2014)**

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/US2014/010071

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		JP 10-083987 A	31/03/1998
		KR 10-0455951 B1	17/01/2005
KR 10-0800401 B1	01/02/2008	None	