



(51) International Patent Classification:

H01L 39/22 (2006.01)

(21) International Application Number:

PCT/US2021/055996

(22) International Filing Date:

21 October 2021 (21.10.2021)

(25) Filing Language:

English

(26) Publication Language:

English

(30) Priority Data:

202011187173.0 29 October 2020 (29.10.2020) CN

(71) Applicant: **ALIBABA GROUP HOLDING LIMITED**

[—/US]; Fourth Floor, One Capital Place, P.O. Box 847,
George Town, Grand Cayman (KY).

(72) Inventors: **GAO, Ran**; Alibaba Group Legal Department,

5/F Bldg 3 No 969 West Wen Yi Rd, Yu Hang Dis-
trict, Hangzhou, Zhejiang 311121 (CN). **QIN, Jin**; Alibaba
Group Legal Department, 5/F Bldg 3 No 969 West Wen Yi
Rd, Yu Hang District, Hangzhou, Zhejiang 311121 (CN).

DENG, Chunqing; Alibaba Group Legal Department, 5/
F Bldg 3 No 969 West Wen Yi Rd, Yu Hang District,
Hangzhou, Zhejiang 311121 (CN).

(74) Agent: **CAPRON, Aaron J.**; Finnegan, Henderson,

Farabow, Garrett & Dunner LLP, 901 New York Avenue,
NW, Washington, DC 20001-4413 (US).

(81) Designated States (unless otherwise indicated, for every

kind of national protection available): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO,
DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN,
HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN,
KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD,
ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO,
NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW,
SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN,
TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States (unless otherwise indicated, for every

kind of regional protection available): ARIPO (BW, GH,
GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ,
UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ,
TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK,
EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV,
MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,
TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW,
KM, ML, MR, NE, SN, TD, TG).

(54) Title: METHOD FOR PREPARING A JOSEPHSON JUNCTION, APPARATUS, AND DEVICE, AND SUPERCONDUCTING DEVICE

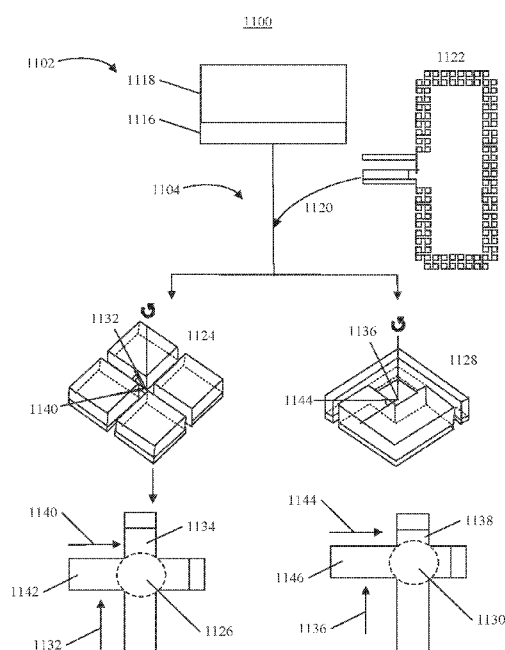


FIG. 11

(57) Abstract: Methods, apparatuses, and devices for Josephson junction preparation includes: obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type; evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission; forming an insulating layer on the first electrode layer, the insulating layer including a compound corresponding to the material; evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission; and forming the first Josephson junction and the plurality of second Josephson junctions.

Published:

— *with international search report (Art. 21(3))*

METHOD FOR PREPARING A JOSEPHSON JUNCTION, APPARATUS, AND DEVICE, AND SUPERCONDUCTING DEVICE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present disclosure claims benefits of and priority to Chinese patent application No. 202011187173.0, filed on October 29, 2020, the content of which is incorporated herein by reference in its entirety.

TECHNICAL FIELD

[0002] The present disclosure relates to the technical field of superconducting circuits, and in particular, to a method for preparing a Josephson junction, apparatus, and device, and a superconducting device.

BACKGROUND

[0003] A Josephson junction, or referred to as a superconducting tunnel junction, is generally a structure including two superconductors sandwiching a very thin barrier layer, such as a Josephson junction formed by a superconductor (S)-insulator (I)-superconductor (S) structure, referred to as SIS. The above Josephson junction is a key component for the realization and application of modern quantum computing. Specifically, in a superconducting quantum computer, superconducting qubits that perform logical operations can be constructed by making one or more Josephson junctions and adding some other additional circuit elements (such as capacitance elements and inductance elements) at the same time. Therefore, the preparation quality of the Josephson junction is the key to the generation of superconducting qubits.

[0004] At present, a preparation method for the Josephson junction usually uses a mask plate to perform shadow evaporation. However, when the above method is used to prepare a Josephson junction, the quality of the Josephson junction largely depends on precise control on the thickness of photoresist and on an evaporation direction. If the evaporation direction changes or the thickness of the photoresist changes, the junction quality of the Josephson

junction will change. Therefore, the preparation quality of the Josephson junction cannot be guaranteed.

SUMMARY

[0005] The embodiments of present disclosure provide methods, apparatuses, and devices for Josephson junction preparation as well as a superconducting circuit. In an aspect, a method for preparing a Josephson junction includes obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions; evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures; forming an insulating layer on the first electrode layer, the insulating layer including a compound corresponding to the material; evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

[0006] In another aspect, an apparatus for preparing a Josephson junction includes: at least one circuitry configured for obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions; causing the apparatus to evaporate a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures; causing the apparatus to form an insulating layer on the first electrode layer, the insulating layer including a compound corresponding to the material; causing the apparatus to evaporate the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and causing the apparatus to form the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and to form the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

[0007] In yet another aspect, a device for preparing a Josephson junction includes at least one processor and a memory configured to store a set of instructions executable by the at least one processor to cause the device to perform: obtaining a first pattern structure for

generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions; evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures; forming an insulating layer on the first electrode layer, the insulating layer including a compound corresponding to the material; evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

[0008] In yet another aspect, a superconducting circuit includes a first Josephson junction of a first type connected in parallel to a plurality of second Josephson junctions of a second type, wherein the plurality of second Josephson junctions are connected in series, and wherein the first Josephson junction and the plurality of second Josephson junctions are generated by a method. The method includes obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for

generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions; evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures; forming an insulating layer on the first electrode layer, the insulating layer including a compound corresponding to the material; evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] To describe the technical solutions in the embodiments of the present disclosure more clearly, the accompanying drawings required for describing the embodiments are briefly introduced below. It is apparent that the accompanying drawings described in the following are merely some embodiments of the present disclosure, and those of ordinary skill in the art can still derive other drawings from these accompanying drawings without creative efforts.

[0010] Figs. 1-3 are schematic diagrams illustrating a process of preparing a Josephson junction.

[0011] Figs. 4A is a schematic diagram illustrating a process of preparing a Josephson junction using a first projection angle.

[0012] Fig. 4B is a schematic diagram illustrating a process of preparing a Josephson junction using a second projection angle.

[0013] Fig. 5A is a schematic diagram illustrating a process of preparing a Josephson junction using photoresist with a first thickness.

[0014] Fig. 5B is a schematic diagram illustrating a process of preparing a Josephson junction using photoresist with a second thickness.

[0015] Fig. 6 is a flowchart illustrating a method for preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0016] Fig. 7 is a flowchart illustrating a method of obtaining a first pattern structure and a plurality of second pattern structures, consistent with some embodiments of this disclosure.

[0017] Fig. 8 is a schematic structural diagram of a mask plate, consistent with some embodiments of this disclosure.

[0018] Fig. 9 is a flowchart of another method for preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0019] Fig. 10 is a flowchart of still another method for preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0020] Fig. 11 is a schematic diagram illustrating a process of preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0021] Fig. 12 is a schematic structural diagram illustrating an apparatus for preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0022] Fig. 13A is a schematic structural diagram illustrating an electronic device for preparing a Josephson junction, consistent with some embodiments of this disclosure.

[0023] Fig. 13B is a block diagram of an example system for operating a quantum circuit, consistent with some embodiments of this disclosure.

[0024] FIG. 13C is a schematic diagram illustrating an example quantum controller for operating quantum circuits, consistent with some embodiments of this disclosure.

[0025] Fig. 14 is a schematic diagram illustrating a superconducting device, consistent with some embodiments of this disclosure.

DETAILED DESCRIPTION

[0026] Reference can now be made in detail to example embodiments, examples of which are illustrated in the accompanying drawings. The following description refers to the accompanying drawings in which the same numbers in different drawings represent the same or similar elements unless otherwise represented. The implementations set forth in the following description of example embodiments do not represent all implementations consistent with the disclosure. Instead, they are merely examples of apparatuses and methods consistent with aspects related to the disclosure as recited in the appended claims. Particular aspects of present disclosure are described in greater detail below. The terms and definitions provided herein control, if in conflict with terms or definitions incorporated by reference.

[0027] The terminology used in the embodiments of the present disclosure is for the purpose of describing particular embodiments only, and is not intended to limit the present disclosure. The singular forms “a,” “said,” and “the” used in the embodiments of the present disclosure and the appended claims are also intended to include plural forms, unless other meanings are clearly indicated in the context, and “multiple” generally includes at least two, but does not exclude the case of including at least one.

[0028] It should be noted that, the relational terms herein such as “first” and “second” are used only to differentiate an entity or operation from another entity or operation, and do not require or imply any actual relationship or sequence between these entities or operations. Moreover, the words “comprising,” “having,” “containing,” and “including,” and other similar forms are intended to be equivalent in meaning and be open ended in that an item or items following any one of these words is not meant to be an exhaustive listing of such item or items, or meant to be limited to only the listed item or items.

[0029] As used herein, unless specifically stated otherwise, the term “or” encompasses all possible combinations, except where infeasible. For example, if it is stated that a component can include A or B, then, unless specifically stated otherwise or infeasible, the component can include A, or B, or A and B. As a second example, if it is stated that a component can include A, B, or C, then, unless specifically stated otherwise or infeasible, the component can include A, or B, or C, or A and B, or A and C, or B and C, or A and B and C.

[0030] Depending on the context, the words “in case of” and “if” as used herein can be interpreted as “at the time of” or “when” or “in response to determination” or “in response to detection.” Similarly, depending on the context, the phrase “if determined” or “if detected (a stated condition or event)” can be interpreted as “when determined” or “in response to determination” or “when detected (a stated condition or event)” or “response to detection (of a stated condition or event).”

[0031] It should be further noted that the terms “include,” “comprise,” or any other variations thereof are intended to cover non-exclusive inclusion, so that a commodity or system including a series of elements not only includes the elements, but also includes other elements not explicitly listed, or further includes elements inherent to the commodity or system. In the absence of more limitations, an element defined by “including a/an ...” does not exclude that the commodity or system including the element further has other identical

elements. In addition, the sequence of steps in the following method embodiments is only an example, not a strict limitation.

[0032] As used herein, a Josephson junction (also referred to as “a superconducting tunnel junction”) can refer to a structure including two superconductors sandwiching a thin barrier layer. By way of example, a Josephson junction can be formed by a superconductor-insulator-superconductor structure (or referred to as an “S-I-S” structure). The Josephson junction can be a key component for implementation and application of modern quantum computing. In some applications, a superconducting quantum computer can utilize a large number (e.g., about 1 million) of superconducting quantum bits (“qubits”) to achieve high-precision data operations. The superconducting qubits that perform logical operations can be constructed by preparing one or more Josephson junctions and adding additional circuit elements (e.g., capacitance elements or inductance elements). Therefore, preparing a large number of superconducting qubits with uniform structures can be very important for superconducting quantum computers. One of the keys to producing superconducting qubits is the preparation quality of the Josephson junction (e.g., an area of the Josephson junction, a critical current of the Josephson junction, a non-superconducting normal-state resistance of the Josephson junction, or any other characteristics of the Josephson junction).

[0033] Existing techniques for preparing a Josephson junction typically include shadow evaporation with a mask plate. Figs. 1-3 are schematic diagrams illustrating a conventional process of preparing a Josephson junction. As shown in Fig. 1, a mask plate 102 can include a first mask pattern 104 and a second mask pattern 106, and a bridge structure 108 is arranged between first mask pattern 104 and second mask pattern 106. Based on mask plate 102 with bridge structure 108, a material can be grown on a bare silicon wafer 110 through first mask pattern 104 to generate a first structure (not shown in Fig. 1).

[0034] As shown in Fig. 2, a process of generating a first structure 204 can include growing a first material 202 on mask plate 102 at a first projection angle θ_1 . First material 202 can be grown on bare silicon wafer 110 through first mask pattern 104 and second mask pattern 106 on the same mask, so that first structure 204 can be generated.

[0035] As shown in Fig. 3, a process of generating a second structure 304 can include growing a second material 302 on first material 202 at a second projection angle θ_2 . Second material 302 can be grown on bare silicon wafer 110 through first mask pattern 104 and second mask pattern 106 on the same mask, so that second structure 304 (represented by a filled pattern) can be generated. The second projection angle θ_2 can be different from the first projection angle θ_1 (as illustrated in Fig. 2). Accordingly, positions of first structure 204 and second structure 304 on bare silicon wafer 110 can be different, so that an overlapping structure can form between first structure 204 and second structure 304. Such an overlapping structure can form a Josephson junction 306 (represented by a structure enclosed in a dash-line circle in Fig. 3).

[0036] When the conventional process described in association with Figs. 1-3 is used to prepare a Josephson junction, the quality of the Josephson junction can largely depend on precise control of thickness of a photoresist and on precise control of an evaporation direction. If the evaporation direction changes, the quality of the Josephson junction can subject to change (e.g., an area of the Josephson junction, a critical current of the Josephson junction, a non-superconducting normal-state resistance of the Josephson junction, or any other characteristics of the Josephson junction).

[0037] Figs. 4A is a schematic diagram illustrating a conventional process of preparing a Josephson junction using a first projection angle 402. As shown in Fig. 4A, for the same photoresist structure and evaporation material, when evaporating the material using first projection angle 402, an electrode layer can be formed on the photoresist layer with a width

404. **Figs. 4B** is a schematic diagram illustrating a conventional process of preparing a Josephson junction using a second projection angle 406. As shown in **Fig. 4B**, when evaporating the material using second projection angle 406, an electrode layer can be formed on the photoresist layer with a width 408. When first projection angle 402 and second projection angle 406 are different, width 404 and width 408 can be different. Therefore, during preparation of a plurality of Josephson junctions, the quality of the plurality of Josephson junctions (e.g., areas of the Josephson junctions) can subject to the changes of the projection angle, so that it can be challenging to ensure the preparation quality of the Josephson junction.

[0038] Similarly, the junction quality of the Josephson junction can change depending on the thickness of the photoresist for preparing the Josephson junction. **Fig. 5A** is a schematic diagram illustrating a conventional process of preparing a Josephson junction using photoresist with a first thickness. As shown in **Fig. 5A**, for the same projection angle and evaporation material, when evaporating the material on a photoresist structure with a photoresist thickness 502 using a projection angle, an electrode layer can be formed on the photoresist layer with width 404. **Fig. 5B** is a schematic diagram illustrating a conventional process of preparing a Josephson junction using photoresist with a second thickness. As shown in **Fig. 5B**, when evaporating the material on a photoresist structure with a photoresist thickness 504 using the same projection angle, an electrode layer can be formed on the photoresist layer with width 408. When photoresist thickness 502 is different from photoresist thickness 504, width 404 and width 408 can also be different. Accordingly, when a plurality of Josephson junctions are prepared using different photoresist thicknesses, the junction quality of the plurality of Josephson junctions (e.g., areas of the Josephson junctions) can subject to changes of the photoresist thicknesses, so that it can be challenging to ensure the preparation quality of the Josephson junction.

[0039] As described above, when preparing a Josephson junction, the evaporation angle and the photoresist thickness have great impacts on the quality of the Josephson junction. Specifically, for the wafer-scale manufacturing of a plurality of Josephson junctions, the evaporation angle and the distribution of the photoresist thickness on the entire wafer can impact the quality of the Josephson junctions and can significantly reduce the preparation yield of the Josephson junctions in some cases.

[0040] To reduce the influence of the change in the evaporation direction or the photoresist thickness on the quality of the Josephson junction, and to improve the uniformity and preparation yield of the Josephson junction at the wafer scale, methods, apparatuses, devices, superconducting devices for preparing a Josephson junction are provided in the present disclosure. Embodiments of this disclosure can provide multiple technical benefits. The first Josephson junction and the plurality of second Josephson junctions can be prepared simultaneously. Moreover, when the first electrode layer and the second electrode layer are generated, the first evaporation direction can be substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures. The second evaporation direction can be substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures. By doing so, the influence of the evaporation direction or the thickness of the photoresist on the quality of the Josephson junction can be effectively reduced. Accordingly, the quality of the first Josephson junction and the plurality of second Josephson junctions can be ensured, and the uniformity and yield of preparing Josephson junctions can be improved.

[0041] Some implementations of the present disclosure will be described in detail below with reference to the accompanying drawings. Provided that there is no conflict between the embodiments, the following embodiments and features in the embodiments can be combined with each other.

[0042] Fig. 6 is a flowchart illustrating a method 600 for preparing a Josephson junction, consistent with some embodiments of this disclosure. Method 600 can be used for preparing a wafer-level Josephson junction. Also, any apparatus capable of performing method 600 can be used for preparing a wafer-level Josephson junction. It is understandable that the apparatus for preparing a Josephson junction can be implemented as software, hardware, or a combination of software and hardware. In some embodiments, method 600 can be implemented by at least one circuitry of the apparatus.

[0043] At step 602, a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type are obtained. A junction area of the first Josephson junction can be different from a junction area of at least one of the plurality of second Josephson junctions.

[0044] In some embodiments, different Josephson junctions can correspond to different junction areas. In order to facilitate the preparation of Josephson junctions while ensuring the uniformity and preparation yield of the Josephson junctions, the Josephson junctions can be classified into the first Josephson junction and the plurality of second Josephson junctions, and the junction area of the first Josephson junction can be different from the junction area of the at least one of the plurality of second Josephson junctions.

[0045] By way of example, the junction area of the first Josephson junction can be smaller than or equal to a preset area, and the junction area of the at least one of the plurality of second Josephson junctions can be greater than the preset area. In such cases, the first Josephson junction can be referred to as a “small junction,” and the plurality of second Josephson junctions can be referred to as “big junctions.”

[0046] In another example, the junction area of the first Josephson junction can be greater than the preset area, and the junction area of the at least one of the plurality of second

Josephson junctions can be less than or equal to the preset area. In such cases, the first Josephson junction can be referred to as a “big junction,” and the plurality of second Josephson junctions can be referred to as “small junctions.”

[0047] For ease of description without causing ambiguities, the following description takes the first Josephson junction as the “small junction” and the plurality of second Josephson junctions as the “big junctions” as an example. In such cases, the preset area for distinguishing the first Josephson junction from the plurality of second Josephson junctions can be preset. For example, the preset area can be the largest area that can be realized by the first Josephson junction. It should be noted that the specific numerical range of the preset area is not limited in the example embodiments of this disclosure, and those skilled in the art can set it according to specific application requirements and design requirements, which will not be detailed herein.

[0048] In some embodiments, to simultaneously prepare the first Josephson junction and the plurality of second Josephson junctions, the first pattern structure and the plurality of second pattern structures can be prepared in advance, so that the first Josephson junction can be generated based on the first pattern structure, and the plurality of second Josephson junctions can be generated based on the plurality of second pattern structures. It is understandable that the first pattern structure and the plurality of second pattern structures can be the same or different. For example, the first pattern structure can be a symmetrical structure, and at least one of the plurality of second pattern structures can be an asymmetrical structure. In some embodiments, the first pattern structure and the plurality of second pattern structures described herein can be obtained by etching through a mask plate.

[0049] In some embodiments, the plurality of second Josephson junctions can be connected in series. The first Josephson junction can be connected in parallel to the plurality of second Josephson junctions. In such cases, the plurality of second Josephson junctions and

the first Josephson junction can be used to generate a superconducting device, thereby improving the practicability of the prepared Josephson junction.

[0050] Still referring to Fig. 6, at step 604, a material is evaporated on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission. The first evaporation direction can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures.

[0051] In some embodiments, after step 602, a material can be evaporated simultaneously on the first pattern structure and the plurality of second pattern structures based on the first evaporation direction. In some embodiments, the material can include at least one of aluminum, binary nitride, ternary nitride, composite oxide, or any other superconducting materials (e.g., at least one of tantalum, molybdenum, vanadium, or the like). It is understandable that the material is not limited to the examples described herein. Those skilled in the art can also select the material according to specific application requirements and design requirements.

[0052] In some embodiments, the first electrode layer for implementing information transmission can be generated by the material evaporated on the first pattern structure and the plurality of second pattern structures. For example, the first electrode layer generated in the first pattern structure can be used to generate the first Josephson junction, and the first electrode layer generated in the plurality of second pattern structures can be used to generate the plurality of second Josephson junctions.

[0053] In some embodiments, the first evaporation direction can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures. By doing so, the influence of the

evaporation angle and the photoresist thickness on the preparation quality of the Josephson junction can be reduced in the process of preparing the first Josephson junction and the plurality of second Josephson junctions. By way of example, an angle formed between the first evaporation direction and a gravity direction can be greater than or equal to 10° and less than or equal to 60° . It is noted that the first evaporation direction is not limited to the example embodiments described herein and can be set by those skilled in the art according to specific application requirements and design requirements, as long as the uniformity and preparation yield of the first Josephson junction and the plurality of second Josephson junctions can be ensured.

[0054] Still referring to **Fig. 6**, at step 606, an insulating layer is formed on the first electrode layer. The insulating layer can include a compound corresponding to the material.

[0055] At step 608, the material is evaporated on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission. The second evaporation direction can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures.

[0056] In some embodiments, the material can be evaporated simultaneously on the first pattern structure and the plurality of second pattern structures based on the second evaporation direction to generate the second electrode layer. In some embodiments, the second electrode layer generated in the first pattern structure can be used to generate the first Josephson junction, and the second electrode layer generated in the plurality of second pattern structures can be used to generate the plurality of second Josephson junctions.

[0057] In some embodiments, the second evaporation direction can be substantially parallel to the edge of the first pattern structure and the edge of the at least one of the

plurality of second pattern structures. By doing so, the influence of the evaporation angle and the photoresist thickness on the preparation quality of the Josephson junction can be reduced in the process of preparing the first Josephson junction and the plurality of second Josephson junctions. It should be noted that the second evaporation direction is not limited to the example embodiments described herein and can be select by those skilled in the art according to specific application requirements and design requirements, as long as the uniformity and preparation yield of preparing the first Josephson junction and the plurality of second Josephson junctions can be ensured. In some embodiments, the first evaporation direction can be perpendicular to the second evaporation direction. In some embodiments, the second evaporation direction can be approximately perpendicular to the first evaporation direction (e.g., within an error range of 1°, 2°, 5°, 10°, or any preset angle range).

[0058] Still referring to Fig. 6, at step 610, the first Josephson junction is formed based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure. The plurality of second Josephson junctions are formed based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

[0059] In some embodiments, the first Josephson junction can be formed as an overlapping structure that include the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure. Similarly, the plurality of second Josephson junctions can be formed as overlapping structures, each of the overlapping structures including the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures. By doing so, accurate and effective preparation operations on Josephson junctions can be effectively implemented.

[0060] As described above, by performing method 600, the first Josephson junction and the plurality of second Josephson junctions can be prepared simultaneously. Moreover, when the first electrode layer and the second electrode layer are generated, the first evaporation direction can be substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures, and the second evaporation direction can be substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures. By doing so, the influence of the evaporation direction or the thickness of the photoresist on the quality of the Josephson junction can be effectively reduced. Accordingly, the quality of the first Josephson junction and the plurality of second Josephson junctions can be ensured, and the uniformity and yield of preparing Josephson junctions can be improved.

[0061] Fig. 7 is a flowchart illustrating a method 700 of obtaining a first pattern structure and a plurality of second pattern structures, consistent with some embodiments of this disclosure. The first pattern structure can be used for generating the first Josephson junction of the first type as described in method 600, and the plurality of second pattern structures can be used for generating the plurality of second Josephson junctions of the second type as described in method 600.

[0062] At step 702, a mask plate is obtained for preparing a wafer-level Josephson junction. The mask plate can include a first mask region for preparing the first Josephson junction and a plurality of second mask regions for preparing the plurality of second Josephson junctions. At step 704, the first pattern structure is obtained through the first mask region, and the plurality of second pattern structures are obtained through the plurality of second mask regions.

[0063] Fig. 8 is a schematic structural diagram of a mask plate 800, consistent with some embodiments of this disclosure. Mask plate 800 can be used for preparing a wafer-level

Josephson junction and can be preset. As shown in Fig. 8, mask plate 800 can include a first mask region 802 for preparing the first Josephson junction and second mask regions 804 for preparing the plurality of second Josephson junctions. It is understandable that the specific numbers of first mask region 802 and second mask regions 804 can be adjusted and set based on specific application scenarios and design requirements. In some embodiments, to prepare the plurality of second Josephson junctions described herein as being connected in series, second mask regions 804 can be connected in series. In some embodiments, to prepare the plurality of second Josephson junctions as being connected in parallel to the first Josephson junction, second mask regions 804 can be connected in parallel to first mask region 802.

[0064] By way of example, the first pattern structure can be obtained through first mask region 802, and the plurality of second pattern structures can be obtained through second mask regions 804. In some embodiments, to obtain the first pattern structure and the plurality of second pattern structures, a substrate structure can be obtained. A photoresist layer can be formed on the substrate structure. Then, etching can be performed on the photoresist layer through mask plate 800 to obtain the first pattern structure and the plurality of second pattern structures.

[0065] In some embodiments, to achieve a stable operation for preparing the Josephson junction, a preset substrate structure for generating the Josephson junction can be obtained. For example, the substrate structure can be a preset bare silicon wafer. After the substrate structure is obtained, a photoresist layer can be formed on the substrate structure. To ensure the quality of the pattern structure generated by the etching operation, in some embodiments, the photoresist layer generated on the substrate structure can be a double-layer structure. For example, the photoresist layer can include an upper photoresist layer and a lower photoresist layer, in which thickness of the upper photoresist layer can be greater than thickness of the lower photoresist layer. After the photoresist layer is generated, etching can be performed on

the photoresist layer through a mask plate (e.g., mask plate 800) to obtain the first pattern structure and the plurality of second pattern structures. By doing so, the accuracy and reliability of obtaining the first pattern structure and the plurality of second pattern structures can be ensured.

[0066] Fig. 9 is a flowchart of a method 900 for preparing a Josephson junction, consistent with some embodiments of this disclosure. In some embodiments, method 900 can be performed in addition to method 600 for preparing the Josephson junction. At step 902, an electrical parameter for defining the first Josephson junction is obtained. At step 904, a junction area of the first Josephson junction is determined based on the electrical parameter. By performing method 900, Josephson junctions of the first type having different junction area sizes can be prepared corresponding to different electrical parameters so as to meet design requirements and application requirements of different users, thereby further improving the flexibility and reliability of preparing the first Josephson junction.

[0067] In some embodiments, the junction area of the first Josephson junction can be related to the electrical parameter. Obtaining the electrical parameter can ensure that the prepared first Josephson junction can meet the design requirements and usage requirements. In some embodiments, the electrical parameter can include at least one of electromagnetic field energy density, capacitance, or inductance. In some embodiments, the electrical parameter can be input by a user in advance or determined according to specific application scenarios and design requirements. By way of example, the user can directly input (e.g., through a user interface) the electrical parameter to an apparatus for implementing method 900. After the electrical parameter is obtained, the junction area of the first Josephson junction can be determined based on the electrical parameter.

[0068] In some embodiments, to determine the junction area of the first Josephson junction based on the electrical parameter, mapping relationships between different electrical

parameters and different junction areas can be predetermined. After obtaining the electrical parameter, the mapping relationships can be used to determine the junction area of the first Josephson junction.

[0069] Fig. 10 is a flowchart of a method 1000 for preparing a Josephson junction, consistent with some embodiments of this disclosure. In some embodiments, method 1000 can be performed in addition to method 600 for preparing the Josephson junction. At step 1002, an evaporation angle is obtained for preparing the plurality of second Josephson junctions. The evaporation angle can correspond to at least one of the first evaporation direction or the second evaporation direction. At step 1004, a designed junction area associated with the plurality of second Josephson junctions is determined based on the evaporation angle.

[0070] In some embodiments, the plurality of second Josephson junctions can correspond to the designed junction area and a junction area (e.g., an actual junction area). By way of example, the designed junction area can be a theoretical junction area to be implemented by the plurality of second Josephson junctions, and the designed junction area and the junction area can be the same or different.

[0071] In some embodiments, the designed junction area associated with the plurality of second Josephson junctions can be related to the evaporation angle for preparing the plurality of second Josephson junctions. In some embodiments, the evaporation angle can include a first evaporation angle corresponding to the first evaporation direction or a second evaporation angle corresponding to the second evaporation direction.

[0072] In some embodiments, after being obtained, the evaporation angle can be analyzed and processed to determine the designed junction area associated with the plurality of second Josephson junctions. For example, to determine the designed junction area associated with the plurality of second Josephson junctions, thickness information of a photoresist layer for

preparing the plurality of second Josephson junctions can be obtained. Then, the designed junction area can be determined based on the thickness information and the evaporation angle. The designed junction area can be greater than or equal to a junction area of at least one of the plurality of second Josephson junctions.

[0073] In some embodiments, to determine the designed junction area based on the thickness information and the evaporation angle, a cosine value corresponding to the evaporation angle can be obtained (e.g., after the evaporation angle is obtained). The product value of the cosine value and the thickness information can be determined. For example, the product value can be used as an area line corresponding to the designed junction area. Then, the designed junction area can be determined based on the product value. For example, the designed junction area can be determined as a square value of the product value.

[0074] Fig. 11 is a schematic diagram illustrating a process 1100 of preparing a Josephson junction, consistent with some embodiments of this disclosure. Process 1100 can achieve simultaneous preparation of a plurality of Josephson junctions at the wafer level, and the plurality of Josephson junctions can include the first Josephson junction and the plurality of second Josephson junctions as described herein. For example, the first Josephson junction can refer to as a small junction with a junction area being smaller than or equal to a preset area, and the plurality of second Josephson junctions can refer to as big junctions with junction areas being greater than the preset area.

[0075] As shown in Fig. 11, at step 1102, a substrate material 1116 is obtained, and a double-layer photoresist layer 1118 is formed on substrate material 1116. In some embodiments, double-layer photoresist layer 1118 can include a top photoresist layer and a bottom photoresist layer (not shown in Fig. 11), in which thickness of the top photoresist layer can be greater than thickness of the bottom photoresist layer. By doing so, the quality

and efficiency of generating the first pattern structure and the plurality of second pattern structures can be ensured.

[0076] As shown in Fig. 11, at step 1104, an etching operation 1120 is performed on double-layer photoresist layer 1118 through a mask plate 1122 to obtain a first pattern structure 1124 for generating a first Josephson junction 1126 (represented by an overlapping area enclosed by a dash-line oval in Fig. 11) of a first type and a plurality of second pattern structures 1128 for generating a plurality of second Josephson junctions 1130 (represented by an overlapping area enclosed by a dash-line oval in Fig. 11) of a second type. As shown in Fig. 11, first pattern structure 1124 can include a pattern area formed by four symmetrically arranged photoresist structure blocks, in which the sizes and shapes of the photoresist structure blocks are the same. There can be a predetermined distance between two adjacent photoresist structure blocks to form first pattern structure 1124, and the whole of first pattern structure 1124 can form a cross-shape structure.

[0077] As shown in Fig. 11, second pattern structures 1128 can include a pattern area formed by two photoresist structure blocks, in which the sizes and shapes of the two photoresist structure blocks are different. Specifically, one of the photoresist structure blocks has an L-shaped structure, the other photoresist structure block has an inverted-L-shaped structure, and there is a predetermined distance between the two photoresist structure blocks.

[0078] In some embodiments, in order to be able to prepare first Josephson junction 1126 and second Josephson junctions 1130 at the same time, arrangement directions of first pattern structure 1124 and second pattern structures 1128 on substrate material 1116 can be the same. For example, as shown in Fig. 11, a first evaporation direction 1132 of a first electrode layer 1134 for generating first Josephson junction 1126 can be the same as a first evaporation direction 1136 of a first electrode layer 1138 for generating second Josephson junctions 1130. A second evaporation direction 1140 of a second electrode layer 1142 for generating first

Josephson junction 1126 can be the same as a second evaporation direction 1144 of a second electrode layer 1146 for generating second Josephson junctions 1130.

[0079] At step 1106 (not illustrated in Fig. 11), a material is loaded into an evaporation tool. The evaporation tool can be used to simultaneously evaporate the material on first pattern structure 1124 in first evaporation direction 1132 to generate first electrode layer 1134 and evaporate the material on second pattern structures 1128 in first evaporation direction 1136 (the same as first evaporation direction 1132) to generate first electrode layer 1138. First evaporation direction 1132 (the same as first evaporation direction 1136) can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to an edge of first pattern structure 1124 and an edge of at least one of second pattern structures 1128.

[0080] At step 1108 (not illustrated in Fig. 11), an insulating layer is formed on first electrode layer 1134 and first electrode layer 1138.

[0081] At step 1110 (not illustrated in Fig. 11), the evaporation tool is used to evaporate the material on first pattern structure 1124 based on second evaporation direction 1140 to generate second electrode layer 1142 and to evaporate the material on second pattern structures 1128 based on second evaporation direction 1144 (the same as second evaporation direction 1140) to generate second electrode layer 1146. Second evaporation direction 1144 (the same as second evaporation direction 1140) can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to another edge of first pattern structure 1124 and another edge of at least one of second pattern structures 1128.

[0082] In some embodiments, first evaporation direction 1132 (the same as first evaporation direction 1136) can be perpendicular to second evaporation direction 1140 (the same as second evaporation direction 1146) to ensure that the size information of the generated Josephson junction meets a preset requirement, and to prevent a line width size of the generated Josephson junction from becoming thinner.

[0083] At step 1112 (not illustrated in Fig. 11), double-layer photoresist layer 1118 is removed to obtain Josephson junctions, including first Josephson junction 1126 and second Josephson junctions 1130. First Josephson junction 1126 can include first electrode layer 1134, the insulating layer, and second electrode layer 1142. Second Josephson junction 1130 can include first electrode layer 1138, the insulating layer, and second electrode layer 1146.

[0084] It should be noted that, due to the correspondence between the junction area of first Josephson junction 1126 and electrical features (e.g., electromagnetic field energy density, capacitance, or inductance), when first Josephson junction 1126 is prepared by process 1100, the influence of the change in the photoresist thickness and the change in the evaporation angle on first Josephson junction 1126 can be effectively reduced. In such cases, the junction area of a Josephson junction can only be related to the line width corresponding to first pattern structure 1124, thus effectively ensuring high-quality preparation operation of the Josephson junctions.

[0085] After the Josephson junction is generated, mask plate 1122 can be removed. In some embodiments, mask plate 1122 can be removed using an organic solvent or a high-frequency vapor phase etching method. Those skilled in the art can use other methods to remove mask plate 1122, as long as it ensures that mask plate 1122 can be removed stably and effectively, which will not be detailed herein.

[0086] At step 1114 (not illustrated in Fig. 11), after first Josephson junction 1126 and second Josephson junctions 1130 are obtained, first Josephson junction 1126 and second Josephson junctions 1130 can be used to prepare a superconducting device. By way of example, second Josephson junctions 1130 can be connected in series, and second Josephson junctions 1130 can be connected in parallel to first Josephson junction 1126, so that a superconducting device with an adjustable magnetic flux can be generated. The superconducting device can have a long correlation time.

[0087] The technical solution described in association with **Fig. 11** can ensure that first Josephson junction 1126 and second Josephson junctions 1130 are prepared simultaneously. Moreover, during generation of a first electrode layer (e.g., first electrode layer 1134 or first electrode layer 1138) and a second electrode layer (e.g., second electrode layer 1142 or second electrode layer 1146), a first evaporation direction (e.g., first evaporation direction 1132 or first evaporation direction 1136) can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to an edge of first pattern structure 1124 and an edge of at least one of second pattern structures 1128. Also, during generation of the first electrode layer and the second electrode layer, a second evaporation direction (e.g., second evaporation direction 1140 or second evaporation direction 1144) can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to another edge of first pattern structure 1124 and another edge of at least one of second pattern structures 1128. By doing so, the influence of the evaporation direction or the influence of the thickness of the photoresist on the quality of the Josephson junction (e.g., an area of the Josephson junction, a critical current of the Josephson junction, or a non-superconducting normal-state resistance of the Josephson junction) can be reduced. Accordingly, the quality of first Josephson junction 1126 and second Josephson junctions 1130 can be ensured, and the uniformity and yield of preparing Josephson junctions can be improved.

[0088] **Fig. 12** is a schematic structural diagram illustrating an apparatus 1200 for preparing a Josephson junction, consistent with some embodiments of this disclosure. Apparatus 1200 can be used for preparing a wafer-level Josephson junction. In some embodiments, apparatus 1200 can perform any of methods 600, 700, 900, or 1000 described in association with **Figs. 6-7** and **Figs. 9-10**. As shown in **Fig. 12**, apparatus 1200 can include an acquisition module 1202, an evaporation module 1204, a generation module 1206, and a preparation module 1208. It should be noted that acquisition module 1202, evaporation

module 1204, generation module 1206, and preparation module 1208 can be implemented as software modules, hardware modules (e.g., including circuitry), or a combination of software modules and hardware modules.

[0089] Acquisition module 1202 can be configured to obtain a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type. A junction area of the first Josephson junction can be different from a junction area of at least one of the plurality of second Josephson junctions.

[0090] Evaporation module 1204 can be configured to cause apparatus 1200 to evaporate a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission. The first evaporation direction can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures.

[0091] Generation module 1206 can be configured to cause apparatus 1200 to form an insulating layer on the first electrode layer. The insulating layer can include a compound corresponding to the material.

[0092] Evaporation module 1204 can be further configured to cause apparatus 1200 to evaporate the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission. The second evaporation direction can be substantially parallel (e.g., within an error range of $\pm 2^\circ$) to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures.

[0093] Preparation module 1208 can be configured to cause apparatus 1200 to form the first Josephson junction based on the first electrode layer generated on the first pattern

structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and to form the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

[0094] In some embodiments, the junction area of the first Josephson junction can be smaller than or equal to a preset area, and the junction area of the at least one of the plurality of second Josephson junctions can be greater than the preset area.

[0095] In some embodiments, to obtain the first pattern structure and the plurality of second pattern structures, acquisition module 1202 can be configured to cause apparatus 1200 to obtain a mask plate for preparing a wafer-level Josephson junction. The mask plate can include a first mask region for preparing the first Josephson junction and a plurality of second mask regions for preparing the plurality of second Josephson junctions. Acquisition module 1202 can be further configured to cause apparatus 1200 to obtain the first pattern structure through the first mask region, and to obtain the plurality of second pattern structures through the plurality of second mask regions.

[0096] In some embodiments, to obtain the first pattern structure and the plurality of second pattern structures, acquisition module 1202 can be further configured to cause apparatus 1200 to obtain a substrate structure, to form a photoresist layer on the substrate structure, and to perform etching on the photoresist layer through the mask plate to obtain the first pattern structure and the plurality of second pattern structures.

[0097] In some embodiments, acquisition module 1202 can be configured to cause apparatus 1200 to obtain an electrical parameter for defining the first Josephson junction. Evaporation module 1204 can be configured to determine a junction area of the first Josephson junction based on the electrical parameter. By way of example, the electrical

parameter can include at least one of electromagnetic field energy density, capacitance, or inductance.

[0098] In some embodiments, acquisition module 1202 can be configured to cause apparatus 1200 to obtain an evaporation angle for preparing the plurality of second Josephson junctions. The evaporation angle can correspond to at least one of the first evaporation direction or the second evaporation direction. Evaporation module 1204 can be configured to determine a designed junction area associated with the plurality of second Josephson junctions based on the evaporation angle.

[0099] In some embodiments, to determine the designed junction area, evaporation module 1204 can be further configured to cause apparatus 1200 to obtain thickness information of the photoresist layer for preparing the plurality of second Josephson junctions, and to determine the designed junction area based on the thickness information and the evaporation angle. The designed junction area can be greater than or equal to a junction area of at least one of the plurality of second Josephson junctions.

[0100] In some embodiments, to determine the designed junction area, evaporation module 1204 can be further configured to obtain a cosine value corresponding to the evaporation angle, to determine the product value of the cosine value and the thickness information, and to determine the designed junction area based on the product value.

[0101] In some embodiments, an angle formed between the first evaporation direction and a gravity direction is greater than or equal to 10° , and less than or equal to 60° . In some embodiments, the first evaporation direction is perpendicular to the second evaporation direction. In some embodiments, the plurality of second Josephson junctions are connected in series, and the first Josephson junction is connected in parallel to the plurality of second Josephson junctions. In some embodiments, the material comprises at least one of aluminum, binary nitride, ternary nitride, or composite oxide.

[0102] Consistent with some embodiments of this disclosure, the structure of apparatus 1200 in Fig. 12 can be implemented as an electronic device. The electronic device can include various devices such as a mobile phone, a tablet computer, or a server. Fig. 13A is a schematic structural diagram illustrating an electronic device 1300A for preparing a Josephson junction, consistent with some embodiments of this disclosure. As shown in Fig. 13A, electronic device 1300A can include a processor 1302 and a memory 1304. Memory 1304 can be used to store a program (e.g., including one or more computer instructions) for electronic device 1300A to perform a method for preparing a Josephson junction, such as methods 600, 700, 900, or 1000 described in association with Figs. 6-7 and Figs. 9-10. Processor 1302 can be configured to execute the program stored in memory 1304. Electronic device 1300A can also include communication interface 1306 for electronic device 1300A to communicate with another device or a communication network.

[0103] Consistent with some embodiments of this disclosure, Fig. 13B is a block diagram of an example system 1300B for operating a quantum circuit, consistent with some embodiments of this disclosure. In some embodiments, system 1300B can include a computer (e.g., a classical computer) configured to execute operations for operating a quantum circuit as described in association with Figs. 6-12. As depicted in Fig. 13B, system 1300B includes a processor 1308 that can be in operable connection with a memory 1310, an input/output (I/O) module 1312, and a network interface controller (NIC) 1316.

[0104] When processor 1308 executes instructions described herein, system 1300B can become a specialized machine for preparing a Josephson junction. Processor 1308 can be any type of circuitry capable of manipulating or processing information. For example, processor 1308 can include any combination of any number of a central processing unit (or “CPU”), a graphics processing unit (or “GPU”), a neural processing unit (“NPU”), a microcontroller unit (“MCU”), an optical processor, a programmable logic controller, a microcontroller, a

microprocessor, a digital signal processor, an intellectual property (IP) core, a Programmable Logic Array (PLA), a Programmable Array Logic (PAL), a Generic Array Logic (GAL), a Complex Programmable Logic Device (CPLD), a Field-Programmable Gate Array (FPGA), a System On Chip (SoC), an Application-Specific Integrated Circuit (ASIC), or the like. In some embodiments, processor 1308 can also be a set of processors (not shown in **Fig. 13B**) grouped as a single logical component.

[0105] Memory 1310 can include a single memory or a plurality of memories that can be configured to store data 1312 (e.g., a set of instructions, computer codes, intermediate data, or data for output). Memory 1310 can include a high-speed random-access storage device or a non-volatile storage device. In some embodiments, memory 1310 can include any combination of any number of a random-access memory (RAM), a read-only memory (ROM), an optical disc, a magnetic disk, a hard drive, a solid-state drive, a flash drive, a security digital (SD) card, a memory stick, a compact flash (CF) card, or the like. Memory 1310 can also be a group of memories (not shown in **Fig. 13B**) grouped as a single logical component. Processor 1308 can access the program instructions and data 1312, and execute the program instructions to perform an operation or manipulation on data 1312. As depicted in **Fig. 13B**, memory 1310 can store an operating system 1318 and a Josephson junction preparer 1320. For example, Josephson junction preparer 1320 can include instructions to implement the method described in association with **Figs. 6-12** to prepare a Josephson junction.

[0106] For ease of explanation without causing ambiguity, processor 1308 and other data processing circuits are collectively referred to as a “data processing circuit” in this disclosure. The data processing circuit can be implemented entirely as hardware, or as a combination of software, hardware, or firmware. In addition, the data processing circuit can be a single

independent module or can be combined entirely or partially into any other component of system 1300B.

[0107] Input/output module (I/O) 1314 can store and retrieve data from a database 1322. For example, database 1322 can include data structures describing quantum circuits and data structures describing quantum gates. NIC 1316 can provide wired or wireless communication between system 1300B and a network (e.g., Internet 1324, an intranet, a local area network, a mobile communications network, or the like). System 1300B can receive data and instructions over a network using NIC 1316 and can transmit data and instructions over a network using NIC 1316. In some embodiments, NIC 1316 can include any combination of a radio frequency (RF) module, a transponder, a transceiver, a modem, a router, a gateway, a wired network adapter, a wireless network adapter, a Bluetooth adapter, an infrared adapter, a near-field communication (“NFC”) adapter, or a cellular network chip.

[0108] As depicted in Fig. 13B, system 1300B can also communicatively couple with (e.g., via I/O 1314 or NIC 1316) a quantum computing device 1326. In some embodiments, system 1300B can be a classical computer (e.g., a desktop computer, a laptop computer, or a tablet computer) that is independent from quantum computing device 1326. In some embodiments, system 1300B can include classical computing devices (e.g., processor 1308, memory 1310, I/O 1314, NIC 1316, or database 1322) and quantum computing devices (e.g., including quantum computing device 1326). Quantum computing device 1326 can include any number of any type of quantum circuits (that include quantum gates) for operating on qubits as well as peripheral devices (e.g., cryostats, laser generators, electric oscillators) for maintaining and supporting the quantum circuits. In some embodiments, quantum computing device 1326 can include hardware components functioning as a quantum data plane for preparing and storing qubits, a control and measurement plane for executing operations on the qubits and measuring the resulting qubits, and a control processor plane for determining

the sequence of operations and measurements based on an algorithm or measurement outcomes. When system 1300B is a classical computer, it can assist quantum computing device 1326 for network access (e.g., via NIC 1316), large storages (e.g., using database 1316), and user interactions (e.g., via I/O 1314).

[0109] Consistent with some embodiments of this disclosure, **Fig. 13C** is a schematic diagram illustrating an example quantum controller 1328 for operating (e.g., controlling qubits for computation, controlling qubits for compiling, or any manipulation of qubit) quantum circuits (e.g., quantum circuit 1330, as shown). Quantum circuit 1330 can include one or more qubits. In the non-limiting example depicted in Fig. 13C, quantum circuit 1330 can include qubits 1332 and 1334. For example, qubits 1332 and 1334 can be fluxonium qubits. To continue this example, each of qubits 1332 and 1334 can be implemented using a Josephson junction (e.g., Josephson junction 1336 or 1338) shunted by a capacitor (e.g., capacitor 1340 or 1342) and an inductor (e.g., inductor 1344 or 1346). Each of inductors 1344 and 1346 can be realized by an array of Josephson junctions (not shown in **Fig. 13C**). Each of qubits 1332 and 1334 can be constructed to operate at a local minimum in frequency with regards to a biasing magnetic flux. In this non-limiting example, qubits 1332 and 1334 can be coupled using a capacitor 1348, implementing transverse resonant coupling (e.g., charge-coupled, or the like) between qubits 1332 and 1334. Such coupling can require alignment of the qubit frequencies. When quantum circuit 1330 is not in operation, qubits 1332 and 1334 can be maintained as different frequencies.

[0110] In some embodiments, quantum circuit 1330 can be realized using a chip containing qubits 1332 and 1334 as well as their coupling in between. In some embodiments, quantum circuit 1330 can be implemented as a chip in quantum computing device 1326 in **Fig. 13B**.

[0111] In some embodiments, the chip can include one or more couplings to a quantum controller 1328. Quantum controller 1328 can be a digital computing device (e.g., a computing device including a central processing unit, graphical processing unit, application specific integrated circuit, field-programmable gate array, or other suitable processor). Quantum controller 1328 can configure quantum circuit 1330 for computation (e.g., by manipulating qubits 1332 and 1334), provide computational gates, or read state information out of quantum circuit 1330.

[0112] Consistent with some embodiments of this disclosure, quantum controller 1328 can configure quantum circuit 1330 by enabling a gate operation to be performed on one or more qubits of circuit quantum 1330 (e.g., including qubits 1332 and 1334). In some embodiments, quantum circuit 1330 can be configured by providing one or more bias drives to move two qubits into resonance. Quantum controller 1328 can provide the one or more bias drives directly to circuit 1330, or can provide instructions to a bias drive source (e.g., waveform generator or the like), causing the bias drive source to provide the bias drives to circuit 1330. In some embodiments, providing the bias drive can include passing a current through a coil external to circuit 1330. In various embodiments, providing the bias drive can include passing a current through a coil on the chip. The disclosed embodiments are not limited to a particular method of providing the bias drive or a particular method of biasing the qubits.

[0113] Consistent with some embodiments of this disclosure, quantum controller 1328 can implement computational gates on circuit 1330. Quantum controller 1328 can implement such gates by providing one or more computational drives to corresponding qubits in circuit 1330, or by providing instructions to a computation drive source (e.g., a waveform generator or the like), causing the computational drive source to provide the one or more computational drives to circuit 1330. Such computational drives can include microwave drives. The

computational drives can include sinusoidal waves, square waves, pulse trains, or other quantum gate drives having parameters selected by the quantum controller 1328 to implement quantum gates on the qubits. The one or more computational drives can be provided to the corresponding qubits using one or more coils coupled to the corresponding qubits. The coils can be external to circuit 1330 or on a chip containing circuit 1330.

[0114] Consistent with some embodiments of this disclosure, quantum controller 1328 can be configured to determine state information for quantum circuit 1330. In some embodiments, quantum controller 1328 can measure a state of one or more qubits of circuit 1330. The state can be measured upon completion of a sequence of one or more quantum operations. In some embodiments, quantum controller 1328 can provide a probe signal (e.g., a microwave probe tone) to a coupled resonator of circuit 1330, or provide instructions to a readout device (e.g., an arbitrary waveform generator) that provides the probe signal. In various embodiments, quantum controller 1328 can include, or be configured to receive information from, a detector configured to determine an amplitude and phase of an output signal received from the coupled resonator in response to provision of the microwave probe tone. The amplitude and phase of the output signal can be used to determine the state of the probed qubit(s). The disclosed embodiments are not limited to any particular method of measuring the state of the qubits.

[0115] The disclosed embodiments are not limited to embodiments in which quantum controller 1328 controls only a single quantum circuit. In some embodiments, quantum controller 1328 can control multiple quantum circuits (which can be identical in implementation or can differ in implementation). For example, quantum controller 1328 can control a first, transmon-qubit-based quantum circuit and a second, fluxonium-qubit-based quantum circuit. In some embodiments, quantum controller 1328 can be capable of independently controlling the multiple quantum circuits. In some instances, for example, each

of the multiple quantum circuits can be performing different, contemporaneous computations. In various instances, the multiple quantum circuit can be involved in the same computation (e.g., parallel computations, or the like).

[0116] Consistent with some embodiments of this disclosure, quantum controller 1328 can configure quantum circuit 1330, and can provide computational gates to circuit 1330, based at least in part on the obtained state information. In some embodiments, quantum controller 1328 can be included as part of computing device 1326 in **Fig. 13B**.

[0117] **Fig. 14** is a schematic diagram illustrating a superconducting device 1400, consistent with some embodiments of this disclosure. In some embodiments, the magnetic flux of superconducting device 1400 can be controllable. As shown in **Fig. 14**, superconducting device 1400 can include a first Josephson junction 1402 of a first type connected in parallel to a plurality of second Josephson junctions 1404 a second type. Second Josephson junctions 1404 are connected in series. By way of example, first Josephson junction 1402 and second Josephson junctions 1404 can be generated by performing at least one of methods 600, 700, 900, or 1000 described in association with **Figs. 6-7** and **Figs. 9-10**.

[0118] Consistent with some embodiments of this disclosure, a non-transitory computer-readable storage medium for storing computer software instructions used by an apparatus is provided herein. The non-transitory computer-readable storage medium can include programs for performing a method for preparing a Josephson junction or process disclosed herein (e.g., methods 600, 700, 900, or 1000 described in association with **Figs. 6-7** and **Figs. 9-10**).

[0119] The embodiments can further be described using the following clauses:

1. A method for preparing a Josephson junction, the method comprising:
obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second

Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

2. The method of clause 1, wherein the junction area of the first Josephson junction is smaller than or equal to a preset area, and the junction area of the at least one of the plurality of second Josephson junctions is greater than the preset area.

3. The method of any of clauses 1-2, wherein obtaining the first pattern structure for generating the first Josephson junction of the first type and the plurality of second pattern

structures for generating the plurality of second Josephson junctions of the second type comprises:

obtaining a mask plate for preparing a wafer-level Josephson junction, the mask plate comprising a first mask region for preparing the first Josephson junction and a plurality of second mask regions for preparing the plurality of second Josephson junctions; and

obtaining the first pattern structure through the first mask region, and obtaining the plurality of second pattern structures through the plurality of second mask regions.

4. The method of clause 3, wherein obtaining the first pattern structure through the first mask region, and obtaining the plurality of second pattern structures through the plurality of second mask regions comprises:

obtaining a substrate structure;

forming a photoresist layer on the substrate structure; and

performing etching on the photoresist layer through the mask plate to obtain the first pattern structure and the plurality of second pattern structures.

5. The method of clause 4, wherein the photoresist layer comprises an upper photoresist layer and a lower photoresist layer.

6. The method of clause 5, wherein thickness of the upper photoresist layer is greater than thickness of the lower photoresist layer.

7. The method of any of clauses 1-6, further comprising:

obtaining an electrical parameter for defining the first Josephson junction; and

determining a junction area of the first Josephson junction based on the electrical parameter.

8. The method of clause 7, wherein the electrical parameter comprises at least one of electromagnetic field energy density, capacitance, or inductance.

9. The method of any of clauses 1-8, further comprising:

obtaining an evaporation angle for preparing the plurality of second Josephson junctions, wherein the evaporation angle corresponds to at least one of the first evaporation direction or the second evaporation direction; and

determining a designed junction area associated with the plurality of second Josephson junctions based on the evaporation angle.

10. The method of clause 9, wherein determining the designed junction area associated with the plurality of second Josephson junctions based on the evaporation angle comprises:

obtaining thickness information of a photoresist layer for preparing the plurality of second Josephson junctions; and

determining the designed junction area based on the thickness information and the evaporation angle, wherein the designed junction area is greater than or equal to a junction area of at least one of the plurality of second Josephson junctions.

11. The method of clause 10, wherein determining the designed junction area based on the thickness information and the evaporation angle comprises:

obtaining a cosine value corresponding to the evaporation angle;

determining a product value of the cosine value and the thickness information; and

determining the designed junction area based on the product value.

12. The method of any of clauses 9-11, wherein the evaporation angle comprises a first evaporation angle corresponding to the first evaporation direction or a second evaporation angle corresponding to the second evaporation direction.

13. The method of any of clauses 1-12, wherein an angle formed between the first evaporation direction and a gravity direction is greater than or equal to 10° , and less than or equal to 60° .

14. The method of any of clauses 1-13, wherein the first evaporation direction is perpendicular to the second evaporation direction.

15. The method of any of clauses 1-14, wherein the plurality of second Josephson junctions are connected in series, and the first Josephson junction is connected in parallel to the plurality of second Josephson junctions.

16. The method of any of clauses 1-15, wherein the material comprises at least one of aluminum, binary nitride, ternary nitride, or composite oxide.

17. An apparatus for preparing a Josephson junction, the apparatus comprising at least one circuitry configured for:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

causing the apparatus to evaporate a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

causing the apparatus to form an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

causing the apparatus to evaporate the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

causing the apparatus to form the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and to form the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

18. A device for preparing a Josephson junction, the device comprising:

at least one processor; and

a memory configured to store one or more computer instructions executable by the at least one processor to cause the device to perform:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is

substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

19. A superconducting circuit including a first Josephson junction of a first type connected in parallel to a plurality of second Josephson junctions of a second type, wherein the plurality of second Josephson junctions are connected in series, and wherein the first Josephson junction and the plurality of second Josephson junctions are generated by a method, the method comprising:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode

layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

20. The superconducting circuit of clause 19, wherein a magnetic flux of the superconducting circuit is controllable.

[0120] It should be noted that the example apparatuses and devices described herein are only schematic, where the units described as separate components can or cannot be physically separated, and the components displayed as units can or cannot be physical units (e.g., can be located in one place, or can be distributed to a plurality of network units). Part or all of the modules can be selected in accordance with actual needs to achieve the purpose of the solution of the present embodiment. Those of ordinary skill in the art can understand and implement the solution of the present embodiment without creative effort.

[0121] From the description of the above implementations, those skilled in the art can clearly understand that the various implementations can be implemented by means of software plus a necessary hardware platform, and can also be implemented by a combination of hardware and software. Based on such understanding, the above technical solution essentially or the part contributing to the prior art can be embodied in the form of a computer product. The present disclosure can be in the form of a computer program product implemented on one or more computer-usable storage media (including, but not limited to, a

magnetic disk memory, a CD-ROM, an optical memory, and the like) including computer usable program code.

[0122] The present disclosure is described with reference to flowcharts or block diagrams of methods, devices, systems, and computer program products in accordance with embodiments of the present disclosure. It should be understood that each flow or block in the flowcharts or block diagrams and a combination of flows or blocks in the flowcharts or block diagrams can be implemented by computer program instructions. These computer program instructions can be provided to a processor of a general-purpose computer, a special-purpose computer, an embedded processor, or another programmable device to produce a machine, so that the instructions executed by the processor of the computer or another programmable device produce an apparatus for realizing the functions specified in one or more flows of the flowcharts or one or more blocks of the block diagrams.

[0123] These computer program instructions can also be stored in a non-transitory computer-readable memory that can direct a computer or another programmable device to work in a specific manner, so that the instructions stored in this computer-readable memory produce an article of manufacture including an instruction apparatus which implements the functions specified in one or more flows of the flowcharts or one or more blocks of the block diagrams.

[0124] These computer program instructions can also be loaded onto a computer or another programmable device, so that a series of operation steps are performed on the computer or another programmable device to produce computer-implemented processing, so that the instructions executed on the computer or another programmable device provide steps for implementing the functions specified in one or more flows of the flowcharts or one or more blocks of the block diagrams.

[0125] In a typical configuration, the computing device includes one or more processors (CPUs), an input/output interface, a network interface, and a memory. The memory can include a volatile memory, a random access memory (RAM), or a non-volatile memory in computer-readable media, e.g., a read-only memory (ROM) or a flash RAM. The memory is an example of the computer-readable medium.

[0126] The non-transitory computer-readable medium can include permanent or non-permanent, removable or non-removable media, which can implement storage of information by using any method or technology. The information can be computer-readable instructions, data patterns, program modules, or other data. Examples of computer storage media include, but are not limited to, a phase change memory (PRAM), a static random access memory (SRAM), a dynamic random access memory (DRAM), other type of random access memory (RAM), a read-only memory (ROM), an electrically erasable programmable read-only memory (EEPROM), a flash memory or other memory technologies, a compact disc read-only memory (CD-ROM), a digital versatile disc (DVD) or other optical storage, a cassette magnetic tape, tape and disk storage or other magnetic storage devices, or any other non-transmission media, which can be configured to store information accessible by a computing device. As defined herein, the non-transitory computer-readable medium does not include computer-readable transitory media, such as a modulated data signal and a carrier.

[0127] Finally, it should be noted that the above embodiments are only used to illustrate the technical solutions of the present disclosure, and are not intended to limit the present disclosure. Although the present disclosure has been described in detail with reference to the foregoing embodiments, those of ordinary skill in the art should understand that the technical solutions recorded in the foregoing various embodiments can still be modified, or some of the technical features thereof can be equivalently replaced. These modifications or replacements

do not cause the essence of the corresponding technical solutions to deviate from the spirit and scope of the technical solutions of the embodiments of the present disclosure.

WHAT IS CLAIMED IS:

1. A method for preparing a Josephson junction, the method comprising:
 - obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;
 - evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;
 - forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;
 - evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and
 - forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

2. The method of claim 1, wherein the junction area of the first Josephson junction is smaller than or equal to a preset area, and the junction area of the at least one of the plurality of second Josephson junctions is greater than the preset area.
3. The method of claim 1, wherein obtaining the first pattern structure for generating the first Josephson junction of the first type and the plurality of second pattern structures for generating the plurality of second Josephson junctions of the second type comprises:
 - obtaining a mask plate for preparing a wafer-level Josephson junction, the mask plate comprising a first mask region for preparing the first Josephson junction and a plurality of second mask regions for preparing the plurality of second Josephson junctions; and
 - obtaining the first pattern structure through the first mask region, and obtaining the plurality of second pattern structures through the plurality of second mask regions.
4. The method of claim 3, wherein obtaining the first pattern structure through the first mask region, and obtaining the plurality of second pattern structures through the plurality of second mask regions comprises:
 - obtaining a substrate structure;
 - forming a photoresist layer on the substrate structure; and
 - performing etching on the photoresist layer through the mask plate to obtain the first pattern structure and the plurality of second pattern structures.
5. The method of claim 4, wherein the photoresist layer comprises an upper photoresist layer and a lower photoresist layer.
6. The method of claim 5, wherein thickness of the upper photoresist layer is greater

than thickness of the lower photoresist layer.

7. The method of claim 1, further comprising:
 - obtaining an electrical parameter for defining the first Josephson junction; and
 - determining a junction area of the first Josephson junction based on the electrical parameter.
8. The method of claim 7, wherein the electrical parameter comprises at least one of electromagnetic field energy density, capacitance, or inductance.
9. The method of claim 1, further comprising:
 - obtaining an evaporation angle for preparing the plurality of second Josephson junctions, wherein the evaporation angle corresponds to at least one of the first evaporation direction or the second evaporation direction; and
 - determining a designed junction area associated with the plurality of second Josephson junctions based on the evaporation angle.
10. The method of claim 9, wherein determining the designed junction area associated with the plurality of second Josephson junctions based on the evaporation angle comprises:
 - obtaining thickness information of a photoresist layer for preparing the plurality of second Josephson junctions; and
 - determining the designed junction area based on the thickness information and the evaporation angle, wherein the designed junction area is greater than or equal to a junction area of at least one of the plurality of second Josephson junctions.

11. The method of claim 10, wherein determining the designed junction area based on the thickness information and the evaporation angle comprises:

- obtaining a cosine value corresponding to the evaporation angle;
- determining a product value of the cosine value and the thickness information; and
- determining the designed junction area based on the product value.

12. The method of claim 9, wherein the evaporation angle comprises a first evaporation angle corresponding to the first evaporation direction or a second evaporation angle corresponding to the second evaporation direction.

13. The method of claim 1, wherein an angle formed between the first evaporation direction and a gravity direction is greater than or equal to 10° , and less than or equal to 60° .

14. The method of claim 1, wherein the first evaporation direction is perpendicular to the second evaporation direction.

15. The method of claim 1, wherein the plurality of second Josephson junctions are connected in series, and the first Josephson junction is connected in parallel to the plurality of second Josephson junctions.

16. The method of claim 1, wherein the material comprises at least one of aluminum, binary nitride, ternary nitride, or composite oxide.

17. An apparatus for preparing a Josephson junction, the apparatus comprising at least one circuitry configured for:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

causing the apparatus to evaporate a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

causing the apparatus to form an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

causing the apparatus to evaporate the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

causing the apparatus to form the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and to form the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

18. A device for preparing a Josephson junction, the device comprising:
at least one processor; and

a memory configured to store a set of instructions that are executable by the at least one processor to cause the device to perform:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

19. A superconducting circuit including a first Josephson junction of a first type connected in parallel to a plurality of second Josephson junctions of a second type, wherein the plurality of second Josephson junctions are connected in series, and wherein the first Josephson junction and the plurality of second Josephson junctions are generated by a method, the method comprising:

obtaining a first pattern structure for generating a first Josephson junction of a first type and a plurality of second pattern structures for generating a plurality of second Josephson junctions of a second type, wherein a junction area of the first Josephson junction is different from a junction area of at least one of the plurality of second Josephson junctions;

evaporating a material on the first pattern structure and the plurality of second pattern structures based on a first evaporation direction to generate a first electrode layer for implementing information transmission, wherein the first evaporation direction is substantially parallel to an edge of the first pattern structure and an edge of at least one of the plurality of second pattern structures;

forming an insulating layer on the first electrode layer, the insulating layer comprising a compound corresponding to the material;

evaporating the material on the first pattern structure and the plurality of second pattern structures based on a second evaporation direction to generate a second electrode layer for implementing information transmission, wherein the second evaporation direction is substantially parallel to the edge of the first pattern structure and the edge of the at least one of the plurality of second pattern structures; and

forming the first Josephson junction based on the first electrode layer generated on the first pattern structure, the insulating layer, and the second electrode layer generated on the first pattern structure, and forming the plurality of second Josephson junctions based on the

first electrode layer generated on the plurality of second pattern structures, the insulating layer, and the second electrode layer generated on the plurality of second pattern structures.

20. The superconducting circuit of claim 19, wherein a magnetic flux of the superconducting circuit is controllable.

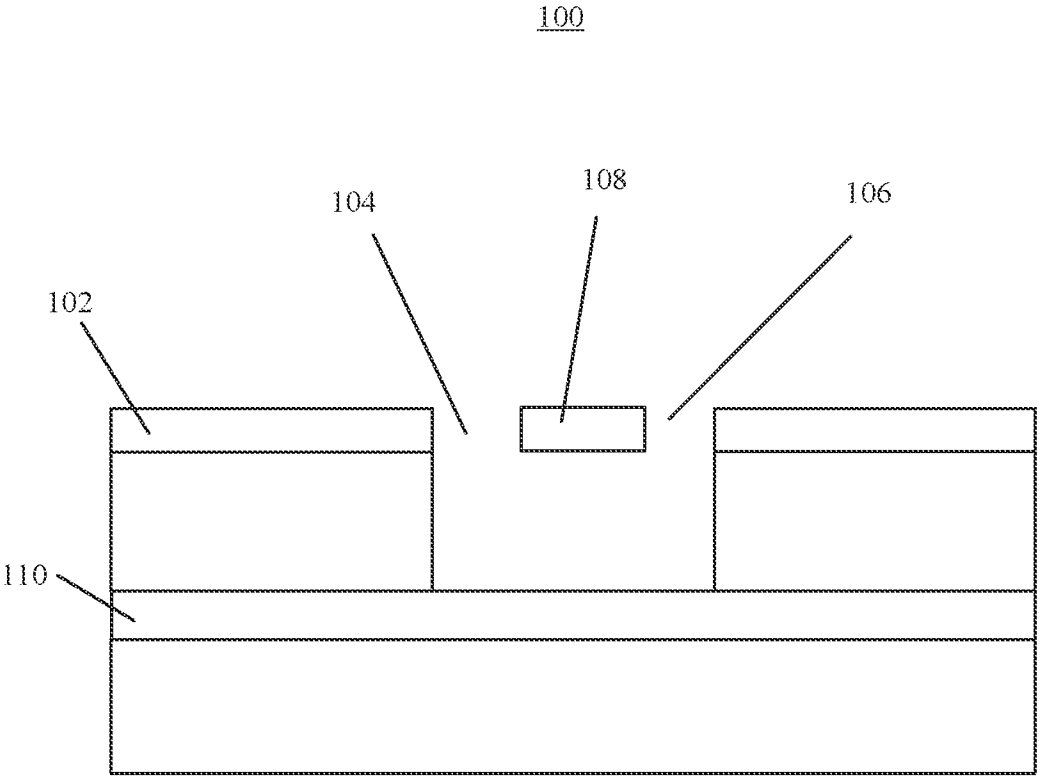


FIG. 1

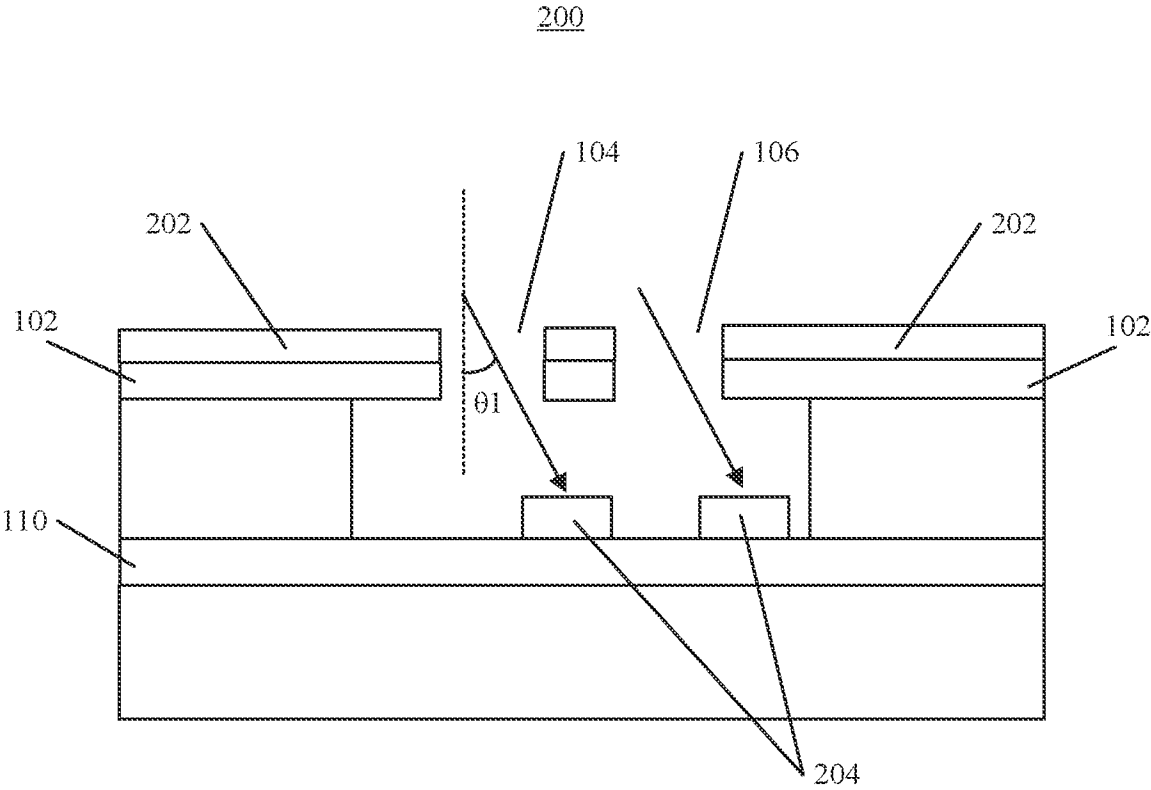


FIG. 2

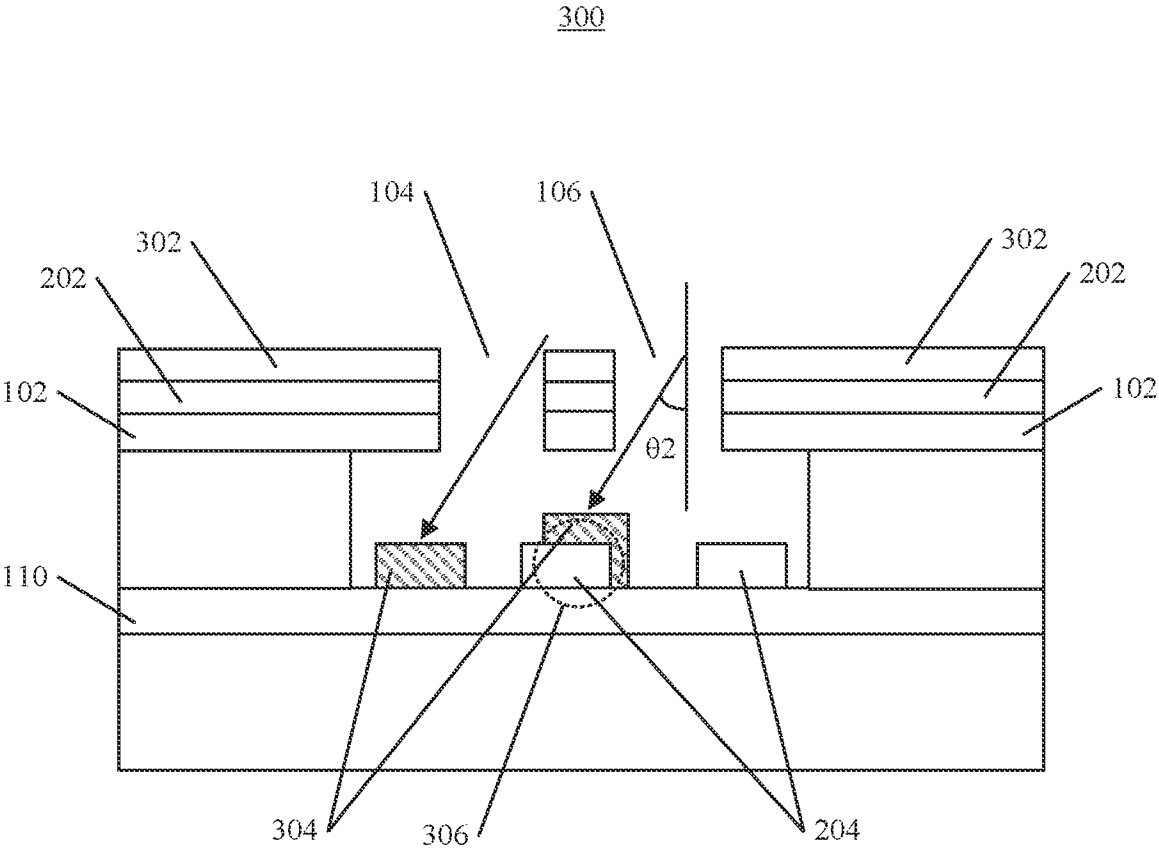


FIG. 3

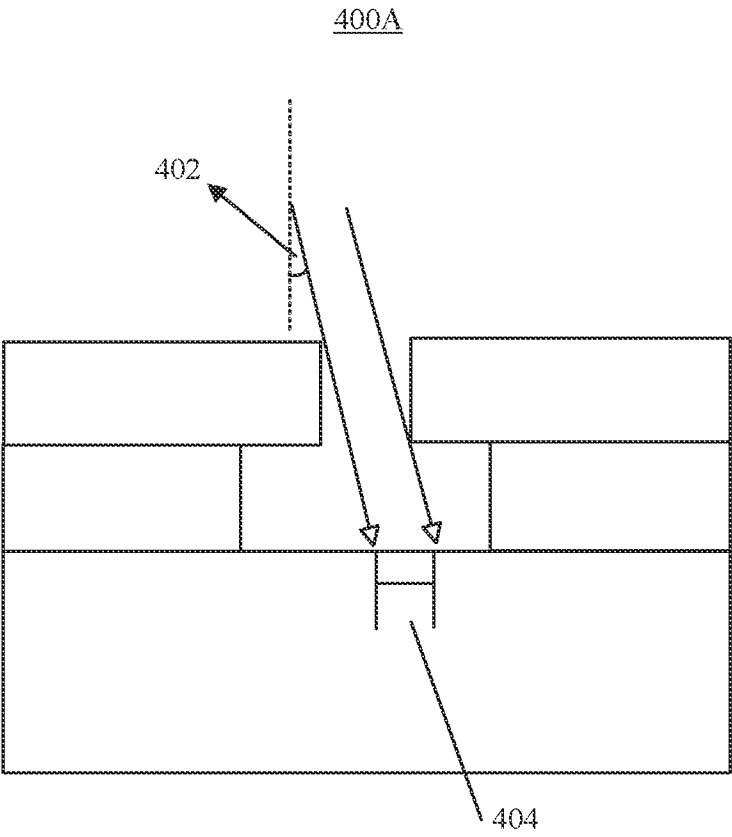


FIG. 4A

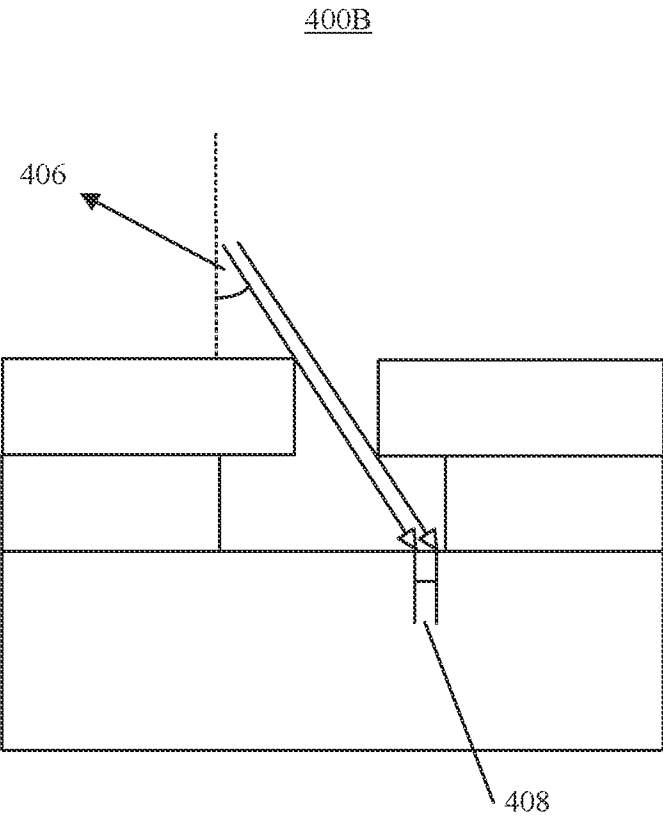


FIG. 4B

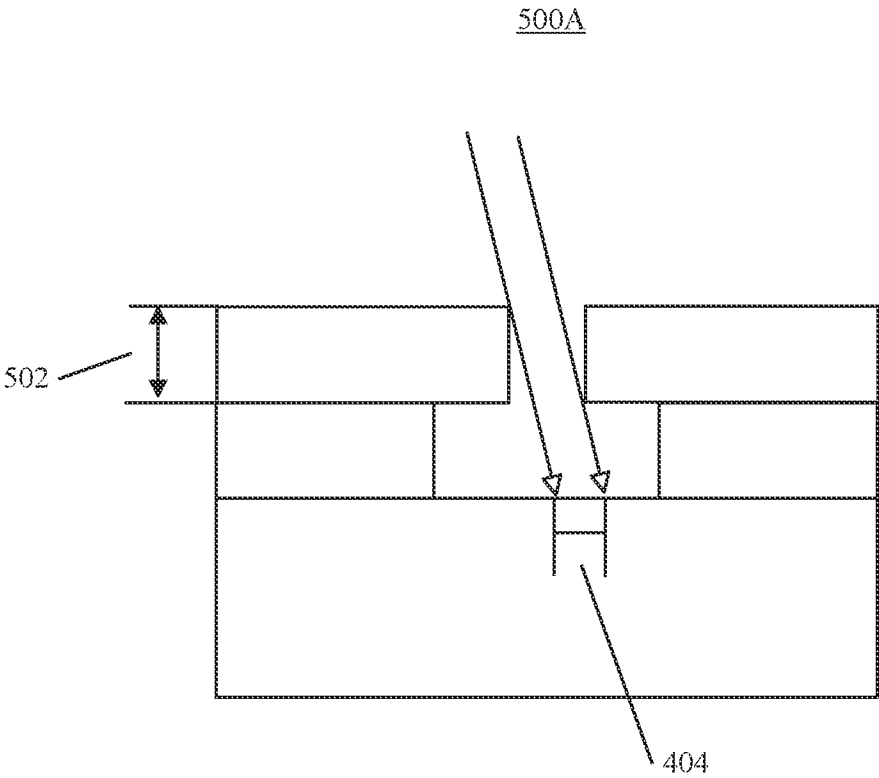


FIG. 5A

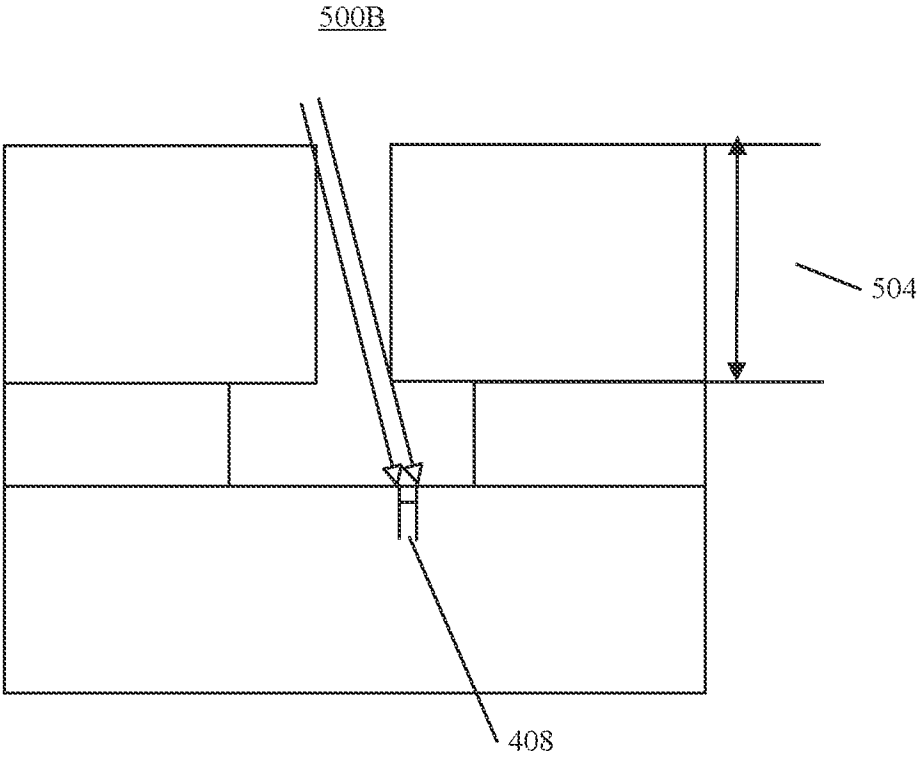
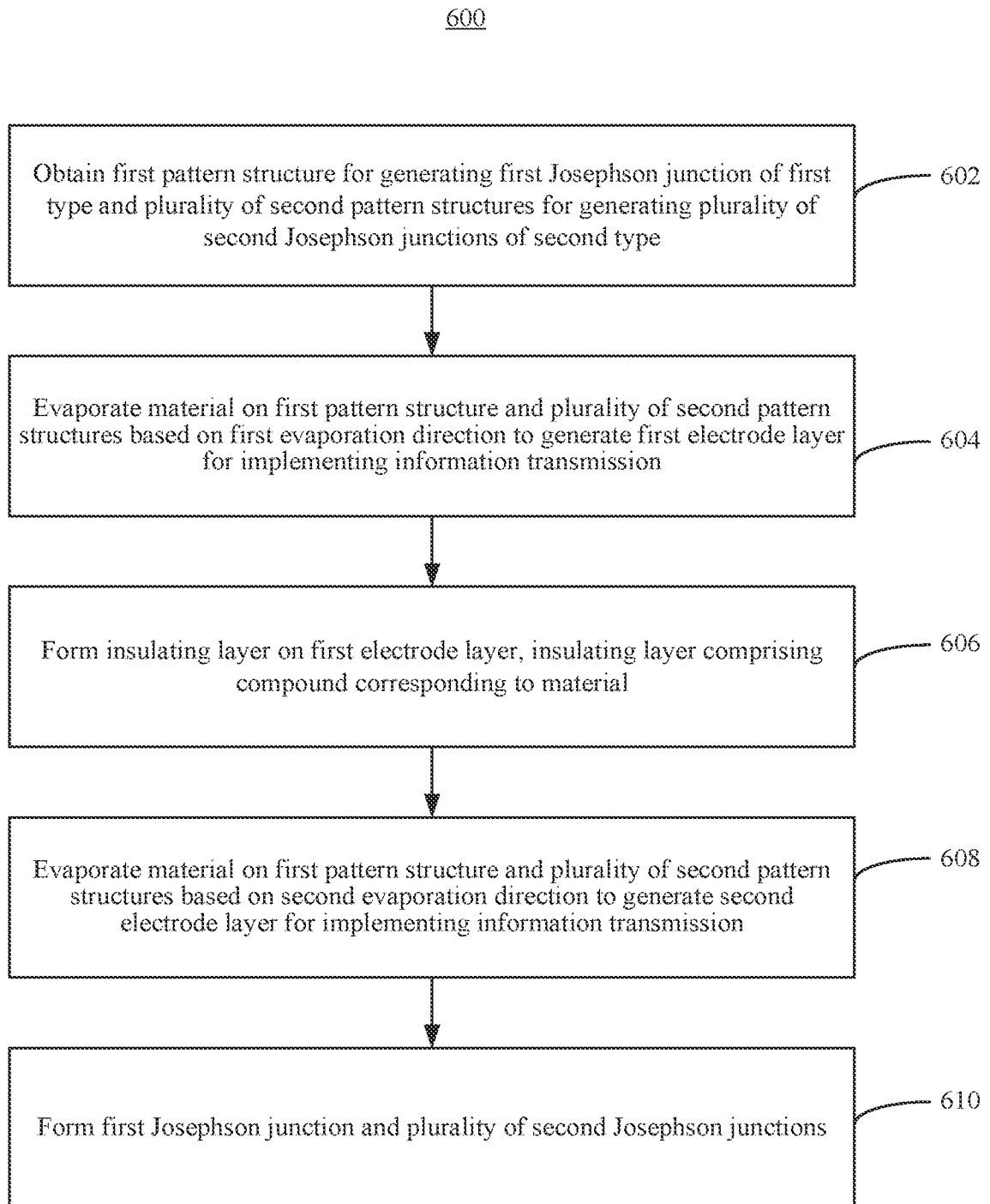


FIG. 5B

**FIG. 6**

700

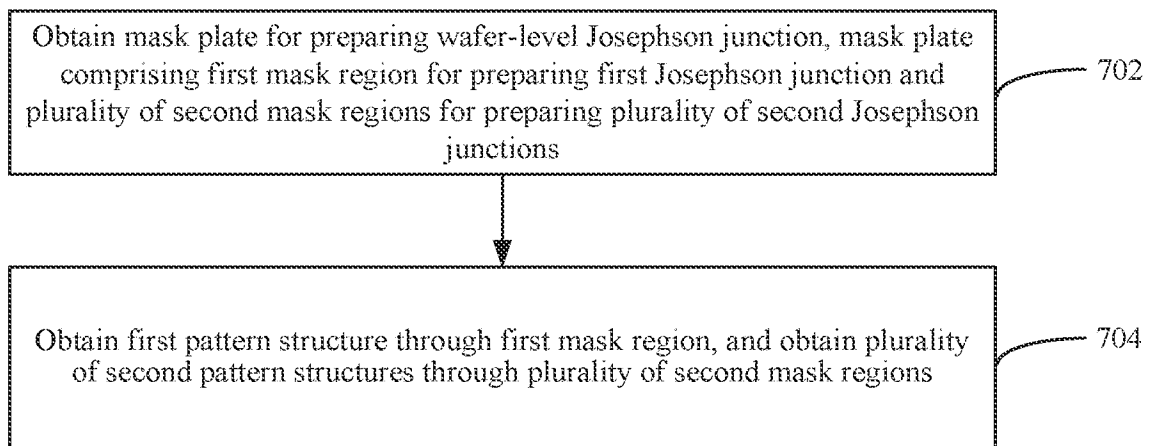


FIG. 7

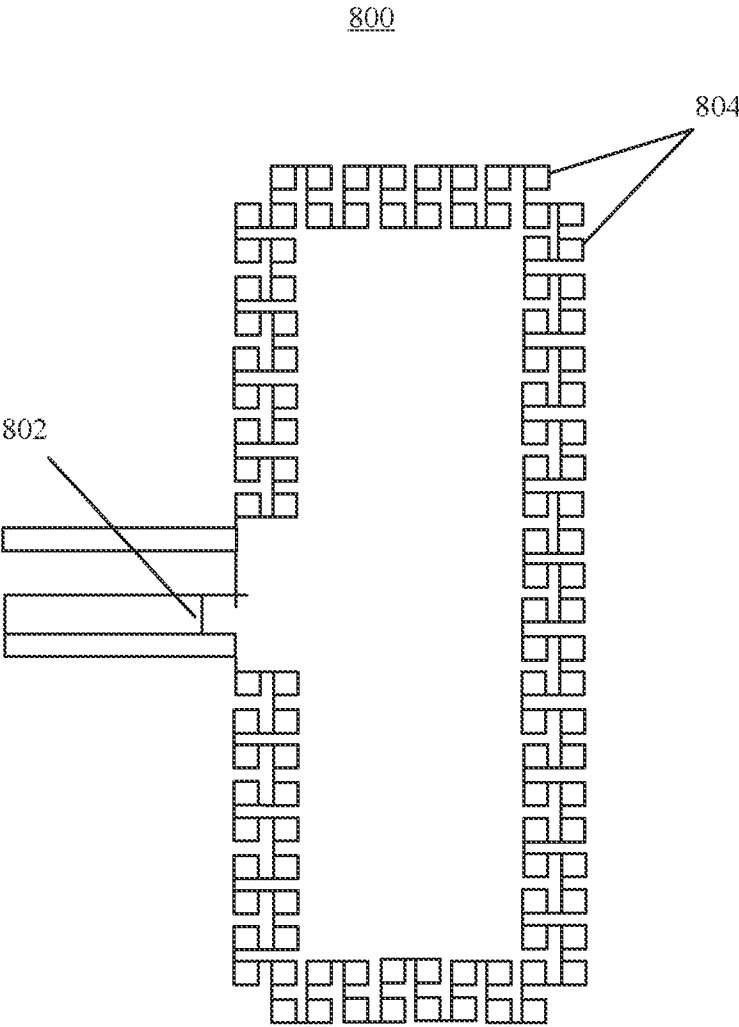
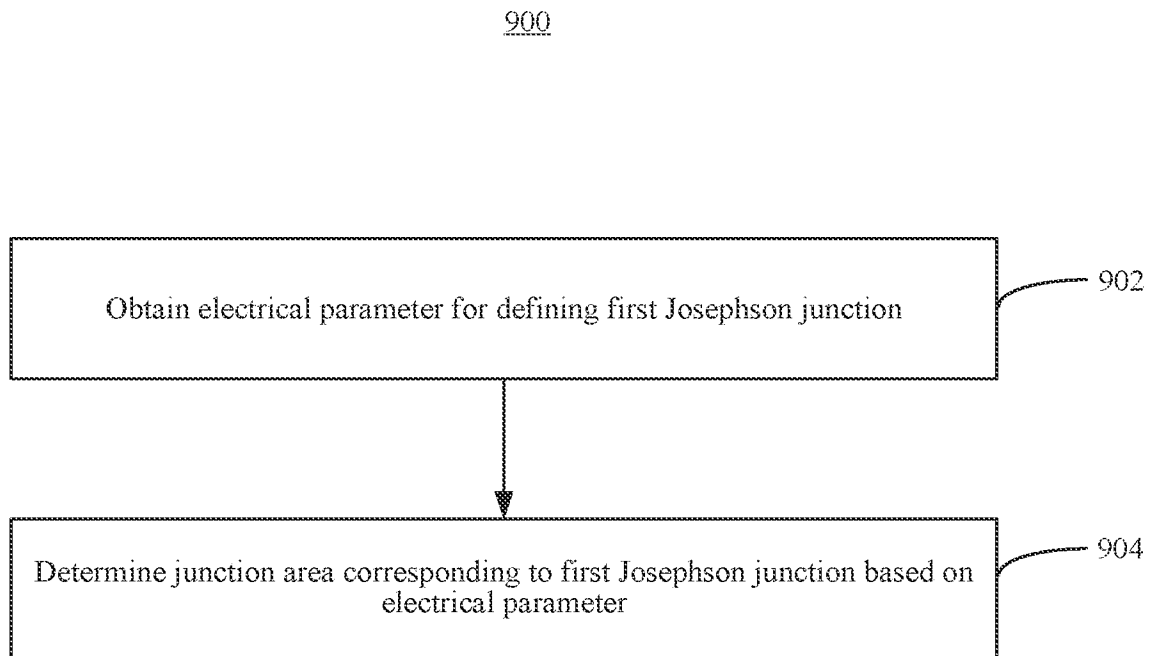
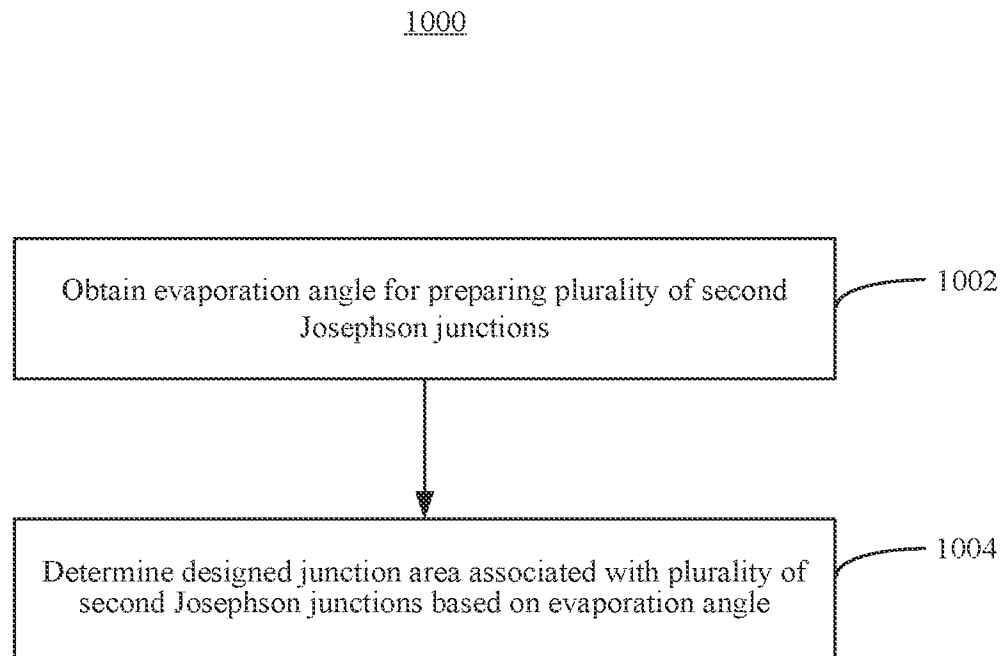


FIG. 8

**FIG. 9**

**FIG. 10**

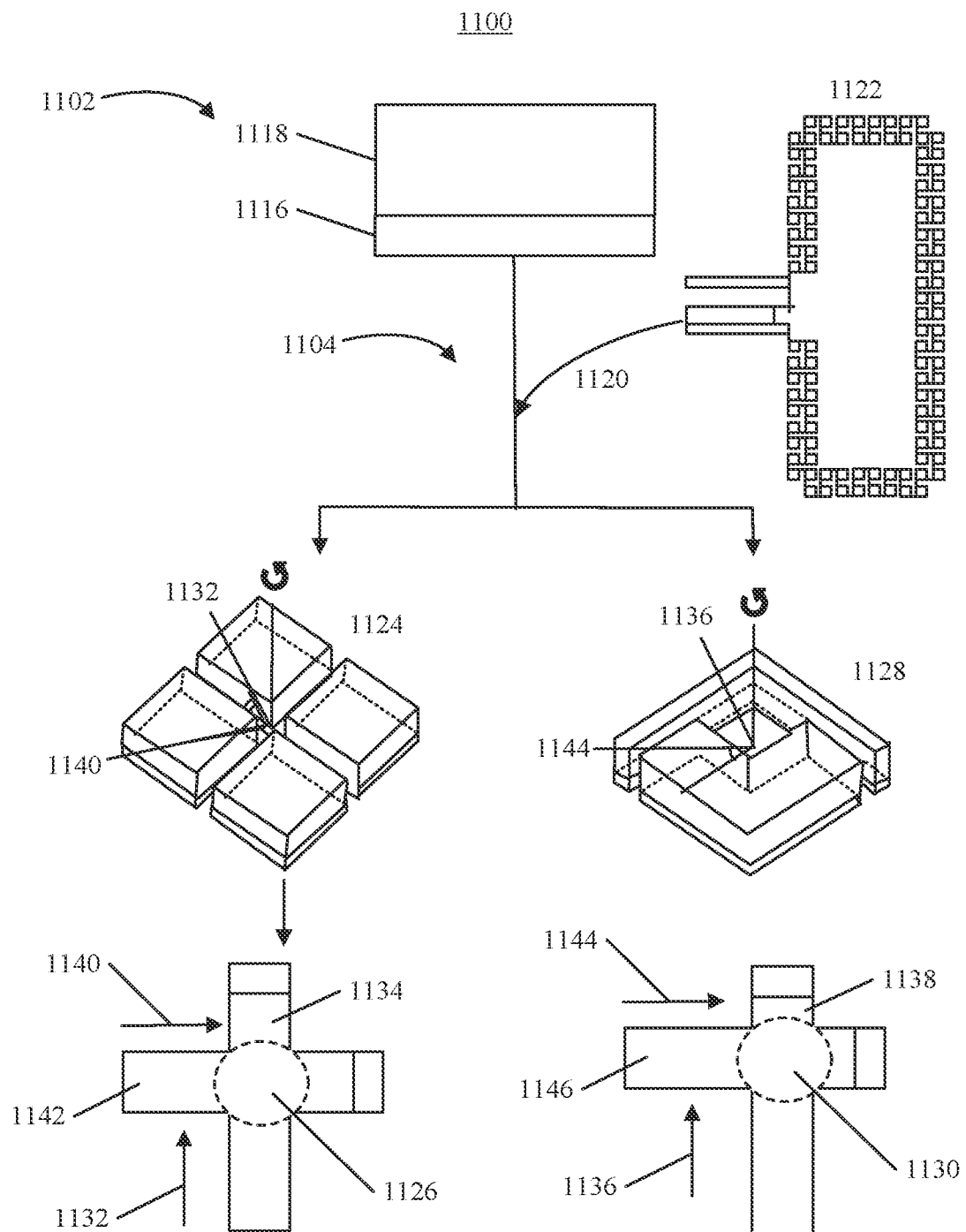
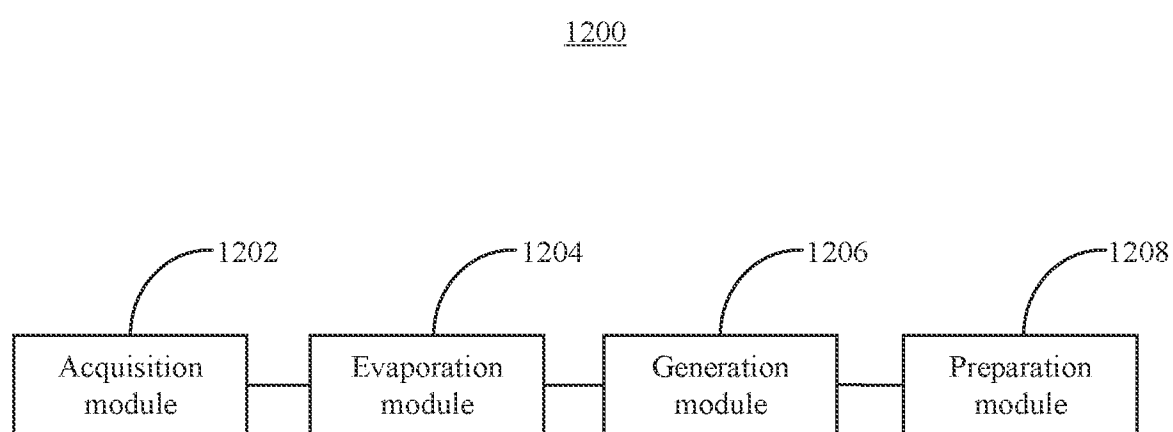
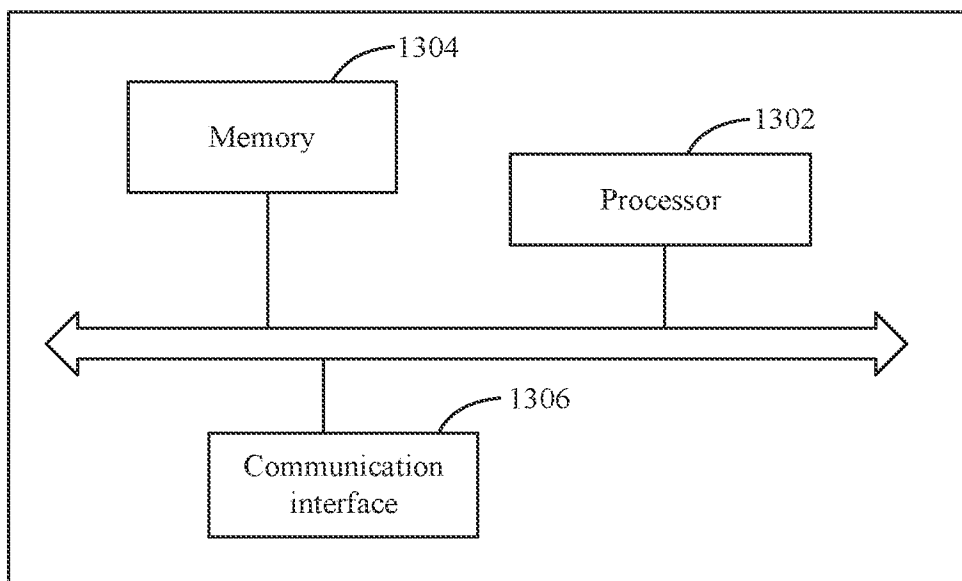
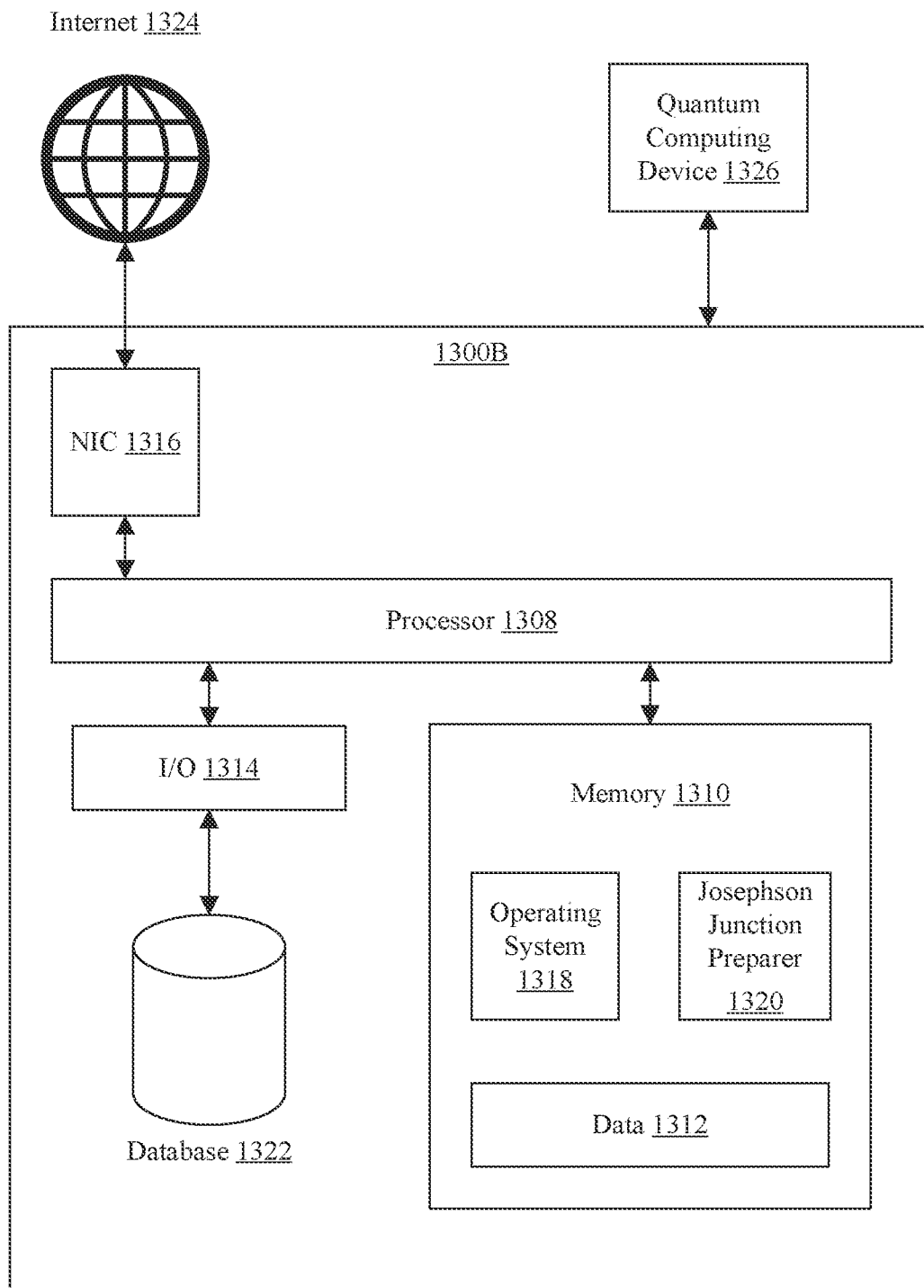


FIG. 11

**FIG. 12**

1300A**FIG. 13A**

**FIG. 13B**

1300C

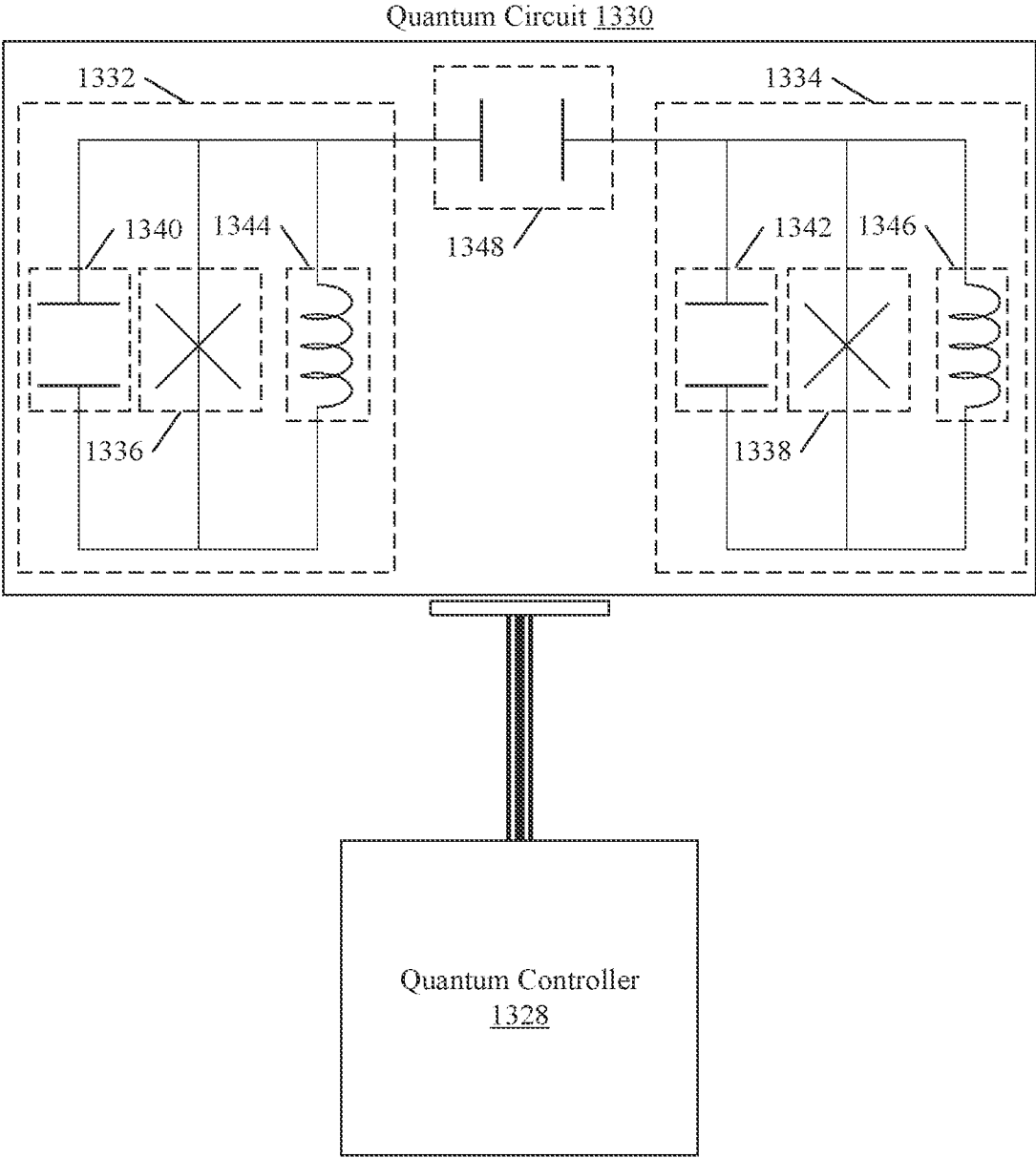


FIG. 13C

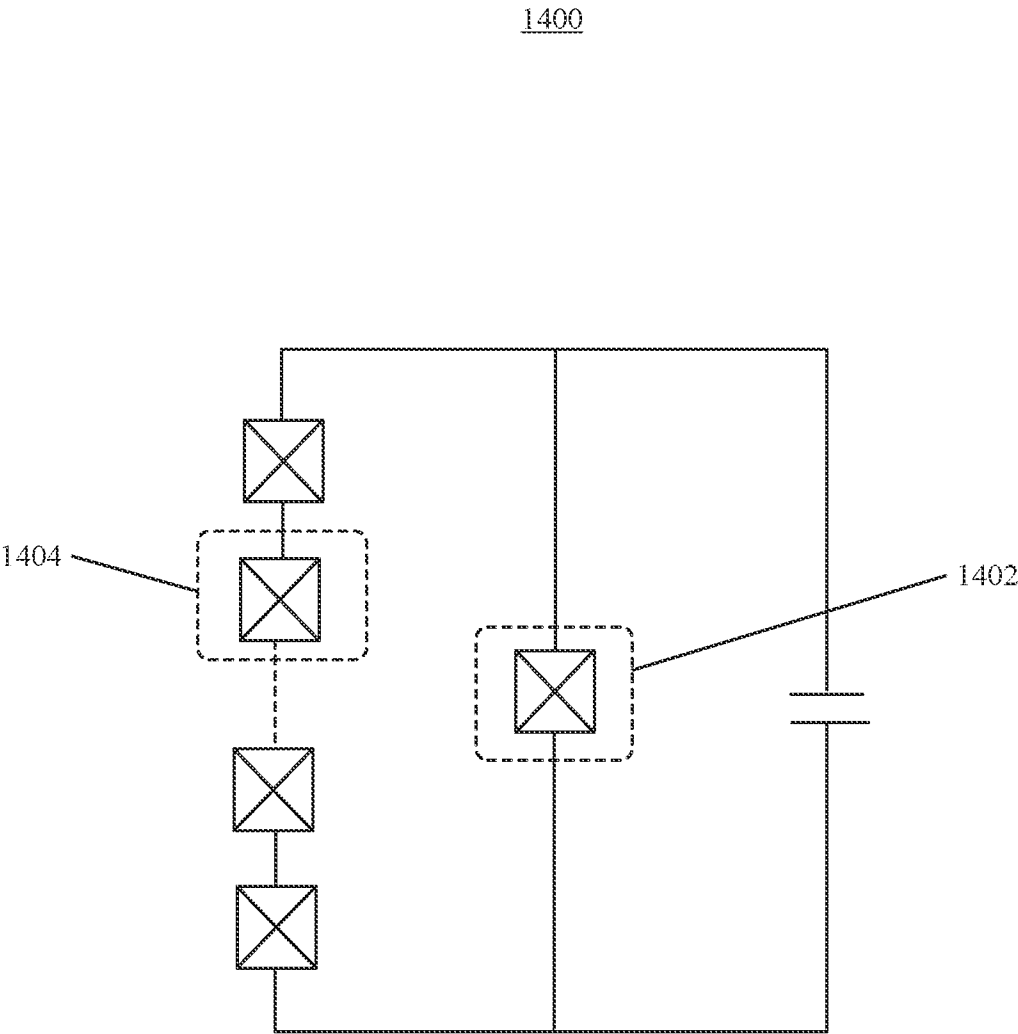


FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US 21/55996

A. CLASSIFICATION OF SUBJECT MATTER

IPC - H01L 39/22 (2021.01)

CPC - H01L 39/2493; H01L 39/025; H01L 39/223

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

See Search History document

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

See Search History document

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

See Search History document

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4,370,359 A (FETTER et al.) 25 January 1983 (25.01.1983) Fig 1, abstract, col 3, ln 7-58, col 5, ln 58-59, col 7, ln 1-31	1-20
A	US 2007/0158791 A1 (WAKANA et al.) 12 July 2007 (12.07.2007) Fig 12, 17, abstract, para [0054], [0087], [0112]	1-20
A	US 2020/0168782 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 28 May 2020 (28.05.2020) Fig 14, abstract, para [0102]-[0106]	1-20
X, P	CN 113257989 A (ALIBABA GROUP HOLDING LTD) 13 August 2021 (13.08.2021) abstract	1-20

☐ Further documents are listed in the continuation of Box C.☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

16 December 2021

Date of mailing of the international search report

JAN 26 2022

Name and mailing address of the ISA/US

Mail Stop PCT, Attn: ISA/US, Commissioner for Patents
P.O. Box 1450, Alexandria, Virginia 22313-1450

Facsimile No. 571-273-8300

Authorized officer

Kari Rodriguez

Telephone No. PCT Helpdesk: 571-272-4300