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Other: EPODOC, WPI, INSPEC

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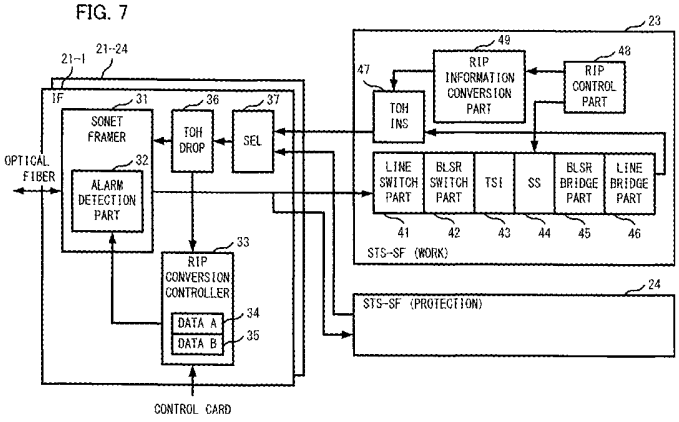
(54) Title of the Invention: **Node apparatus**
Abstract Title: **SONET/SDH network element with ring cross connection with path selection in switch fabric and alarm detection/setting in interface card**

(57) A SONET/SDH ring network element comprises interface cards 21-1/4 and work/protection switching fabrics 23/24. Input signals are fed through framer 31 which detects 31 alarm conditions on the line in the line card. They then pass through switching section 41-46 and transport overhead TOH inserter 47 and back to the line card.
The service selector decides which of work/protection inputs to forward to the output based upon alarm/quality information. Depending upon the selection made routing information protocol (RIP) data is adjusted 49 and inserted in the TOH.
Back in the line card selection between work and protection fabrics 37 is performed and the TOH drop function feeds RIP data to controller 33. Depending upon the information supplied the controller 33 feeds alarm settings 34/35 to the alarm detector 32, which applies them to incoming signals.
The invention allows alarm detection to be offloaded from the switch fabric to the interface cards.

FIG. 7



GB 2465456 A

FIG. 1A

RELATED ART

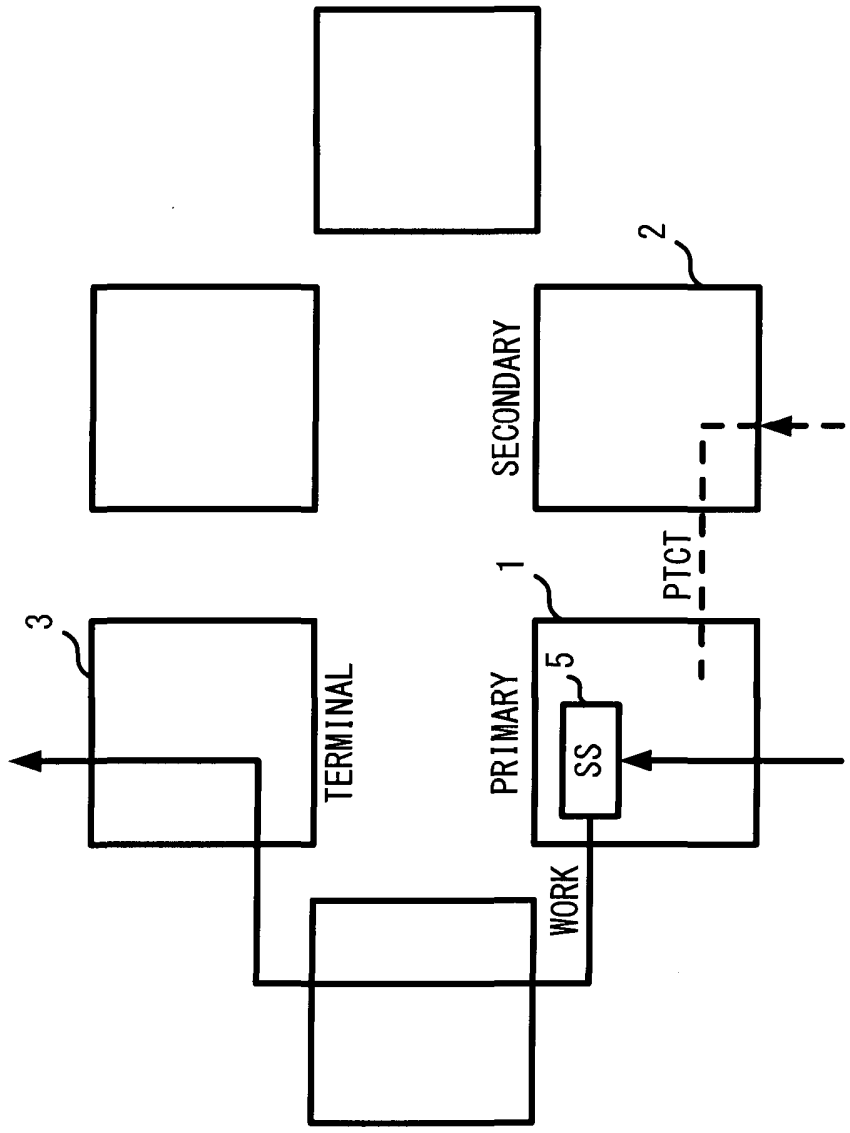
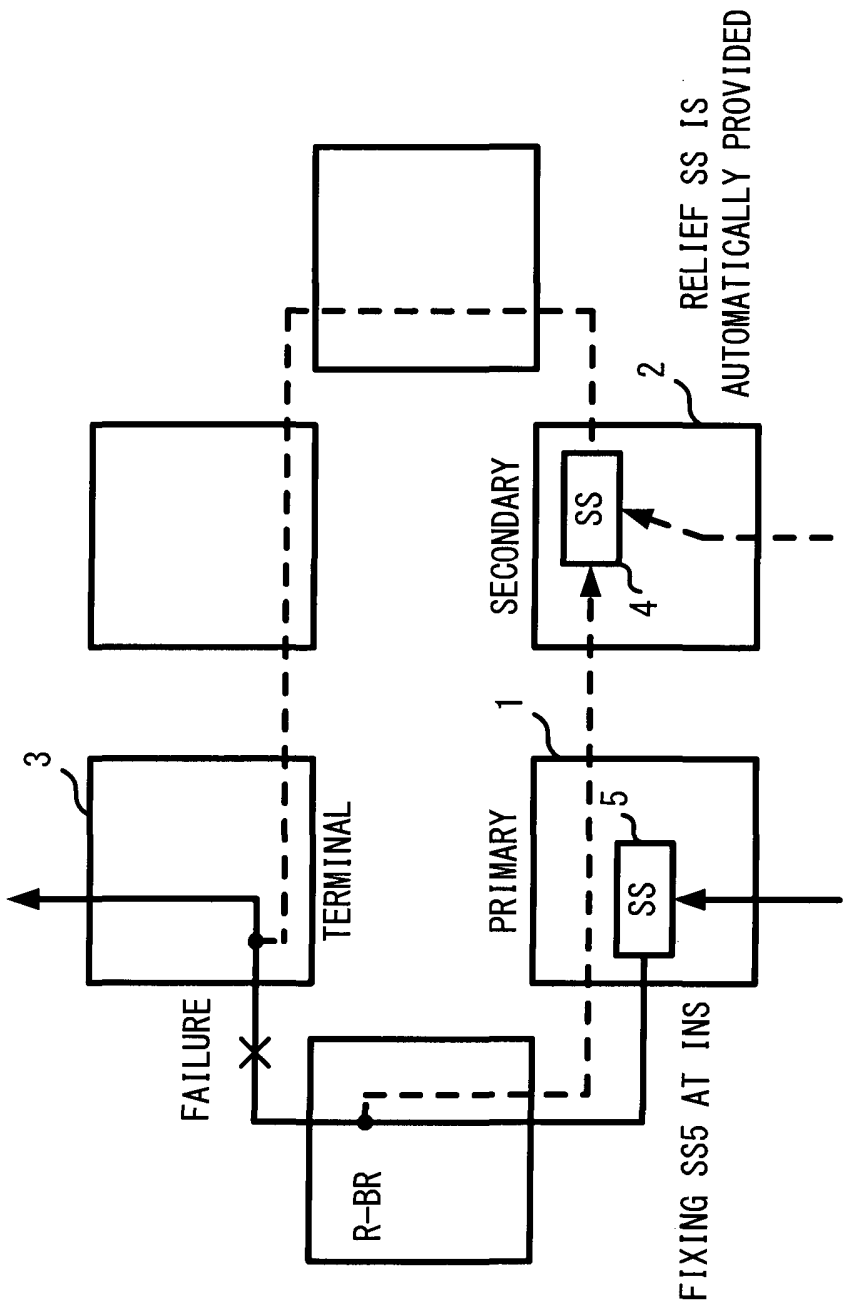


FIG. 1B

RELATED ART



RELATED ART

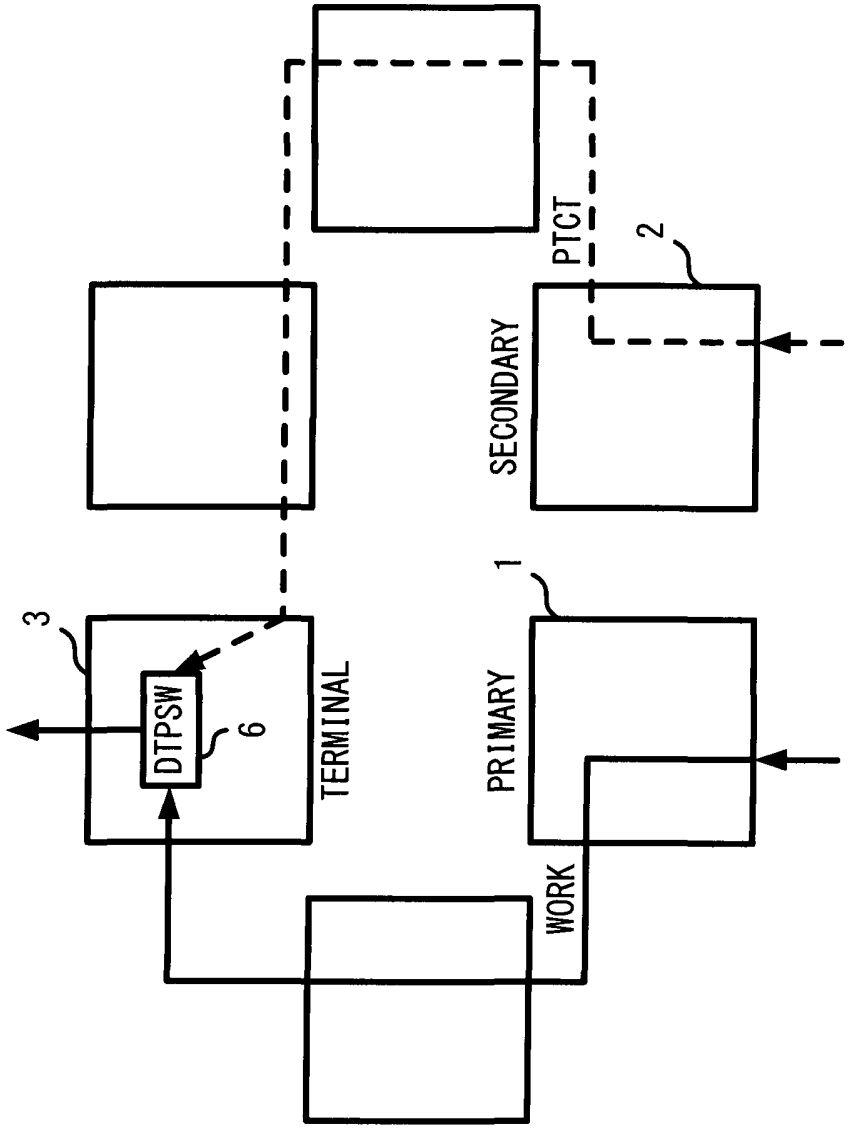


FIG. 2A

FIG. 2B

RELATED ART

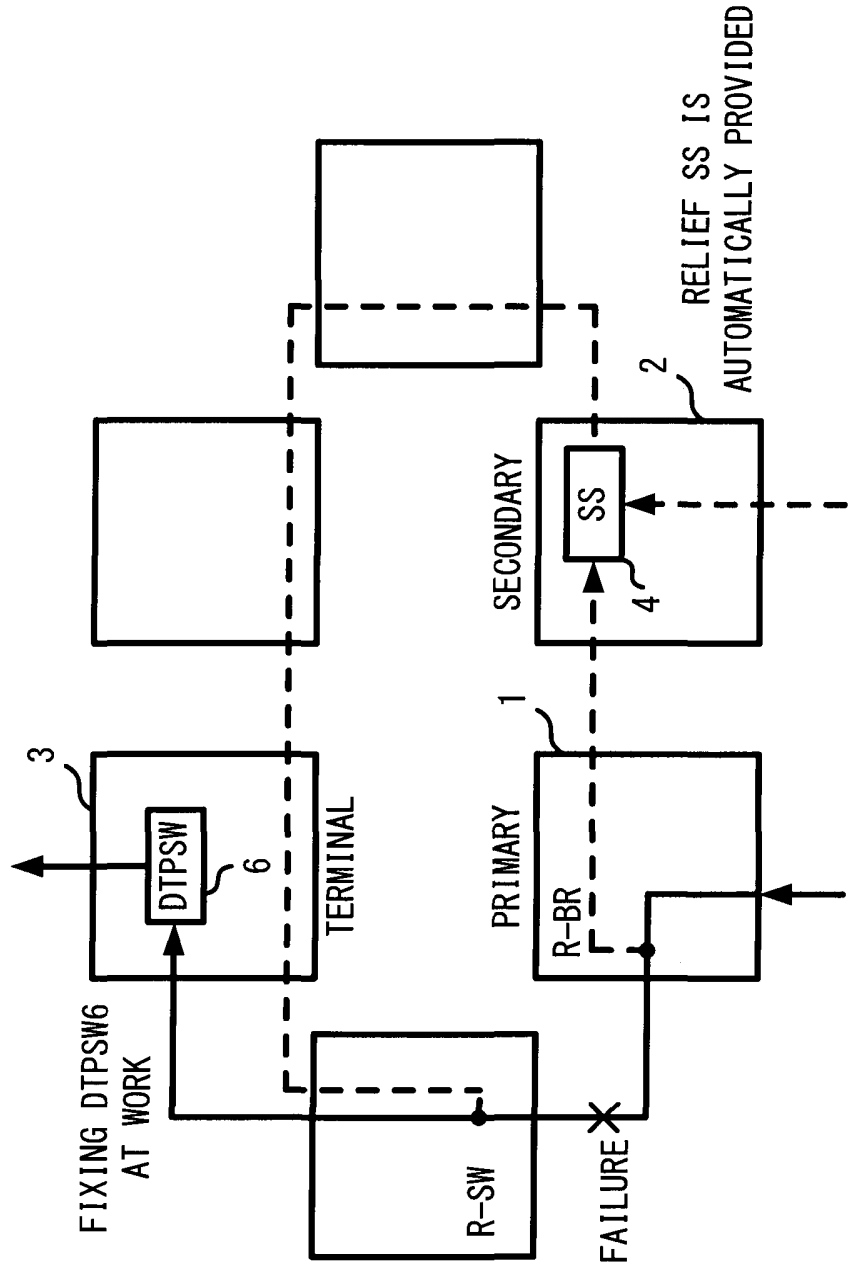


FIG. 3 RELATED ART

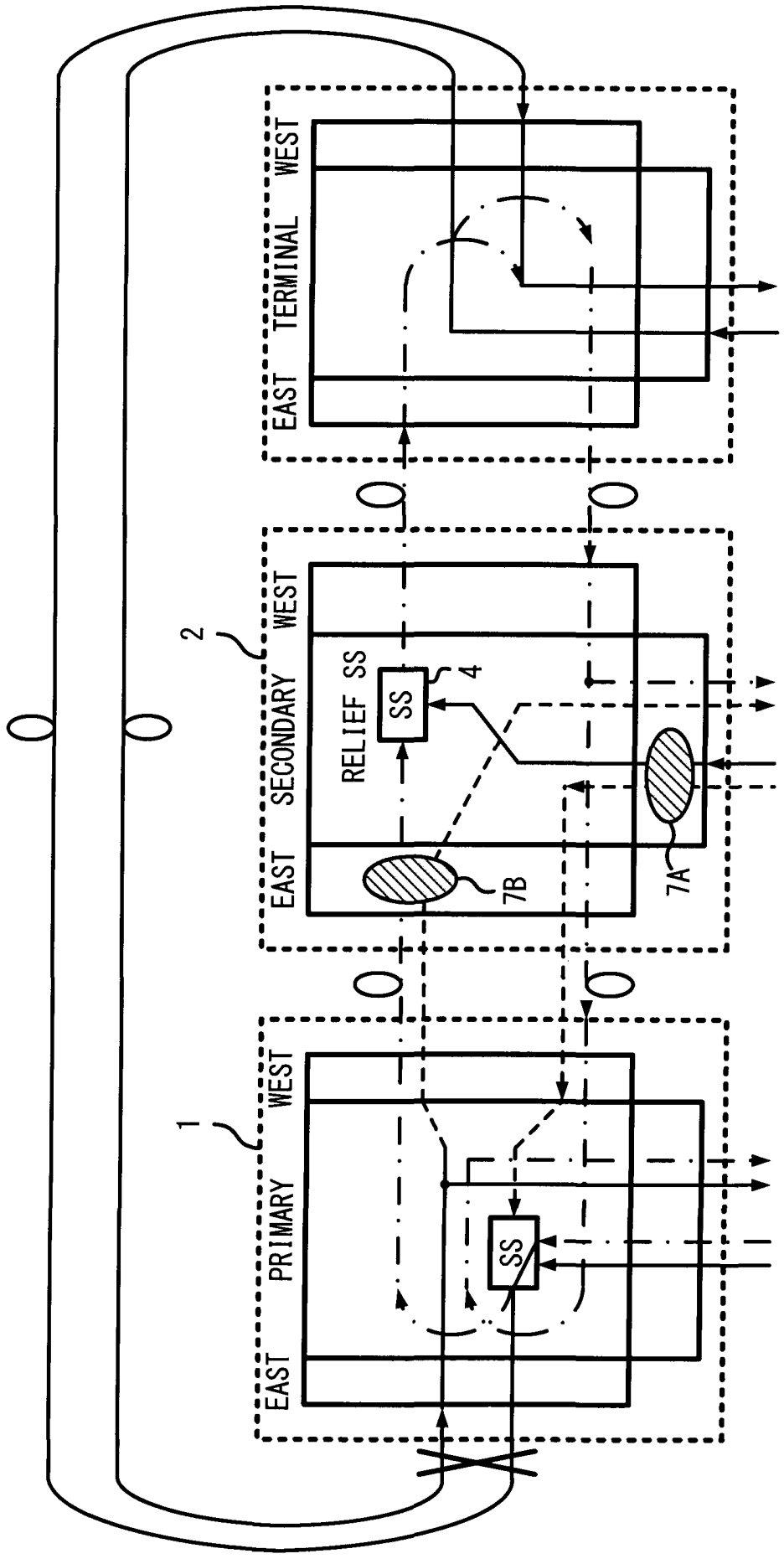


FIG. 4 RELATED ART

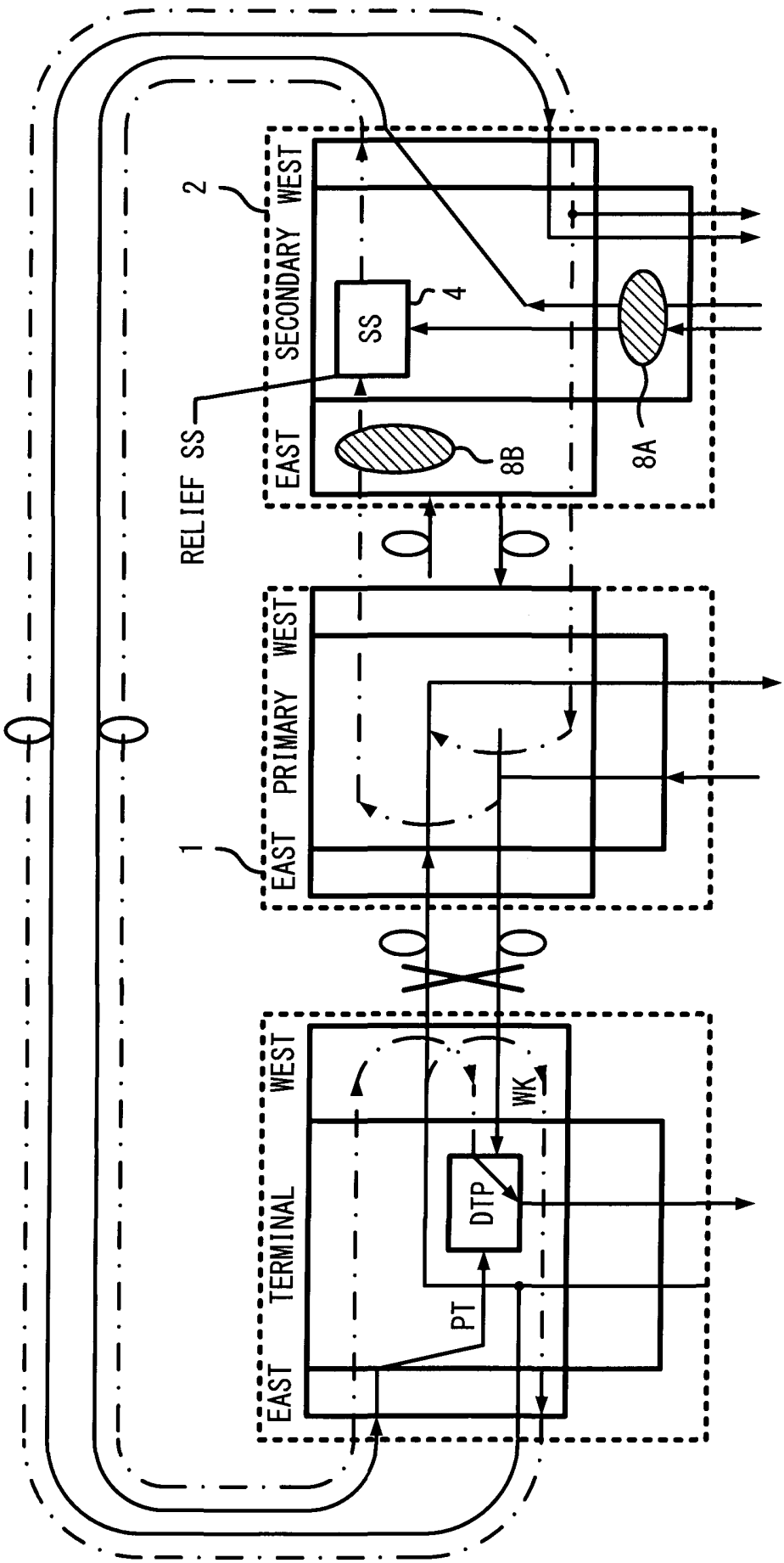
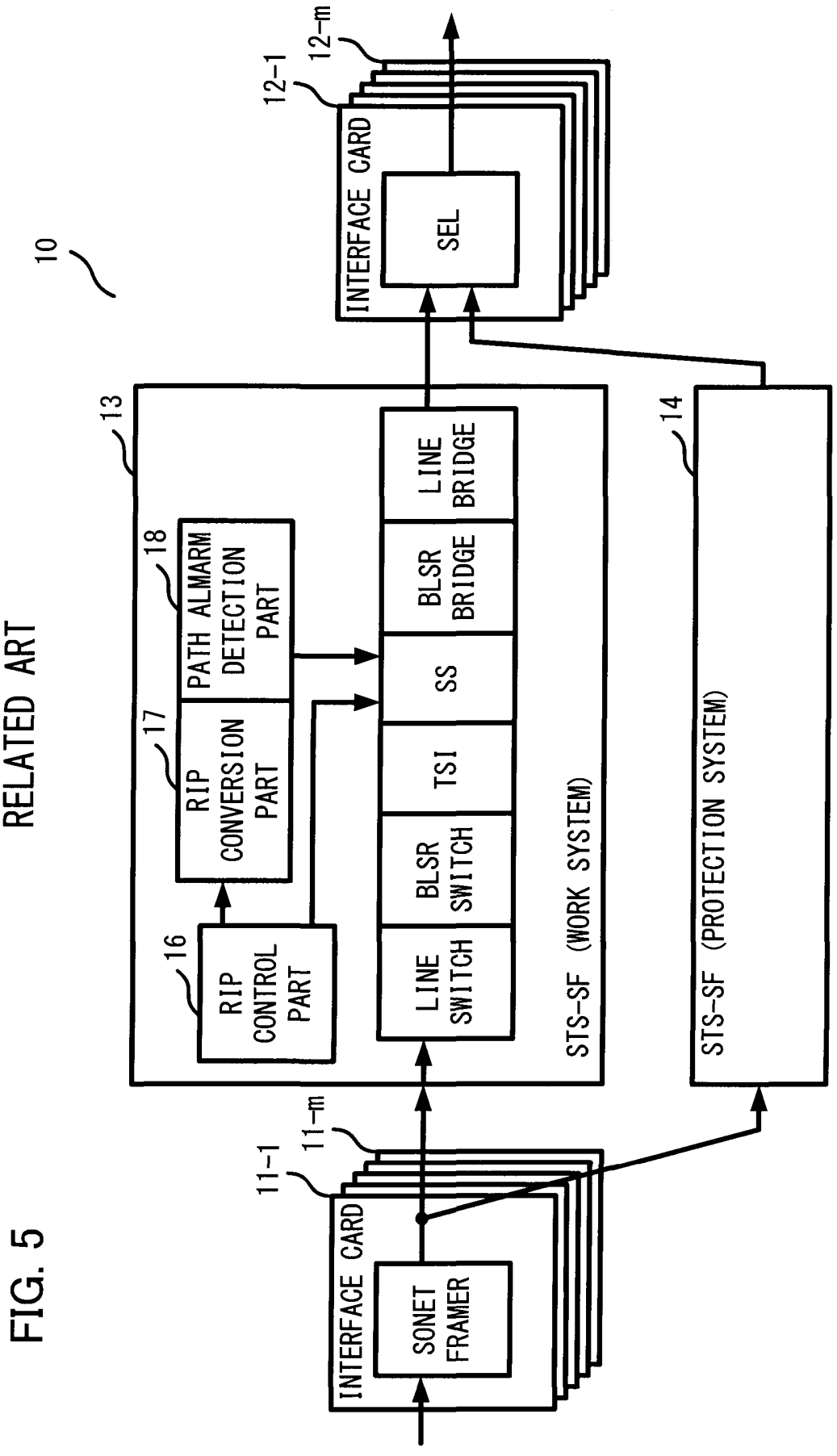


FIG. 5

RELATED ART



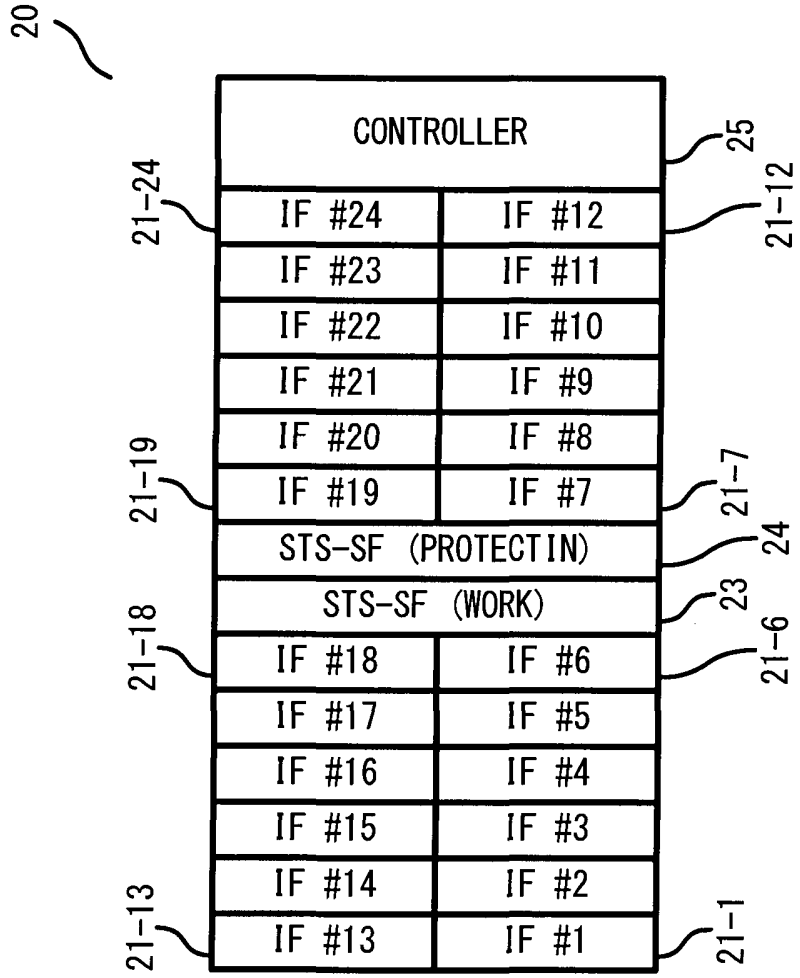

20
CONTROLLER
25
21-24
IF #24
IF #12
21-12
IF #23
IF #11
IF #22
IF #10
IF #21
IF #9
21-19
IF #20
IF #8
IF #19
IF #7
21-7
STS-SF (PROTECTIN)
24
STS-SF (WORK)
23
21-18
IF #18
IF #6
21-6
IF #17
IF #5
IF #16
IF #4
IF #15
IF #3
IF #14
IF #2
21-13
IF #13
IF #1
21-1

FIG. 6

FIG. 7

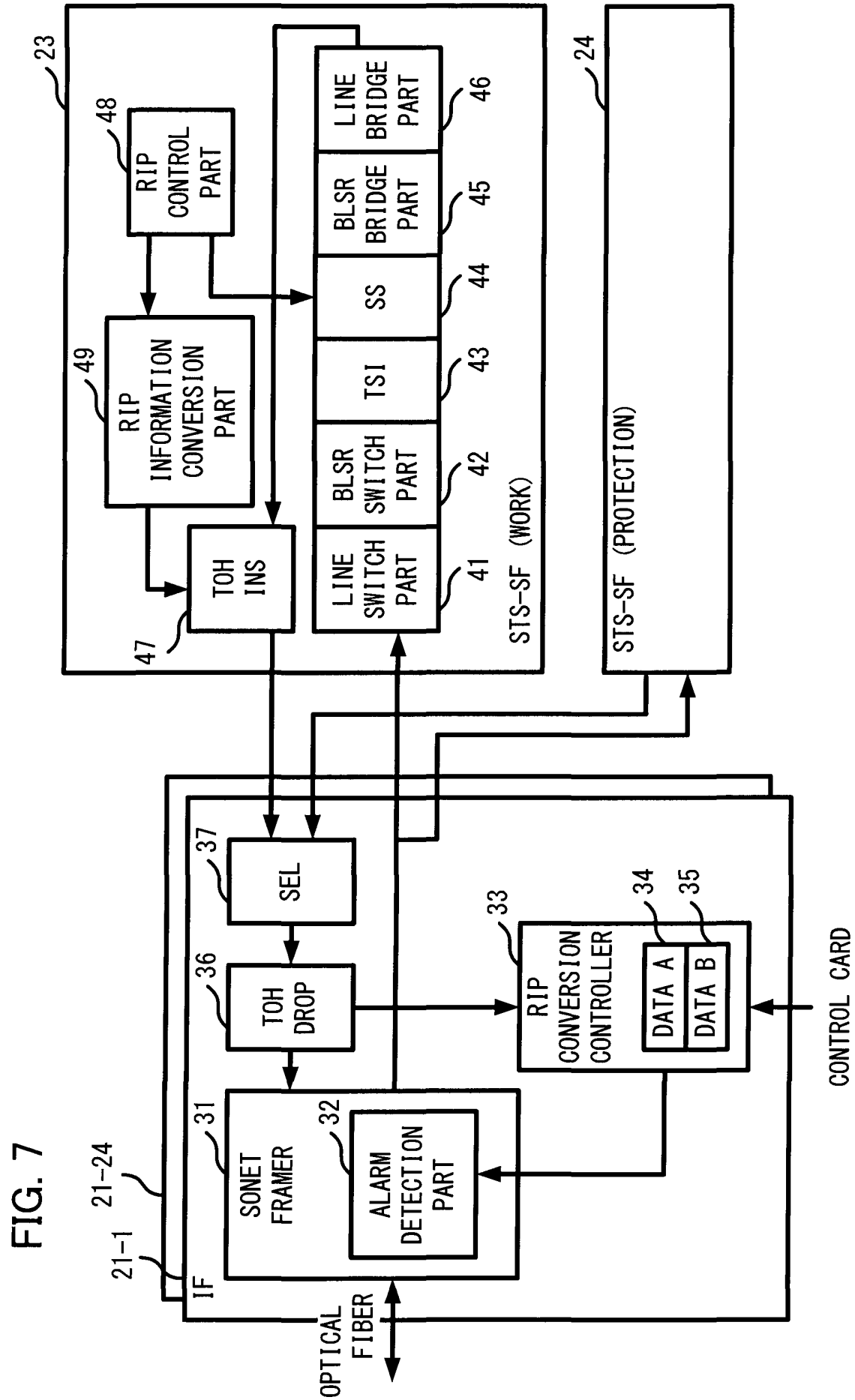

23
24
48
RIP CONTROL PART
49
RIP INFORMATION CONVERSION PART
47
TOH INS
LINE SWITCH PART
41
BLSR SWITCH PART
42
TSI
43
SS
44
BLSR BRIDGE PART
45
LINE BRIDGE PART
46
STS-SF (WORK)
STS-SF (PROTECTION)
37
SEL
36
TOH DROP
31
SONET FRAMER
32
ALARM DETECTION PART
33
RIP CONVERSION CONTROLLER
34
DATA A
35
DATA B
CONTROL CARD
21-24
21-1
IF
OPTICAL FIBER

FIG. 8

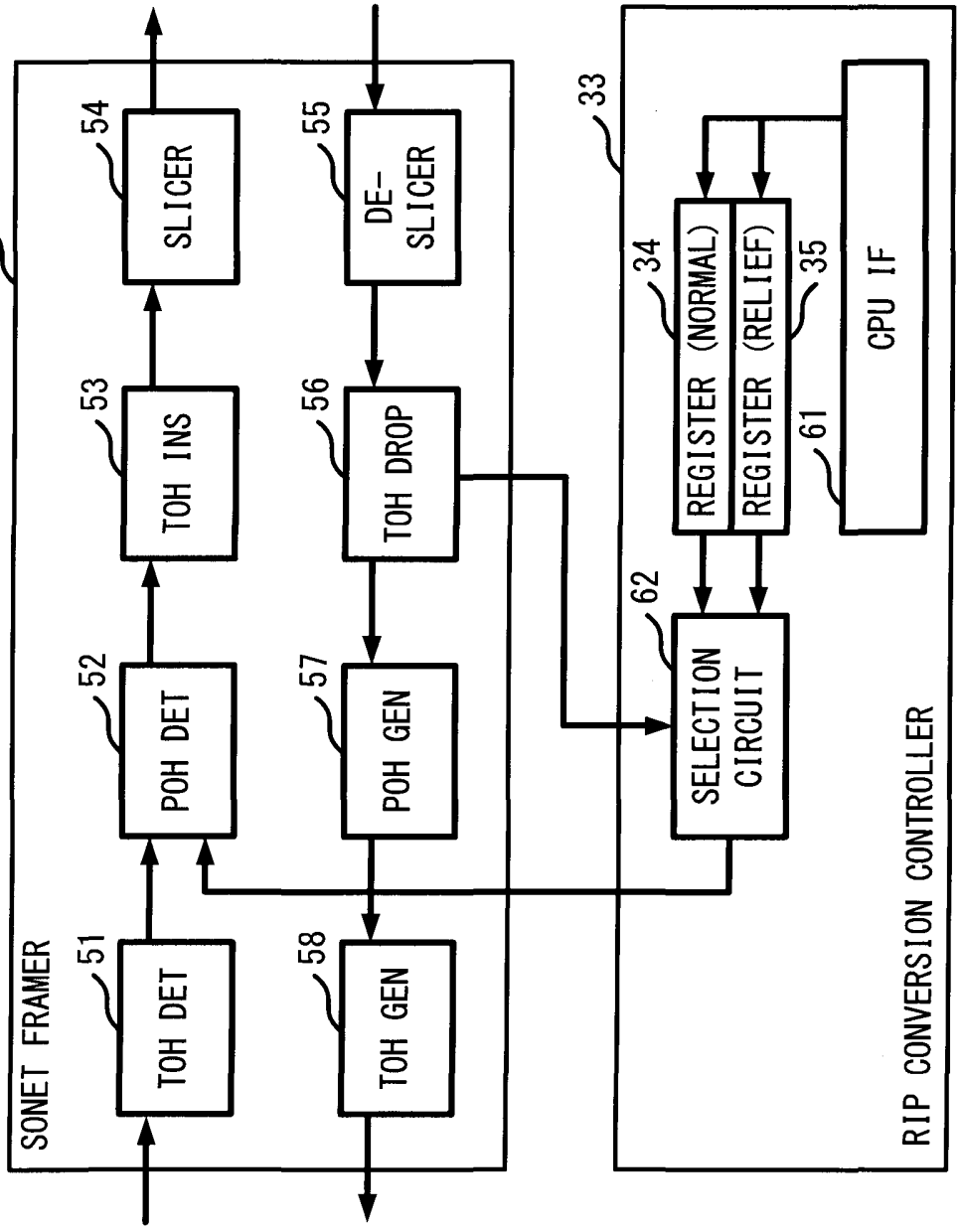

SONET FRAMER
31
TOH DET
51
POH DET
52
TOH INS
53
SLICER
54
DE-SLICER
55
TOH DROP
56
POH GEN
57
TOH GEN
58
RIP CONVERSION CONTROLLER
33
REGISTER (NORMAL)
34
REGISTER (RELIEF)
35
CPU IF
61
SELECTION CIRCUIT
62

FIG. 9

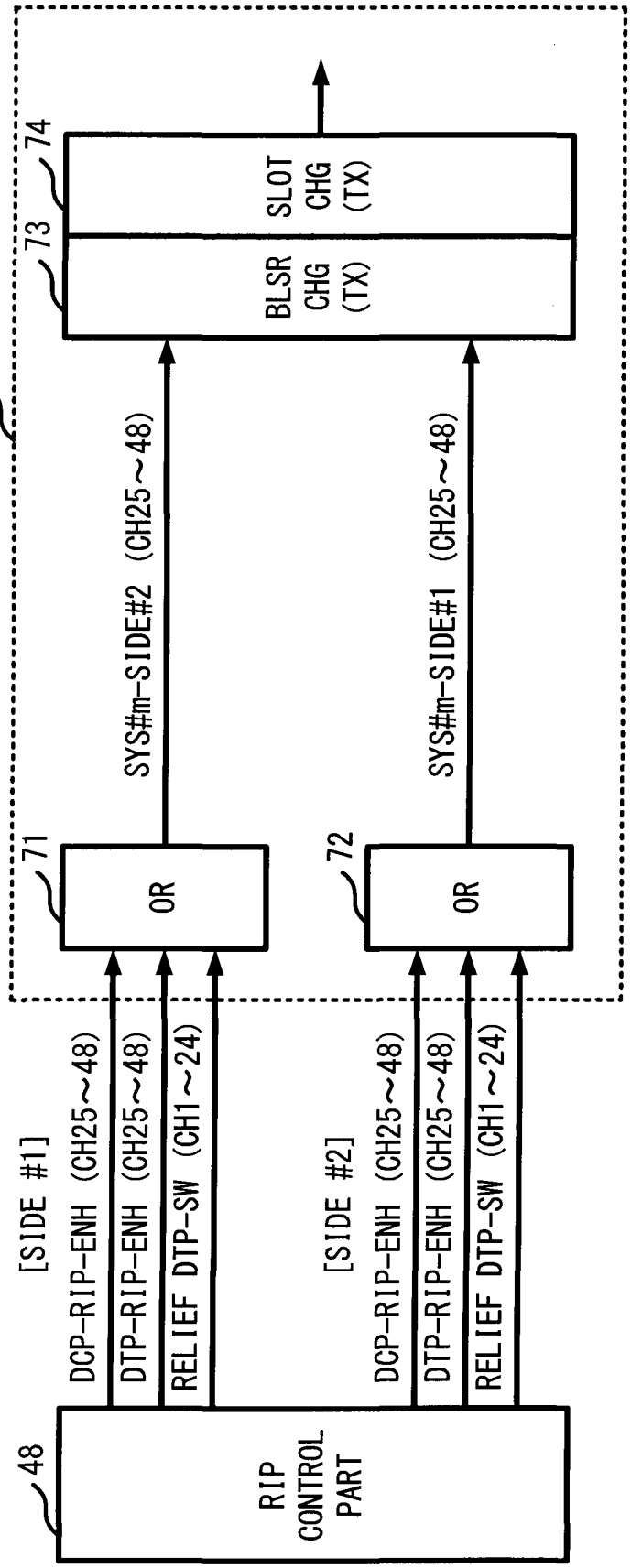

48
RIP CONTROL PART
[SIDE #1]
DCP-RIP-ENH (CH25～48)
DTP-RIP-ENH (CH25～48)
RELIEF DTP-SW (CH1～24)
[SIDE #2]
DCP-RIP-ENH (CH25～48)
DTP-RIP-ENH (CH25～48)
RELIEF DTP-SW (CH1～24)
71
OR
72
OR
SYS#m-SIDE#2 (CH25～48)
SYS#m-SIDE#1 (CH25～48)
49
73
BLSR CHG (TX)
74
SLOT CHG (TX)

FIG. 10

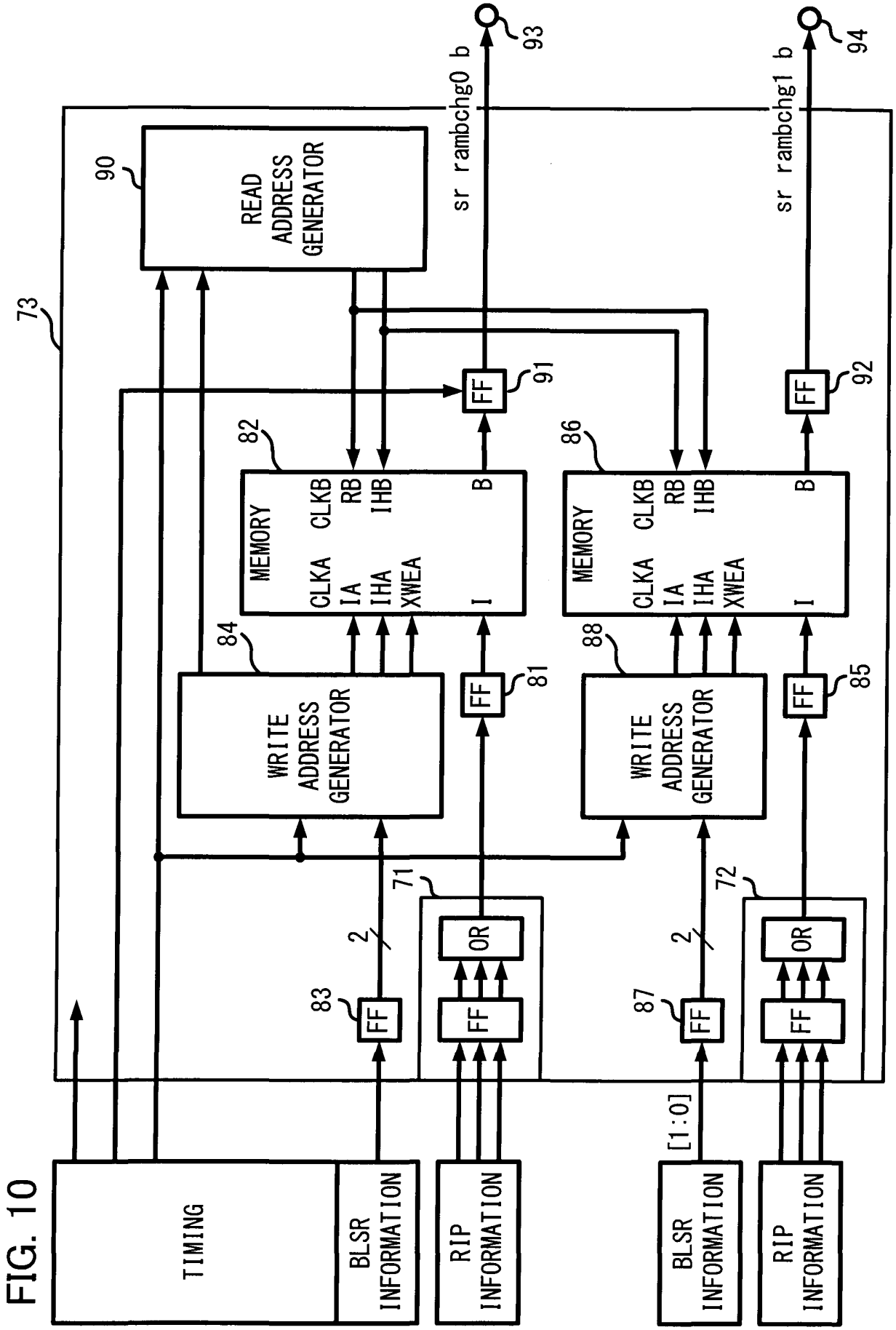

TIMING
BLSR INFORMATION
RIP INFORMATION
BLSR INFORMATION
RIP INFORMATION
[1:0]
FF
OR
2
71
72
83
87
WRITE ADDRESS GENERATOR
84
88
81
85
MEMORY
CLKA
IA
IHA
XWEA
I
CLKB
RB
IHB
B
82
86
91
92
READ ADDRESS GENERATOR
90
73
sr rambchg0 b
sr rambchg1 b
93
94

FIG. 11

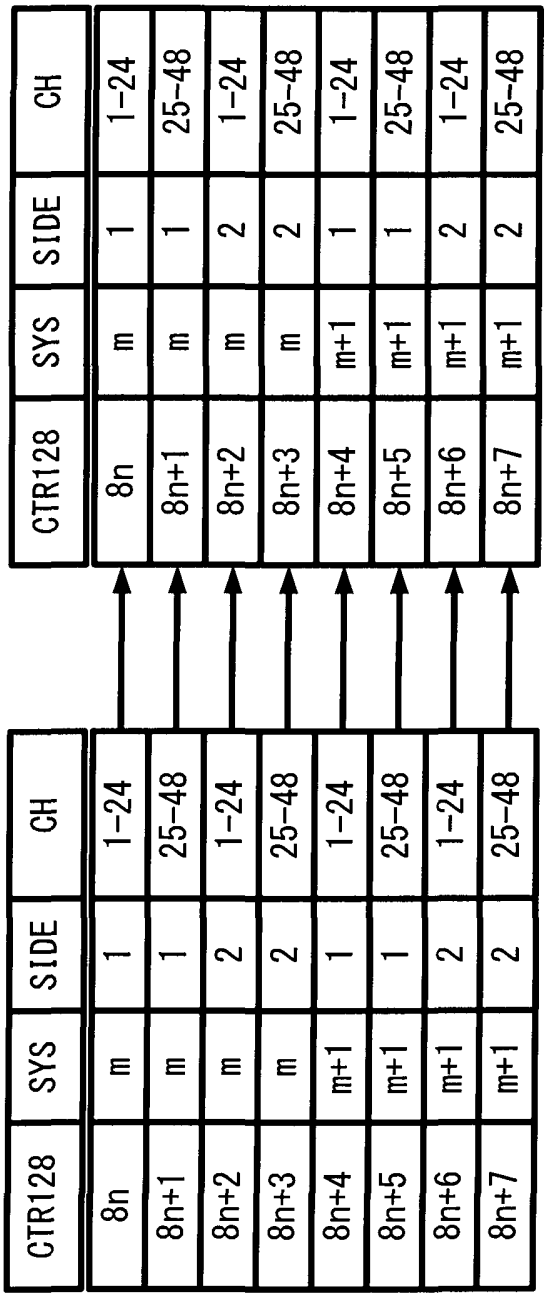
SYS	SIDE	CH		
		DCP RIP -ENH	DTP RIP -ENH	RELIEF DTP -SW
0	2	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24
	1	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24
1	2	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24
…	…	…	…	…
E	1	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24
F	2	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24
	1	1	1	–
		…	…	…
		24	24	–
		25	25	1
		…	…	…
		48	48	24

24CH	CH
CTR64	CTR24
0	0
	…
	23
1	0
	…
	23
2	0
	…
	23
3	0
	…
	23
4	0
	…
	23
5	0
	…
	23
…	…
58	0
	…
	23
59	0
	…
	23
60	0
	…
	23
61	0
	…
	23
62	0
	…
	23
63	0
	…
	23

RIP-ENH SIDE1: USED AS SIDE2 INFORMATION IN BLSR CHG

RIP-ENH SIDE2: USED AS SIDE1 INFORMATION IN BLSR CHG

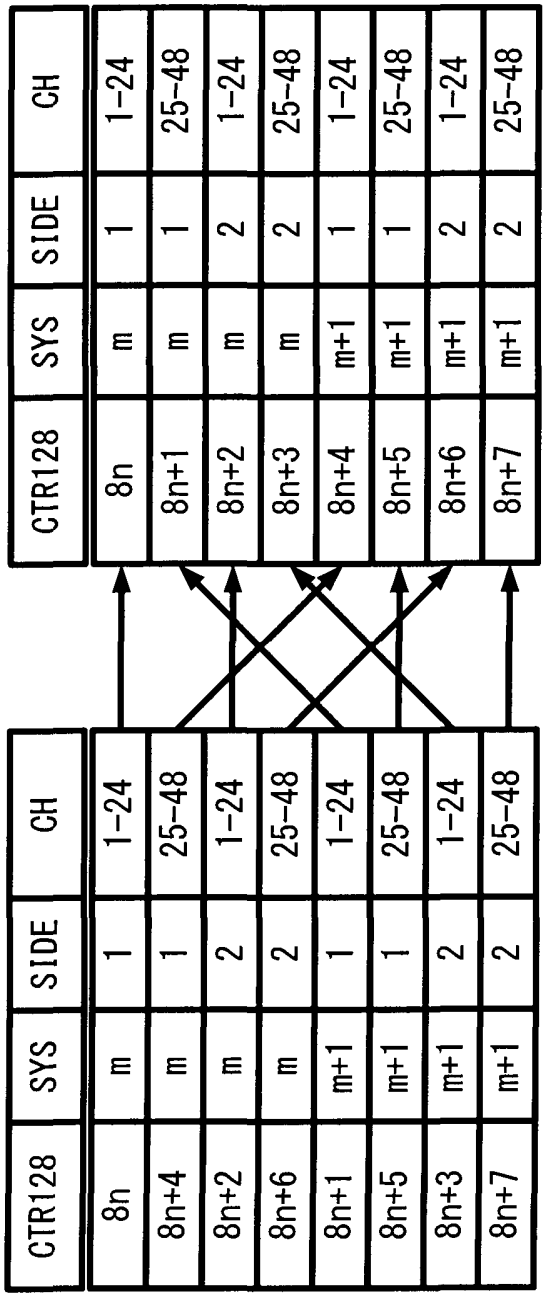
FIG. 12



n=0, 1, ···, 14, 15

m=0, 2, 6, 8, A, C, E

FIG. 13



n=0, 1, ···, 14, 15

m=0, 2, 6, 8, A, C, E

FIG. 14

CTR 128	SYS	SIDE	CH
32n + 0	m	1	1-24
32n + 16	m	1	25-48
32n + 2	m	2	1-24
32n + 18	m	2	25-48
32n + 1	m+1	1	1-24
32n + 17	m+1	1	25-48
32n + 3	m+1	2	1-24
32n + 19	m+1	2	25-48
32n + 8	m+2	1	1-24
32n + 24	m+2	1	25-48
32n + 10	m+2	2	1-24
32n + 26	m+2	2	25-48
32n + 9	m+3	1	1-24
32n + 25	m+3	1	25-48
32n + 11	m+3	2	1-24
32n + 27	m+3	2	25-48
32n + 4	m+4	1	1-24
32n + 20	m+4	1	25-48
32n + 6	m+4	2	1-24
32n + 22	m+4	2	25-48
32n + 5	m+5	1	1-24
32n + 21	m+5	1	25-48
32n + 7	m+5	2	1-24
32n + 23	m+5	2	25-48
32n + 12	m+6	1	1-24
32n + 28	m+6	1	25-48
32n + 14	m+6	2	1-24
32n + 30	m+6	2	25-48
32n + 13	m+7	1	1-24
32n + 29	m+7	1	25-48
32n + 15	m+7	2	1-24
32n + 31	m+7	2	25-48

n=0, 1, 2, 3
m=0, 8

CTR 128	SYS	SIDE	CH
32n + 0	m	1	1-24
32n + 1	m	1	25-48
32n + 2	m	2	1-24
32n + 3	m	2	25-48
32n + 4	m+1	1	1-24
32n + 5	m+1	1	25-48
32n + 6	m+1	2	1-24
32n + 7	m+1	2	25-48
32n + 8	m+2	1	1-24
32n + 9	m+2	1	25-48
32n + 10	m+2	2	1-24
32n + 11	m+2	2	25-48
32n + 12	m+3	1	1-24
32n + 13	m+3	1	25-48
32n + 14	m+3	2	1-24
32n + 15	m+3	2	25-48
32n + 16	m+4	1	1-24
32n + 17	m+4	1	25-48
32n + 18	m+4	2	1-24
32n + 19	m+4	2	25-48
32n + 20	m+5	1	1-24
32n + 21	m+5	1	25-48
32n + 22	m+5	2	1-24
32n + 23	m+5	2	25-48
32n + 24	m+6	1	1-24
32n + 25	m+6	1	25-48
32n + 26	m+6	2	1-24
32n + 27	m+6	2	25-48
32n + 28	m+7	1	1-24
32n + 29	m+7	1	25-48
32n + 30	m+7	2	1-24
32n + 31	m+7	2	25-48

n=0, 1, 2, 3
m=0, 8

FIG. 15

CTR 128	SYS	SIDE	CH
32n + 0	m	1	1-24
32n + 2	m	1	25-48
32n + 16	m	2	1-24
32n + 18	m	2	25-48
32n + 1	m+1	1	1-24
32n + 3	m+1	1	25-48
32n + 17	m+1	2	1-24
32n + 19	m+1	2	25-48
32n + 8	m+2	1	1-24
32n + 10	m+2	1	25-48
32n + 24	m+2	2	1-24
32n + 26	m+2	2	25-48
32n + 9	m+3	1	1-24
32n + 11	m+3	1	25-48
32n + 25	m+3	2	1-24
32n + 27	m+3	2	25-48
32n + 4	m+4	1	1-24
32n + 6	m+4	1	25-48
32n + 20	m+4	2	1-24
32n + 22	m+4	2	25-48
32n + 5	m+5	1	1-24
32n + 7	m+5	1	25-48
32n + 21	m+5	2	1-24
32n + 23	m+5	2	25-48
32n + 12	m+6	1	1-24
32n + 14	m+6	1	25-48
32n + 28	m+6	2	1-24
32n + 30	m+6	2	25-48
32n + 13	m+7	1	1-24
32n + 15	m+7	1	25-48
32n + 29	m+7	2	1-24
32n + 31	m+7	2	25-48

n=0, 1, 2, 3
m=0, 8

CTR 128	SYS	SIDE	CH
32n + 0	m	1	1-24
32n + 1	m	1	25-48
32n + 2	m	2	1-24
32n + 3	m	2	25-48
32n + 4	m+1	1	1-24
32n + 5	m+1	1	25-48
32n + 6	m+1	2	1-24
32n + 7	m+1	2	25-48
32n + 8	m+2	1	1-24
32n + 9	m+2	1	25-48
32n + 10	m+2	2	1-24
32n + 11	m+2	2	25-48
32n + 12	m+3	1	1-24
32n + 13	m+3	1	25-48
32n + 14	m+3	2	1-24
32n + 15	m+3	2	25-48
32n + 16	m+4	1	1-24
32n + 17	m+4	1	25-48
32n + 18	m+4	2	1-24
32n + 19	m+4	2	25-48
32n + 20	m+5	1	1-24
32n + 21	m+5	1	25-48
32n + 22	m+5	2	1-24
32n + 23	m+5	2	25-48
32n + 24	m+6	1	1-24
32n + 25	m+6	1	25-48
32n + 26	m+6	2	1-24
32n + 27	m+6	2	25-48
32n + 28	m+7	1	1-24
32n + 29	m+7	1	25-48
32n + 30	m+7	2	1-24
32n + 31	m+7	2	25-48

n=0, 1, 2, 3
m=0, 8

FIG. 16

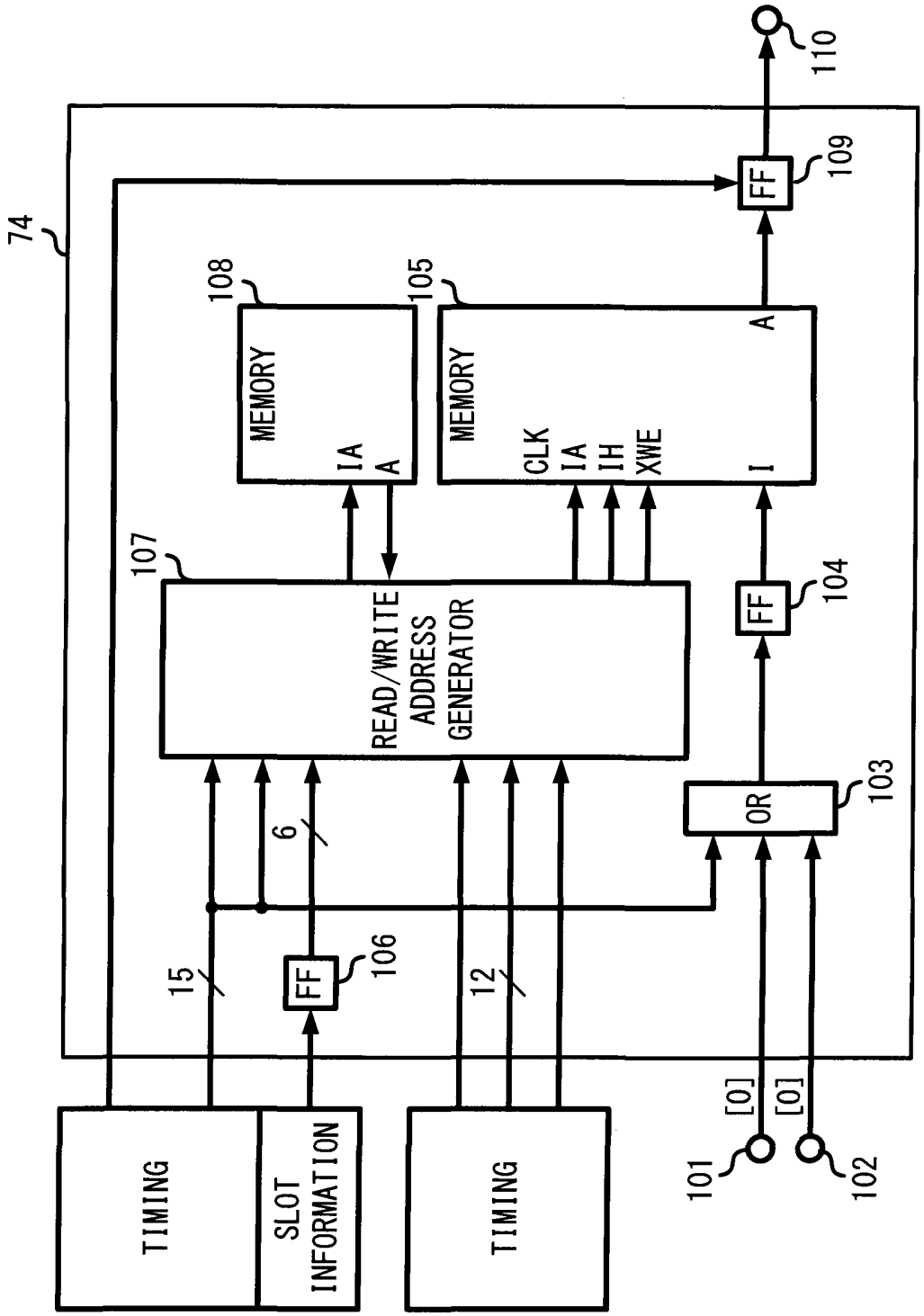
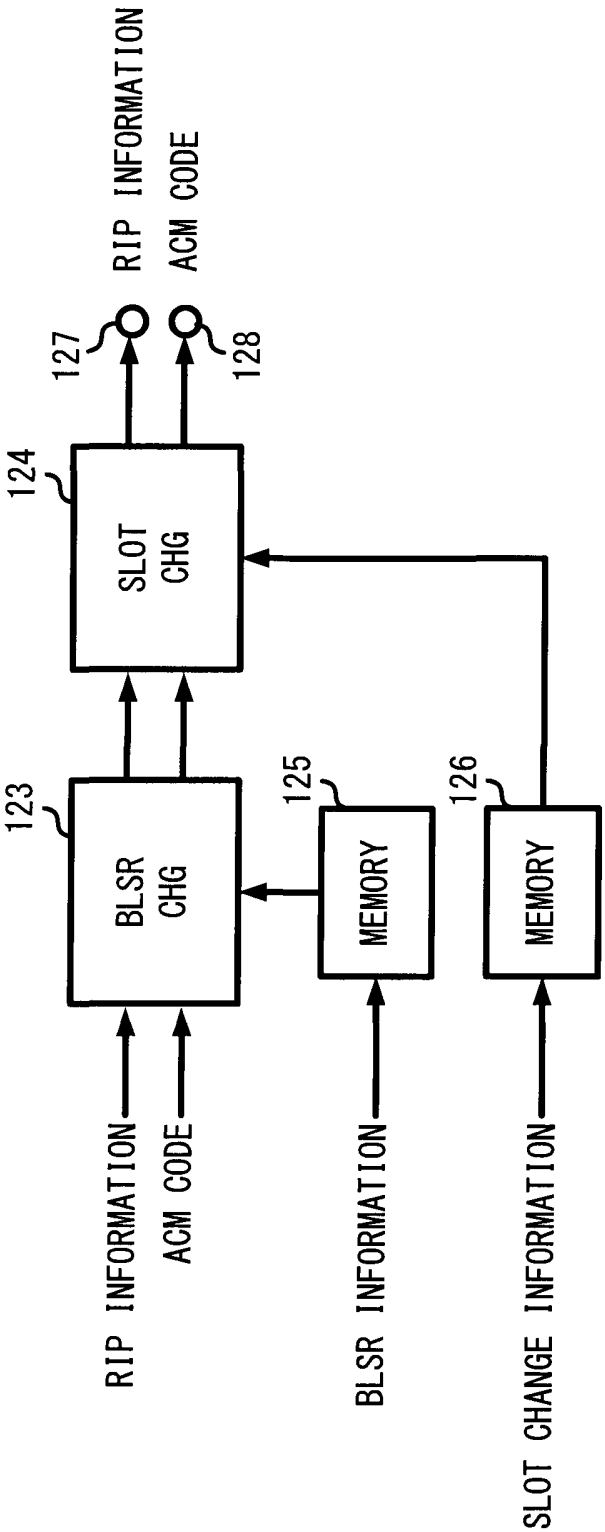

74
110
109
FF
108
105
MEMORY
IA
A
MEMORY
CLK
IA
IH
XWE
I
A
107
READ/WRITE
ADDRESS
GENERATOR
104
FF
103
OR
6
15
FF
106
12
TIMING
SLOT
INFORMATION
TIMING
[0]
[0]
101
102

FIG. 17


RIP INFORMATION
ACM CODE
BLSR INFORMATION
SLOT CHANGE INFORMATION
BLSR CHG
MEMORY
MEMORY
SLOT CHG
RIP INFORMATION
ACM CODE
123
125
126
124
127
128

NODE APPARATUS

The present invention is related to a node apparatus for relieving a failure of a network in which ring networks are interconnected.

In a SONET (synchronous optical network)/ SDH (synchronous digital hierarchy) network which is a synchronous network, in a BLSR (Bi-Directional Line Switched Ring) network defined in GR-1230, there is a restriction that the number of nodes which can be set in one ring is not more than 16, and a configuration called a Ring Inter Connection is used when constructing a network whose node number exceeds 16.

At this time, in order to efficiently utilize a main signal band, an application for relieving a failure over the ring network (ring failure), such as DCP (Drop & Continue on Protection Channel) or DTP (Dual Transmission Protection Channel) or the like, has been used.

When DCP/DTP configuration (RIP (Ring Interconnection Protection)-Enhance) is built, it is necessary to convert provisioning information for the alarm detecting setting of B3 error related to an SS (Service Selector) switching operation and PDI (payload defect indicator)/ PLM (payload mismatch)/ TIM (trace identifier mismatch) so as to be adapted to a traffic that is to be actually relieved.

DCP/DTP

Figs. 1A and 1B are diagrams illustrating a DCP operation.

Figs. 2A and 2B are diagrams illustrating a DTP operation.

In DCP, DTP which is a ring interconnection that is supported by BLSR of 2 fibers or 4 fibers, when BLSR network failure is generated, an SS is automatically provided in a secondary node 2 according to the link where the BLSR network failure is generated. The automatically provided SS is referred to as a relief SS (relieving type SS). There is a case that the relief SS is provided and there is a case that the relief SS is not provided depending on the link where the BLSR network failure is generated (see SS 4 of Fig. 1A, Fig. 2A).

Further, in a DCP, DTP, a normal SS provided in a primary mode 1 is referred to as a regular SS. That is, the different names are used as the situation demands in order to separate with the relief SS. When simply expressed as SS, the SS denotes the regular SS in general (see SS 5 of Figs. 1A-1B).

In the BLSR network, when ring failure is generated, a protection channel (line) is used for relieving a work line, so that a channel (PCA ch) accessing to a protection line generally ceases the access (case 1).

However in the DCP, DTP, there is a case that relieving of other work channel is not disturbed even when accessing to a protection channel is not ceased, and in such a case, accessing to the protect channel is continued (case 2).

Further, there is a case that a signal bridged to a protection channel by a ring bridge (R-BR) in a switching node is the same as a signal that have been accessed to a protection channel in the secondary node 2 of the original DCP or DTP configuration, and the relief SS 4 is formed in such a case (case 3).

In the DCP, DTP, the secondary node 2 executes any one of the aforementioned cases 1 to 3 depending on a link where a network failure is occurred.

As for the primary node 1 and a terminal node 3, the operation is not changed even when the network failure is occurred anywhere in the ring, and the primary node 1 of the DCP fixes the regular SS 5 at INS (insertion) side. The terminal node 3 of the DTP fixes a DTP-SW 6 at the work side.

The other functions are the same as the normal BLSR functions, and a PCA (Protection Channel Access) cease and a protection channel through are executed, and the switching node executes a ring bridge (R-BR) and a ring switch (R-SW).

Alarm Detection Setting Conversion

Fig. 3 is a diagram illustrating an alarm detection setting convert in the DCP.

In the BLSR, when a ring failure, a failure over a ring network, is occurred, a protection line is used for relieving the work line. In the DCP/DTP configuration, a signal bridged to a protection channel by the ring bridge in the switching node may be the same signal which has been accessed to a protection channel in the secondary node 2 of the original DCP or DTP configuration, and in this case, the relief SS 4 is formed.

When determining a switching operation of the relief SS 4, an alarm detection setting which is a setting of a threshold value or the like for detecting the alarm of B3 (error monitoring of path)/ C2 (Path Signal Label)/ J1 (path trace) in POH (Path OverHead) of SONET/SDH requires PCA (Protection Channel Access) which has been input in the secondary node 2 before the ring switch is switched as a dedicated setting of another relief SS.

This is apparent by comparing the route before the ring switch is switched illustrated in a solid line and the route at the time when a relief SS is activated after the ring switch is switched illustrated in a chain line as shown in Fig. 3.

That is, this is because that a main signal of a protection channel input in the secondary node 2 at a normal time and a main signal input in the relief SS 4 at a relieving time is absolutely different in content although physical input channels are the same.

In Fig. 3, the PCA (broken line) that is a signal input to East side of the secondary node 2 before the ring switch is switched and a circuit signal (chain line) after the ring switch is switched are different data signals. Accordingly, it is necessary that detection setting of the alarm which is detected as a switching

trigger is also respectively set to be appropriate for detection.

The input signal at East side of the secondary node 2 after the ring switch is switched is the same as an input signal of a ring interconnection side of the secondary node 2 before the ring switch is switched. In the secondary node 2, an alarm detection setting 7A at the ring interconnection side may be converted and used as an alarm detection setting 7B at East side after the ring switch is switched.

Fig. 4 is a diagram illustrating an alarm detection setting converted in the DTP. In the diagram, the route before the ring switch is switched is illustrated by a solid line, and the route when the relief SS is activated after the ring switch is switched is illustrated by a chain line.

Also in the case of the DTP configuration, basically similar to the case of the DCP, in the secondary node 2, the input signal at East side after the ring switch is switched is the same as the ring interconnection side input signal before the ring switch is switched. In the secondary node 2, an alarm detection setting 8A at the ring interconnection side may be used as an alarm detection setting 8B at East side after the ring switch is switched.

Fig. 5 is a diagram illustrating a block diagram of an example of a conventional node apparatus. In the diagram, the node apparatus 10 includes interface cards 11-1 to 11-m, 12-1 to 12-m, a work SF (Switch Fabric) 13, and a protection SF (Switch Fabric) 14. The SF's 13, 14 are necessary to provide the circuit by a synchronous transmission signal STS-1 unit, illustrated as STS-SF in diagrams.

An RIP control part 16 provided in the SF's 13, 14, identifies DCP/DTP by soft setting information such as DCP, DTP, or the like and by an RIP (routing information protocol) table in which a span (from primary node to terminal node) passed by each channel is registered and judges whether or not a relief SS is activated.

An RIP conversion part 17 converts a detection setting of B3/C2/J1 alarm in a path alarm detection part 18 by controlling of the RIP control part 16.

Note that an alarm processing technique for eliminating the circuit size of hardware in an ADM device having the BLSR function equipped with a service selector has been known in Japanese Laid-open Patent Publication No. 11-122269.

The speed and the capacity of transmission signal have been increased with recent increase of transmission information quantity. The circuit size has been also increased with the increase. Under the circumstance, the setting space and power consumption of a node apparatus is increased in proportion to the increase of capacity.

In the conventional node apparatus, since the RIP conversion part 17 and the path alarm detection part 18 which are dedicated hardware circuits are provided in

the SF's 13, 14 in a concentrated manner, so that it is basically necessary to provide the circuit by a synchronous transmission signal STS-1 unit, and there is a restriction when increasing the processing capacity to the requirement of the increase of capacity.

Accordingly, it is desirable to decentralize functions by providing an RIP converting function in an interface unit, thereby flexibly coping with increase of processing.

According to an aspect of the invention, there is provided a node apparatus having a plurality of interface units for interfacing to a transmission line, switch units of a work system and a protection system for switching signals of the transmission line, and a service selector used to relieve a network failure over ring networks interconnected by node apparatuses, the node apparatus including a first controller for controlling the service selector in the switch units, and a second controller for controlling setting information of alarm detection in case of using the service selector in the interface units.

The advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are not restrictive of the invention, as claimed.

Reference is made, by way of example only, to the accompanying drawings in which:

Figs. 1A and 1B are diagrams illustrating a DCP operation;

Figs. 2A and 2B are diagrams illustrating a DTP operation;

Fig. 3 is a diagram illustrating an alarm detection setting convert in the DCP;

Fig. 4 is a diagram illustrating an alarm detection setting converted in the DTP;

Fig. 5 is a diagram illustrating a block diagram of an example of a conventional node apparatus;

Fig. 6 is diagram illustrating a configuration of an embodiment of a node apparatus;

Fig. 7 is a diagram illustrating a block diagram of an embodiment of the node apparatus;

Fig. 8 is a diagram illustrating a block diagram of an embodiment of an interface card and an RIP conversion controller;

Fig. 9 is a diagram illustrating a block diagram of an embodiment of the RIP information conversion part;

Fig. 10 is a diagram illustrating a block diagram of an embodiment of an OR circuit and a BLSR change part;

Fig. 11 is a diagram illustrating a BLSR change;

Fig. 12 is a diagram illustrating a BLSR change;

Fig. 13 is a diagram illustrating a BLSR change;

Fig. 14 is a diagram illustrating a BLSR change;

Fig. 15 is a diagram illustrating a BLSR change;

Fig. 16 is a diagram illustrating a block diagram of an embodiment of the slot change part; and

Fig. 17 is a diagram illustrating a block diagram of an embodiment in which the RIP information conversion part and an ACM code conversion part are partly commoditized.

Hereinafter, an embodiment will be described based on the drawings.

Node apparatus

Fig. 6 is a diagram illustrating a configuration of an embodiment of a node apparatus.

Fig. 7 is a diagram illustrating a block diagram of the embodiment of the node apparatus.

In Figs. 6, 7, the node apparatus 20 includes interface cards 21-1 (IF#1) to 21-24 (IF#24) for interfacing with a transmission line as a interface unit, and switch fabrics (STS-SF) 23, 24 for switching the transmission line signal as a switch unit, and a control card (controller) 25 for controlling the node apparatus 20.

The switch fabric 23 for work is mutually connected with the interface cards 21-1 to 21-24 by a back plate board not illustrated, illustrated as STS-SF (WORK) in diagrams. Further, the switch fabric 24 for protection (PTCT) is mutually connected with the interface cards 21-1 to 21-24 by the back plate board, illustrated as STS-SF (PTCT) in diagrams.

The control card 25 is mutually connected with the interface cards 21-1 to 21-24 and the switch fabrics 23, 24, and executes control of the entire node apparatus 20.

In Fig. 7, the interface card (IF#1) 21-1 to the interface card (IF#24) 21-24 execute a transmission/ reception processing of, for example, an optical signal of SONET/SDH. An input optical signal is subjected to a photoelectric conversion processing and a serial/parallel conversion processing, and is supplied to a SONET framer 31. Further, an output signal output from the SONET framer 31 is subjected to a parallel/serial conversion processing and a photoelectric conversion processing, and is transmitted to an optical fiber.

The SONET framer 31 includes an alarm detection part 32. The alarm

detection part 32 detects an alarm of B3 (error monitoring of path)/ C2 (information identification of path)/ J1 (path trace) in POH of input signal. A threshold value for detecting the alarm is supplied from an RIP conversion controller 33.

The RIP conversion controller 33 having an RIP conversion function includes a normal time register 34 for holding a setting data for alarm detection (provisioning information: data A) at a normal time, and a relief time register 35 for holding a setting data for alarm detection (provisioning information: data B) at a relief SS time when the relief SS is provided. And the RIP conversion controller 33 switches any of the setting data for alarm detection at a normal time and the setting data for alarm detection at a relief SS time and supplies to the alarm detection part 32 by the channel unit. For example, the aforementioned setting data for alarm detection at a normal time and the setting data for alarm detection at a relief SS time are threshold values, used for detecting alarm, and are set from a CPU in the control card 25.

The switching control is executed based on RIP information (information for relief SS enhancement) as activation information of relieving the ring failure separated by a transport overhead separation part (TOH DROP) 36 by the channel unit.

Note that a selector (SEL) 37 executes switching of a work signal and a protection signal, and selects an output SONET signal of any one of the STS-SFs 23, 24 and supplies to the TOH DROP 36.

Note that in the embodiment, the description is made for SONET as an example, the minimum unit of the channel is synchronous transfer signal STS-1 frame of SONET. Further, a transport overhead in SONET corresponds to a section overhead of SDH, and a section overhead in SONET corresponds to Regenerator Section Over Head (RSOH) of SDH, and a line overhead in SONET corresponds to Multiplex Section Over Head (MSOH) of SDH.

A SONET signal output from the SONET framer 31 is supplied to the switch fabrics 23, 24 for work and protection. The switch fabrics 23, 24 execute switch control of a main signal, and the main signal is switched by a BLSR switch part 42, and thereafter subjected to a cross connect processing in a cross connect part (TSI) 43. Then, the main signal is switched by a service selector part (SS) 44, and is branched by a line bridge part 45 and a BLSR bridge part 46, and is supplied to a transport overhead insertion part (TOH INS) 47.

An RIP control part 48 determines whether the relief SS is activated or not by identifying the DCP or DTP based on soft setting information of the DCP, DTP, or the like preliminarily internally set and an RIP table in which a span (from primary node to terminal node) passed by each channel is registered. And the RIP control

part 48 generates RIP information, and executes switching control of the SS 44 when activating the relief SS. At the same time, the RIP information is supplied to an RIP information conversion part 49.

The RIP control part 48 executes generation of RIP information by a system number rule indicating the switch processing unit of the switch fabric. Consequently, the RIP information conversion part 49 converts the RIP information into a slot rule which is alignment of the time slot of the SONET signal to be output and which indicates the signal processing unit of the interface card in order to transfer to the interface card at the input side by multiplexing the RIP information for every time slot of the SONET signal to be output, and supplies to the TOH INS 47.

The TOH INS 47 inserts the RIP information converted into the aforementioned slot rule in, for example, a free byte following B1 byte of a section overhead of the SONET signal to be output and supplies to the interface cards 21-1 to 21-24.

Interface Card and RIP Information Interchange Unit

Fig. 8 is a diagram illustrating a block diagram of an embodiment of the interface card and the RIP conversion controller. In the diagram, a transport overhead detection part (TOH DET) 51 of the SONET framer 31 executes detection processing of the section overhead and the line overhead of the input signal, and a path overhead detection part (POH DET) 52 executes detection processing of a path overhead. The alarm detection part 32 for detecting B3/ C2/ J1 is provided in the POH DET 52.

A transport overhead insertion part (TOH INS) 53 provided to the next executes insertion processing of the section overhead and the line overhead, and a slicer 54 executes a bit slice conversion processing so as to match with the interface of the switch fabric and supplies the SONET signal to the switch fabrics 23, 24.

A de-slicer 55 executes a reverse conversion processing of the bit slice of the SONET signal supplied from the switch fabrics 23, 24.

A transport overhead separation unit (TOH DROP) 56 (corresponding to TOH DROP 36 of Fig. 7) separates RIP information (information for relief SS enhance) from, for example, a free byte following B1 bite of the section overhead and supplies to a selection circuit 62 in the RIP conversion controller 33 and supplies the main signal to a path overhead generation part (POH GEN) 57.

The POH GEN 57 generates a path overhead and adds the path overhead to the main signal.

A transport overhead generation part (TOH GEN) 58 generates a transport overhead and adds the transport overhead to the main signal and outputs as a

SONET signal.

In the RIP conversion controller 33, provisioning information is supplied from a CPU in the controller 25 to a CPU interface part (CPU INF) 61, and provisioning information including the setting data for alarm detection at a normal time is held by normal time register 34, and the provisioning information including the setting data for alarm detection at the relief time SS when the relief SS is provided, is held by the relief time register 35.

The selection circuit 62 holds RIP information (information for relief SS enhance) supplied from the TOH DROP 56 by a channel unit. And the selection circuit 62 selects the setting data for alarm detection at a normal time in the case where the RIP information (information for relief SS enhance) is, for example, value zero by the channel unit, and selects the setting data for alarm detection at the relief SS time in the case of value one, and supplies to the alarm detection part 32 in the POH DET 52.

The alarm detection part 32 detects the alarm of B3/ C2/ J1 in POH of the input signal by using the supplied the setting data for alarm detection.

Herewith, distributed processing can be executed by the interface cards 21-1 to 21-24 and the switch fabrics 23, 24, and a configuration having expandability by which it becomes possible to easily cope with increase of capacity is provided.

RIP Information Conversion Part

Fig. 9 is a diagram illustrating a block diagram of an embodiment of the RIP information conversion part 49. In the diagram, the RIP control part 48 outputs any of DCP-RIP-ENH (CH25 to 48) which is RIP information of the DCP of a protection channel, DTP-RIP-ENH (CH25 to 48) which is RIP information of the DTP corresponding to 24 channels, or relief DTP-SW (CH1 to 24) which is the rest of the RIP information with respect to each of East side (side #1) and West side (side #2) as RIP information. Note that since DCP-RIP-ENH (CH1 to 24), DTP-RIP-ENH (CH1 to 24) are work channels, it is prohibited that every channel is converted by zero.

An OR (logical disjunction) circuit (OR) 71 in the RIP information conversion part 49 executes OR operation of DCP-RIP-ENH (CH25 to 48), DTP-RIP-ENH (CH25 to 48), relief DTP-SW (CH1 to 24) at East side, and obtains any one type of RIP information (for example, DCP-RIP-ENH), and supplies to a BLSR change part (BLSR CHG) 73 as RIP information (CH25 to 48) at West side.

Further, an OR (logical disjunction) circuit (OR) 72 executes OR operation of DCP-RIP-ENH (CH25 to 48), DTP-RIP-ENH (CH25 to 48), relief DTP-SW (CH1 to 24) at West side, and obtains any one type of RIP information (for example, DCP-RIP-ENH) and supplies to the BLSR CHG 73 as RIP information (CH25 to 48) at East side.

The BLSR CHG 73 changes the alignment of the RIP information (BLSR change) based on BLSR information which is configuration information of the ring network. Further, a slot change part (SLOT CHG) 74 changes the alignment of RIP information output from the BLSR CHG 73 based on slot information which is physical configuration information of the node apparatus. Herewith, the RIP information is converted to the alignment of the time slot of the SONET signal to be output and is supplied to the TOH INS 47.

BLSR Change Part (BLSR CHG)

Fig. 10 is a diagram illustrating a block diagram of an embodiment of the OR 71, 72 and the BLSR CHG 73. In the diagram, DCP-RIP-ENH (CH25 to 48), DTR-RIP-ENH (CH25 to 48), relief DTP-SW (CH1 to 24) at East side are supplied to the OR 71, and synchronized in a flip flop (FF) and subjected to OR operation, and synchronized in a flip flop (FF) 81 and supplied to a two port memory (MEMORY) 82 as the RIP information (CH25-48) at East side.

Further, the BLSR information of two bits is synchronized by a flip flop (FF) 83, and is supplied to a write address generator 84. The write address generator 84 generates a write address based on a timing signal and the aforementioned BLSR information and supplies to the memory 82. The write address is the value associated with the BLSR information, and the RIP information (CH25 to 48) at West side is written in the memory 82 at an address associated with the BLSR information.

Similarly, DCP-RIP-ENH (CH25 to 48), DTR-RIP-ENH (CH25 to 48), relief DTP-SW (CH1 to 24) at West side are supplied to the OR 72, and synchronized in a flip flop (FF) and subjected to OR operation, and synchronized in a flip flop (FF) 85 and supplied to a two port memory (MEMORY) 86 as the RIP information (CH25-48) at East side.

Further, the BLSR information of two bits is synchronized by a flip flop (FF) 87, and is supplied to a write address generator 88. The write address generator 88 generates a write address based on a timing signal and the aforementioned BLSR information and supplies to the memory 86. The write address is the value associated with the BLSR information, and the RIP information (CH25 to 48) at East side is written in the memory 86 at an address associated with the BLSR information.

A read address generator 90 generates a read address for synchronizing the memories 82, 86 based on a timing signal for sequential read, and supplies to the memories 82, 86. Herewith, the RIP information (CH25-48) at West side, East side in which channels are arranged in accordance with the configuration of BLSR is read from the memories 82, 86 and output from terminals 93, 94.

Incidentally, BLSR information of two bits indicates two fiber BLSR of OC-48

by "00", indicates two fiber BLSR of OC-192 by "01", indicates two fiber BLSR of OC-768 by "10", and indicates four fiber BLSR of OC-192 or OC-768 by "11".

The RIP control part 48 illustrated in Fig. 7 outputs RIP information of sys-number rule in which logical number is attached to a time slot as illustrated in Fig. 11. Sys numbers of 0 to F (hexadecimal) are attached for every side 1 (East side), side 2 (West side) of 48 channels. Note that among the aforementioned 48 channels, 0 to 24 channels are work channels and 25 to 48 channels are protection channels.

In the case (2F-BLSR of OC-48) where the BLSR information is "00", the setting unit is considered as channels corresponding to 4 sys (=386 channels), and as illustrated in Fig. 12, the read address of 128-adic counter (CTR 128) illustrated at right side is regarded as the same as the write address of 128-adic counter (CTR 128) illustrated at left side.

In the case (2F-BLSR of OC-192) where the BLSR information is "01", the setting unit is considered as channels corresponding to 4 sys (=384 channels), and as illustrated in Fig. 13, a read address of 128-adic counter (CTR 128) illustrated at right side is generated with respect to the write address of 128-adic counter (CTR 128) illustrated at left side. That is, [2:0] of three bits of the low-order of the read address of the memory are interchanged to [0], [1], [2] in the write address, thereby converting into alignment of the output of the BLSR change (BLSR CHG).

In the case (2F-BLSR of OC-768) where the BLSR information is "10", the setting unit is considered as channels corresponding to 16 sys (=1536 channels), and as illustrated in Fig. 14, a read address of 128-adic counter (CTR 128) illustrated at right side is generated with respect to the write address of 128-adic counter (CTR 128) illustrated at left side. That is, [4:0] of five bits of the low-order of the read address of the memory are interchanged to [0], [3], [4], [1], [2] in the write address, thereby converting into alignment of the output of the BLSR change (BLSR CHG). Note that, in Fig. 14, channels corresponding to 8 sys are illustrated, and the channels corresponding to the remaining 8 sys are also the same.

In the case (4F-BLSR of OC-192 or OC-768) where the BLSR information is "11", the setting unit shall be channels corresponding to 8 sys for OC-192, and channels corresponding to 32 sys for OC-768, and as illustrated in Fig. 15, a read address of 128-adic counter (CTR 128) illustrated at right side is generated with respect to the write address of 128-adic counter (CTR 128) illustrated at left side. That is, [4:0] of five bits of the low-order of the read address of the memory are interchanged to [1], [3], [4], [0], [2] in the write address, thereby converting into the alignment of the output of the BLSR change (BLSR CHG). Note that, in Fig. 15, channels corresponding to 8 sys are illustrated and the channels corresponding to

the remaining 24 sys for OC-768 are also the same.

Slot Change part (SLOT CHG)

Fig. 16 is a diagram illustrating a block diagram of an embodiment of the slot change part 74. In the diagram, RIP information of one bit at East side, West side is respectively input to terminals 101, 102. One of the RIP information is selected by a selector 103, and is supplied to a one port memory (MEMORY) 105 via a flip flop (FF) 104. Further, slot information of 6 bits is supplied to a read/write address generator 107 via a flip flop (FF) 106.

Herein, the slot information is physical configuration information of the node apparatus. Numbers are attached to the slot information to divide the interface cards 21-1 (IF#1) to 21-24 (IF#24) illustrated in Fig. 6 into, for example, a first half portion (first portion) and a second half portion (second portion). The slot information indicates a portion (first portion or second portion) of the interface card from which a time slot being input and being subjected to a cross connect processing at the present time is output.

A memory 108 has a slot change table in which slot information for indicating the first portion or the second portion of the interface card to which a time slot subjected to a cross connect processing is output by means of the slot information as an address is preliminarily stored. The slot change table is preliminarily determined for every node apparatus depending on the configuration of the node apparatus.

The read/write address generator 107 reads the memory 108 by means of the supplied information as an address, obtains slot information for indicating the first portion or the second portion of the interface card to which the time slot is output, generates a write address in which the slot information indicating the first portion or the second portion of the interface card is a high order address and count value (number of time slot) which is the counted timing signal is a low order address, and supplies to the memory 105. Herewith, RIP information corresponding to the time slot is written at the position corresponding to the first portion or the second portion of the interface card to which the time slot is output.

Further, the read/write address generator 107 counts a timing signal and generates a sequential read address and supplies to the memory 105. And time slot change is executed by reading the RIP information corresponding to the time slot in the order of the time slot of the SONET signal to be output. The RIP information read from the memory 105 is output from a terminal 110 via a flip flop (FF) 109, and is supplied to the transport overhead insertion part (TOH INS) 47.

ACM Code Interchange

Incidentally, an ACM code which is cross connect information used in the cross connect part (TSI) 43 illustrated in Fig. 7 is generated to be the same sys-

number rule as the RIP information, and the ACM code is subjected to a BLSR change and a slot change so as to be the slot rule, and is supplied to the TSI 43, and a cross connect of the time slot of the actual main signal is executed.

Fig. 17 is a diagram illustrating a block diagram of an embodiment in which the RIP information conversion part and an ACM code conversion part are partly commoditized. In the diagram, the RIP information (output of OR 71, 72) and the ACM code (after processed by service selector) are supplied to a BLSR change part (BLSR CHG) 123.

BLSR information is supplied to the BLSR CHG 123 from a memory 125, and the BLSR CHG 123 executes a BLSR change of the RIP information and the ACM code at the same time by simultaneously writing and reading the RIP information and the ACM code in and from an embedded memory corresponding to the memories 82, 83 in the RLSR CHG 73 illustrated in Fig. 10.

Slot information is supplied to a slot change part (SLOT CHG) 124 from a memory 126, and the SLOT CHG 124 executes a slot change of the RIP information and the ACM code at the same time by simultaneously writing and reading the RIP information and the ACM code in and from an embedded memory corresponding to the memory 105 in the SLOT CHG 74 illustrated in Fig. 16.

The RIP information output from the SLOT CHG 124 is supplied to the TOH INS 47 from a terminal 127. Further, the ACM code output from the SLOT CHG 124 is supplied to the TSI 43 from a terminal 128.

In the aforementioned embodiment, distributed processing becomes possible by providing the RIP conversion controller 33 that executes an RIP conversion processing in the interface card, thereby flexibly coping with increase of processing of the node apparatus.

Further, in the interface card, by separating the RIP information from the transport overhead after switching the work signal and protection signal by the SEL 37, increase of circuit dimension and power consumption is restrained, and it becomes easy to expand capacity for the future.

Further, by selecting alarm detection setting data (provisioning information) at a normal time and a relief SS time when the relief SS is provided for providing one system by the RIP conversion controller 33, the interface card is provided by using a generic ASSP (Application Specific Standard Product) chip.

Further, by equipping the BLSR CHG 73 and the SLOT CHG 74 in the switch fabrics 23, 24, RIP information is rearranged to meet the slot rule in the interface card, so that a path alarm detection function is equipped in the interface card, and it becomes possible for the interface card to execute a processing without depending on an application.

Further, by executing the processing of the BLSR change and the slot change

at the same time by using the BLSR CHG 123 and the SLOT CHG 124 by letting run cross connect information (ACM code) and converting information of RIP information in parallel, the circuit for executing the BLSR change and the slot change are commoditized and increase of circuit dimension/ power consumption are restrained.

Further, by transmitting RIP information to the interface card from the switch fabric by multiplexing in the section overhead of a SONET signal, increase of signal lines of the back plane board for connecting the switch fabric and the interface card are restrained.

Consequently, the above-mentioned node apparatus makes it possible to distribute processing by providing an RIP conversion processing in an interface unit, thereby flexibly coping with increase of processing.

All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions, nor does the organization of such examples in the specification relate to a showing of the superiority and inferiority of the invention. Although the embodiment of the present inventions has been described in detail, it should be understood that the various changes, substitutions, and alterations could be made hereto without departing from the scope of the claims.

CLAIMS

1. A node apparatus having a plurality of interface units for interfacing to a transmission line, switch units of a work system and a protection system for switching signals of the transmission line, and a service selector used to relieve a network failure over ring networks interconnected by node apparatuses, the node apparatus comprising:

a first controller for controlling the service selector in the switch units; and

a second controller for controlling setting information of alarm detection in case of using the service selector in the interface units.

2. The node apparatus according to claim 1, wherein

the second controller comprises storage for storing first setting information of a path alarm applied in case of a normal operation and storage for storing second setting information for the path alarm applied in case of using the service selector,

the second controller selects the first or second setting information, and applies the selected setting information for detecting the path alarm.

3. The node apparatus according to claim 2, wherein the second controller is allocated to connect a selector for selecting signals from the switch units of the work system and the protection system.

4. The node apparatus according to claim 3, wherein the switch unit comprises:

generation means of starting information for generating starting information used to relieve the network failure based on setting information used to relieve the network failure and information stored in a table for storing a span for passing through a channel signal;

allocating means of starting information for allocating the starting information into a time slot of a signal outputted from the switch unit; and

multiplexing means for multiplexing the starting information allocated into the time slot on an overhead area in the signal outputted from the switch unit.

5. The node apparatus according to claim 4, wherein the allocating means of starting information comprises a first allocating means for allocating the starting information based on a network formation and a second allocating means for allocating the starting information allocated by the first allocating means based on information of a physical formation.

6. The node apparatus according to claim 5, wherein the multiplexing means

multiplexes the starting information on a section overhead area in the signal outputted from the switch unit.

7. The node apparatus according to claim 6, wherein the second controller demultiplexes the starting information from the section overhead area received from the switch units of the work system and the protection system.

8. The node apparatus according to claim 7, wherein the allocating means of starting information that is shared with an allocating means of cross-connecting information of a main signal.

9. A node apparatus substantially in accordance with any of the embodiments hereinbefore described with reference to Figures 6 to 17 of the drawings.

Application No:	GB0918542.2	**Examiner:**	Owen Wheeler
Claims searched:	1-9	**Date of search:**	29 January 2010

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1 at least	US 5265096 A [PARRUCK] See Figs. 4,5a,5b and col. 6 ln. 7 to col. 7 ln. 31
X	1 at least	US 2006/274782 A1 [RIKITAKE] See whole document
X	1 at least	US 2006/018260 A1 [RICHMOND] See abstract
X	1 at least	US 2004/151172 A1 [NOTANI] See Fig. 5 and paras. 65-68
A	-	US 6337848 B1 [TAKATSU] See abstract.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
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Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC^{X} :

Worldwide search of patent documents classified in the following areas of the IPC

H04J; H04L

The following online and other databases have been used in the preparation of this search report

EPODOC, WPI, INSPEC

International Classification:

Subclass	Subgroup	Valid From
H04L	0012/437	01/01/2006