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(54) **METHOD AND SYSTEM FOR INTEGRATION OF BLUETOOTH AND FM LOCAL OSCILLATOR GENERATION INTO A SINGLE UNIT USING A DDFS**

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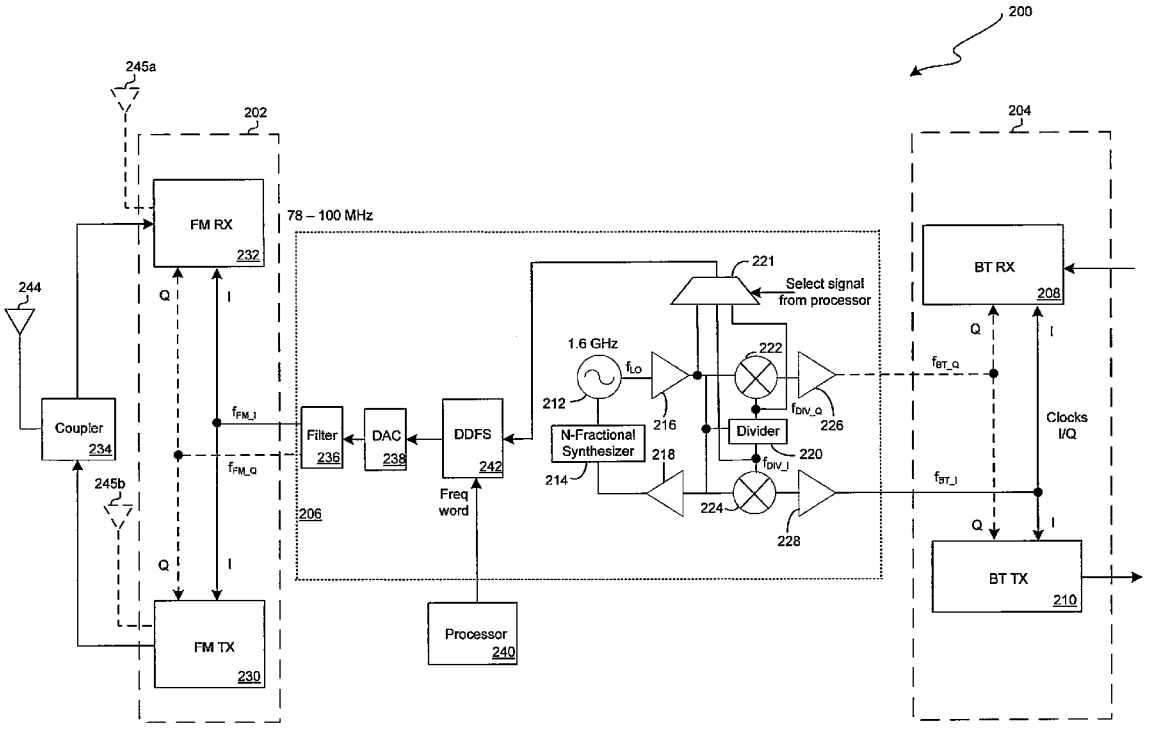
H04B 7/26 (2006.01)

(52) **U.S. Cl.** **375/355**

(57) **ABSTRACT**

Certain aspects of a method and system for integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS) may be disclosed. Aspects of the method may include generating a clock signal at a particular frequency in a chip that handles communication of Bluetooth signals and FM signals. The generated clock signal may be divided to produce a frequency divided clock signal, which may be mixed with the generated clock signal to enable transmission and/or reception of Bluetooth signals. The generated clock signal or the frequency divided clock signal may be selected for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission and/or reception of the FM signals.



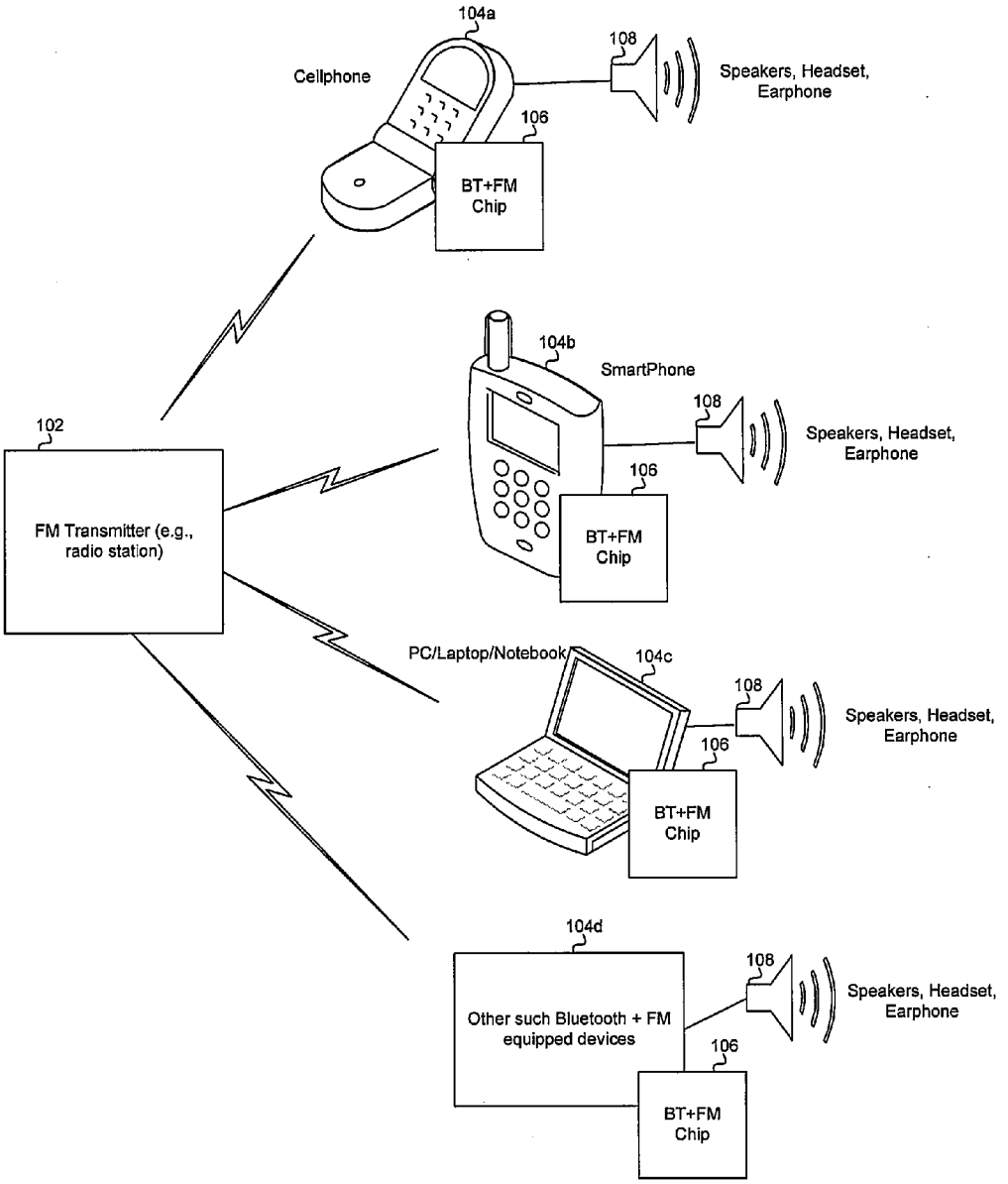

104a
Cellphone
108
Speakers, Headset, Earphone
106
BT+FM Chip
104b
SmartPhone
108
Speakers, Headset, Earphone
106
BT+FM Chip
102
FM Transmitter (e.g., radio station)
PC/Laptop/Notebook
104c
108
Speakers, Headset, Earphone
106
BT+FM Chip
104d
Other such Bluetooth + FM equipped devices
108
Speakers, Headset, Earphone
106
BT+FM Chip

FIG. 1A

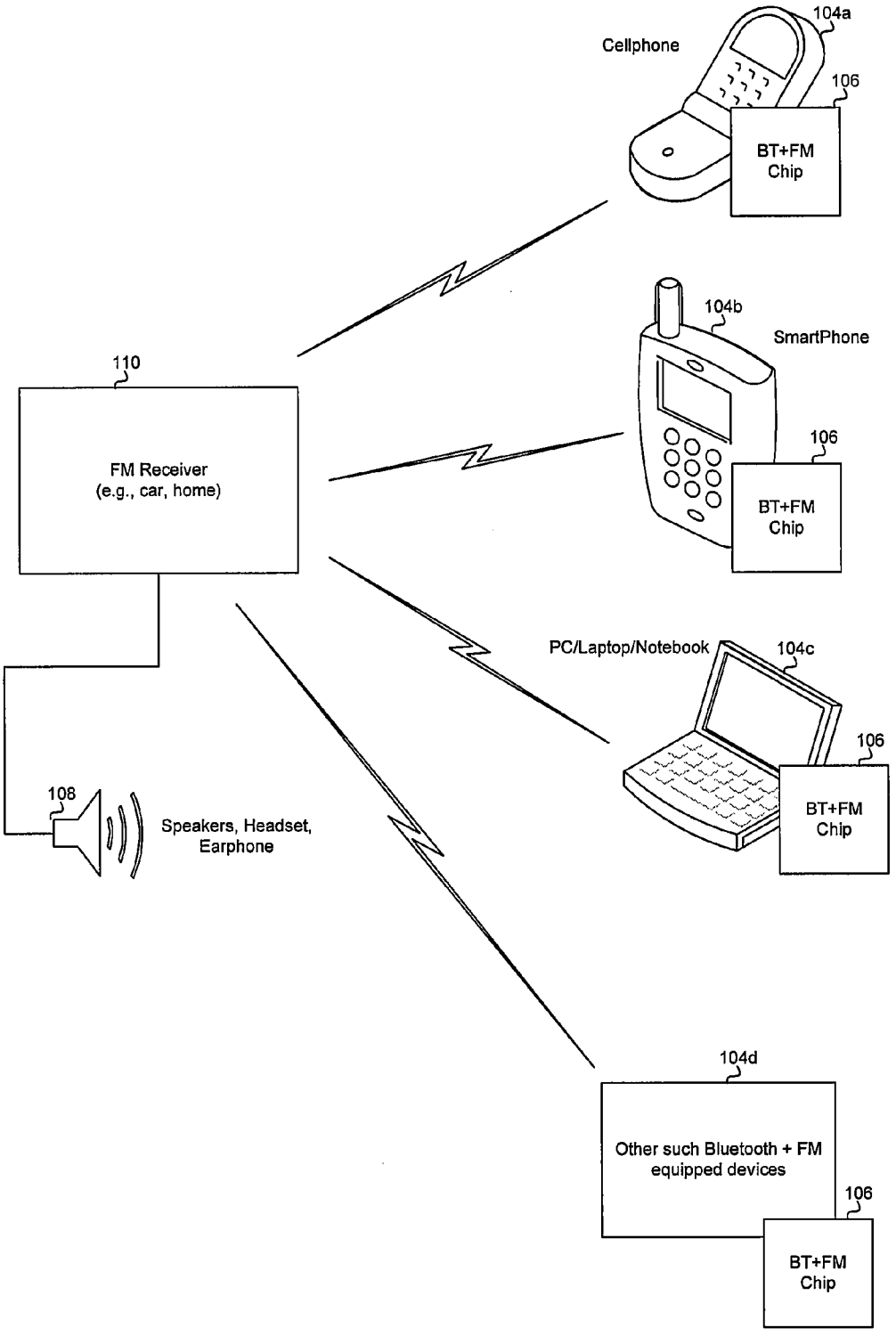

Cellphone
104a
106
BT+FM Chip
104b
SmartPhone
106
BT+FM Chip
110
FM Receiver (e.g., car, home)
PC/Laptop/Notebook
104c
106
BT+FM Chip
108
Speakers, Headset, Earphone
104d
Other such Bluetooth + FM equipped devices
106
BT+FM Chip

FIG. 1B

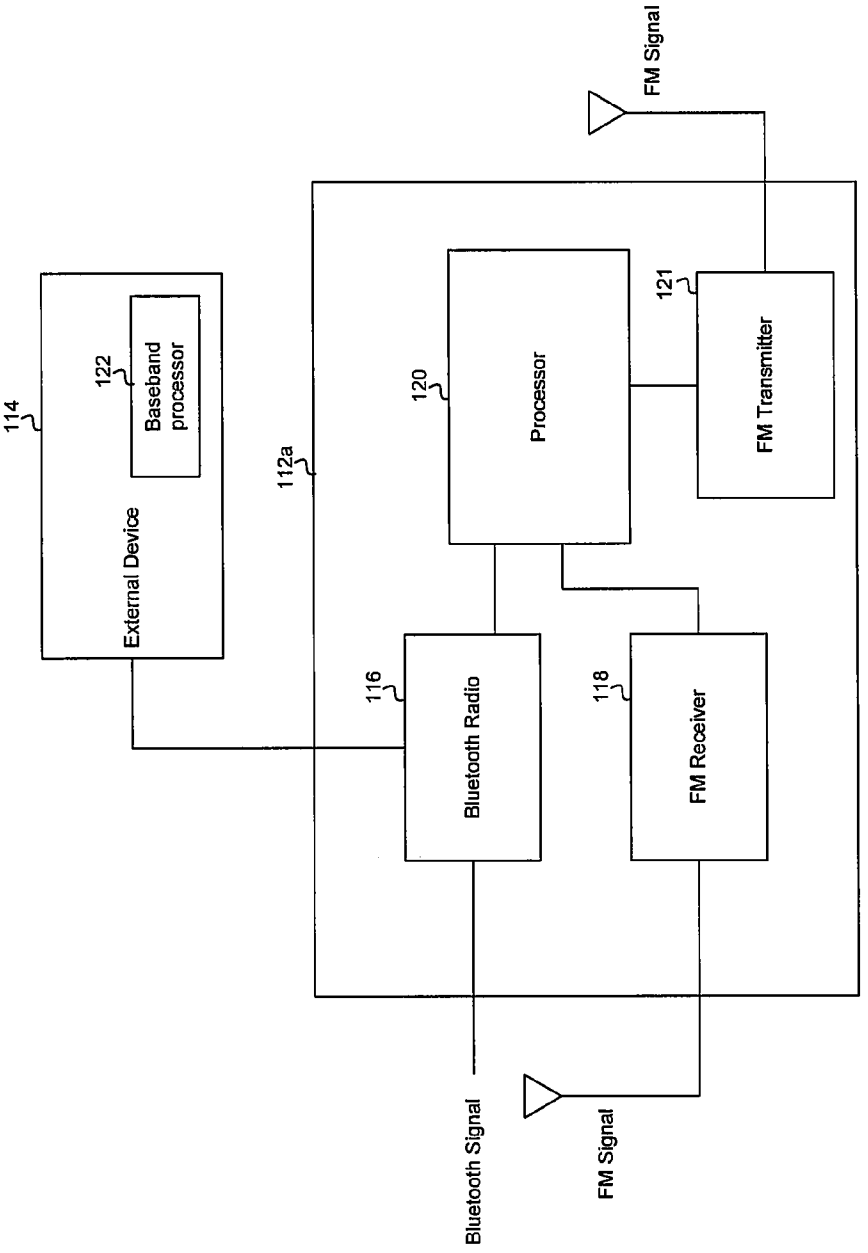

FM Signal
114
External Device
122
Baseband processor
112a
120
Processor
121
FM Transmitter
116
Bluetooth Radio
118
FM Receiver
Bluetooth Signal
FM Signal

FIG. 1C

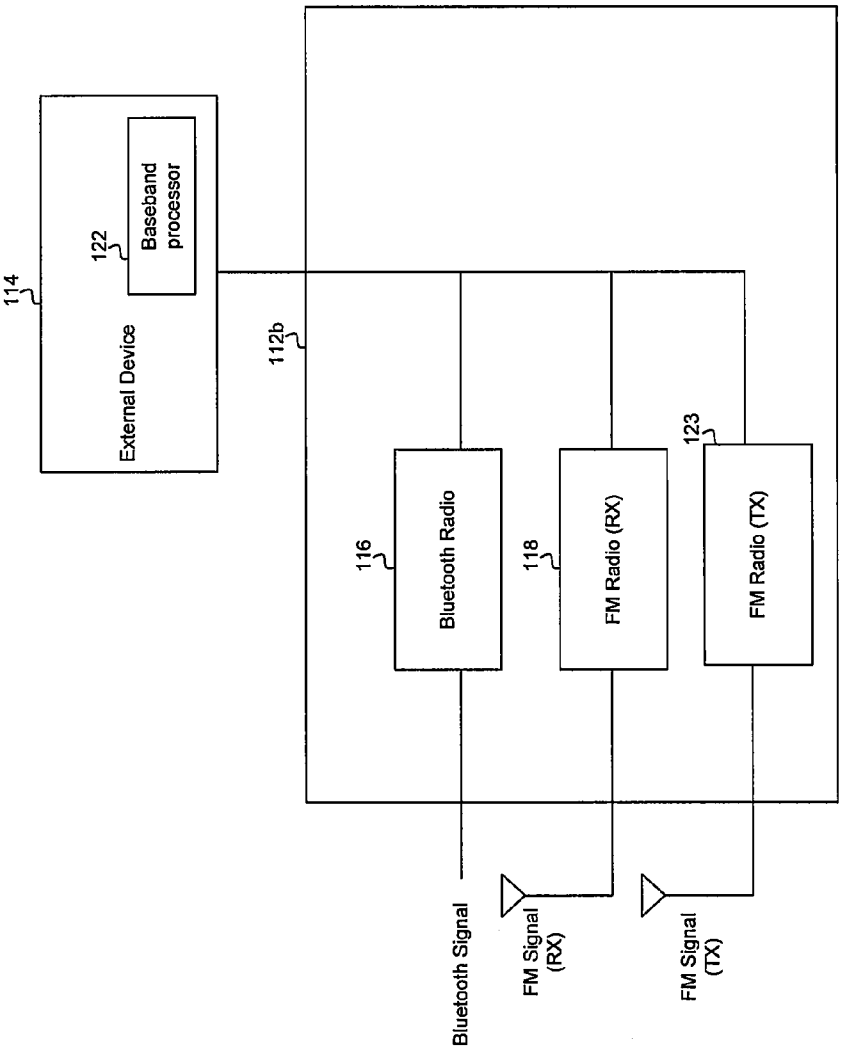

114
External Device
122
Baseband processor
112b
116
Bluetooth Radio
118
FM Radio (RX)
123
FM Radio (TX)
Bluetooth Signal
FM Signal (RX)
FM Signal (TX)

FIG. 1D

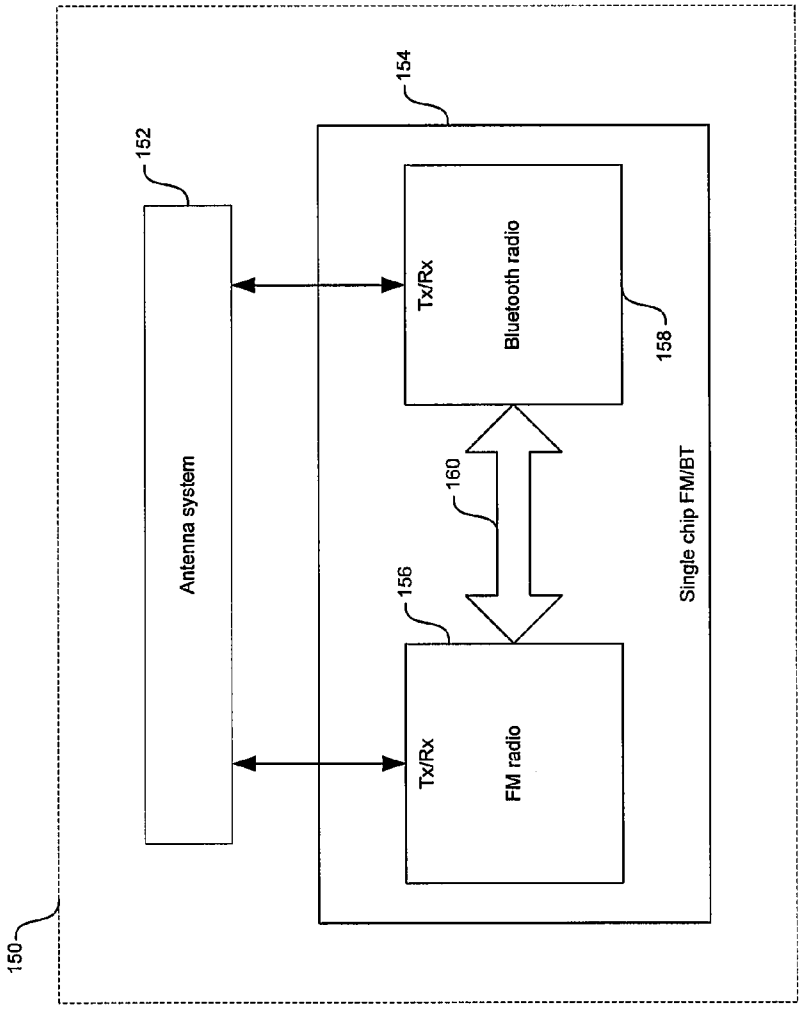

150
152
154
Antenna system
Tx/Rx
Bluetooth radio
158
160
156
Tx/Rx
FM radio
Single chip FM/BT

FIG. 1E

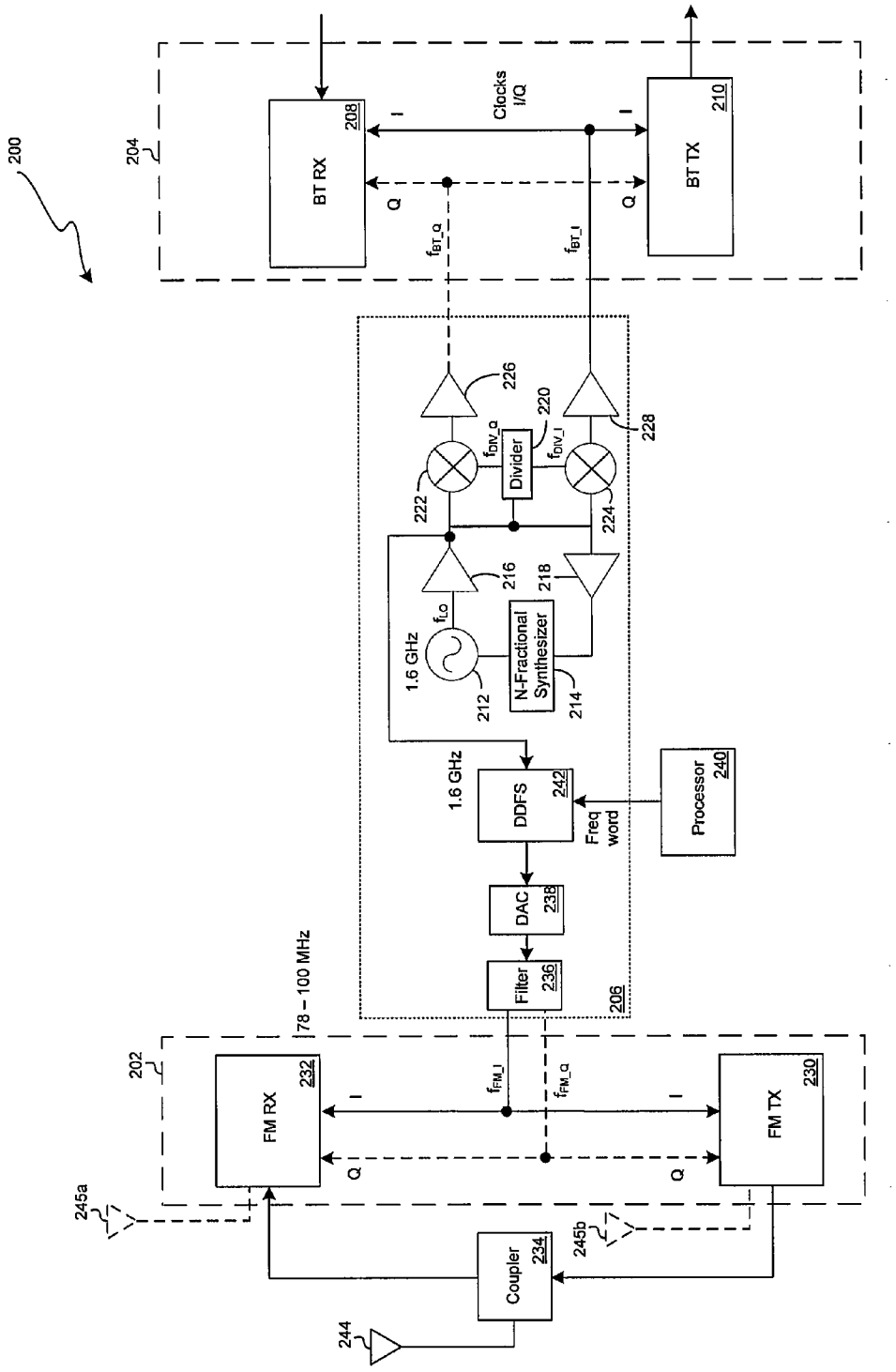

200
204
BT RX
208
Clocks
I/Q
BT TX
210
I
Q
f_{BT_Q}
f_{BT_I}
226
220
228
f_{DIV_Q}
Divider
f_{DIV_I}
222
224
216
218
f_{LO}
1.6 GHz
N-Fractional Synthesizer
212
214
1.6 GHz
DDFS
242
Freq word
Processor
240
DAC
238
Filter
236
206
78 – 100 MHz
202
FM RX
232
f_{FM_I}
f_{FM_Q}
FM TX
230
245a
245b
Coupler
234
244

FIG. 2A

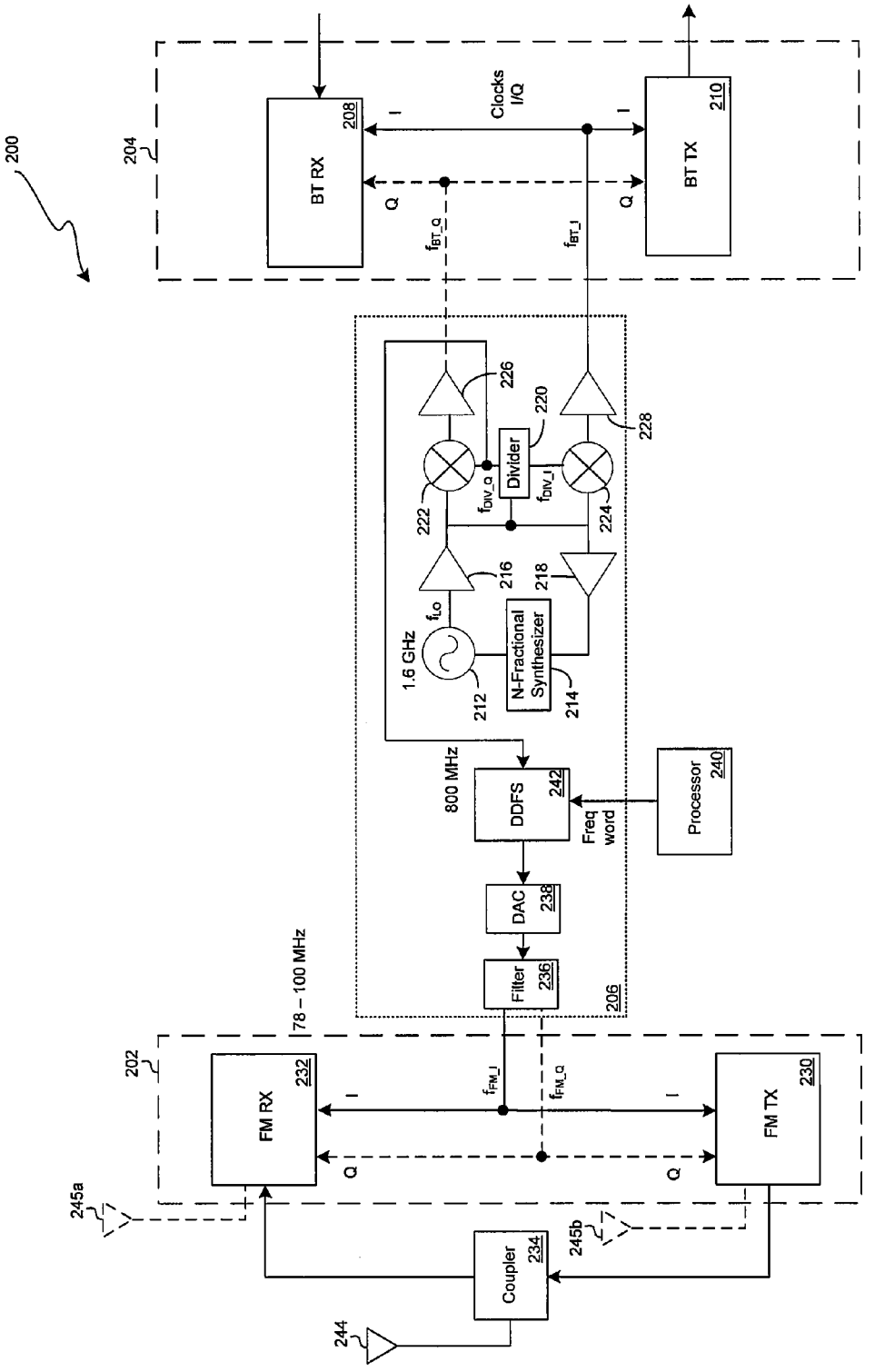

200
204
BT RX
208
Clocks
I/Q
BT TX
210
I
Q
f_{BT_Q}
f_{BT_I}
206
226
220
228
Divider
f_{DIV_Q}
f_{DIV_I}
222
224
216
218
f_{LO}
1.6 GHz
212
N-Fractional Synthesizer
214
800 MHz
DDFS
242
Freq word
Processor
240
DAC
238
Filter
236
78 – 100 MHz
202
FM RX
232
f_{FM_I}
f_{FM_Q}
FM TX
230
245a
245b
Coupler
234
244

FIG. 2B

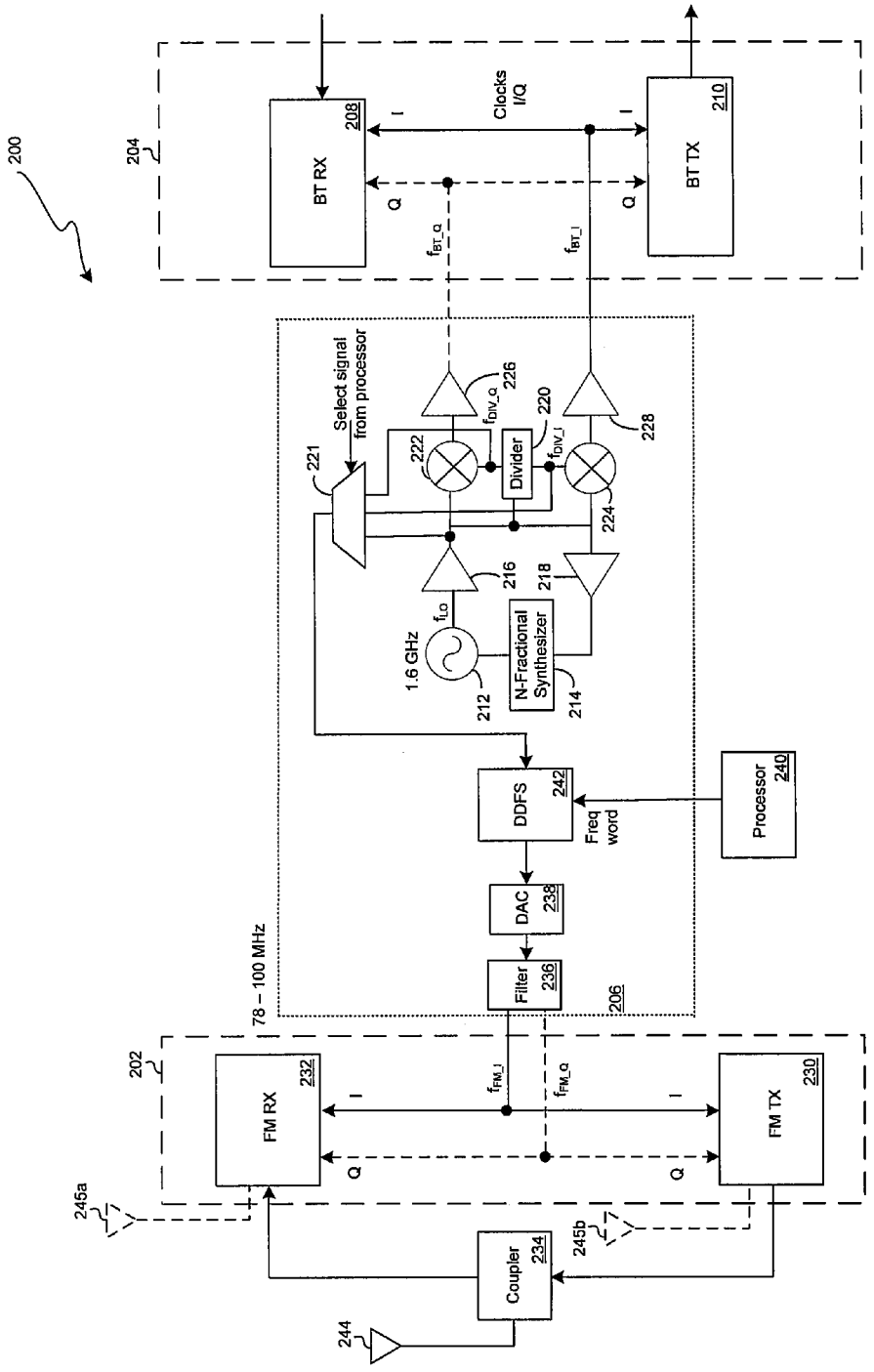

200
204
BT RX
208
Clocks
I/Q
BT TX
210
I
Q
f_{BT_Q}
f_{BT_I}
Select signal from processor
221
222
226
f_{DIV_Q}
220
Divider
f_{DIV_I}
228
224
216
218
f_{LO}
1.6 GHz
212
N-Fractional Synthesizer
214
DDFS
242
Freq word
Processor
240
DAC
238
Filter
236
206
78 – 100 MHz
202
FM RX
232
f_{FM_I}
f_{FM_Q}
FM TX
230
246a
245b
Coupler
234
244

FIG. 2C

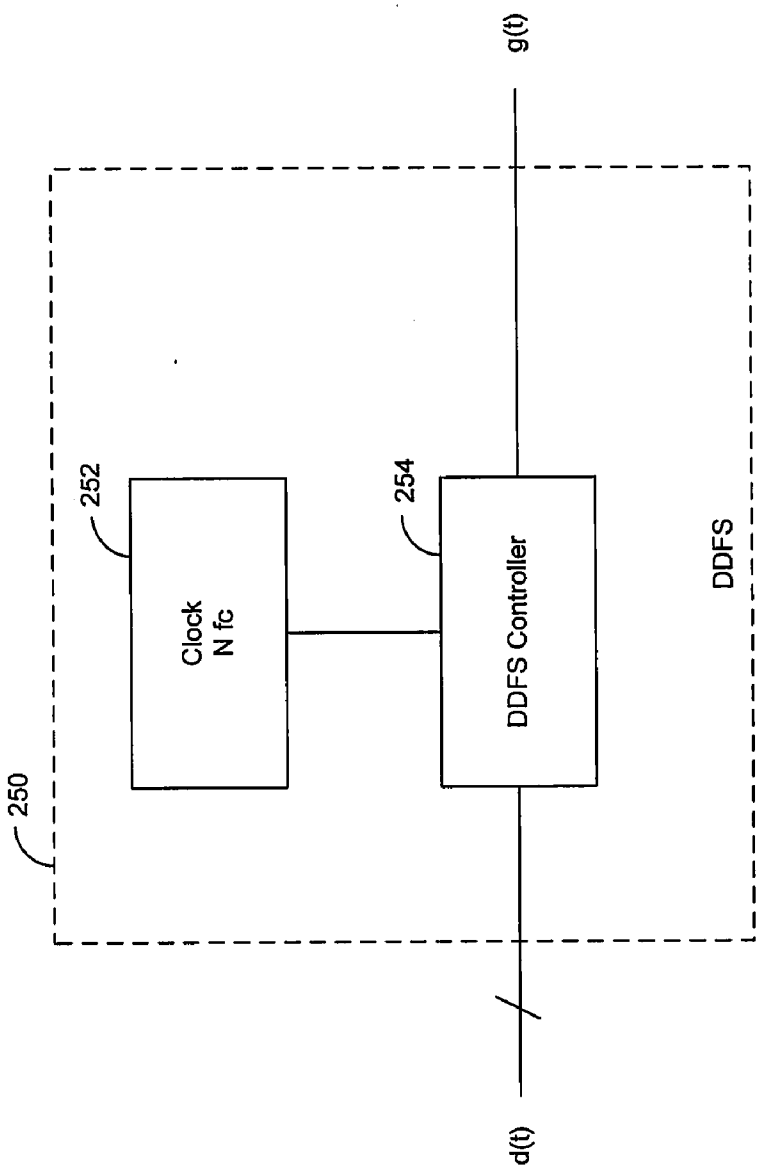


FIG. 2D

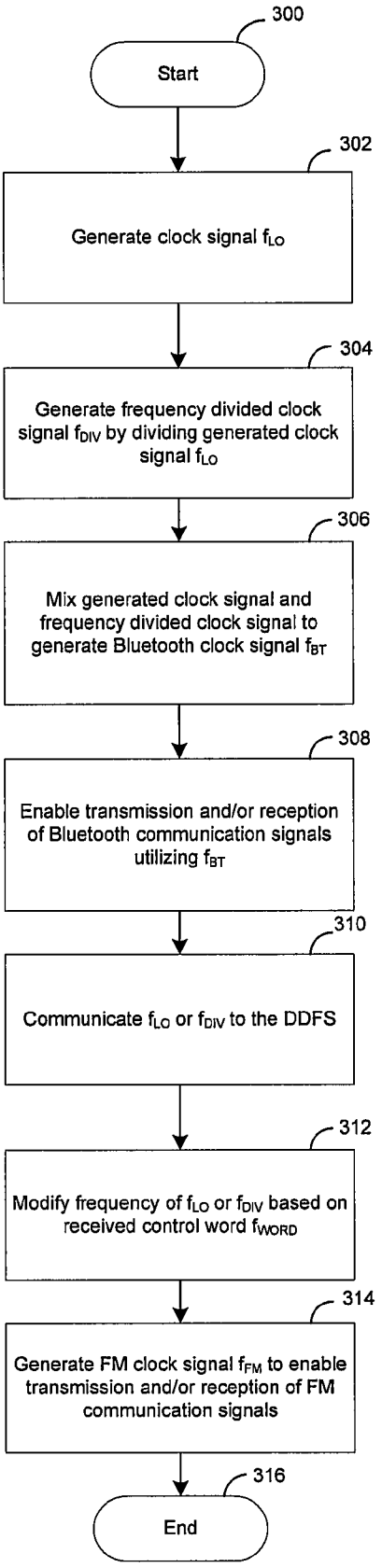

300
Start
302
Generate clock signal f_{LO}
304
Generate frequency divided clock signal f_{DIV} by dividing generated clock signal f_{LO}
306
Mix generated clock signal and frequency divided clock signal to generate Bluetooth clock signal f_{BT}
308
Enable transmission and/or reception of Bluetooth communication signals utilizing f_{BT}
310
Communicate f_{LO} or f_{DIV} to the DDFS
312
Modify frequency of f_{LO} or f_{DIV} based on received control word f_{WORD}
314
Generate FM clock signal f_{FM} to enable transmission and/or reception of FM communication signals
316
End

FIG. 3

METHOD AND SYSTEM FOR INTEGRATION OF BLUETOOTH AND FM LOCAL OSCILLATOR GENERATION INTO A SINGLE UNIT USING A DDFS

CROSS-REFERENCE TO RELATED APPLICATIONS/INCORPORATION BY REFERENCE

[0001] This application makes reference to, claims priority to, and claims benefit of U.S. Provisional Application Ser. No. 60/895,698 (Attorney Docket No. 18372US01) filed Mar. 19, 2007.

[0002] This application also makes reference to:
U.S. patent application Ser. No. _____ (Attorney Docket Number 18372US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18575US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18576US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18577US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18578US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18579US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18580US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18581US02) filed on even date herewith;
U.S. patent application Ser. No. _____ (Attorney Docket Number 18590US02) filed on even date herewith; and
U.S. patent application Ser. No. _____ (Attorney Docket Number 18591US02) filed on even date herewith.

[0003] Each of the above stated applications is hereby incorporated herein by reference in its entirety.

FIELD OF THE INVENTION

[0004] Certain embodiments of the invention relate to multi-standard systems. More specifically, certain embodiments of the invention relate to a method and system for integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS).

BACKGROUND OF THE INVENTION

[0005] A direct digital frequency synthesizer (DDFS) is a digitally-controlled signal generator that may vary the output signal frequency over a large range of frequencies, based on a single fixed-frequency precision reference clock. In addition, a DDFS is also phase-tunable. In essence, within the DDFS, discrete amplitude levels are input to a digital-to-analog converter (DAC) at a sampling rate determined by the fixed-frequency reference clock. The output of the DDFS may provide a signal whose shape may depend on the sequence of discrete amplitude levels that are input to the DAC at the constant sampling rate. The DDFS is particularly well suited as a frequency generator that outputs a sine or other periodic waveforms over a large range of frequencies, from almost DC to approximately half the fixed-frequency reference clock frequency.

[0006] A DDFS offers a larger range of operating frequencies and requires no feedback loop, thereby providing near instantaneous phase and frequency changes, avoiding overshooting, undershooting and settling time issues associated with other analog systems. A DDFS may provide precise digitally-controlled frequency and/or phase changes without signal discontinuities.

[0007] With the popularity of portable electronic devices and wireless devices that support audio applications, there is a growing need to provide a simple and complete solution for audio communications applications. For example, some users may utilize Bluetooth-enabled devices, such as headphones and/or speakers, to allow them to communicate audio data with their wireless handset while freeing to perform other activities. Other users may have portable electronic devices that may enable them to play stored audio content and/or receive audio content via broadcast communication, for example.

[0008] However, integrating multiple audio communication technologies into a single device may be costly. Combining a plurality of different communication services into a portable electronic device or a wireless device may require separate processing hardware and/or separate processing software. Moreover, coordinating the reception and/or transmission of data to and/or from the portable electronic device or a wireless device that uses FM transceivers may require significant processing overhead that may impose certain operation restrictions and/or design challenges.

[0009] Furthermore, simultaneous use of a plurality of radios in a handheld may result in significant increases in power consumption. Power being a precious commodity in most wireless mobile devices, combining devices such as a Bluetooth radio and a FM radio requires careful design and implementation in order to minimize battery usage. Additional overhead such as sophisticated power monitoring and power management techniques are required in order to maximize battery life.

[0010] Further limitations and disadvantages of conventional and traditional approaches will become apparent to one of skill in the art, through comparison of such systems with some aspects of the present invention as set forth in the remainder of the present application with reference to the drawings.

BRIEF SUMMARY OF THE INVENTION

[0011] A method and/or system for integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), substantially as shown in and/or described in connection with at least one of the figures, as set forth more completely in the claims.

[0012] These and other advantages, aspects and novel features of the present invention, as well as details of an illustrated embodiment thereof, will be more fully understood from the following description and drawings.

BRIEF DESCRIPTION OF SEVERAL VIEWS OF THE DRAWINGS

[0013] FIG. **1**A is a block diagram of an exemplary FM transmitter that communicates with handheld devices that utilize a single chip with integrated Bluetooth and FM radios, in accordance with an embodiment of the invention.

[0014] FIG. **1**B is a block diagram of an exemplary FM receiver that communicates with handheld devices that utilize a single chip with integrated Bluetooth and FM radios, in accordance with an embodiment of the invention.

[0015] FIG. **1**C is a block diagram of an exemplary single chip with integrated Bluetooth and FM radios that supports FM processing and an external device that supports Bluetooth processing, in accordance with an embodiment of the invention.

[0016] FIG. **1**D is a block diagram of an exemplary single chip with integrated Bluetooth and FM radios and an external device that supports Bluetooth and FM processing, in accordance with an embodiment of the invention.

[0017] FIG. **1**E is a block diagram that illustrates an exemplary single integrated circuit (IC) that supports FM and Bluetooth radio operations, in accordance with an embodiment of the invention.

[0018] FIG. **2**A is an exemplary block diagram of integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention.

[0019] FIG. **2**B is an exemplary block diagram of another embodiment of integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention.

[0020] FIG. **2**C is an exemplary block diagram of another embodiment of integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention.

[0021] FIG. **2**D is a block diagram illustrating an exemplary DDFS, in accordance with an embodiment of the invention.

[0022] FIG. **3** is a flowchart illustrating exemplary steps for integration of Bluetooth and FM local oscillator generation in a single unit using a DDFS, in accordance with an embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0023] Certain embodiments of the invention may be found in a method and system for integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS). Aspects of the method and system may comprise generating a clock signal f_{LO} at a particular frequency in a chip that handles communication of Bluetooth signals and FM signals. The generated clock signal f_{LO} may be divided to produce a frequency divided clock signal f_{DIV}, which may be mixed with the generated clock signal f_{LO} to enable transmission and/or reception of Bluetooth signals. The generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} may be selected for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission and/or reception of the FM signals.

[0024] FIG. **1**A is a block diagram of an exemplary FM transmitter that communicates with handheld devices that utilize a single chip with integrated Bluetooth and FM radios, in accordance with an embodiment of the invention. Referring to FIG. **1**A, there is shown an FM transmitter **102**, a cellular phone **104***a*, a smart phone **104***b*, a computer **104***c*, and an exemplary FM and Bluetooth-equipped device **104***d*. The FM transmitter **102** may be implemented as part of a radio station or other broadcasting device, for example. Each of the cellular phone **104***a*, the smart phone **104***b*, the computer **104***c*, and the exemplary FM and Bluetooth-equipped device **104***d* may comprise a single chip **106** with integrated Bluetooth and FM radios for supporting FM and Bluetooth data communications. The FM transmitter **102** may enable communication of FM audio data to the devices shown in FIG. **1**A by utilizing the single chip **106**. Each of the devices in FIG. **1**A may comprise and/or may be communicatively coupled to a listening device **108** such as a speaker, a headset, or an earphone, for example.

[0025] The cellular phone **104***a* may be enabled to receive an FM transmission signal from the FM transmitter **102**. The user of the cellular phone **104***a* may then listen to the transmission via the listening device **108**. The cellular phone **104***a* may comprise a "one-touch" programming feature that enables pulling up specifically desired broadcasts, like weather, sports, stock quotes, or news, for example. The smart phone **104***b* may be enabled to receive an FM transmission signal from the FM transmitter **102**. The user of the smart phone **104***b* may then listen to the transmission via the listening device **108**.

[0026] The computer **104***c* may be a desktop, laptop, notebook, tablet, and a PDA, for example. The computer **104***c* may be enabled to receive an FM transmission signal from the FM transmitter **102**. The user of the computer **104***c* may then listen to the transmission via the listening device **108**. The computer **104***c* may comprise software menus that configure listening options and enable quick access to favorite options, for example. In one embodiment of the invention, the computer **104***c* may utilize an atomic clock FM signal for precise timing applications, such as scientific applications, for example. While a cellular phone, a smart phone, computing devices, and other devices have been shown in FIG. **1**A, the single chip **106** may be utilized in a plurality of other devices and/or systems that receive and use Bluetooth and/or FM signals.

[0027] A clock signal f_{LO} may be generated at a particular frequency in the single chip **106** that handles communication of Bluetooth signals and FM signals. The generated clock signal f_{LO} may be utilized for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission of the FM signals.

[0028] FIG. **1**B is a block diagram of an exemplary FM receiver that communicates with handheld devices that utilize a single chip with integrated Bluetooth and FM radios, in accordance with an embodiment of the invention. Referring to FIG. **1**B, there is shown an FM receiver **110**, the cellular phone **104***a*, the smart phone **104***b*, the computer **104***c*, and the exemplary FM and Bluetooth-equipped device **104***d*. In this regard, the FM receiver **110** may comprise and/or may be communicatively coupled to a listening device **108**. A device equipped with the Bluetooth and FM transceivers, such as the single chip **106**, may be able to broadcast its respective signal to a "deadband" of an FM receiver for use by the associated audio system. For example, a cellphone or a smart phone, such as the cellular phone **104***a* and the smart phone **104***b*, may transmit a telephone call for listening over the audio system of an automobile, via usage of a deadband area of the car's FM stereo system. One advantage may be the universal ability to use this feature with all automobiles equipped simply with an FM radio with few, if any, other external FM transmission devices or connections being required.

[0029] In another example, a computer, such as the computer **104***c*, may comprise an MP3 player or another digital music format player and may broadcast a signal to the deadband of an FM receiver in a home stereo system. The music on the computer may then be listened to on a standard FM receiver with few, if any, other external FM transmission devices or connections. While a cellular phone, a smart

phone, and computing devices have been shown, a single chip that combines a Bluetooth and FM transceiver and/or receiver may be utilized in a plurality of other devices and/or systems that receive and use an FM signal.

[0030] A clock signal f_{LO} may be generated at a particular frequency in the single chip **106** that handles communication of Bluetooth signals and FM signals. The generated clock signal f_{LO} may be utilized for clocking one or more direct digital frequency synthesizers (DDFSs) to enable reception of the FM signals.

[0031] FIG. **1**C is a block diagram of an exemplary single chip with integrated Bluetooth and FM radios that supports FM processing and an external device that supports Bluetooth processing, in accordance with an embodiment of the invention. Referring to FIG. **1**C, there is shown a single chip **112***a* that supports Bluetooth and FM radio operations and an external device **114**. The single chip **112***a* may comprise an integrated Bluetooth radio **116**, an integrated FM receiver **118**, an integrated FM transmitter **121** and an integrated processor **120**. The Bluetooth radio **116** may comprise suitable logic, circuitry, and/or code that enable Bluetooth signal communication via the single chip **112***a*. In this regard, the Bluetooth radio **116** may support audio signals or communication. The FM receiver **118** may comprise suitable logic, circuitry, and/or code that enable FM signal communication via the single chip **112***a*.

[0032] The integrated processor **120** may comprise suitable logic, circuitry, and/or code that may enable processing of the FM data received by the FM receiver **118**. Moreover, the integrated processor **120** may enable processing of FM data to be transmitted by the FM receiver **118** when the FM receiver **118** comprises transmission capabilities. The external device **114** may comprise a baseband processor **122**. The baseband processor **122** may comprise suitable logic, circuitry, and/or code that may enable processing of Bluetooth data received by the Bluetooth radio **116**. Moreover, the baseband processor **122** may enable processing of Bluetooth data to be transmitted by the Bluetooth radio **116**. In this regard, the Bluetooth radio **116** may communicate with the baseband processor **122** via the external device **114**. The Bluetooth radio **116** may communicate with the integrated processor **120**. The FM transmitter **121** may comprise suitable logic, circuitry, and/or that may enable transmission of FM signals via appropriate broadcast channels, for example.

[0033] FIG. **1**D is a block diagram of an exemplary single chip with integrated Bluetooth and FM radios and an external device that supports Bluetooth and FM processing, in accordance with an embodiment of the invention. Referring to FIG. **1**D, there is shown a single chip **112***b* that supports Bluetooth and FM radio operations and an external device **114**. The single chip **112***b* may comprise the Bluetooth radio **116**, FM receive radio **118**, and FM transmit radio **123**. The Bluetooth radio **116**, the FM receive radio **118** and FM transmit radio **123** may be integrated into the single chip **112***b*. The external device **114** may comprise a baseband processor **122**. The baseband processor **122** may comprise suitable logic, circuitry, and/or code that may enable processing of Bluetooth data received by the Bluetooth radio **116** and/or processing of Bluetooth data to be transmitted by the Bluetooth radio **116**. In this regard, the Bluetooth radio **116** may communicate with the baseband processor **122** via the external device **114**. Moreover, the baseband processor **122** may comprise suitable logic, circuitry, and/or code that may enable processing of the FM data received by the FM receive radio **118**. The baseband processor **122** may enable processing FM data to be transmitted by the FM transmit radio **123**. In this regard, the FM receive radio **118** and the FM transmit radio **123** may communicate with the baseband processor **122** via the external device **114**.

[0034] FIG. **1**E is a block diagram that illustrates an exemplary single radio chip that supports FM and Bluetooth radio operations, in accordance with an embodiment of the invention. Referring to FIG. **1**F, there is shown a mobile phone **150** that may comprise a FM/Bluetooth coexistence antenna system **152** and a single chip FM/Bluetooth (FM/BT) radio device **154**. The single chip FM/BT radio device **154** may comprise a FM radio portion **156** and a Bluetooth radio portion **158**. The single chip FM/BT radio device **154** may be implemented based on a system-on-chip (SOC) architecture, for example.

[0035] The FM/Bluetooth coexistence antenna system **152** may comprise suitable hardware, logic, and/or circuitry that may be enabled to provide FM and Bluetooth communication between external devices and a coexistence terminal. The FM/Bluetooth coexistence antenna system **152** may comprise at least one antenna for the transmission and reception of FM and Bluetooth packet traffic.

[0036] The FM radio portion **156** may comprise suitable logic, circuitry, and/or code that may be enabled to process FM packets for communication. The FM radio portion **156** may be enabled to transfer and/or receive FM packets and/or information to the FM/Bluetooth coexistence antenna system **152** via a single transmit/receive (Tx/Rx) port. In some instances, the transmit port (Tx) may be implemented separately from the receive port (Rx). The FM radio portion **156** may also be enabled to generate signals that control at least a portion of the operation of the FM/Bluetooth coexistence antenna system **152**. Firmware operating in the FM radio portion **156** may be utilized to schedule and/or control FM packet communication, for example.

[0037] The FM radio portion **156** may also be enabled to receive and/or transmit priority signals **160**. The priority signals **160** may be utilized to schedule and/or control the collaborative operation of the FM radio portion **156** and the Bluetooth radio portion **158**. The Bluetooth radio portion **158** may comprise suitable logic, circuitry, and/or code that may be enabled to process Bluetooth protocol packets for communication. The Bluetooth radio portion **158** may be enabled to transfer and/or receive Bluetooth protocol packets and/or information to the FM/Bluetooth coexistence antenna system **152** via a single transmit/receive (Tx/Rx) port. In some instances, the transmit port (Tx) may be implemented separately from the receive port (Rx). The Bluetooth radio portion **158** may also be enabled to generate signals that control at least a portion of the operation of the FM/Bluetooth coexistence antenna system **152**. Firmware operating in the Bluetooth radio portion **158** may be utilized to schedule and/or control Bluetooth packet communication. The Bluetooth radio portion **158** may also be enabled to receive and/or transmit priority signals **160**. A portion of the operations supported by the FM radio portion **156** and a portion of the operations supported by the Bluetooth radio portion **158** may be performed by common logic, circuitry, and/or code.

[0038] In some instances, at least a portion of either the FM radio portion **156** or the Bluetooth radio portion **158** may be disabled and the wireless terminal may operate in a single-communication mode, that is, coexistence may be disabled. When at least a portion of the FM radio portion **156** is dis-

abled, the FM/Bluetooth coexistence antenna system **152** may utilize a default configuration to support Bluetooth communication. When at least a portion of the Bluetooth radio portion **158** is disabled, the FM/Bluetooth coexistence antenna system **152** may utilize a default configuration to support FM communication.

[0039] In accordance with an embodiment of the invention, a clock signal f_{LO} may be generated at a particular frequency in the single chip FM/BT radio device **154** that handles communication of Bluetooth signals and FM signals. The generated clock signal f_{LO} may be divided to produce a frequency divided clock signal f_{DIV}, which may be mixed with the generated clock signal f_{LO} to enable transmission and/or reception of Bluetooth signals. The generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} may be selected for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission and/or reception of the FM signals.

[0040] FIG. **2**A is an exemplary block diagram of integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention. Referring to FIG. **2**A, there is shown a communication system **200**. The communication system **200** comprises a FM transceiver **202**, a Bluetooth transceiver **204**, a processor **240**, a local oscillator generation unit (LOGEN) **206**, and a coupler **234** coupled to an antenna **244**. The FM transceiver **202** may comprise a FM receiver **232** and a FM transmitter **230**. The Bluetooth transceiver **204** may comprise a Bluetooth receiver **208** and a Bluetooth transmitter **210**. The LOGEN **206** may comprise a filter **236**, a digital to analog converter (DAC) **238** a direct digital frequency synthesizer (DDFS) **242**, a voltage controlled oscillator (VCO) **212**, a plurality of loop amplifiers **216**, **218**, **226**, and **228**, a plurality of mixers **222** and **224**, a fractional synthesizer **214**, and a divider **220**.

[0041] The LOGEN **206** may comprise suitable logic, circuitry, and/or code that may be enabled to generate a Bluetooth clock signal f_{BT} comprising an in-phase (I) component f_{BT_I} and a quadrature-phase (Q) component f_{BT_Q}. The I component and Q component signals may be communicated to the Bluetooth receiver **208** and the Bluetooth transmitter **210**. The frequency of the generated Bluetooth clock signal f_{BT} to the Bluetooth receiver **208** and the Bluetooth transmitter **210** may be about 2.4 GHz, for example, and may be enabled to clock one or more of the Bluetooth receiver **208** and the Bluetooth transmitter **210**. The LOGEN **206** may also be enabled to generate an I component and a Q component output signal, f_{FM_I} and f_{FM_Q} respectively to the FM transceiver **202**. The I and Q component signals, f_{FM_I} and f_{FM_Q} respectively may be communicated to the FM receiver **232** and the FM transmitter **230**. The frequency of the generated FM clock signal f_{FM} to the FM receiver **232** and the FM transmitter **230** may be about 78-100 MHz, for example, and may be enabled to clock one or more of the FM receiver **232** and the FM transmitter **230**.

[0042] The VCO **212** may comprise suitable logic, circuitry, and/or code that may be enabled to generate a clock signal f_{LO} at a particular frequency that may be N times the frequency of the reference oscillator, Nf_0, for example, where f_0 is the frequency of the reference oscillator. For example, the VCO **212** may be enabled to generate a 1.6 GHz clock signal.

[0043] The loop amplifier **216** may comprise suitable logic, circuitry, and/or code that may be enabled to amplify the generated clock signal f_{LO} received from the VCO **212**. The loop amplifier **216** may be enabled to generate an amplified output signal to the plurality of mixers **222** and **224**, and the divider **220**. The loop amplifier **218** may comprise suitable logic, circuitry, and/or code that may be enabled to amplify a received signal from the loop amplifier **216** and generate an amplified output signal to the fractional synthesizer **214**.

[0044] The fractional synthesizer **214** may comprise suitable logic, circuitry, and/or code that may be enabled to divide the output of the VCO **212** by N, for example, to match the frequency of a reference oscillator. The fractional synthesizer **214** may be programmable to synthesize a plurality of closely spaced frequencies, which enables it to be utilized in applications such as in commercial wireless applications with multiple channels, for example. In an embodiment, the fractional synthesizer **214** may be enabled to adjust a clock signal f_{LO} generated by the VCO **212** without affecting the Bluetooth clock signals f_{BT} communicated to the Bluetooth transceiver **204**.

[0045] The divider **220** may comprise suitable logic, circuitry, and/or code that may be enabled to divide a frequency of a received input signal into one or more signals with different frequencies. For example, the divider **220** may be enabled to receive a 1.6 GHz input signal from the loop amplifier **222** and generate two 800 MHz output signals, for example, to the plurality of mixers **222** and **224**. The divider **220** may be enabled to generate an output clock signal f_{DIV} by dividing a frequency of the generated clock signal f_{LO}.

[0046] The mixer **222** may comprise suitable logic, circuitry, and/or code that may be enabled to mix the received input signals from the loop amplifier **216** and the divider **220** and generate an output signal to the loop amplifier **226**. For example, the mixer **222** may be enabled to mix a 1.6 GHz input signal from the loop amplifier **216** and a 800 MHz input signal from the divider **220** and generate a 2.4 GHz output signal to the loop amplifier **226**. The loop amplifier **226** may be enabled to amplify the received input signal from the mixer **222** and generate an amplified output signal to one or more of the Bluetooth receiver **208** and the Bluetooth transmitter **210**. For example, the loop amplifier **226** may be enabled to generate the Q component f_{BT_Q} of the amplified output signal to one or more of the Bluetooth receiver **208** and the Bluetooth transmitter **210**.

[0047] The mixer **224** may comprise suitable logic, circuitry, and/or code that may be enabled to mix the received input signals from the loop amplifier **216** and the divider **220** and generate an output signal to the loop amplifier **228**. For example, the mixer **224** may be enabled to mix a 1.6 GHz input signal from the loop amplifier **216** and a 800 MHz input signal from the divider **220** and generate a 2.4 GHz output signal to the loop amplifier **228**. The loop amplifier **228** may be enabled to amplify the received input signal from the mixer **224** and generate an amplified output signal to one or more of the Bluetooth receiver **208** and the Bluetooth transmitter **210**. For example, the loop amplifier **228** may be enabled to generate the I component f_{BT_I} of the amplified output signal to one or more of the Bluetooth receiver **208** and the Bluetooth transmitter **210**.

[0048] In operation, the fractional synthesizer **214** may be enabled to generate a control signal, which may be utilized by the VCO **212** to generate a clock signal f_{LO}. In an exemplary embodiment of the invention, the frequency of the clock signal, f_{LO}, may be about 1.6 GHz. The fractional synthesizer **214** may utilize the clock signal, f_{LO} to adjust a subsequent control signal communicated to the VCO **212**. The clock

signal, f_{LO}, may be communicated to a divider **220**, which may implement frequency division on the received signal f_{LO}. The divider **220** may generate an output clock signal, f_{DIV} comprising in-phase (I) component frequency division signal, f_{DIV_I}, and a quadrature-phase (Q) component frequency division signal, f_{DIV_Q}. In an exemplary embodiment of the invention:

$$f_{\mathrm{DIV\_I}} = f_{\mathrm{DIV\_Q}} = \frac{f_{LO}}{2} \quad [1]$$

[0049] The mixer **224** may be enabled to mix the signals, f_{LO} and f_{DIV_I}, and generate a signal f_{BT_I}. The mixer **222** may mix the signals, f_{LO} and f_{DIV_Q}, and generate a signal f_{BT_Q}. In an exemplary embodiment of the invention, the frequencies of the signals f_{BT_I} and f_{BT_Q} may be represented as follows:

$$f_{BT\_I}=f_{LO}+f_{DIV\_I} \quad [2]$$

and

$$f_{BT\_Q}=f_{LO}+f_{DIV\_Q} \quad [3]$$

The signals f_{BT_I} and f_{BT_Q} may be communicated to the Bluetooth receiver **208** and/or to the Bluetooth transmitter **210**. In an exemplary embodiment of the invention, the frequency of the signals f_{BT_I} and f_{BT_Q} may be about 2.4 GHz.

[0050] In an embodiment of the invention, the clock signal f_{LO} may be communicated to the DDFS **242**. The DDFS **242** may comprise suitable logic, circuitry and/or code that may enable reception of the clock signal f_{LO} and generate a sequence of binary numbers. The process of converting the clock signal f_{LO} input signal to a sequence of binary numbers may comprise analog to digital conversion (ADC) whereby each distinct voltage, current and/or power level associated with the received clock signal, f_{LO} may be represented as a binary number selected from a plurality of binary numbers. Conversely, each binary number may correspond to a range of voltage, current and/or power levels in the received clock signal f_{LO}. An exemplary clock signal, f_{LO} may be a sinusoidal signal for which the corresponding period may be equal to the inverse of the frequency, $(1/f_{LO})$.

[0051] The number of binary numbers may be determined by the number of bits, b, in the binary number representation. Each binary number may comprise a least significant bit (LSB) and a most significant bit (MSB). In an exemplary numerical representation, each of binary numbers may have a value within the range 0 to 2^b-1. The operation of the DDFS **242** may be such that a period of the received clock signal, f_{LO} may be converted to a binary sequence $0, 1, \ldots, 2^b-1$, wherein upon reaching the value 2^b-1 the next number in the binary sequence may be 0 with the sequence continuing. The set of numbers from 0 to 2^b-1 may represent a period of the binary sequence. The DDFS **242** may receive a frequency word input signal, f_{Word}, from the processor **240** upon which the value of b may be determined. Consequently, the period of the sequence of binary numbers generated by the DDFS may be programmable based on the f_{Word} input signal.

[0052] The DAC **238** may comprise suitable logic, circuitry and/or code that may enable generation of an analog output signal based on a received sequence of input binary numbers. The DAC **238** may be enabled to generate a corresponding analog voltage level for each input binary number. The number of distinct analog voltage levels may be equal to the number of distinct binary numbers in the input sequence.

[0053] The filter **238** may comprise suitable logic, circuitry and/or code that may enable low pass filtering (LPF) of signal components contained in a received input signal. The filter **238** may enable smoothing of the received input signal to attenuate amplitudes for undesirable frequency components contained in the received input signal. The filter **238** may generate a signal, f_{FM}, having a frequency in the FM frequency band. In an exemplary embodiment of the invention, the range of frequencies for the signal f_{FM} may be between about 78 MHz and 100 MHz, for example. The signal f_{FM} may be a quadrature signal comprising I and Q signal components, f_{FM_I} and f_{FM_Q} respectively. The 78-100 MHz I and Q signals may be communicated to an FM transmitter **230** and/or an FM receiver **232**.

[0054] In an exemplary embodiment of the invention, the FM transmitter **230** and the FM receiver **232** may be coupled to an antenna **244** via a bidirectional coupler **234**. The bidirectional coupler **234** may couple the antenna to the FM receiver **232** at a given time instant, such that the FM receiver **232** signal may receive signals via the antenna **244**. The bidirectional coupler **234** may couple the antenna to the FM transmitter **230** at a different time instant under the control of a different f_{Word} to the DDFS **242**, such that the FM transmitter **230** signal may transmit signals via the antenna **244**. In another exemplary embodiment of the invention, the FM transmitter **230** may be coupled to a transmitting antenna **245***b*, while the FM receiver **232** may be coupled to a receiving antenna **245***a*.

[0055] In operation, the value f_{Word} may be selected to maintain an approximately constant frequency for the signal f_{FM} despite changes that may occur in the signal f_{LO}, which may occur due to frequency hopping in the Bluetooth communication signal.

[0056] FIG. **2**B is an exemplary block diagram of another embodiment illustrating integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention. Referring to FIG. **2**B, there is shown a communication system **200**. The communication system **200** comprises a FM transceiver **202**, a Bluetooth transceiver **204**, a processor **240**, a local oscillator generation unit (LOGEN) **206**, and a coupler **234** coupled to an antenna **244**. The FM transceiver **202** may comprise a FM receiver **232** and a FM transmitter **230**. The Bluetooth transceiver **204** may comprise a Bluetooth receiver **208** and a Bluetooth transmitter **210**. The LOGEN **206** may comprise a filter **236**, a digital to analog converter (DAC) **238**, a direct digital frequency synthesizer (DDFS) **242**, a voltage controlled oscillator (VCO) **212**, a plurality of loop amplifiers **216**, **218**, **226**, and **228**, a plurality of mixers **222** and **224**, a fractional synthesizer **214**, and a divider **220**. The various components of FIG. **2**B may be substantially as described in FIG. **2**A

[0057] In operation, the fractional synthesizer **214** may be enabled to generate a control signal, which may be utilized by the VCO **212** to generate a clock signal. In an exemplary embodiment of the invention, the frequency of the clock signal, f_{LO}, may be about 1.6 GHz. The fractional synthesizer **214** may utilize the clock signal, f_{LO} to adjust a subsequent control signal communicated to the VCO **212**. The clock signal, f_{LO}, may be communicated to a divider **220**, which may implement frequency division on the received signal f_{LO}. The divider **220** may generate an in-phase (I) component

frequency division signal, f_{DIV_I}, and a quadrature-phase (Q) component frequency division signal, f_{DIV_Q}. In an exemplary embodiment of the invention:

$$f_{DIV\_I} = f_{DIV\_Q} = \frac{f_{LO}}{2} \quad [1]$$

[0058] The mixer **224** may be enabled to receive the signals, f_{LO} and f_{DIV_I}, and generate a signal f_{BT_I}. The mixer **222** may receive the signals, f_{LO} and f_{DIV_Q}, and generate a signal f_{BT_Q}. In an exemplary embodiment of the invention, the frequencies of the signals f_{BT_I} and f_{BT_Q} may be represented as follows:

$$f_{BT\_I}=f_{LO}+f_{DIV\_I} \quad [2]$$

and

$$f_{BT\_Q}=f_{LO}=f_{DIV\_Q} \quad [3]$$

The signals f_{BT_I} and f_{BT_Q} may be communicated to the Bluetooth receiver **208** and/or to the Bluetooth transmitter **210**. In an exemplary embodiment of the invention, the frequency of the signals f_{BT_I} and f_{BT_Q} may be about 2.4 GHz.

[0059] In another embodiment of the invention, the signal f_{DIV_I} or the signal f_{DIV_Q} may be communicated to the DDFS **242**. The DDFS **242** may comprise suitable logic, circuitry and/or code that may enable reception of the f_{DIV_I} or f_{DIV_Q} input signal and subsequent generation of a sequence of binary numbers. The process of converting the f_{DIV_I} or f_{DIV_Q} input signal to a sequence of binary numbers may comprise analog to digital conversion (ADC) whereby each distinct voltage, current and/or power level associated with the received f_{DIV_I} or f_{DIV_Q} signal may be represented as a binary number selected from a plurality of binary numbers. Conversely, each binary number may correspond to a range of voltage, current and/or power levels in the received f_{DIV_I} or f_{DIV_Q} signal.

[0060] In an embodiment of the invention, f_{DIV_I} or f_{DIV_Q} may be a sinusoidal signal for which the corresponding period may be equal to the inverse of the frequency, $(1/f_{DIV\_I})$ or $(1/f_{DIV\_Q})$. The number of binary numbers in the plurality may be determined by the number of bits, b, contained in the binary number representation. Each binary number may comprise a least significant bit (LSB) and a most significant bit (MSB). In an exemplary numerical representation, each of the binary numbers may have a value within the range 0 to 2^b-1. The operation of the DDFS **242** may be such that a period of the received f_{DIV_I} or f_{DIV_Q} signal may be converted to binary sequence 0, 1, . . . , 2^b-1, wherein upon reaching the value 2^b-1 the next number in the binary sequence may be 0 with the sequence continuing. The set of numbers from 0 to 2^b-1 may represent a period of the binary sequence. The DDFS **242** may receive a frequency word input signal, f_{Word}, from the processor **240** upon which the value of b may be determined. Consequently, the period of the sequence of binary numbers generated by the DDFS **242** may be programmable based on the f_{Word} input signal.

[0061] FIG. **2**C is an exemplary block diagram of another embodiment illustrating integration of Bluetooth and FM local oscillator generation in a single unit using a direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention. Referring to FIG. **2**C, there is shown a communication system **200**. The communication system **200** comprises a FM transceiver **202**, a Bluetooth transceiver **204**, a processor **240**, a local oscillator generation unit (LOGEN) **206**, and a coupler **234** coupled to an antenna **244**. The FM transceiver **202** may comprise a FM receiver **232** and a FM transmitter **230**. The Bluetooth transceiver **204** may comprise a Bluetooth receiver **208** and a Bluetooth transmitter **210**. The LOGEN **206** may comprise a filter **236**, a digital to analog converter (DAC) **238**, a direct digital frequency synthesizer (DDFS) **242**, a voltage controlled oscillator (VCO) **212**, a plurality of loop amplifiers **216**, **218**, **226**, and **228**, a plurality of mixers **222** and **224**, a fractional synthesizer **214**, a divider **220** and a multiplexer **221**. The various components of FIG. **2**C may be substantially as described in FIG. **2**A.

[0062] The clock signal f_{LO} may be generated at a particular frequency, for example, at 1.6 GHz in a chip capable of handling communication of Bluetooth signals and FM signals. The divider **220** may be enabled to divide the generated clock signal f_{LO} to produce a frequency divided clock signal f_{DIV}, which may be mixed with the generated clock signal f_{LO} to enable transmission and/or reception of Bluetooth signals. The multiplexer **221** may be enabled to select the generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} for clocking one or more direct digital frequency synthesizers (DDFSs) **242** to enable transmission and/or reception of the FM signals based on a select signal received from the processor **240**. The generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} may be enabled to clock at least one of the DDFSs **242** to enable the transmission and/or reception of the FM signals.

[0063] FIG. **2**D is a block diagram illustrating an exemplary direct digital frequency synthesizer (DDFS), in accordance with an embodiment of the invention. Referring to FIG. **2**D, there is shown a DDFS **250**, a clock **252** and a DDFS controller **254**. The DDFS **250** may be a digitally-controlled signal generator that may vary the analog output signal g(t) over a large range of frequencies, based on a single fixed-frequency precision reference clock, for example, clock **252**. Notwithstanding, the DDFS **250** may also be phase-tunable. The digital input signal d(t) may comprise control information regarding the frequency and/or phase of the analog output signal g(t) that may be generated as a function of the digital input signal d(t). The clock **252** may provide a reference clock that may be N times higher than the frequency fc of the generated output signal g(t). The DDFS controller **254** may generate a variable frequency analog output signal g(t) by utilizing the clock **252** and the digital input signal d(t).

[0064] FIG. **3** is a flowchart illustrating exemplary steps for integration of Bluetooth and FM local oscillator generation in a single unit using a DDFS, in accordance with an embodiment of the invention. Referring to FIG. **3**, exemplary steps may begin at step **300**. In step **302**, a VCO may generate a clock signal f_{LO} at a particular frequency, for example, 1.6 GHz utilizing a fractional synthesizer. In step **304**, a frequency divided clock signal f_{DIV} may be generated by dividing a frequency of the generated clock signal f_{LO}. In step **306**, a Bluetooth clock signal f_{BT} may be generated by mixing the generated clock signal f_{LO} with the frequency divided clock signal f_{DIV}. In step **308**, the generated Bluetooth clock signal f_{BT} may be utilized to enable the transmission and/or reception of the Bluetooth communication signals. In step **310**, the generated clock signal f_{LO} or the generated frequency divided clock signal f_{DIV} may be communicated to the DDFS. In step **312**, the DDFS may enable modification of a frequency of the

generated clock signal f_{LO} or the generated frequency divided clock signal f_{DIV} based on a received control word f_{WORD}. In step **314**, a FM clock signal f_{FM} may be generated utilizing the generated clock signal f_{LO} or the generated frequency divided clock signal f_{DIV} to enable the transmission and/or reception of FM communication signals. Control then passes to end step **316**.

[0065] In accordance with an embodiment of the invention, a method and system for integration of Bluetooth and FM local oscillator generation in a single unit using a DDFS may include generating a clock signal f_{LO} at a particular frequency in a chip that handles communication of Bluetooth signals and FM signals. The generated clock signal f_{LO} may be divided to produce a frequency divided clock signal f_{DIV}, which may be mixed with the generated clock signal f_{LO} to enable transmission and/or reception of Bluetooth signals. The generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} may be selected by a multiplexer **221** for clocking one or more direct digital frequency synthesizers (DDFSs) **242** to enable transmission and/or reception of the FM signals. The generated clock signal f_{LO} or the frequency divided clock signal f_{DIV} may be enabled to clock at least one of the DDFSs **242** to enable the transmission and/or reception of the FM signals.

[0066] A Bluetooth clock signal f_{BT} maybe generated by mixing the generated clock signal f_{LO} with the produced frequency divided clock signal f_{DIV}. The generated Bluetooth clock signal f_{BT} may comprise an in phase (I) component f_{BT_I} and a quadrature phase (Q) component f_{BT_Q}. The generated Bluetooth clock signal f_{BT} may enable transmission and/or reception of the Bluetooth signals. A FM clock signal f_{FM} may be generated to enable the transmission and/or reception of the FM signals via one or more DDFSs **242**. The generated FM clock signal f_{FM} may comprise an in phase (I) component f_{FM_I} and a quadrature phase (Q) component f_{FM_Q}. The clock signal f_{LO} may be generated at the particular frequency, for example, at 1.6 GHz utilizing one or more of: a voltage controlled oscillator (VCO) **212** and a fractional synthesizer **214**. The transmission and/or reception of the FM signals may be controlled via a bi-directional coupler **234**. The DDFS **242** may be enabled to modify the frequency of the selected clock signal f_{LO} or the frequency divided clock signal f_{DIV} based on a received control word f_{WORD}. The processor **240** may be enabled to adjust the received control word f_{WORD} to compensate for changes in the generated clock signal.

[0067] Another embodiment of the invention may provide a machine-readable storage, having stored thereon, a computer program having at least one code section executable by a machine, thereby causing the machine to perform the steps as described above for integration of Bluetooth and FM local oscillator generation in a single unit using a DDFS.

[0068] Accordingly, the present invention may be realized in hardware, software, or a combination of hardware and software. The present invention may be realized in a centralized fashion in at least one computer system, or in a distributed fashion where different elements are spread across several interconnected computer systems. Any kind of computer system or other apparatus adapted for carrying out the methods described herein is suited. A typical combination of hardware and software may be a general-purpose computer system with a computer program that, when being loaded and executed, controls the computer system such that it carries out the methods described herein.

[0069] The present invention may also be embedded in a computer program product, which comprises all the features enabling the implementation of the methods described herein, and which when loaded in a computer system is able to carry out these methods. Computer program in the present context means any expression, in any language, code or notation, of a set of instructions intended to cause a system having an information processing capability to perform a particular function either directly or after either or both of the following: a) conversion to another language, code or notation; b) reproduction in a different material form.

[0070] While the present invention has been described with reference to certain embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the scope of the present invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the present invention without departing from its scope. Therefore, it is intended that the present invention not be limited to the particular embodiment disclosed, but that the present invention will include all embodiments falling within the scope of the appended claims.

What is claimed is:

1. A method for communicating signals, the method comprising:

in a chip that handles communication of Bluetooth signals and FM signals:

generating a clock signal at a particular frequency;

dividing said generated clock signal to produce a frequency divided clock signal, which is mixed with said generated clock signal to enable transmission of said Bluetooth signals or reception of said Bluetooth signals; and

selecting said generated clock signal or said frequency divided clock signal for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission of said FM signals or reception of said FM signals.

2. The method according claim **1**, comprising clocking via said generated clock signal or said frequency divided clock signal, at least one of said DDFSs to enable said transmission of said FM signals or said reception of said FM signals.

3. The method according to claim **1**, comprising generating a Bluetooth clock signal by mixing said generated clock signal with said produced frequency divided clock signal.

4. The method according claim **3**, wherein said generated Bluetooth clock signal comprises an in phase (I) component and a quadrature phase (Q) component.

5. The method according claim **3**, wherein said generated Bluetooth clock signal enables said transmission of said Bluetooth signals or said reception of said Bluetooth signals.

6. The method according to claim **1**, comprising generating a FM clock signal to enable said transmission of said FM signals or said reception of said FM signals via said one or more DDFSs.

7. The method according claim **6**, wherein said generated FM clock signal comprises an in phase (I) component and a quadrature phase (Q) component.

8. The method according to claim **1**, comprising generating said clock signal at said particular frequency utilizing one or more of: a voltage controlled oscillator (VCO) and a fractional synthesizer.

9. The method according to claim **1**, comprising controlling said transmission of said FM signals or said reception of said FM signals via a bidirectional coupler.

10. The method according to claim **1**, comprising modifying a frequency of said selected said generated clock signal or said frequency divided clock signal based on a received control word.

11. The method according to claim **10**, comprising adjusting said received control word to compensate for changes in said generated clock signal.

12. A system for communicating signals, the system comprising:

one or more circuits in a chip that handles communication of Bluetooth signals and FM signals, wherein said one or more circuits enable generation of a clock signal at a particular frequency;

said one or more circuits enable division of said generated clock signal to produce a frequency divided clock signal, which is mixed with said generated clock signal to enable transmission of said Bluetooth signals or reception of said Bluetooth signals; and

said one or more circuits enable selection of said generated clock signal or said frequency divided clock signal for clocking one or more direct digital frequency synthesizers (DDFSs) to enable transmission of said FM signals or reception of said FM signals.

13. The system according claim **12**, wherein said one or more circuits enable clocking via said generated clock signal or said frequency divided clock signal, at least one of said DDFSs to enable said transmission of said FM signals or said reception of said FM signals.

14. The system according claim **12**, wherein said one or more circuits enable generation of a Bluetooth clock signal by mixing said generated clock signal with said produced frequency divided clock signal.

15. The system according claim **14**, wherein said generated Bluetooth clock signal comprises an in phase (I) component and a quadrature phase (Q) component.

16. The system according claim **14**, wherein said generated Bluetooth clock signal enables said transmission of said Bluetooth signals or said reception of said Bluetooth signals.

17. The system according to claim **12**, wherein said one or more circuits enable generation of a FM clock signal to enable said transmission of said FM signals or said reception of said FM signals via said one or more DDFSs.

18. The system according claim **17**, wherein said generated FM clock signal comprises an in phase (I) component and a quadrature phase (Q) component.

19. The system according to claim **12**, wherein said one or more circuits enable generation of said clock signal at said particular frequency utilizing one or more of: a voltage controlled oscillator (VCO) and a fractional synthesizer.

20. The system according to claim **12**, wherein said one or more circuits enable controlling of said transmission of said FM signals or said reception of said FM signals via a bidirectional coupler.

21. The system according to claim **12**, wherein said one or more circuits enable modification of a frequency of said selected said generated clock signal or said frequency divided clock signal based on a received control word.

22. The system according to claim **21**, wherein said one or more circuits enable adjusting of said received control word to compensate for changes in said generated clock signal.

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