

- [54] DATA SIGNALLING SYSTEMS

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- [52] **U.S. Cl.**..... **340/413; 340/150**

- [51] Int. Cl. G08b 19/00; H04g 3/00

- [58] **Field of Search** 340/413, 412, 408, 213.1,
340/150, 151, 223, 163

- [56]
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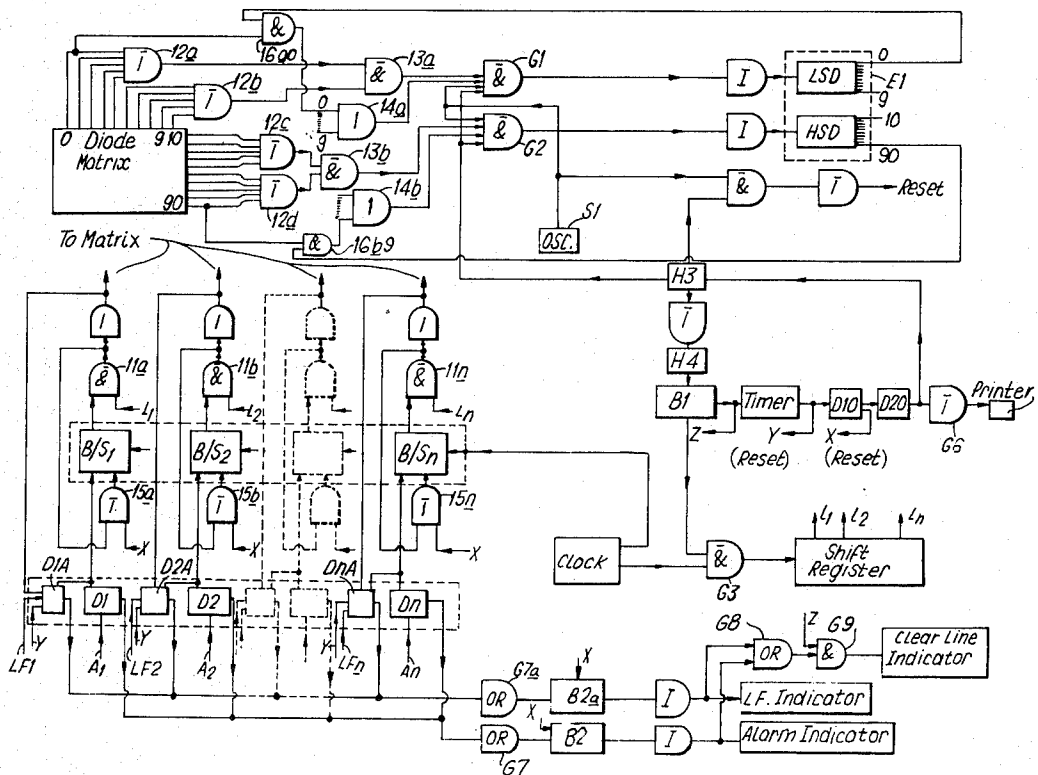
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[57]

ABSTRACT

In a security alarm signalling system in which a signal may be transmitted from any one of a number of remote stations to a central receiving station, the receiving station includes a multiple input encoder responsive to a change of state on any one of its inputs for presenting a coded output representative of the number of the input on which the change of state has occurred, and a digital display device including means for scanning the coded output to obtain a digital read-out of the said number and thereby, in use, identifying the associated remote station.

7 Claims, 2 Drawing Figures



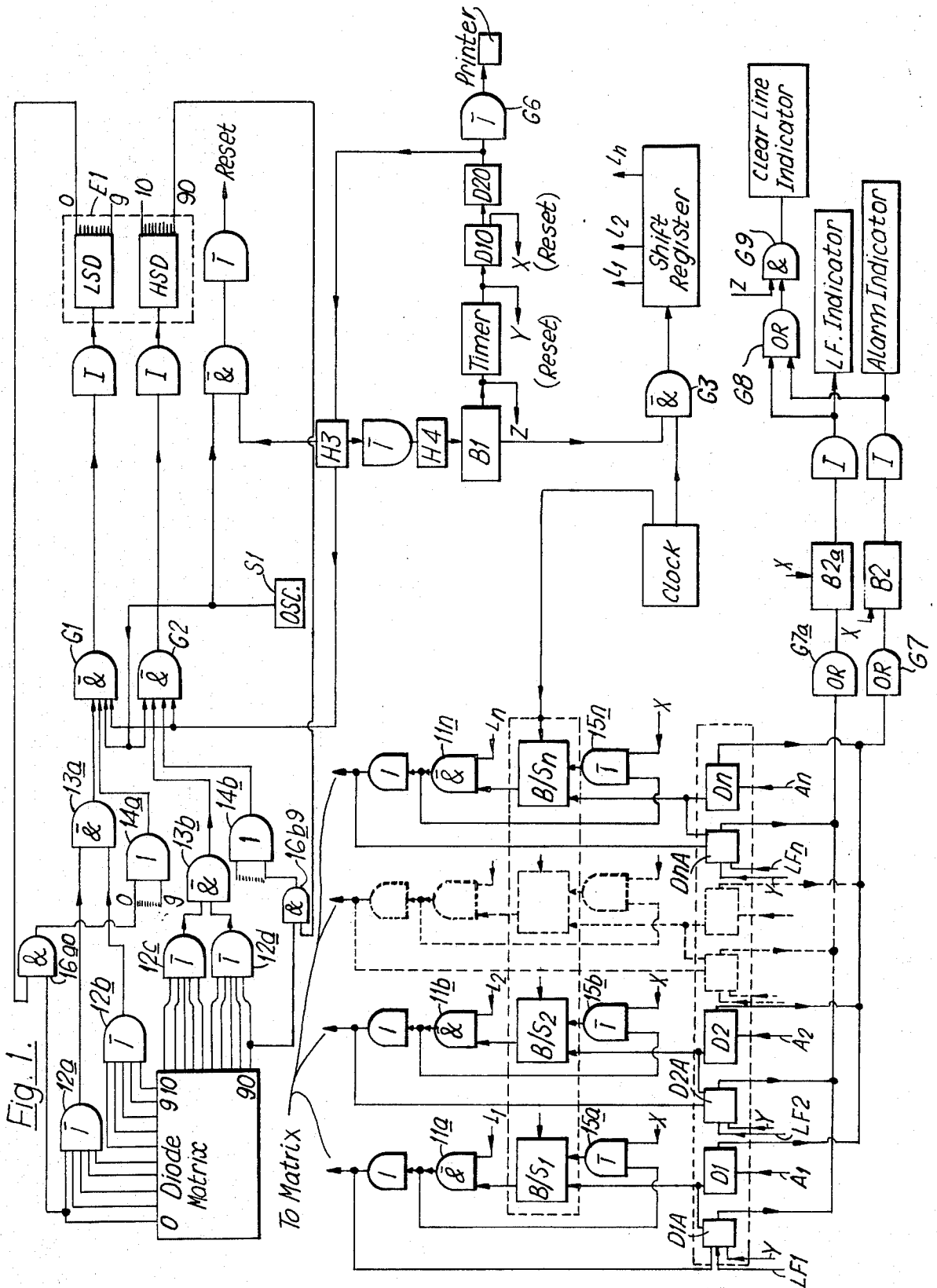
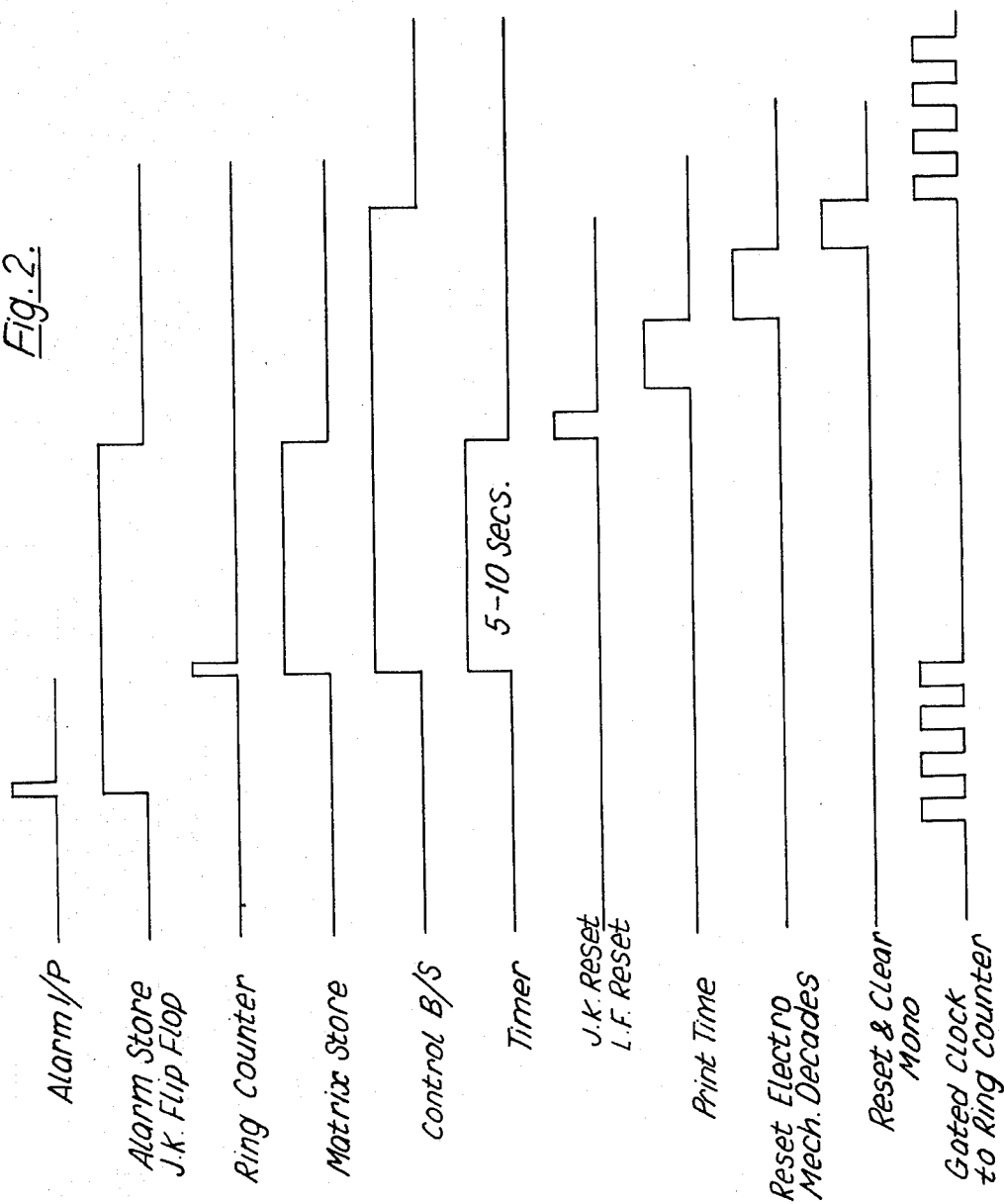


Fig. 2.



DATA SIGNALLING SYSTEMS

This invention relates to signalling systems, and has particular application to a multi-line security alarm system in which alarm signals from different remote stations are fed to a central receiving station.

At present the central receiving station normally includes one or more indicator panels having indicator lights to identify the different remote station. Such panels are generally bulky. Moreover, with systems handling a large number of input lines, more than one security officer is often required to maintain adequate supervision of the different panels.

In accordance with the present invention a receiver for use in a security alarm signalling system in which a signal may be transmitted from any one of a number of remote stations to a central receiving station, includes: a multiple input encoder responsive to a change of state on any one of its inputs for presenting a coded output representative of the number of the input on which the change of state has occurred, and a digital display device including means for scanning the coded output to obtain a digital read-out of the said number and thereby, in use, identifying the associated remote station.

In one embodiment of the invention the appearance or disappearance of input signals from the remote stations trigger respective bistable devices, and a gating circuit is connected between each of the bistable devices and respective inputs of the encoder. The system then includes a shift register for enabling each of the gating circuits in turn and means for inhibiting the shift register whenever a signal is transferred into the encoder. This prevents further signals being transferred into the encoder before the original signal has been encoded and read out on the display device. The encoder may comprise, for example, a matrix, each input being connected to a pair of mutually perpendicular coordinate lines, and the scanning means then includes a pair of counters arranged to hunt synchronously along the co-ordinate lines until a coincidence is obtained for each counter. The two counters then give a combined read out in which the two digits represent the least significant digit and the most significant digit of the line number on which a change of state has occurred.

One example of the invention is shown in the accompanying drawings in which:

FIG. 1 is a block circuit diagram of a multiple line alarm security system which presents a visual digital read-out and prints information relating to the date, time and place at which an alarm signal was generated.

FIG. 2 is a waveform diagram illustrating the operation of the circuit in FIG. 1.

Referring to these figures, the appearance or disappearance of an alarm input A_1 – A_n triggers a corresponding pulse stretching circuit D_1 – D_n which in turn transfers the J-K flip-flops B/S_1 – B/S_n to a 1.

The flip-flops acts as a binary store and a 1 in the store is transferred to a preselected address in a matrix through NAND gates $11a$, $11b$, etc., by the appearance of enabling shift register signals f_1 , f_2 , etc., on the second NAND gate input. A signal is transferred to a particular address in the diode matrix by feeding the outputs of each NAND gate to a predetermined intersection of the coordinate lines of the matrix. Each output is thereby connected to the junction of a pair of forward biased diodes in the matrix so that an output is ob-

tained on each of the respective coordinate lines. The coordinate address of each store element is selected to correspond to the number of the input on which the appearance or disappearance of a signal has been detected. For example, the coordinates (3, 4) will correspond to line No. 34.

The presence of a 1 in the matrix enables NAND gates G_1 , G_2 from the outputs of NOR gates $12a$ – $12d$ and NAND gates $13a$, $13b$ such that pulses from an oscillator S_1 are gated to master electromagnetic decade counters E_1 having decimal read-out wires connected to AND gates $16a$, $16b$. Only two of these gates $16a_0$ and $16b_9$ (these connected to the 0 and 90 read out wires) are shown in the figure for the sake of clarity.

The second input of the gates $16a$, $16b$ is connected to the corresponding one of the 0–9 and 10–90 lines of the matrix. The counters then hunt synchronously along the mutually perpendicular matrix lines until the two coordinates are found which give a coincidence output from the gates $16a$, $16b$. The coincidence outputs are fed to OR gates $14a$, $14b$ which inhibit the gates G_1 , G_2 respectively to stop the counters. The number indicated on the counters then corresponds to the number of the input on which a change of state has been detected.

Ancillary slave counters controlling the print wheels of a printer (not shown) are wired in parallel to the master counters so that a visible read out of the final number displayed by the counters can be supplemented by printing the number with the time and date at which it occurred.

The presence of a 1 in the matrix also inhibits the shift register by triggering a control bistable B_1 to close a gate G_3 between a clock C_1 and the shift register. This prevents any further signals being read into the matrix before the original signal has been read out.

The resetting of the flip-flops is controlled by an input from the NOR gates $15a$ – $15n$. The gates $15a$ – $15n$ can only be enabled by the coincidence of an X input from a 20 micro-second delay circuit D_{10} responsive to the output of bistable B_1 and a second input which is connected to the respective matrix store input. In other words, when a particular flip-flop transfers data to the matrix store, only that flip-flop can be reset after the data has been read out. This ensures that if at any time two or more alarm inputs appear simultaneously, they will be read out serially.

A complete cycle of operation commencing with an alarm input is clearly illustrated in FIG. 2. The alarm input triggers one of the J-K flip-flops B/S_1 – B/S_n and when the output from the flip-flop next coincides with the output of the shift register a pulse is fed into the matrix. The presence of the pulse in the matrix triggers the control bistable B_1 which in turn triggers a timer giving a pulse of between 5 and 10 seconds. During this time the master decade counters hunt for the address of the stored signal and at the end of the timer period a reset pulse from the delay circuit D_{10} resets the J-K flip-flop. This in turn cancels the data in the matrix store.

The signal from the delay circuit D_{10} also triggers a second 150 mS delay circuit D_{20} , and the output from D_{20} enables a gate G_6 to permit the printing of the final count displayed by the slave counters of the printer. At the end of the print time a monostable M_3 is triggered which closes the gates G_1 , G_2 and feeds a reset signal to the electro-magnetic decade counters and to the slave counters of the printer. The trailing edge of the pulse from the monostable M_3 triggers a 5

μ s monostable M4 and the output from M4 resets the control bistable B1. This enables the gate G3 so that clock pulses are again fed to the shift register.

The shift register also clears the dynamic "bit" on every 99th pulse of the clock to avoid any trailing pulses.

The appearance or disappearance of line fault inputs LFI—LFI trigger pulse stretching circuits D1A—DnA corresponding to the pulse stretching circuits D1—Dn so that line fault inputs are displayed in the same way as the alarm inputs. In order to distinguish between line fault and alarm conditions separate indicators are provided for each condition. Thus during an alarm display, an output from the pulse stretching circuits D1—Dn enables OR gates G7 which triggers bistable B2 to energize the alarm indicator. During a line fault condition, on the other hand, an output from the pulse stretching circuits D/A—DnA enables OR gate G7a which triggers bistable B2a to energize the line fault indicator. Further, in order to distinguish between the appearance and disappearance of an alarm or line fault input the outputs of the bistables B2, B2a are fed to an OR gate G8, and the output of G8 inhibits an AND gate G9 connected to a clear line indicator. The second input of the AND gate G9 receives a Z pulse output from the bistable B1 which occurs each time a number is loaded into the matrix and displayed by the counters; if a number is displayed in response to the disappearance of an alarm input the AND gate G9 will no longer be inhibited because there is no input to the gates G7, G7a and the clear line indicator will therefore be energized by the Z pulse.

In one alternative system (not illustrated) for handling up to 1000 input lines, a change of state on any one input line is fed to an encoder which converts the single input into binary coded decimal (BCD) form representing the number of the input. This has the advantage of requiring not more than 12 output wires for each input. The BCD outputs representing the most and least significant digits may then either be synchronously scanned to search for the marked lines (this requires a display device which is capable of decoding the detected BCD (information) or they may be first decoded back into decimal form and then fed to AND gates such as those shown as 16a, 16b etc., in the drawing for comparison with the decimal outputs of the electro-mechanical decade counters.

We claim:

1. A receiver for use in a security alarm signalling system in which a predetermined number of remote stations are each connected to a central receiving station by respective pairs of wires, each remote station being identified by a different predetermined number, and the receiver including a multiple input encoder, each input of said encoder being connected, when in use, to a respective pair of wires from one of the numbered remote stations, and the receiver also including a multiple input binary store; gating means connected between the outputs of said binary store and corresponding inputs of said encoder; scanning means for periodically scanning the inputs of said encoder, said scanning means including enabling means for periodically enabling each of said gating means in turn; said encoder including means responsive to a change in the signal level on any one of its inputs for generating a coded output signal representative of the number of the remote station to which the input is connected, and a digital display device including means for converting the coded output into a digital read-out of said number; and means responsive to the presence of a signal in said encoder for inhibiting the enabling means until the signal has been encoded and read out on the display device.

2. A receiver according to claim 1 in which the digital display device includes a counter, and the receiver further includes an oscillator for feeding pulses to the counter in response to a detected change of signal level on one of the inputs to the encoder, a coincidence detector connected to compare the output of the encoder representing the number of the remote station associated with the change of signal level with the number present in the counter, and inhibiting means connected to receive an output from the coincidence detector when the two numbers being compared are equal for inhibiting the supply of pulses to the counter such that the final number displayed by the counter represents the number of the remote station.

3. A receiver according to claim 1, further including a clear line indicator connected to receive an energising signal from a control circuit whenever a change in signal level has been detected at one of the encoder inputs, and means for inhibiting operation of the indicator whenever an alarm signal is present at one of the inputs to the encoder whereby the indicator distinguishes between the display of a number in response to the appearance of an input signal and the display of a number in response to the disappearance of an input signal.

4. A receiver according to claim 2, in which the digital display device further includes a printer for printing the said input number displayed by the counter.

5. A receiver according to claim 2 in which the encoder includes a diode matrix of perpendicular coordinate lines, the output of each gating circuit being connected to the junction of a respective pair of diodes in the matrix such that an output is obtained from the corresponding pair of coordinate lines which intersect at the junction, the two coordinates together representing the two digits of the numbered input line to be displayed.

6. A receiver according to claim 2 in which the counter includes means for hunting synchronously for each of the pair of coordinates.

7. A receiver according to claim 2 in which the counter comprises a pair of electromagnetic decade counters arranged to give a two digit decimal output display; a first of the decade counters hunting for the least significant coordinate and the second decade counter hunting for the most significant coordinate of the number to be displayed.

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