

[54] **SYSTEM FOR PRODUCING CHARACTERS ON A CATHODE RAY TUBE DISPLAY BY INTENSITY CONTROLLED POINT-TO-POINT VECTOR GENERATION**

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[22] Filed: **May 11, 1970**

[21] Appl. No.: **36,054**

[52] U.S. Cl. **340/324 A, 315/18, 315/22**

[51] Int. Cl. **G06f 3/14**

[58] Field of Search **340/324 A; 315/18, 22**

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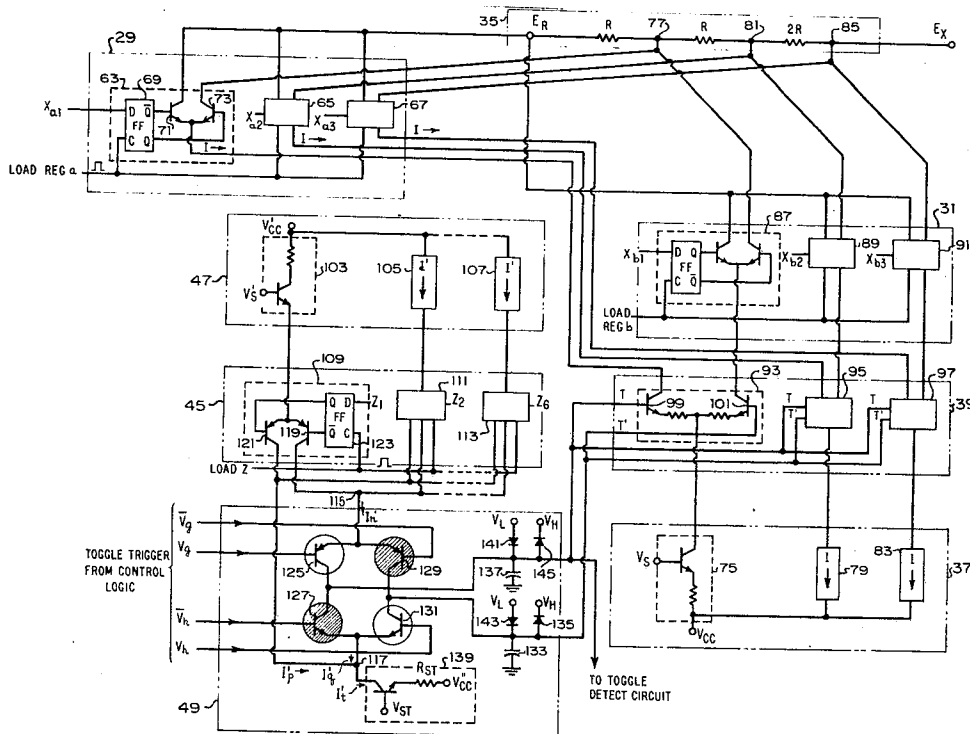
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[57] **ABSTRACT**

An alpha-numeric character generating system receives digital codes representing characters and controls a CRT to trace a plurality of vectors which in combination form the characters displayed. A read-only memory provides in sequence a plurality of sets of X, Y and Z parameters for each character. Succeeding X and Y parameters are each stored in corresponding alternate registers. The sets of X and Y parameters define the end points of the vectors forming a character. Two digital to analog converters responsive to the X and Y parameters, respectively, provide signals for deflecting the CRT beam. The inputs of the digital to analog converters are transferred between corresponding alternate registers to cause the CRT beam to trace from one vector end point to the next in sequence. A toggle circuit responsive to the Z parameter associated with each set of X and Y parameters controls the transfer time between registers and thus the brightness of each vector traced on the CRT screen.

12 Claims, 13 Drawing Figures



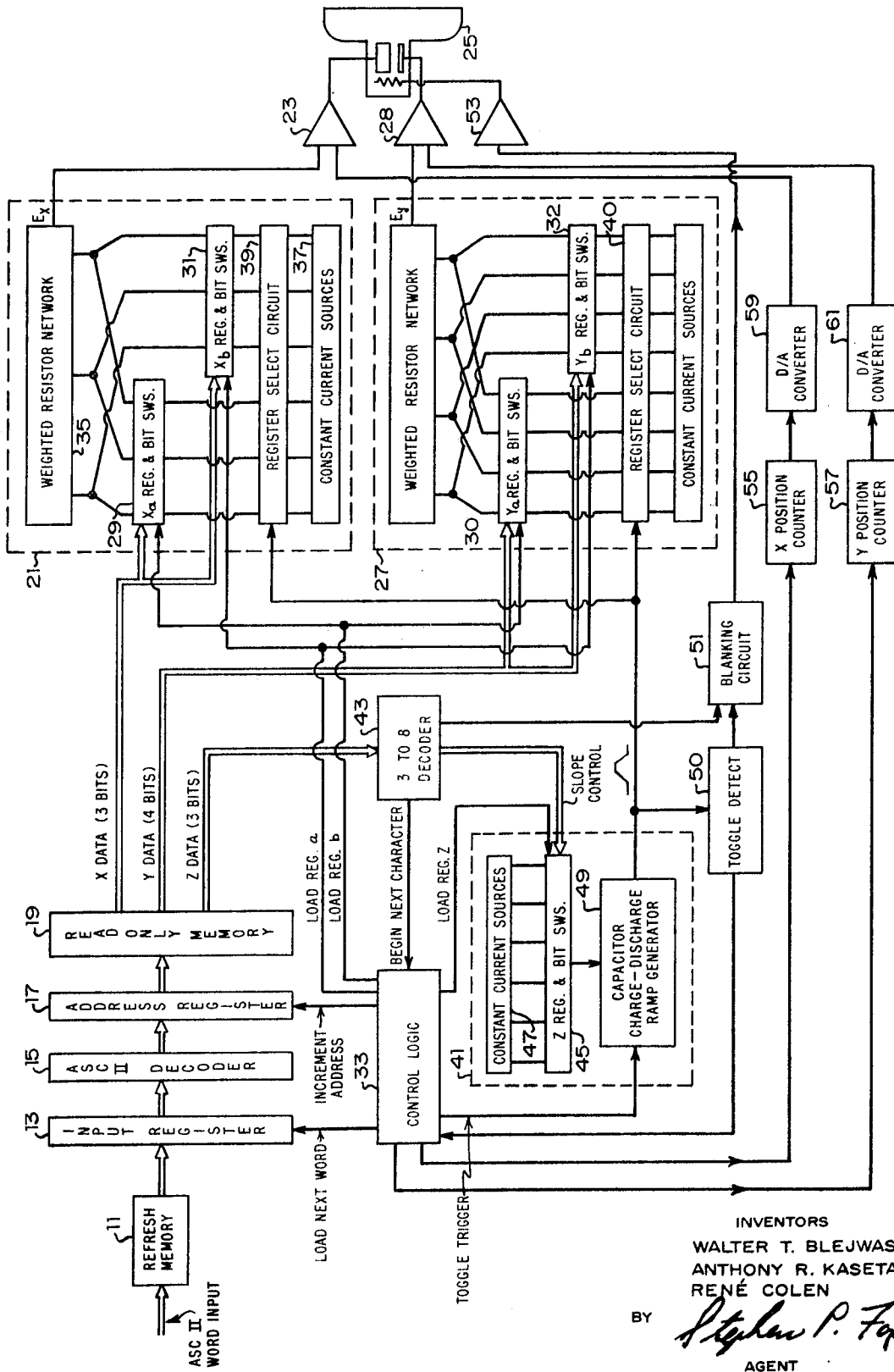


Figure 1

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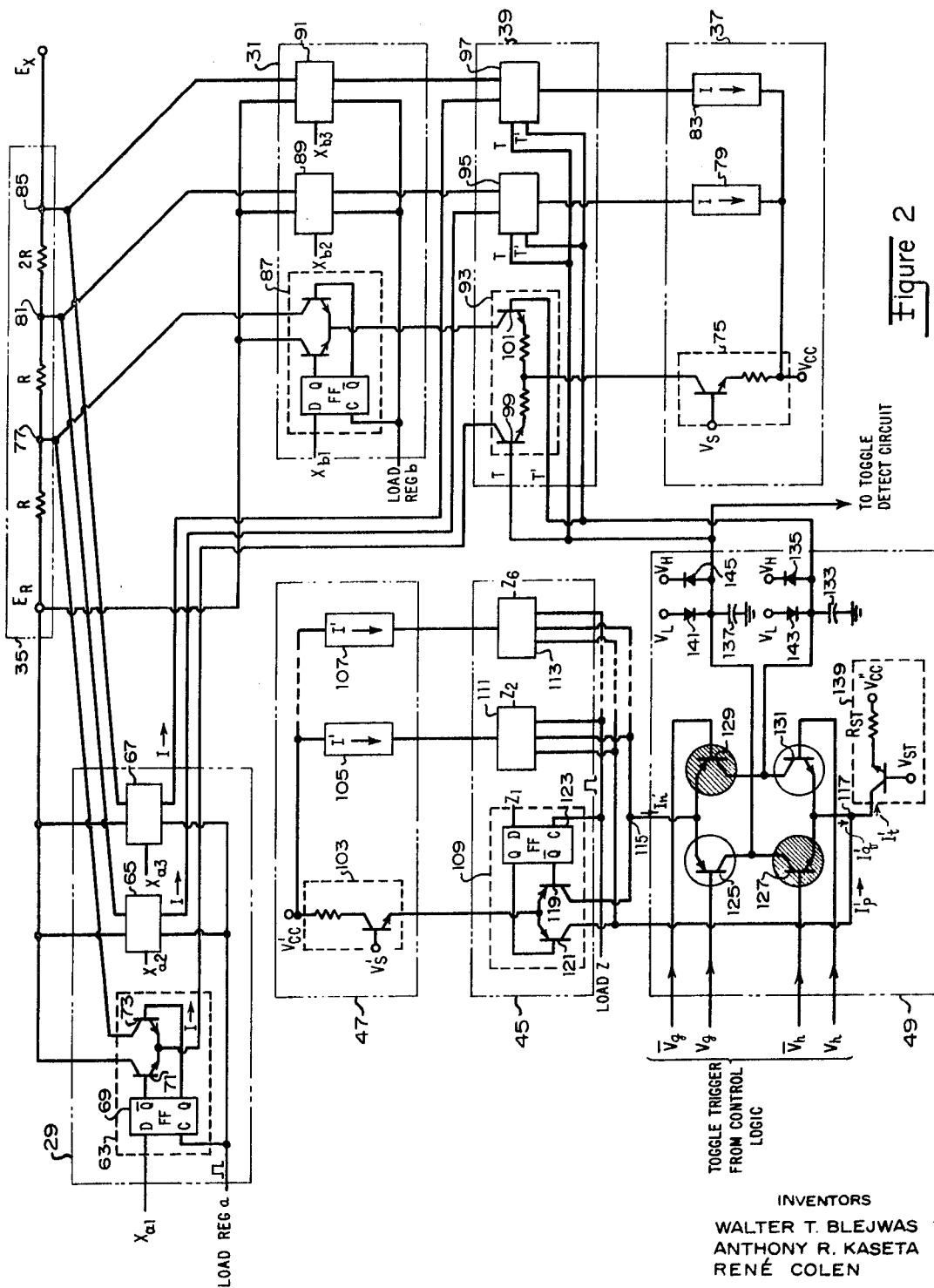


Figure 2

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SYSTEM FOR PRODUCING CHARACTERS ON A CATHODE RAY TUBE DISPLAY BY INTENSITY CONTROLLED POINT-TO-POINT VECTOR GENERATION

BACKGROUND OF THE INVENTION

The present invention relates generally to a system for receiving digitally encoded alpha-numeric characters and generating signals for controlling a cathode ray tube (CRT) to display the characters on the CRT screen.

A number of techniques are known for generating characters to be displayed on a CRT screen. According to one system, characters are formed from a plurality of contiguous light spots produced by selectively deflecting and unblanking the CRT beam within a dot matrix. One problem with this method is that the intelligibility of the characters displayed depends on the density of the dots in the matrix and the number of light spots used to form each character. Character resolution may be poor and the display difficult to read unless a high density dot matrix is used. In this case, there is the undesirable requirement that a large capacity memory unit be used to store the digital information defining the positions of the light spots in the dot matrix for each character displayed.

Another method of displaying characters is known as the starburst technique. Characters are formed from a pattern of lines in the shape of a rectangle and lines extending from the center of the rectangle to the corners and sides thereof. Selected ones of the lines in the pattern are traced by the CRT beam to produce the characters. One disadvantage of this method is that visual character recognition is often difficult. Also, the style of characters obtainable by this method is restricted. In particular, lower case letters are difficult to produce.

SUMMARY OF THE INVENTION

The present invention provides a character generator system for controlling a CRT beam to trace a plurality of vectors which define the characters displayed. The vectors forming each character are produced sequentially in a predetermined order. Each vector has a length and direction determined by defining the end points of the vector in a matrix and tracing a line between the end points. The CRT beam is controlled to trace each vector during a time period dependent on the length of the vector, thereby to maintain the vectors forming a character at a uniform brightness on the display screen. A feature of the system is that a wide variety of character shapes and styles may be produced, and the characters are easily visually recognizable. Also, the vector information stored for the characters is such that memory capacity is conserved.

In the illustrated embodiment of the invention, a memory unit stores a plurality of data words for each character. Each data word represents three digital parameters: two for defining the end point of a vector in an X-Y coordinate matrix, and the third for selectively blanking the CRT beam and for controlling the time interval in which the beam is to trace a vector to the associated end point. In operation, a digital code representing a character interrogates the memory unit to begin sequential output of the corresponding group of digital parameters defining the vectors which are used to form the character on the CRT screen. Succeeding ones of the digital X and Y parameters provided in sequence from the memory are each alternately loaded into two registers and converted into analog signals for deflecting the CRT beam. Thus one X register and the corresponding Y register contain parameters representing one vector end point, the other X register and Y register contain parameters representing another vector end point, and the CRT beam is controlled to trace a line between these end points. In continuous operation, the CRT beam progresses from one end point to the next as they are loaded into the registers, and the resulting combination of vectors traced form the desired character.

The digital representations of the vector end points in the registers are converted into analog beam deflection signals by X and Y digital to analog converters, each of which includes a weighted resistor network and a plurality of current sources. The two registers associated with each digital to analog converter select the current sources to be coupled to the resistor network. A toggle circuit transfers control of current source coupling from one register to the other in a transfer time interval determined by the third parameter associated with each set of X and Y parameters. The transfer time controls the rate of beam deflection between the vector end points stored in the registers and thus controls the brightness of the trace on the CRT screen. The third parameter also determines whether the beam will be blanked when moving between vector end points, thereby to permit versatility in programming the characters to be generated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the preferred embodiment of the system incorporating the present invention.

FIG. 2 is a combined schematic and block diagram showing in more detail a portion of the system in FIG. 1.

FIGS. 3a-C are diagrams and charts used to illustrate the generation of a typical character by the system in FIGS. 1 and 2.

FIGS. 4a-h are a series of waveforms used to illustrate the operation of the system in FIGS. 1 and 2.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to FIG. 1, the system input receives multibit data words representing alpha-numeric characters in standard ASCII coded form. These data words are temporarily stored in a refresh memory 11 and then applied through an input register 13, a decoder 15, and an address register 17 to a read-only memory 19.

The read-only memory 19 is programmed to contain a plurality of ten bit data words corresponding to each alpha-numeric character. Each ten bit data word represents one set of X, Y, and Z parameters. The pairs of X and Y parameters define the end points of vectors which form a character in an X-Y coordinate matrix. The Z parameter associated with each pair of X and Y parameters defines the rate at which a vector is to be traced by the CRT beam to the particular X-Y coordinate position associated with the Z parameter.

When an ASCII coded character is received in the input register 13, it is decoded by the decoder 15 and applied to the address register 17 which, in turn, selects one set of X, Y, and Z parameters in the read-only memory 19 as the starting point. From that starting point, the read-only memory 19 provides, in sequence, the plurality of sets of X, Y, and Z parameters corresponding to the character.

The X parameters in digital form are fed to a circuit contained within the dashed outline block 21. This circuit provides an analog signal output E which is coupled through an amplifier 23 to control the horizontal deflection of the beam of a CRT 25. Similarly, the Y parameters in digital form are fed to the circuit within the dashed outline 27, and the output E therefrom is applied through an amplifier 28 to control the vertical deflection of the CRT beam. The two circuits 21, 27 are similar in configuration and operation, except that circuit 21 is adapted to receive X parameters represented by three binary bits, whereas circuit 27 receives Y parameters represented by four binary bits. Therefore, only the circuit 21 for the X parameter will be described in detail below.

As successive sets of X, Y, and Z parameters are provided in sequence by the read-only memory 19, the X parameters are loaded alternately into two register and bit switch circuits 29, 31. Each of the circuits 29, 31 includes a three bit storage register and a current switch associated with each bit. The current switches are controlled in response to the binary state of the corresponding bits. In operation, the X register receives one X parameter, the X register receives the next X parameter,

ter, the X_n register receives the third parameter and so on in alternate fashion. The alternate loading of the X_n and X_b registers is controlled by signals from a control logic circuit 33.

The digital contents of the X_n and X_b registers are converted into analog signals by a digital to analog converter circuit including a weighted resistor network 35 and a plurality of constant current sources 37. The analog output voltage E_x depends upon the particular combination of current sources applied to the weighted resistor network 35, as described hereinafter. This combination is controlled by the bit switches in one or the other of the circuits 29, 31. Control of the coupling of the current sources 37 to the resistor network 35 is transferred back and forth between the two circuits 29, 31 by a register select circuit 39. The time interval during which control is transferred from one to the other of circuits 29, 31 depends on the output of a toggle circuit indicated within the dashed outline 41 and described hereinafter.

As stated above, the configuration and operation of the circuit 27 for the Y parameter is similar to that of circuit 21 for the X parameter. As the set of X, Y, and Z parameters are provided in sequence, the Y parameters are alternately stored in digital form in the Y_n and Y_b registers of circuits 30, 32. Also, control of the digital to analog conversion circuitry is transferred back and forth between the two register circuits 30, 32 by a signal from the toggle circuit 41.

After at least two sets of X, Y, and Z parameters have been provided by the read-only memory 19, one of the X registers, for example register X_n , and the corresponding register Y_n contain parameters representing the coordinate position of one vector end point, and the other registers X_b , Y_b contain parameters representing the coordinate position of another vector end point. At this time, it is assumed that the register select circuit 39 for the X parameter and the corresponding register select circuit 40 for the Y parameter have activated the register circuits 29, 30 so that X_n and Y_n control the selective coupling of the constant current sources to the corresponding weighted resistor networks. Thus, the output voltages E_x and E_y represent the analog value of the digital parameters in the corresponding X_n and Y_n registers. The signals E_x and E_y hold the CRT beam at a particular point on the screen. At this time, the toggle circuit 41 operates the two register select circuits 39, 40 to transfer the inputs of the X and Y digital to analog converter circuits from registers X_n , Y_n to registers X_b , Y_b . As a result, registers X_b , Y_b will control selection of the constant current sources to be applied to the weighted resistor networks. The voltages E_x and E_y will then correspond respectively to the value of the parameters in registers X_b and Y_b . The transition from registers X_n , Y_n to registers X_b , Y_b is performed gradually according to a predetermined time function thereby to cause the CRT beam to trace a vector from the coordinate position defined in registers X_n , Y_n to the position defined in registers X_b , Y_b .

The brightness of each vector traced on the CRT screen depends on the rate of beam movement. This, in turn, depends on the time interval during which the digital to analog converters in the X and Y circuits 21, 27 are transferred from one to the other of the corresponding registers. As mentioned above, the transfer between registers X_n , Y_n and X_b , Y_b is achieved by the register select circuits, under control of the toggle circuit 41. The time duration of the transfer signal from the toggle circuit is controlled by the Z parameter associated with each pair of X and Y parameters provided by the read-only memory 19. More specifically, the Z parameter in the form of a three bit digital word is applied to a decoding circuit 43 which decodes the three bits into eight signals. Six of these eight signals are loaded into the Z register and bit switching circuit 45. In response to the six signals, selected ones of a plurality of constant current sources 47 are coupled to a ramp generator 49 to charge and discharge capacitors therein, as described hereinafter. The ramp generator produces a ramp signal and the transfer rate between registers X_n , Y_n and X_b , Y_b depends on the slope of the ramp signal.

The Z parameter associated with each pair of X and Y parameters is programmed to provide a shorter transfer time between registers when the succeeding coordinate positions contained therein are closely spaced than when the coordinate positions are spaced further apart. The transfer times are controlled so that the CRT beam traces each vector at the same rate. Therefore, the vectors have the same intensity and the characters produced thereby are of uniform brightness on the screen.

In continuous operation of the system, the CRT beam traces vectors from one coordinate position to the next as they are alternately loaded into registers X_n , Y_n and X_b , Y_b . A toggle detect circuit 50 signals the control logic 33 in response to the occurrence of each ramp signal. This, in turn, causes the control logic 33 to advance the address in address register 17 by one so that the read-only memory 19 provides at its output the next set of X, Y, and Z parameters. The resulting combination of vectors traced by the beam form the desired character.

The Z parameter performs several functions in addition to the transfer time between registers as described above. When certain Z codes are detected by the decoder 43, a blanking circuit 51 is activated when a signal from the toggle detect circuit 50 indicates that a vector is being traced. The output of blanking circuit 51 is applied through an amplifier 53 to blank the beam of the CRT. This feature permits the beam to be deflected from one coordinate position to the next without displaying a vector, thereby expanding system capability to permit generation of a wide variety of characters. Another Z code detected by the decoder 43 signals the control logic 33 to indicate that the coordinate position of the last vector in a series of vectors forming a character has been received and that tracing of the next character should begin. In response to this signal, the control logic 33 operates to load into the input register 13 the next character from the refresh memory 11. At the same time, the control logic 33 increments the X and Y position counters 55, 57. The outputs of these counters 55, 57 are converted to analog signals by respective digital to analog converters 59, 61 and applied to amplifiers 23, 28, respectively, to shaft the reference voltage on the horizontal and vertical deflection plates of the CRT. As a result, the beam is moved into position for tracing the next character in a line.

The CRT beam is shifted horizontally one character position after each character is generated. The characters are generated one-by-one until an entire line is filled or until a "carriage return" signal is received at the system input. Thereafter, the beam is shifted vertically into position to generate the next line of characters. The refresh memory 11 has a capacity large enough to store data words for a predetermined number of character positions on the CRT screen. This memory may be repeatedly cycled to output previously received characters. Each time this memory is cycled, the display of characters is refreshed on the CRT screen. Thus, a desired character display may be held on the screen for continued viewing. Subsequently received characters update the refresh memory 11 and the display on the screen.

FIG. 2 shows in more detail the X parameter circuit 21 and the toggle circuit 41 described above. The X_n register and bit switch circuit 29 (FIG. 1) comprises three circuits 63, 65, 67 (FIG. 2) associated respectively with the three X bits designated X_{n1} , X_{n2} , and X_{n3} . The three circuits are identical so only one will be described in detail. In circuit 63, the binary bit X_{n1} is applied to the D input of a flip-flop memory element 69. The D input is activated in synchronism with a pulse on the clock input C produced by the "load reg. a" output of the control logic 33 (FIG. 1). Flip-flop 69 is driven into one or the other of two stable states, as represented by different voltage levels on the complimentary outputs Q and $\bar{Q}$. The bit switch associated with flip-flop 63 includes two transistors 71, 73 which are driven into opposite states of conduction by the signals on the outputs Q and $\bar{Q}$. The emitters of transistors 71, 73 are coupled to a constant current source 75 through additional circuitry hereinafter described. Current source 75 is one of those represented by block 37 in FIG. 1. In response,

transistor 71 is cut off and transistor 73 conducts, thereby to couple the constant current source 75 to a tap point 77. In response to $X_{n1} = 0$, transistor 73 is cut off and transistor 71 conducts, thereby to couple the constant current source 75 to a reference voltage E_b instead of the tap point 77. This effectively decouples the current source 75 from the resistor network 35.

As shown, weighted resistor network 35 includes three resistors connected in series and having tap points 77, 81, 85. Constant current source 75 is selectively coupled to the tap point 77 by circuit 63 described above. Similarly, a constant current source 79 is selectively coupled to tap point 81 by the circuit 65, and the constant current source 83 is selectively coupled to tap point 85 by the circuit 67. The resistor network 35 produces the output voltage E_x which depends on the voltage drop across each of the series resistors. The voltage drops, in turn, depend on the combination of current sources 75, 79, 83 coupled to the tap points by their corresponding circuits 63, 65, 67 in response to the binary bits representing the X parameter. In this manner, the X parameter in digital form is converted to the analog output signal E_x .

The X_b register and bit switch circuit 31 (FIG. 1) includes three circuits 87, 89, 91 (FIG. 2) which correspond to and are identical with the three circuits 63, 65, 67 described above. The three circuits 87, 89, 91 operate to selectively couple the three constant current sources 75, 79, 83 to the corresponding tap points 77, 81, 85 of the resistor network 35 in response to the binary bits applied to the inputs X_{b1} , X_{b2} , X_{b3} . In steady state operating conditions, only one of the X_n and X_b register and bit switch circuits will be active to selectively couple the constant current sources 75, 79, 83 to the resistor network.

Control of the digital to analog converter input circuit is transferred back and forth between registers X_n and X_b by the register select circuit 39 (FIG. 1), which includes three coupling circuits 93, 95, 97 (FIG. 2) associated respectively with the three bits defining the X parameter. The coupling circuits 93, 95, 97 are identical, so only one will be described in detail. The coupling circuit 93 includes two variably conducting transistors 99, 101 connected in a differential amplifier configuration. These two transistors are driven at the base control inputs thereof by complimentary toggling signals T and T'. In one mode, transistor 99 is conducting and transistor 101 is cut off. Thus, current from the constant current source 75 is conducted to the circuit 63 and bit X_{n1} controls whether this current is coupled to tap point 77. In another mode, transistor 101 is conducting and transistor 99 cut off, so that current source 75 is coupled to circuit 87 and bit X_{b1} controls whether current will be conducted to the tap point 77. The transfer between these two modes of operation is made gradually because the toggling signals T and T' are ramp waveforms. For example, as signal T drives transistor 99 toward cut off, the complimentary signal T' drives transistor 101 into conduction. Transistor 99 is driven from a conducting to a non-conducting state, and transistor 101 is simultaneously driven from a non-conducting to a conducting state during a time interval dependent on the slope of the ramp waveforms T and T'.

The three circuits 93, 95, 97 are controlled simultaneously by the ramp signals T and T' to transfer the current input circuit of the digital to analog converter from one to the other of the X_n and X_b registers. Thus, the analog output voltage E_x changes gradually between two values in accordance with the ramp function.

As described above, the toggling signals T and T' are produced by the toggle circuit 41 (FIG. 1). Circuit 41 includes a plurality of constant current sources 47, represented by the three current sources 103, 105, 107 (FIG. 2). Also the Z register and bit switches 45 (FIG. 1) include the circuits 109, 111, and 113 (FIG. 2) associated respectively with the current sources 103, 105 and 107. There are a total of six such current sources and associated switching circuits; however, only three are shown in FIG. 2. These current sources and switching circuits are identical, so only the source 103 and switching cir-

cuit 109 will be described in detail. The current source 103 provides a constant current I' which is coupled to one or the other of two summing points 115, 117 through transistors 119, 121, respectively. These two transistors are driven into opposite conduction states by the complimentary outputs of a flip-flop 123 in a manner similar to that described above with respect to circuit 63. One or the other of transistors 119, 121 conducts, depending on the state of the binary input Z_1 to the D input of flip-flop 123 when the C input thereof is pulsed by the load Z signal from control logic 33 (FIG. 1). The six binary inputs $Z_1, Z_2, \dots, Z_6$ are derived from the decoder 43 (FIG. 1) in accordance with a value of the Z parameter. Each time a set of X, Y, and Z parameters is provided by the read-only memory 19, the inputs $Z_1, Z_2, \dots, Z_6$ are loaded into their corresponding flip-flops and couple one or more of the current sources to the summing point to produce a current I'_n . Currents from the remaining current sources are summed to apply a current I'_p to the summing point 117.

The capacitor charge-discharge circuit 49 (FIG. 1) includes four switching transistors 125, 127, 129, 131 (FIG. 2) the base inputs of which are driven by suitable signals from the control logic 33 (FIG. 1) so that in one mode, transistors 127, 129 are conducting and transistors 125, 131 are cut off, and in another mode, transistors 125, 131 are conducting, and the other two transistors 127, 129 are cut off. In the mode of operation shown in FIG. 2, the shaded transistors 127, 129 are conducting so that the current I'_n from summing point 115 is applied to a capacitor 133 to charge this capacitor to a predetermined voltage V_H . A clamping diode 135 insures that the voltage on capacitor 133 does not exceed the voltage V_H . At the same time, another capacitor 137 is coupled through transistor 127 through summing point 117 to a current sink 139. The current sink draws a total current I'_t . Part of this current is the current I'_p , and the remaining current is I'_q drawing through transistor 127 from capacitor 137 thereby to discharge this capacitor. The capacitor 137 is discharged to a predetermined low voltage V_L , and a clamping diode 141 insures that the voltage on capacitor 137 does not fall below V_L . The current I'_t drawn by current sink 139 is selected so that the discharging current I'_q from capacitor 137 is equal to the charging current I'_n applied to capacitor 133. Therefore, capacitors 133, 137, respectively charge and discharge at the same rate and the output signals T and T' from these capacitors are complimentary ramp signals.

In the other mode of operation, transistors 127, 129 are cut off and transistors 125, 131 conduct, so that capacitor 133 is discharged to a voltage level V_L and maintained at that level by clamping diode 143, while capacitor 137 is charged to the voltage V_H and maintained at that level by the clamping diode 145.

The control logic 33 controls the sequence of operation of the toggle generator 41 in a manner such that the Z parameter signals are first loaded into the circuits 109, 111, 113 to select a particular combination of current sources. Each time after the Z data is loaded, the four transistors 125, 127, 129, 131 are switched from one state of conduction to the other to thereby charge one of the capacitors 133, 137 and simultaneously discharge the other of these capacitors. These two capacitors will always charge and discharge at the same rate to produce the complimentary ramp signal outputs; however, the time required for the ramp signal to go from one to the other of the voltage levels V_L and V_H will depend on the Z parameter which determines the charging current I'_n and the discharging current I'_q . Thus, it can be seen that the toggle generator 41 is digitally programmed to produce ramp signals of varying duration.

The overall operation of the system will now be described with reference to FIGS. 3 and 4. For purposes of example, it will be assumed that the system input receives a data word representing the character "A." As shown in FIG. 3a, this character will be drawn in eight by sixteen coordinate reference frame. In order to trace this character on the CRT screen, a total of four vectors are required, and the X, Y, and Z information required to produce these four vectors is stored

in succeeding memory positions in the read-only memory 19. As shown in the chart of FIG. 3b, there are five sets of X, Y, and Z parameters required to define the character "A." The X and Y parameters define the end points of vectors to be generated in sequence in the X-Y coordinate matrix, and the Z parameter associated with each pair of X and Y parameters determines three control functions: (1) the time interval during which the vector will be traced; (2) whether the CRT beam will be blanked during the trace; and (3) whether the end point is the first for a particular character. The chart of FIG. 3c shows the eight possible values of the Z parameter, along with the vector drawing times and other control features associated with each value.

FIG. 4 shows some of the timing diagrams for the system when the character "A" is generated. Initially, the control logic 33 pulses the input register 13 to load into this register the data word corresponding to the letter "A," as shown in FIG. 4a. This code word selects the starting point in the read-only memory 19, which in the present example will be the data word defining the set of X, Y, and Z parameters corresponding to the values 0, 4, 7, respectively (see FIG. 3b). As shown in FIG. 4b, the control logic 33 pulses the clock inputs to the register X_n to load into this register the three bit code corresponding to $X=0$. Simultaneously, the value $Y=4$ is loaded into the register Y_n ; however, the timing control pulses therefore are not shown. Also, as shown in FIG. 4d, the control logic 33 pulses the Z register 45 to load into this register the parameter $Z=7$. Thereafter, the toggle trigger signal from the control logic 33 changes levels, as shown in FIG. 4e, to start the charging of one of the two capacitors 133, 137 (FIG. 2) and the discharging of the other of these two capacitors. The resulting ramp toggle signals T and T' transfer control of the digital to analog converters from registers X_n , Y_n to registers X_b , Y_b .

FIG. 4f illustrates the analog beam deflection signal E_x produced by the digital to analog converter for the CRT horizontal deflection circuit. Similarly, an analog deflection signal E_y is produced for the vertical deflection circuit; however, this signal is not shown. At the time that the first set of X, Y, and Z parameters for the character "A" is loaded into register X_n , the CRT beam is maintained deflected at a coordinate position corresponding to the end point of the last vector traced for a preceding character. As shown by the dashed line portion of the waveform in FIG. 4f, the beam deflection signal E_x is transferred from some value corresponding to the parameter in the X_b register to the starting point $X=0$, $Y=4$. The Z parameter associated with the 0, 4, coordinate has a value of 7, which as indicated in FIG. 3c will cause the CRT beam to be blanked during the trace to the 0, 4 end point.

The toggle detect circuit 50 produces a high level signal during the time when the beam is being deflected between two end points, as shown in FIG. 4g. When the beam reaches the 0, 4 end point defined in registers X_n , Y_n , the toggle detect signal goes low, and this, in turn, advances the address in the address register 17 by one, thereby to cause the read only memory 19 to output the next set of X, Y, and Z parameters. At this time, the X_b register is loaded with the parameter $X=3$ (see FIGS. 3b and 4c), the Y_b register is loaded with the parameter $Y=15$, and the Z register is loaded with the parameter $Z=6$. Thereafter, the toggle trigger signal (FIG. 4e) changes levels and the control of the digital to analog converters is changed from registers X_n , Y_n to registers X_b , Y_b , thereby to cause the analog signal E_x to change along a ramp function from the analog value corresponding to $X=0$ to that corresponding to $X=3$ as shown in FIG. 4f. The value of the parameter $Z=6$ causes the beam to trace the first vector in a time of 3 microseconds.

Subsequent vectors forming the character "A" are generated in a similar manner. That is, each time one vector is completed, a toggle detect signal causes the next set of X, Y, and Z parameters to be read out from the read-only memory 19, the X and Y parameters in this next set are loaded into either the registers X_n , Y_n or the registers X_b , Y_b , and the next

vector is traced in accordance with the time interval and blanking control indicated by the value of the Z parameter. It is to be noted that the longer vectors forming the left and right hand sides of the character "A" are traced in a longer time interval than the shorter vectors. These time intervals are chosen so that the rate of beam movement on the CRT screen is constant for all vectors. Therefore, the intensity of each vector is the same, and the character as displayed appears to be of uniform brightness.

After the CRT beam traces a vector to the last end point defining a character, for example, the coordinate point 5, 9 for the character "A," the toggle detect signal (FIG. 4g) will cause the read-only memory 19 to output the next set of parameters stored in sequence. This set defines the starting point for a new character and the Z parameter thereof will have the value 7. The decoder 43 detects this Z parameter and signals the control logic 33 so that it will begin a control sequence for the next character by loading the next data word into the input register 13. The signal from the decoder 43 which indicates that a 7 has been detected is shown in FIG. 4h. The control logic 33 contains suitable logic and timing circuitry responsive to the toggle detect signal and the seven detect signal so that the next character is requested only when $Z=7$ is detected after the character tracing is in progress. Thus, after a new character has been loaded into register 13, the first seven which appears in the Z register circuit 45 will be ignored, but the second seven will cause the control logic 33 to request the next character.

We claim:

1. Apparatus responsive to digital codes representative of characters for controlling a cathode ray tube to display said characters in a predetermined coordinate system, said apparatus comprising:

programming means including digital memory for providing in sequence a plurality of sets of first, second and third digital parameters in response to each of said character codes, said first and second parameters defining end points of each of the vectors forming a character and said third parameter defining the time interval during which each vector between said end points is to be traced by the beam to said cathode ray tube;

first and second circuit means respectively responsive to said first and second digital parameters from said programming means for providing signals to deflect the beam of said cathode ray tube, each of said first and second circuit means including:

a digital to analog converter;

first and second register means for alternately storing successive digital parameters provided in sequence by said programming means;

means for coupling the digital input of said digital to analog converter to one or the other of said register means; and

means for controlling the coupling means of said first and second circuit means to transfer the digital inputs of said digital to analog converters simultaneously and gradually from one to the other of the corresponding first and second register means according to a time transfer function determined in response to said third parameter from said programming means;

whereby the outputs of said digital to analog converters produce deflection signals for tracing vectors during selected time intervals between end points which are stored in succession in said first and second register means and provided in a predetermined sequence by said programming means thereby to generate characters.

2. The apparatus of claim 1 wherein the coupling means of said first and second circuit means each includes a pair of variably conducting means coupled respectively from the corresponding first and second register means to the digital input of the corresponding digital to analog converter.

3. The apparatus of claim 2 wherein said means for controlling said coupling means includes:

generator means providing two predetermined waveforms coupled to the pair of variably conducting means in each of said first and second circuit means for causing complementary conduction of the variably conducting means of each pair between conducting and non-conducting states; and

means for adjusting said two waveforms in response to said third digital parameter from said programming means to thereby vary the rate of change of said variably conducting means between said conducting and non-conducting states.

4. The apparatus of claim 3

said two predetermined waveforms being ramp signals having opposite polarity slopes; and

said adjusting means being operable to vary the slopes of said ramp signals.

5. The apparatus of claim 3 wherein said generator means includes:

two capacitors each having an output terminal for providing one of said two predetermined waveforms;

means providing a current source;

means providing a current sink;

switching means operable alternately in first and second modes for selectively coupling said two capacitors to said current source and said current sink, said first mode being operable to charge one of said capacitors and discharge the other of said capacitors, said second mode being operable to discharge said one capacitor and charge said other capacitor.

6. The apparatus of claim 5,

said means providing a current source including a plurality of incremental current sources; and

said adjusting means including switching means responsive to said third parameter for coupling said incremental current source to said two capacitors to simultaneously charge one capacitor and discharge the other capacitor at the same rate.

7. The apparatus of claim 1 wherein in each of said first and second circuit means;

said digital to analog converter includes:

a weighted resistance network having a plurality of intermediate input tap points and an output providing analog signals;

a plurality of current sources connectable respectively to the tap points of said resistance network;

said first and second register means each includes switch means for conducting current from selected ones of said current sources to the corresponding tap points of said resistance network in response to said digital parameters;

said coupling means includes a plurality of differentially conducting means corresponding respectively to said current sources, each of said differentially conducting means having first and second main current carrying paths for respectively coupling the corresponding one of said current sources to said first and second register means.

8. The apparatus of claim 7,

said plurality of differentially conducting means of said coupling means each having first and second gate control inputs for controlling current conduction through said first and second main current carrying paths, respectively; and

said means for controlling said coupling means including signal generating means providing waveforms to said first and second gate control inputs for causing complementa-

ry current conduction through said first and second main current carrying paths between conducting and non-conducting states.

9. The apparatus of claim 8, wherein said last named controlling means further includes means responsive to said third parameter for adjusting the waveforms applied to said first and second gate control inputs to thereby control the time interval during which current conduction through said first and second main current carrying paths changes from one to the other of said conducting and non-conducting states.

10. The apparatus of claim 7, wherein said plurality of current sources each provide the same magnitude of output current.

11. A system responsive to digital codes representative of characters for controlling a cathode ray tube to display said characters on the screen thereof, said system comprising:

programming means including a digital memory for providing in sequence a plurality of sets of first, second and third digital parameters in response to each of said character codes, said first and second parameters having values defining end points of vectors forming a character and said third parameter having values defining the time interval during which vectors between said end points are to be traced by the beam of said cathode ray tube;

register means for storing the first and second digital parameters of the last two sets of parameters provided in sequence by said programming means, said register means being updated with each succeeding set of parameters provided by said programming means;

digital to analog converter means responsive to said first and second digital parameters for providing deflection signals to position the beam of said cathode ray tube;

means synchronized with said programming means for repeatedly transferring the digital inputs of said digital to analog converter means from the pair of first and second parameters in one set to the pair of first and second parameters in the next succeeding set of parameters stored in said register means, said transferring means being operable to effect a transfer according to a time function selected in response to the third parameter in said next succeeding set;

said transferring means including:

variably conducting means for coupling the digital inputs of said digital to analog converter means from one to the other of the succeeding pairs of first and second digital parameters stored in said register means;

generator means providing a signal having a predetermined waveform for gradually changing the conduction of said variably conducting means;

means for adjusting said waveform in response to said third parameter from said programming means to vary the rate of change of conduction of variably conducting means;

whereby said digital to analog converter means produces deflection signals for tracing vectors of controlled intensity between successive end points which are stored in said register means and provided in a predetermined sequence by said programming means thereby to form characters.

12. The apparatus of claim 11, further including means responsive to selected values of said third parameter for selectively blanking the beam of said cathode ray tube during operation of said transferring means, thereby to inhibit display of selected vectors traced during the formation of a character.

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UNITED STATES PATENT OFFICE
CERTIFICATE OF CORRECTION

Patent No. 3,660,833 Dated May 2, 1972

Inventor(s) Walter T. Blejwas, Jr. et al

It is certified that error appears in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Column 2, line 24, "3a-C" should read -- 3a-c --;
line 57, "E" should read -- E_x --; line 61, "E" should read -- E_y --; line 74, "X register" should read -- X_a register --;
line 75, "X register" should read -- X_b register --;

Column 4, line 40, "shaft" should read -- shift --;

Column 5, line 9, "85," should read -- 85. --;

Column 8, line 35, after "including" insert -- a --;
lines 60-61, after "time transfer function" insert -- , the duration of which is --;

Column 9, line 39, "means;" should read -- means: --.

Signed and sealed this 5th day of September 1972.

(SEAL)

Attest:

EDWARD M. FLETCHER, JR.
Attesting Officer

ROBERT GOTTSCHALK
Commissioner of Patents

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