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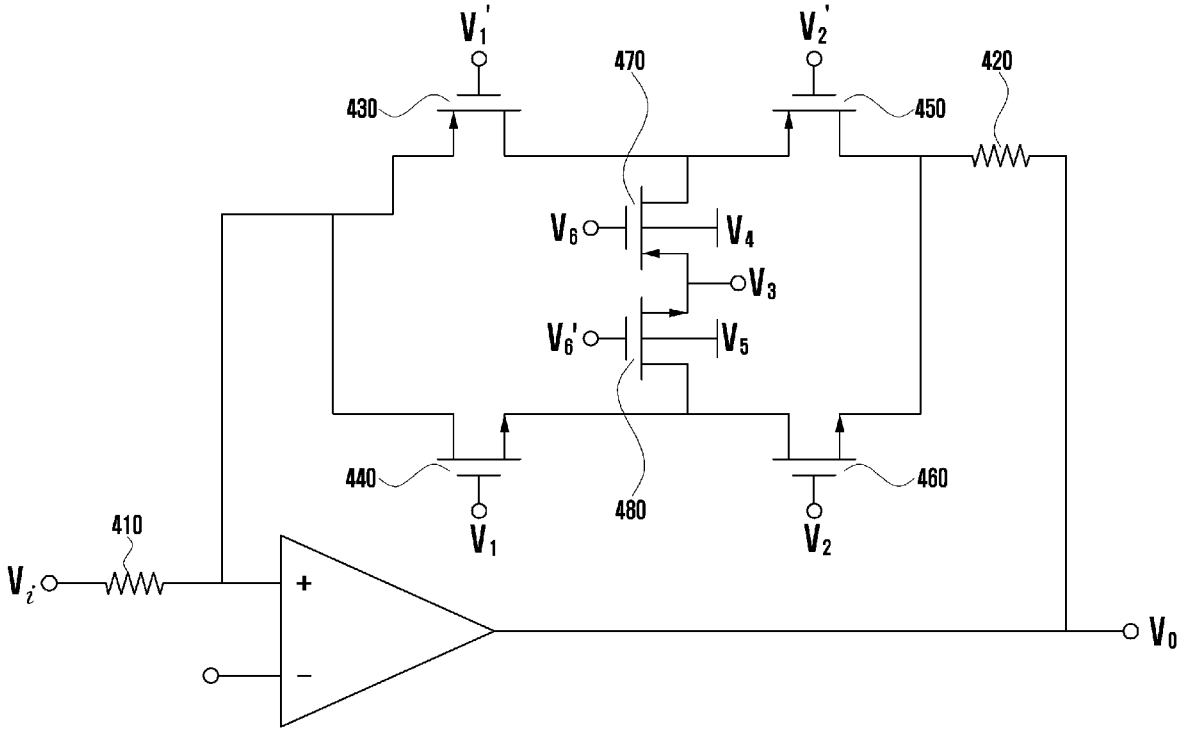
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(54) Title: AMPLIFIER HAVING SWITCH AND SWITCH CONTROL PROCESSOR CONTROLLING SWITCH



(57) Abstract: The present disclosure relates to a pre-5th-Generation (5G) or 5G communication system to be provided for supporting higher data rates Beyond 4th-Generation (4G) communication system such as Long Term Evolution (LTE). An amplifier is provided. The amplifier includes a first resistor electrically connected to the input terminal, a second resistor electrically connected to the output terminal, a switch including a metal-oxide-semiconductor field-effect transistor (MOSFET) and electrically connected to one end of the second resistor, and a switch control processor configured to electrically connect the gate terminal of the MOSFET constituting the switch and the bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

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Description

Title of Invention: AMPLIFIER HAVING SWITCH AND SWITCH CONTROL PROCESSOR CONTROLLING SWITCH

Technical Field

[1] The disclosure relates to an amplifier that includes a plurality of switches and a switch control circuit to thereby adjust the gain.

Background Art

[2] Since the commercial deployment of 4th generation (4G) communication systems, efforts have been made to develop improved 5th generation (5G) or pre-5G communication systems to meet the ever increasing demand for wireless data traffic. As such, 5G or pre-5G communication systems are also called "beyond 4G network" or "post long term evolution (LTE) system." To achieve higher data rates, 5G communication systems consider utilization of the mmWave band (e.g., 60 GHz band). To decrease path loss and increase the transmission distance in the mmWave band, various technologies including beamforming, massive multiple-input multiple-output (massive MIMO), full dimensional MIMO (FD-MIMO), array antennas, analog beamforming, and large scale antennas are considered for 5G communication systems. To improve system networks in 5G communication systems, technology development is under way regarding evolved small cells, advanced small cells, cloud radio access networks (cloud RANs), ultra-dense networks, device-to-device (D2D) communication, wireless backhaul, moving networks, cooperative communication, coordinated multi-points (CoMP), reception interference cancellation, and the like. In addition, advanced coding and modulation (ACM) schemes such as hybrid frequency shift keying (FSK) and quadrature amplitude modulation (QAM) (FQAM) and sliding window superposition coding (SWSC), and advanced access technologies such as filter bank multi carrier (FBMC), non-orthogonal multiple access (NOMA), and sparse code multiple access (SCMA) are also under development for 5G communication systems.

[3] Meanwhile, the Internet is evolving from a human centered network where humans create and consume information into the Internet of Things (IoT) where distributed elements or things process and exchange information. There has also emerged the Internet of Everything (IoE) technology that combines IoT technology with big data processing technology through connection with cloud servers. To realize IoT services, base technologies related to sensing, wired/wireless communication and network infrastructure, service interfacing, and security are needed, and technologies interconnecting things such as sensor networks, machine-to-machine (M2M) or machine type communication (MTC) are under development. In IoT environments, it is possible

to provide intelligent Internet technology services, which collect and analyze data created by interconnected things to add new values to human life. Through convergence and combination between existing information technologies and various field technologies, IoT technology may be applied to various areas such as smart homes, smart buildings, smart cities, smart or connected cars, smart grids, health-care, smart consumer electronics, and advanced medical services.

[4] Accordingly, various attempts are being made to apply 5G communication systems to IoT networks. For example, sensor networks and machine-to-machine or machine type communication are being realized by use of 5G communication technologies including beamforming, MIMO, and array antennas. Application of cloud RANs to big data processing described above may be an instance of convergence of 5G communication technology and IoT technology.

[5] The above information is presented as background information only to assist with an understanding of the disclosure. No determination has been made, and no assertion is made, as to whether any of the above might be applicable as prior art with regard to the disclosure.

Disclosure of Invention

Technical Problem

[6] Aspects of the disclosure are to address at least the above-mentioned problems and/or disadvantages and to provide at least the advantages described below. Accordingly, an aspect of the disclosure is to provide an apparatus to change the gain of an amplifier including a resistor element. A plurality of switches may be required, and each switch may be implemented using a metal-oxide-semiconductor field-effect transistor (MOSFET). Meanwhile, in a 5G mobile communication system using the mmWave band, the performance (e.g., gain or bandwidth) of the amplifier may be reduced due to parasitic capacitance components caused by the MOSFETs. Accordingly, there is a need for an amplifier structure that can solve this problem.

Solution to Problem

[7] Additional aspects will be set forth in part in the description which follows and, in part, will be apparent from the description, or may be learned by practice of the presented embodiments.

[8] In accordance with an aspect of the disclosure, an amplifier is provided. The amplifier includes a first resistor electrically connected to the input terminal, a second resistor electrically connected to the output terminal, a switch including a MOSFET and electrically connected to one end of the second resistor, and a switch control processor configured to electrically connect the gate terminal of the MOSFET constituting the switch and the bulk terminal of the MOSFET constituting the switch to an

impedance having an impedance value higher than a preset first threshold.

[9] In accordance with another aspect of the disclosure, an electronic device having an amplifier is provided. The amplifier includes a first resistor electrically connected to the input terminal, a second resistor electrically connected to the output terminal, a switch including a MOSFET and electrically connected to one end of the second resistor, and a switch control processor configured to electrically connect the gate terminal of the MOSFET constituting the switch and the bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

[10] Other aspects, advantages, and salient features of the disclosure will become apparent to those skilled in the art from the following detailed description, which, taken in conjunction with the annexed drawings, discloses various embodiments of the disclosure.

Advantageous Effects of Invention

[11] According to an embodiment of the disclosure, it is possible to prevent reduction of the gain of the amplifier due to the parasitic capacitance caused by the MOSFET constituting the switch. In addition, it is possible to prevent reduction of the bandwidth of the amplifier due to the Miller effect.

Brief Description of Drawings

[12] The above and other aspects, features and advantages of certain embodiments of the disclosure will be more apparent from the following description, taken in conjunction with the accompanying drawings, in which:

[13] FIG. 1A shows the structure of an amplifier according to the related art;

[14] FIG. 1B shows a switch control processor for controlling the switch of an amplifier according to the related art;

[15] FIG. 2A shows a switch control processor according to an embodiment of the disclosure;

[16] FIG. 2B illustrates an amplifier according to an embodiment of the disclosure;

[17] FIG. 3A illustrates an amplifier including a two-stage switch and a short-circuit switch according to an embodiment of the disclosure;

[18] FIG. 3B illustrates a switch control processor for controlling the two-stage switch and the short-circuit switch according to an embodiment of the disclosure;

[19] FIG. 4 illustrates a case where the short-circuit switch includes a p-type metal-oxide-semiconductor (PMOS) and an n-type metal-oxide-semiconductor (NMOS) according to an embodiment of the disclosure; and

[20] FIG. 5 illustrates a variable gain amplifier according to an embodiment of the disclosure.

[21] Throughout the drawings, like reference numerals will be understood to refer to like

parts, components, and structures.

Mode for the Invention

[22] The following description with reference to the accompanying drawings is provided to assist in a comprehensive understanding of various embodiments of the disclosure as defined by the claims and their equivalents. It includes various specific details to assist in that understanding but these are to be regarded as merely exemplary. Accordingly, those of ordinary skill in the art will recognize that various changes and modifications of the various embodiments described herein can be made without departing from the scope and spirit of the disclosure. In addition, descriptions of well-known functions and constructions may be omitted for clarity and conciseness.

[23] The terms and words used in the following description and claims are not limited to the bibliographical meanings, but, are merely used by the inventor to enable a clear and consistent understanding of the disclosure. Accordingly, it should be apparent to those skilled in the art that the following description of various embodiments of the disclosure is provided for illustration purpose only and not for the purpose of limiting the disclosure as defined by the appended claims and their equivalents.

[24] It is to be understood that the singular forms "a," "an," and "the" include plural referents unless the context clearly dictates otherwise. Thus, for example, reference to "a component surface" includes reference to one or more of such surfaces.

[25] In the drawings, some elements are exaggerated, omitted, or only outlined in brief, and thus may be not drawn to scale. The same or similar reference symbols are used throughout the drawings to refer to the same or like parts.

[26] The aspects, features, and advantages of certain embodiments of the disclosure will be more apparent from the following detailed description taken in conjunction with the accompanying drawings. The description of the various embodiments is to be construed as exemplary only and does not describe every possible instance of the disclosure. It should be apparent to those skilled in the art that the following description of various embodiments of the disclosure is provided for illustrative purposes only and not for the purpose of limiting the disclosure as defined by the appended claims and their equivalents. The same reference symbols are used throughout the description to refer to the same parts.

[27] Meanwhile, it is known to those skilled in the art that blocks of a flowchart (or sequence diagram) and a combination of flowcharts may be represented and executed by computer program instructions. These computer program instructions may be loaded on a processor of a general purpose computer, special purpose computer, or programmable data processing equipment. When the loaded program instructions are executed by the processor, they create a means for carrying out functions described in

the flowchart. As the computer program instructions may be stored in a computer readable memory that is usable in a specialized computer or a programmable data processing equipment, it is also possible to create articles of manufacture that carry out functions described in the flowchart. As the computer program instructions may be loaded on a computer or a programmable data processing equipment, when executed as processes, they may carry out operations of functions described in the flowchart.

[28] A block of a flowchart may correspond to a module, a segment or a code containing one or more executable instructions implementing one or more logical functions, or to a part thereof. In some cases, functions described by blocks may be executed in an order different from the listed order. For example, two blocks listed in sequence may be executed at the same time or executed in reverse order.

[29] In the description, the word "unit," "module," or the like may refer to a software component or hardware component such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) capable of carrying out a function or an operation. However, "unit" or the like is not limited to hardware or software. A unit or the like may be configured so as to reside in an addressable storage medium or to drive one or more processors. Units or the like may refer to software components, object-oriented software components, class components, task components, processes, functions, attributes, procedures, subroutines, program code segments, drivers, firmware, microcode, circuits, data, databases, data structures, tables, arrays, or variables. A function provided by a component and unit may be a combination of smaller components and units, and it may be combined with others to compose large components and units. Components and units may be configured to drive a device or one or more processors in a secure multimedia card. In a certain embodiment, a unit or the like may include at least one processor.

[30] FIG. 1A shows the structure of an amplifier according to the related art.

[31] Referring to FIG. 1A, in the related art, the amplifier may include a first resistor 110 connected to the input terminal and a second resistor 120 connected to the output terminal. The input signal Vi input to the input terminal may be amplified through the first resistor 110 and the second resistor 120 and appear as an output signal Vo at the output terminal. The gain of the amplifier may be determined based on the ratio between the resistance value of the first resistor 110 and the resistance value of the second resistor 120.

[32] In the related art, a switch may be electrically connected to one end of the second resistor 120 to turn the amplifier on or off or to change the gain of the amplifier. This switch may be implemented using a complementary metal-oxide semiconductor (CMOS) in which a p-type metal-oxide-semiconductor (PMOS) 130 and an n-type metal-oxide-semiconductor (NMOS) 140 are combined.

[33] According to the related art, when V_1 is higher than the threshold voltage of the metal-oxide-semiconductor field-effect transistor (MOSFET), both the PMOS 130 and the NMOS 140 may be turned on. When V_1 is lower than the threshold voltage of the MOSFET, both the PMOS 130 and the NMOS 140 may be turned off. That is, turn-on/turn-off control of the switch including the PMOS 130 and the NMOS 140 may be achieved by controlling the V_1 voltage.

[34] FIG. 1B shows a switch control processor for controlling the switch of an amplifier according to the related art.

[35] Referring to FIG. 1B, in the related art, the PMOS may be turned on when the voltage applied to the gate terminal is less than the threshold voltage, and the NMOS may be turned on when the voltage applied to the gate terminal exceeds the threshold voltage. Hence, the switch control processor for controlling the switch of the amplifier according to the related art may be configured as shown in FIG. 2B.

[36] In the related art, the first inverter 150 may receive an input signal V_1 as input to the switch control processor and produce an output signal V_1'. The signal V_1' output by the first inverter 150 may be supplied to the gate terminal of the PMOS constituting the switch. The signal V_1' output by the first inverter 150 may be input to the second inverter 160, and the second inverter 160 may produce an output signal V_1. The signal V_1 output by the second inverter 160 may be supplied to the gate terminal of the NMOS constituting the switch.

[37] In the related art, due to the characteristic of the MOSFETs, parasitic capacitance components may be generated between the gate terminal and the source terminal of the PMOS, between the gate terminal and the drain terminal of the PMOS, between the source terminal and the bulk terminal of the PMOS, and between the drain terminal and the bulk terminal of the PMOS.

[38] According to the related art, when the amplifier operates in a low frequency band, as the impedance of the parasitic capacitance components is sufficiently high, the fundamental signal to be amplified may not flow through the parasitic capacitance even when the switch is turned on. However, when the amplifier operates in a very high frequency band such as the 5G mobile communication system, as the impedance value of the parasitic capacitance components becomes low, the fundamental signal to be amplified may flow through the parasitic capacitance when the switch is turned on. That is, in the related art, as a portion of the fundamental signal to be amplified may not flow to the output terminal of the amplifier but may flow through the parasitic capacitance, the gain of the amplifier can be reduced particularly in a high frequency range.

[39] FIG. 2A shows a switch control processor according to an embodiment of the disclosure.

[40] Referring to FIG. 2A, in one embodiment, the switch control processor may include a first inverter 230 for receiving a control signal V_1, a first CMOS where the gate terminal of the first PMOS 241 and the gate terminal of the first NMOS 242 are electrically connected to the output terminal of the first inverter 230, a second inverter 250 electrically connected to the output terminal of the first inverter 230, a second CMOS where the gate terminal of the second PMOS 251 and the gate terminal of the second NMOS 252 are electrically connected to the output terminal of the second inverter 250, a first impedance 210 electrically connected to the source terminal of the first PMOS 241 and the source terminal of the second PMOS 251 and having an impedance value higher than a first threshold value, and a second impedance 220 electrically connected to the source terminal of the first NMOS 242 and the source terminal of the second NMOS 252 and having an impedance value higher than the first threshold value.

[41] In one embodiment, when the control signal V_1 is set to V_{DD}, the output signal of the first inverter 230 may be zero. When the output signal of the first inverter 230 is 0, the first PMOS 241 may be turned on and the first NMOS 242 may be turned off. When only the first PMOS 241 is turned on, the output signal at the output terminal of the first CMOS may be set to V_{DD}. The output signal from the output terminal of the first CMOS may be used as a control signal for the gate terminal of the NMOS constituting the switch. That is, when V_1 is set to V_{DD}, as the control signal supplied to the gate terminal of the NMOS constituting the switch is V_{DD}, the NMOS may be turned on.

[42] In one embodiment, when the NMOS constituting the switch is turned on, the gate terminal of the NMOS may be electrically connected to the first impedance 210 having an impedance value higher than the first threshold value. In various embodiments, the first impedance 210 may include a resistor and an inductor.

[43] In one embodiment, the first impedance 210 having a high impedance value may prevent a current from flowing through the parasitic capacitance between the gate terminal and the source terminal of the NMOS constituting the switch and through the parasitic capacitance between the gate terminal and the drain terminal of the NMOS constituting the switch. (The blocking effect of the current flowing through the parasitic capacitance will be described later with reference to FIG. 2B.)

[44] In one embodiment, when the output signal from the first inverter 230 is 0, the output signal from the second inverter 250 may be V_{DD}. When the output signal of the second inverter 250 is V_{DD}, the second PMOS 251 may be turned off and the second NMOS 252 may be turned on. When only the second NMOS 252 is turned on, the output signal from the output terminal of the second CMOS may be zero. The output signal from the output terminal of the second CMOS may be used as a control signal for the gate terminal of the PMOS constituting the switch. That is, when V_1 is set to V_{DD}, as the control signal supplied to the gate terminal of the NMOS constituting the switch is

0, the PMOS may be turned on.

[45] In one embodiment, when the PMOS constituting the switch is turned on, the gate terminal of the PMOS may be electrically connected to the second impedance 220 having an impedance value higher than the first threshold value. In various embodiments, the second impedance 220 may include a resistor and an inductor.

[46] In one embodiment, the second impedance 220 having a high impedance value may prevent a current from flowing through the parasitic capacitance between the gate terminal and the source terminal of the PMOS constituting the switch and through the parasitic capacitance between the gate terminal and the drain terminal of the PMOS constituting the switch.

[47] In one embodiment, the bulk terminal of the PMOS constituting the switch may be electrically connected to the source terminal of the first PMOS 241 or the source terminal of the second PMOS 251. The bulk terminal of the PMOS constituting the switch may be electrically connected to the first impedance 210. Hence, the first impedance 210 may prevent a current from flowing through the parasitic capacitance between the bulk terminal and the source terminal of the PMOS constituting the switch and through the parasitic capacitance between the bulk terminal and the drain terminal of the PMOS constituting the switch.

[48] In one embodiment, the bulk terminal of the NMOS constituting the switch may be electrically connected to the source terminal of the first NMOS 242 or the source terminal of the second NMOS 252. The bulk terminal of the NMOS constituting the switch may be electrically connected to the second impedance 220. Hence, the second impedance 220 may prevent a current from flowing through the parasitic capacitance between the bulk terminal and the source terminal of the NMOS constituting the switch and through the parasitic capacitance between the bulk terminal and the drain terminal of the NMOS constituting the switch.

[49] In one embodiment, the bulk terminal of the PMOS constituting the switch may be electrically connected to the V_2 node of the switch control processor, and the bulk terminal of the NMOS constituting the switch may be electrically connected to the V_3 node of the switch control processor.

[50] FIG. 2B illustrates an amplifier according to an embodiment of the disclosure.

[51] More specifically, FIG. 2B illustrates an equivalent circuit when the MOSFET constituting the switch is turned on in the amplifier including the switch control processor shown in FIG. 2A.

[52] Referring to FIG. 2A, the switch is a CMOS including a PMOS and an NMOS. FIG. 2B illustrates a case where the switch includes only one PMOS, to avoid repeated descriptions.

[53] Referring to FIG. 2B, in one embodiment, when the switch is turned on, the source

terminal s and the drain terminal d of the PMOS constituting the switch may be electrically connected through the resistor $R_{sd,on}$. For example, the resistor $R_{sd,on}$ may be generated between the drain terminal and the source terminal when the PMOS is turned on, and may have a low impedance value. Due to the characteristics of the MOSFET, a first parasitic capacitance component C_{gs} may be generated between the gate terminal and the source terminal, a second parasitic capacitance component C_{gd} may be generated between the gate terminal and the drain terminal, a third parasitic capacitance component C_{sb} may be generated between the source terminal and the bulk terminal, and a fourth parasitic capacitance component C_{db} may be generated between the drain terminal and the bulk terminal.

[54] In one embodiment, the higher the operating frequency band of the amplifier, the lower the impedance value of the parasitic capacitance component. When the operating frequency band of the amplifier is sufficiently high such that the impedance value of the parasitic capacitor is less than or equal to a preset threshold, a portion of the fundamental signal to be amplified may flow through the parasitic capacitor. In one embodiment, the fundamental signal may be amplified based on the ratio between the value of a first resistor 235 at the input stage of the amplifier and the value of a second resistor 240 at the output stage of the amplifier.

[55] In one embodiment, a first impedance 210 having a high impedance value may be electrically connected to the bulk terminal of the MOSFET, and a second impedance 220 having a high impedance value may be electrically connected to the gate terminal of the MOSFET. Although current flows through the first parasitic capacitance component C_{gs} and the second parasitic capacitance component C_{gd}, as the second impedance 220 having a high impedance value is connected to the gate terminal of the PMOS constituting the switch, the fundamental signal to be amplified may not flow through the gate terminal. Similarly, although current flows through the third parasitic capacitance component C_{sb} and the fourth parasitic capacitance component C_{db}, as the first impedance 210 having a high impedance value is connected to the bulk terminal of the PMOS constituting the switch, the fundamental signal to be amplified may not flow through the bulk terminal.

[56] In other words, according to an embodiment of the disclosure, the gain of the amplifier may be increased by blocking the current flowing through the parasitic capacitor of the MOSFET constituting the switch by use of the first impedance 210 having a high impedance value and the second impedance 220 having a high impedance value.

[57] In one embodiment, the first impedance 210 and the second impedance 220 may include a resistor or an inductor. When the first impedance 210 and the second impedance 220 comprise a resistor having a high impedance value, the current flowing

through the parasitic capacitor of the MOSFET may be blocked regardless of the operating frequency of the amplifier. When the first impedance 210 and the second impedance 220 comprise an inductor, as the impedance value of the inductor increases with the increasing operating frequency of the amplifier, the current flowing through the parasitic capacitor of the MOSFET can be blocked.

[58] FIG. 3A illustrates an amplifier including a two-stage switch and a short-circuit switch according to an embodiment of the disclosure.

[59] Referring to FIG. 3A, in one embodiment, when increasing the impedance of the gate and bulk terminals of the MOSFETs constituting the switch, the amount of amplifier feedback signal through the switch that is turned off may be increased. That is, the amount of the output signal fed back from the output terminal of the amplifier to the input terminal of the amplifier can increase. When the amount of the amplifier feedback signal increases, the bandwidth of the amplifier may be reduced due to the Miller effect.

[60] In one embodiment, to prevent the bandwidth reduction effect due to the increased feedback signal through the turned-off switch, as shown in FIG. 3A, the switch may be configured in two stages, and a short-circuit switch may be disposed between the two switches. In an embodiment, a two-stage switch may be disposed at the output terminal of the amplifier including a first resistor 310 at the input terminal and a second resistor 315 at the output terminal. In various embodiments, the two-stage switch and the short-circuit switch may be controlled in a suitable manner so that the feedback signal of the amplifier can flow through the short-circuit switch.

[61] In one embodiment, the two-stage switch constituting the amplifier may be configured by connecting a first switch, which includes a first CMOS based on a first PMOS 320 and a first NMOS 330, and a second switch, which includes a second CMOS based on a second PMOS 340 and a second NMOS 350, in series. The first switch and the second switch may operate in a manner identical or similar to that of the switch described with reference to FIG. 1A. For example, when V_1 and V_2 are set to V_{DD}, all of the first PMOS 320, the first NMOS 330, the second PMOS 340, and the second NMOS 350 may be turned on.

[62] In one embodiment, the short-circuit switch connected between the first switch and the second switch may include a third NMOS 361 and a fourth NMOS 362. When the first switch and the second switch are turned on (i.e., when V_1 and V_2 are set to V_{DD}), both the third NMOS 361 and the fourth NMOS 362 may be turned off.

[63] In one embodiment, when the first switch and the second switch are turned off (i.e., when V_1 and V_2 are set to 0), both the third NMOS 361 and the fourth NMOS 362 may be turned on. Even when the first switch and the second switch are turned off, the feedback signal may flow in the amplifier through the parasitic capacitor of the

MOSFET. Most of the feedback signal passing through the second switch may flow to the short-circuit switch having a low impedance value. That is, according to an embodiment of the disclosure, most of the feedback signal passing through the second switch flows through the short-circuit switch, which prevents reduction of the bandwidth of the amplifier due to the feedback signal flowing to the input stage of the amplifier.

[64] FIG. 3B illustrates a switch control processor for controlling the two-stage switch according to an embodiment of the disclosure.

[65] Referring to FIG. 3B, in one embodiment, the switch control processor may be divided into a first switch control processor for controlling the first switch constituting the two-stage switch and a second switch control processor for controlling the second switch. The first switch control processor for controlling the first switch may include a first inverter 371 for receiving a control signal V_I, a first CMOS where the gate terminal of a first PMOS 391 and the gate terminal of a first NMOS 392 are electrically connected to the output terminal of the first inverter 371, a second inverter 372 electrically connected to the output terminal of the first inverter 371, a second CMOS where the gate terminal of a second PMOS 393 and the gate terminal of a second NMOS 394 are electrically connected to the output terminal of the second inverter 372, a first impedance 381 electrically connected to the source terminal of the first PMOS 391 and the source terminal of the second PMOS 393 and having an impedance value higher than a first threshold value, and a second impedance 382 electrically connected to the source terminal of the first NMOS 392 and the source terminal of the second NMOS 394 and having an impedance value higher than the first threshold value.

[66] In one embodiment, when the control signal V_I is set to V_{DD}, the output signal of the first inverter 371 may be zero. When the output signal of the first inverter 371 is 0, the first PMOS 391 may be turned on and the first NMOS 392 may be turned off. When only the first PMOS 391 is turned on, the output signal at the output terminal of the first CMOS may be V_{DD}. The output signal at the output terminal of the first CMOS may be used as a control signal for the gate terminal of the NMOS constituting the switch. That is, when V_I is set to V_{DD}, as the control signal supplied to the gate terminal of the NMOS constituting the switch is V_{DD}, the NMOS may be turned on.

[67] In one embodiment, when the NMOS constituting the switch is turned on, the gate terminal of the NMOS may be electrically connected to the first impedance 381 having an impedance value higher than the first threshold value. The first impedance 381 may include a resistor and an inductor.

[68] In one embodiment, when the output signal of the first inverter 371 is set to 0, the output signal of the second inverter 372 may be V_{DD}. When the output signal of the second inverter 372 is V_{DD}, the second PMOS 393 may be turned off and the second

NMOS 394 may be turned on. When only the second NMOS 394 is turned on, the output signal at the output terminal of the second CMOS may be zero. The output signal at the output terminal of the second CMOS may be used as a control signal for the gate terminal of the PMOS constituting the switch. That is, when V_1 is set to V_{DD}, as the control signal supplied to the gate terminal of the NMOS constituting the switch is 0, the PMOS may be turned on.

[69] In one embodiment, when the PMOS constituting the switch is turned on, the gate terminal of the PMOS may be electrically connected to the second impedance 382 having an impedance value higher than the first threshold value. The second impedance 382 may include a resistor and an inductor.

[70] In one embodiment, the bulk terminal of the PMOS constituting the first switch of the two-stage switch may be electrically connected to the source terminal of the first PMOS 391 or the source terminal (V_3 node) of the second PMOS in the switch control processor, and the bulk terminal of the NMOS constituting the first switch may be electrically connected to the source terminal of the first NMOS 392 or the source terminal (V_4 node) of the second NMOS 394.

[71] In one embodiment, the second switch control processor for controlling the second switch may include a third CMOS where the gate terminal of a third PMOS 395 and the gate terminal of a third NMOS 396 are electrically connected to the output terminal of the first inverter 371, a fourth CMOS where the gate terminal of a fourth PMOS 397 and the gate terminal of a fourth NMOS 398 are electrically connected to the output terminal of the second inverter 372, a third impedance 383 electrically connected to the source terminal of the third PMOS 395 and the source terminal of the fourth PMOS 397 and having an impedance value higher than the first threshold value, and a fourth impedance 384 electrically connected to the source terminal of the third NMOS 396 and the source terminal of the fourth NMOS 398 and having an impedance value higher than the first threshold value. The bulk terminal of the PMOS constituting the second switch may be electrically connected to the source terminal of the third PMOS 395 or the source terminal (V_5 node) of the fourth PMOS 397, and the bulk terminal of the NMOS constituting the second switch may be electrically connected to the source terminal of the third NMOS 396 or the source terminal (V_6 node) of the fourth NMOS 398.

[72] In one embodiment, the operation of the first switch control processor may be the same as or similar to the operation of the switch control processor described with reference to FIG. 2A. The operation of the second switch control processor may be the same as or similar to the operation of the first switch control processor described above.

[73] Meanwhile, the circuit diagrams shown in FIGS. 3A and 3B are only an embodiment

of the disclosure, and the scope of the disclosure should not be limited to the circuit diagrams shown in FIGS. 3A and 3B.

[74] FIG. 4 illustrates a case where the short-circuit switch includes a PMOS and an NMOS according to an embodiment of the disclosure.

[75] Referring to FIG. 4, in one embodiment, a two-stage switch may be disposed at the output terminal of the amplifier including a first resistor 410 at the input terminal and a second resistor 420 at the output terminal. The two-stage switch may include a first switch including a first CMOS based on a first PMOS 430 and a first NMOS 440, and a second switch including a second CMOS based on a second PMOS 450 and a second NMOS 460.

[76] In one embodiment, a short-circuit switch including a third PMOS 470 and a third NMOS 480 may be disposed between the first switch and the second switch. When V_1 and V_2 are set to V_{DD} (i.e., when the first switch and the second switch are turned on), V_6 may be V_{DD}. In other words, when the first switch and the second switch are turned on, both the third PMOS 470 and the third NMOS 480 may be turned off.

[77] In one embodiment, When V_1 and V_2 are set to 0 (i.e., when the first switch and the second switch are turned off), V_6 may be 0. In other words, when the first switch and the second switch are turned off, both the third PMOS 470 and the third NMOS 480 may be turned on. The V_3 node, which is the source terminals of the third PMOS 470 and the third NMOS 480, may have an impedance value lower than a preset threshold. Consequently, most of the feedback signal in the amplifier can flow through the short-circuit switch with a low impedance value.

[78] In one embodiment, the voltage of the bulk terminal of the third PMOS 470 may be set to V_4, and the voltage of the bulk terminal of the third NMOS 480 may be set to V_5. The bulk terminals of the third PMOS and the third NMOS constituting the short-circuit switch may be electrically connected to an impedance having a high impedance value as shown in FIG. 2B.

[79] FIG. 5 illustrates a variable gain amplifier according to an embodiment of the disclosure.

[80] Referring to FIG. 5, in one embodiment, the amplifier may include a first resistor 510 at the input terminal. To vary the gain of the amplifier, a plurality of resistors 521, 522, and 523 may be connected in parallel to the output terminal, and switches 531, 532, and 533 corresponding respectively to the resistors 521, 522, and 523 may be disposed. The gain of the amplifier may be changed by controlling the turning on/off of each switch.

[81] In one embodiment, when the switches 531, 532, and 533 are implemented using MOSFETs, the gain of the amplifier may be reduced due to the parasitic capacitance components of the switches connected in parallel as described above. Accordingly, the

disclosure provides a switch control processor to prevent reduction of the gain of the amplifier due to the switch. The switch and switch control processor of the disclosure may be applied to each of the switches 531, 532 and 533 constituting the amplifier.

[82] In addition, according to the disclosure, when the switch is configured as a two-stage switch in which a first switch and a second switch are connected in series and a short-circuit switch is placed between the first switch and the second switch, it is possible to reduce the amount of the feedback signal through the turned-off switch. Hence, the bandwidth of the amplifier can be increased by reducing the feedback signal that affects the input stage of the amplifier through the turned-off switch.

[83] According to various embodiments of the disclosure, an amplifier may include: a first resistor electrically connected to the input terminal; a second resistor electrically connected to the output terminal; a switch including a MOSFET and electrically connected to one end of the second resistor; and a switch control processor configured to electrically connect the gate terminal of the MOSFET constituting the switch and the bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

[84] In one embodiment, the switch may include a CMOS, and the switch control processor may include: a first impedance electrically connected to the gate terminal and the bulk terminal of the PMOS constituting the CMOS and having an impedance value higher than the first threshold; and a second impedance electrically connected to the gate terminal and the bulk terminal of the NMOS constituting the CMOS and having an impedance value higher than the first threshold.

[85] In one embodiment, the switch control processor may include: a first inverter for receiving a control signal; a first CMOS in which the gate terminal of a first PMOS and the gate terminal of a first NMOS are electrically connected to the output terminal of the first inverter; a second inverter electrically connected to the output terminal of the first inverter; a second CMOS in which the gate terminal of a second PMOS and the gate terminal of a second NMOS are electrically connected to the output terminal of the second inverter; a first impedance electrically connected to the source terminal of the first PMOS and the source terminal of the second PMOS and having an impedance value higher than the first threshold; and a second impedance electrically connected to the source terminal of the first NMOS and the source terminal of the second NMOS and having an impedance value higher than the first threshold.

[86] In one embodiment, the bulk terminal of the PMOS constituting the switch may be electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS, and the bulk terminal of the NMOS constituting the switch may be electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS.

[87] In one embodiment, the gate terminal of the PMOS constituting the switch may be electrically connected to the output terminal of the first CMOS, and the gate terminal of the NMOS constituting the switch may be electrically connected to the output terminal of the second CMOS.

[88] In one embodiment, the switch may include a first switch including a CMOS and electrically connected to one end of the second resistor, and a second switch including a CMOS and electrically connected to one end of the first switch.

[89] In one embodiment, the switch control processor may include: a first inverter for receiving a control signal; a first CMOS in which the gate terminal of a first PMOS and the gate terminal of a first NMOS are electrically connected to the output terminal of the first inverter; a second inverter electrically connected to the output terminal of the first inverter; a second CMOS in which the gate terminal of a second PMOS and the gate terminal of a second NMOS are electrically connected to the output terminal of the second inverter; a first impedance electrically connected to the source terminal of the first PMOS and the source terminal of the second PMOS and having an impedance value higher than the first threshold; a second impedance electrically connected to the source terminal of the first NMOS and the source terminal of the second NMOS and having an impedance value higher than the first threshold; a third CMOS in which the gate terminal of a third PMOS and the gate terminal of a third NMOS are electrically connected to the output terminal of the first inverter; a fourth CMOS in which the gate terminal of a fourth PMOS and the gate terminal of a fourth NMOS are electrically connected to the output terminal of the second inverter; a third impedance electrically connected to the source terminal of the third PMOS and the source terminal of the fourth PMOS and having an impedance value higher than the first threshold; and a fourth impedance electrically connected to the source terminal of the third NMOS and the source terminal of the fourth NMOS and having an impedance value higher than the first threshold.

[90] In one embodiment, the bulk terminal of the PMOS constituting the first switch may be electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS, the bulk terminal of the NMOS constituting the first switch may be electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS, the bulk terminal of the PMOS constituting the second switch may be electrically connected to the source terminal of the third PMOS or the source terminal of the fourth PMOS, and the bulk terminal of the NMOS constituting the second switch may be electrically connected to the source terminal of the third NMOS or the source terminal of the fourth NMOS.

[91] In one embodiment, the amplifier may further include a third switch having an impedance value lower than a preset second threshold between the first switch and the

second switch.

[92] In one embodiment, the third switch may include: a fifth PMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the PMOS constituting the first switch and the PMOS constituting the second switch; and a fifth NMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the NMOS constituting the first switch and the NMOS constituting the second switch.

[93] According to various embodiments of the disclosure, an electronic device may include an amplifier. The amplifier may include: a first resistor electrically connected to the input terminal; a second resistor electrically connected to the output terminal; a switch including a MOSFET and electrically connected to one end of the second resistor; and a switch control processor configured to electrically connect the gate terminal of the MOSFET constituting the switch and the bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

[94] In one embodiment, the switch may include a complementary metal-oxide semiconductor (CMOS), and the switch control processor may include: a first impedance electrically connected to the gate terminal and the bulk terminal of the PMOS constituting the CMOS and having an impedance value higher than the first threshold; and a second impedance electrically connected to the gate terminal and the bulk terminal of the NMOS constituting the CMOS and having an impedance value higher than the first threshold.

[95] In one embodiment, the switch control processor may include: a first inverter for receiving a control signal; a first CMOS in which the gate terminal of a first PMOS and the gate terminal of a first NMOS are electrically connected to the output terminal of the first inverter; a second inverter electrically connected to the output terminal of the first inverter; a second CMOS in which the gate terminal of a second PMOS and the gate terminal of a second NMOS are electrically connected to the output terminal of the second inverter; a first impedance electrically connected to the source terminal of the first PMOS and the source terminal of the second PMOS and having an impedance value higher than the first threshold; and a second impedance electrically connected to the source terminal of the first NMOS and the source terminal of the second NMOS and having an impedance value higher than the first threshold.

[96] In one embodiment, the bulk terminal of the PMOS constituting the switch may be electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS, and the bulk terminal of the NMOS constituting the switch may be electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS.

[97] In one embodiment, the gate terminal of the PMOS constituting the switch may be electrically connected to the output terminal of the first CMOS, and the gate terminal of the NMOS constituting the switch may be electrically connected to the output terminal of the second CMOS.

[98] In one embodiment, the switch may include a first switch including a CMOS and electrically connected to one end of the second resistor, and a second switch including a CMOS and electrically connected to one end of the first switch.

[99] In one embodiment, the switch control processor may include: a first inverter for receiving a control signal; a first CMOS in which the gate terminal of a first PMOS and the gate terminal of a first NMOS are electrically connected to the output terminal of the first inverter; a second inverter electrically connected to the output terminal of the first inverter; a second CMOS in which the gate terminal of a second PMOS and the gate terminal of a second NMOS are electrically connected to the output terminal of the second inverter; a first impedance electrically connected to the source terminal of the first PMOS and the source terminal of the second PMOS and having an impedance value higher than the first threshold; a second impedance electrically connected to the source terminal of the first NMOS and the source terminal of the second NMOS and having an impedance value higher than the first threshold; a third CMOS in which the gate terminal of a third PMOS and the gate terminal of a third NMOS are electrically connected to the output terminal of the first inverter; a fourth CMOS in which the gate terminal of a fourth PMOS and the gate terminal of a fourth NMOS are electrically connected to the output terminal of the second inverter; a third impedance electrically connected to the source terminal of the third PMOS and the source terminal of the fourth PMOS and having an impedance value higher than the first threshold; and a fourth impedance electrically connected to the source terminal of the third NMOS and the source terminal of the fourth NMOS and having an impedance value higher than the first threshold.

[100] In one embodiment, the bulk terminal of the PMOS constituting the first switch may be electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS, the bulk terminal of the NMOS constituting the first switch may be electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS, the bulk terminal of the PMOS constituting the second switch may be electrically connected to the source terminal of the third PMOS or the source terminal of the fourth PMOS, and the bulk terminal of the NMOS constituting the second switch may be electrically connected to the source terminal of the third NMOS or the source terminal of the fourth NMOS.

[101] In one embodiment, the amplifier may further include a third switch having an impedance value lower than a preset second threshold between the first switch and the

second switch.

[102] In one embodiment, the third switch may include: a fifth PMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the PMOS constituting the first switch and the PMOS constituting the second switch; and a fifth NMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the NMOS constituting the first switch and the NMOS constituting the second switch.

[103] While the disclosure has been shown and described with reference to various embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the disclosure as defined by the appended claims and their equivalents.

Claims

[Claim 1] An amplifier for amplifying an input signal, the amplifier comprising:
a first resistor electrically connected to an input terminal;
a second resistor electrically connected to an output terminal;
a switch including a metal-oxide-semiconductor field-effect transistor (MOSFET) and electrically connected to one end of the second resistor; and
a switch control processor configured to electrically connect a gate terminal of the MOSFET constituting the switch and a bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

[Claim 2] The amplifier of claim 1,
wherein the switch comprises a complementary metal-oxide semi-conductor (CMOS), and
wherein the switch control processor comprises:
a first impedance electrically connected to a gate terminal and a bulk terminal of a p-type metal-oxide-semiconductor (PMOS) constituting the CMOS and having an impedance value higher than the first threshold, and
a second impedance electrically connected to a gate terminal and a bulk terminal of an n-type metal-oxide-semiconductor (NMOS) constituting the CMOS and having an impedance value higher than the first threshold.

[Claim 3] The amplifier of claim 2, wherein the switch control processor comprises:
a first inverter configured to receive a control signal;
a first CMOS in which a gate terminal of a first PMOS and a gate terminal of a first NMOS are electrically connected to an output terminal of the first inverter;
a second inverter electrically connected to the output terminal of the first inverter;
a second CMOS in which a gate terminal of a second PMOS and a gate terminal of a second NMOS are electrically connected to an output terminal of the second inverter;
a first impedance electrically connected to a source terminal of the first PMOS and a source terminal of the second PMOS and having an impedance value higher than the first threshold; and

a second impedance electrically connected to a source terminal of the first NMOS and a source terminal of the second NMOS and having an impedance value higher than the first threshold.

[Claim 4] The amplifier of claim 3, wherein the bulk terminal of the PMOS constituting the switch is electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS, and the bulk terminal of the NMOS constituting the switch is electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS.

[Claim 5] The amplifier of claim 3, wherein the gate terminal of the PMOS constituting the switch is electrically connected to an output terminal of the first CMOS, and the gate terminal of the NMOS constituting the switch is electrically connected to an output terminal of the second CMOS.

[Claim 6] The amplifier of claim 1,

wherein the switch comprises: a first switch including a CMOS and electrically connected to one end of the second resistor; and a second switch including a CMOS and electrically connected to one end of the first switch, and

wherein the switch control processor comprises: a first inverter configured to receive a control signal; a first CMOS in which a gate terminal of a first PMOS and a gate terminal of a first NMOS are electrically connected to an output terminal of the first inverter; a second inverter electrically connected to the output terminal of the first inverter; a second CMOS in which a gate terminal of a second PMOS and a gate terminal of a second NMOS are electrically connected to an output terminal of the second inverter; a first impedance electrically connected to a source terminal of the first PMOS and a source terminal of the second PMOS and having an impedance value higher than the first threshold; a second impedance electrically connected to a source terminal of the first NMOS and a source terminal of the second NMOS and having an impedance value higher than the first threshold; a second impedance electrically connected to a source terminal of the first NMOS and a source terminal of the second NMOS and having an impedance value higher than the first threshold; a third CMOS in which a gate terminal of a third PMOS and a gate terminal of a third NMOS are electrically connected to the output terminal of the first inverter; a fourth CMOS in which a gate terminal of a fourth PMOS and a gate terminal of a fourth NMOS are electrically connected to the output

terminal of the second inverter; a third impedance electrically connected to a source terminal of the third PMOS and a source terminal of the fourth PMOS and having an impedance value higher than the first threshold; and a fourth impedance electrically connected to a source terminal of the third NMOS and a source terminal of the fourth NMOS and having an impedance value higher than the first threshold.

[Claim 7] The amplifier of claim 6,
wherein a bulk terminal of a PMOS constituting the first switch is electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS,
wherein a bulk terminal of an NMOS constituting the first switch is electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS,
wherein a bulk terminal of a PMOS constituting the second switch is electrically connected to the source terminal of the third PMOS or the source terminal of the fourth PMOS, and
wherein a bulk terminal of an NMOS constituting the second switch is electrically connected to the source terminal of the third NMOS or the source terminal of the fourth NMOS.

[Claim 8] The amplifier of claim 6, further comprising a third switch having an impedance value lower than a preset second threshold between the first switch and the second switch,
wherein the third switch comprises: a fifth PMOS having an impedance value lower than the second threshold, a drain terminal of the fifth PMOS being electrically connected between the PMOS constituting the first switch and the PMOS constituting the second switch; and a fifth NMOS having an impedance value lower than the second threshold, a drain terminal of the fifth NMOS being electrically connected between the NMOS constituting the first switch and the NMOS constituting the second switch.

[Claim 9] An electronic device including an amplifier, wherein the amplifier comprises:
a first resistor electrically connected to an input terminal;
a second resistor electrically connected to an output terminal;
a switch including a metal-oxide-semiconductor field-effect transistor (MOSFET) and electrically connected to one end of the second resistor; and
a switch control processor configured to electrically connect a gate

terminal of the MOSFET constituting the switch and a bulk terminal of the MOSFET constituting the switch to an impedance having an impedance value higher than a preset first threshold.

[Claim 10] The electronic device of claim 9,
wherein the switch comprises a complementary metal-oxide semiconductor (CMOS),
wherein the switch control processor comprises:
a first impedance electrically connected to a gate terminal and a bulk terminal of a p-type metal-oxide-semiconductor (PMOS) constituting the CMOS and having an impedance value higher than the first threshold; and
a second impedance electrically connected to a gate terminal and a bulk terminal of an n-type metal-oxide-semiconductor (NMOS) constituting the CMOS and having an impedance value higher than the first threshold, and
wherein the switch control processor comprises:
a first inverter configured to receive a control signal;
a first CMOS in which a gate terminal of a first PMOS and a gate terminal of a first NMOS are electrically connected to an output terminal of the first inverter;
a second inverter electrically connected to the output terminal of the first inverter;
a second CMOS in which a gate terminal of a second PMOS and a gate terminal of a second NMOS are electrically connected to an output terminal of the second inverter;
a first impedance electrically connected to a source terminal of the first PMOS and a source terminal of the second PMOS and having an impedance value higher than the first threshold; and
a second impedance electrically connected to a source terminal of the first NMOS and a source terminal of the second NMOS and having an impedance value higher than the first threshold.

[Claim 11] The electronic device of claim 10,
wherein the bulk terminal of the PMOS constituting the switch is electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS,
wherein the bulk terminal of the NMOS constituting the switch is electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS,

wherein the gate terminal of the PMOS constituting the switch is electrically connected to an output terminal of the first CMOS, and
wherein the gate terminal of the NMOS constituting the switch is electrically connected to an output terminal of the second CMOS.

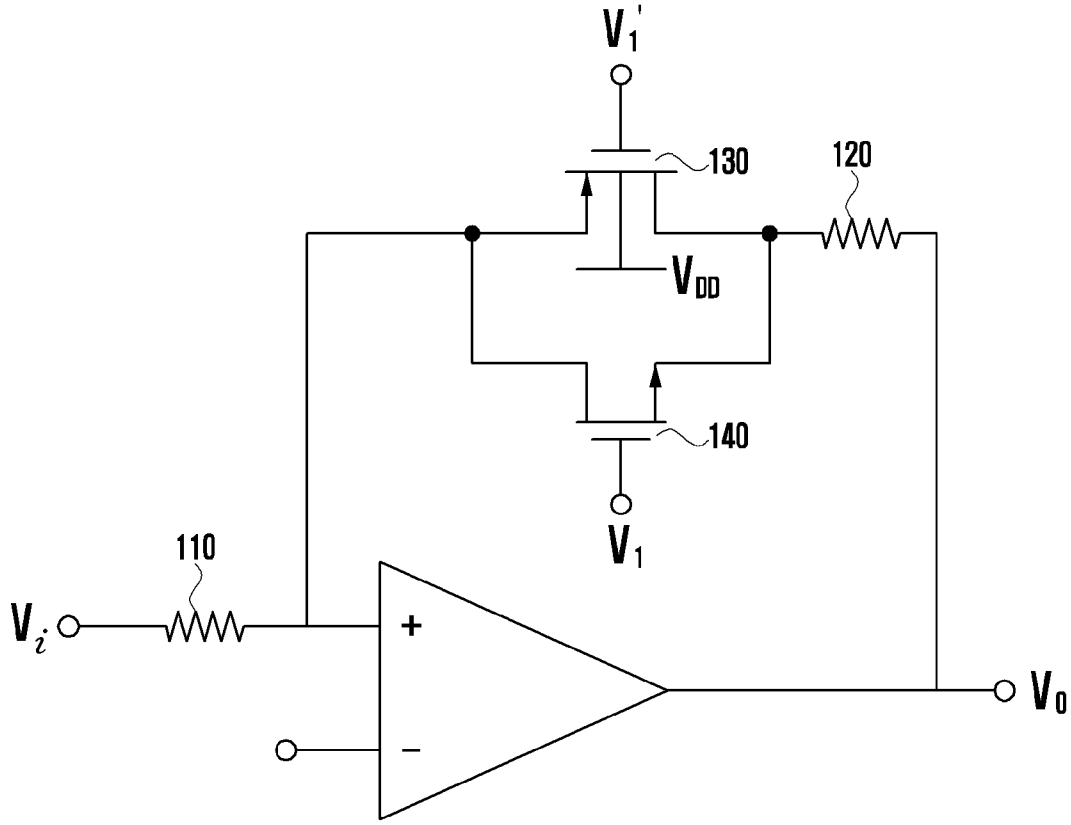
[Claim 12] The electronic device of claim 9, wherein the switch comprises:
a first switch including a CMOS and electrically connected to one end of the second resistor; and
a second switch including a CMOS and electrically connected to one end of the first switch.

[Claim 13] The electronic device of claim 12, wherein the switch control processor comprises:
a first inverter configured to receive a control signal;
a first CMOS in which a gate terminal of a first PMOS and a gate terminal of a first NMOS are electrically connected to an output terminal of the first inverter;
a second inverter electrically connected to the output terminal of the first inverter;
a second CMOS in which a gate terminal of a second PMOS and a gate terminal of a second NMOS are electrically connected to an output terminal of the second inverter;
a first impedance electrically connected to a source terminal of the first PMOS and a source terminal of the second PMOS and having an impedance value higher than the first threshold;
a second impedance electrically connected to a source terminal of the first NMOS and a source terminal of the second NMOS and having an impedance value higher than the first threshold;
a third CMOS in which a gate terminal of a third PMOS and a gate terminal of a third NMOS are electrically connected to the output terminal of the first inverter;
a fourth CMOS in which a gate terminal of a fourth PMOS and a gate terminal of a fourth NMOS are electrically connected to the output terminal of the second inverter;
a third impedance electrically connected to a source terminal of the third PMOS and a source terminal of the fourth PMOS and having an impedance value higher than the first threshold; and
a fourth impedance electrically connected to a source terminal of the third NMOS and a source terminal of the fourth NMOS and having an impedance value higher than the first threshold.

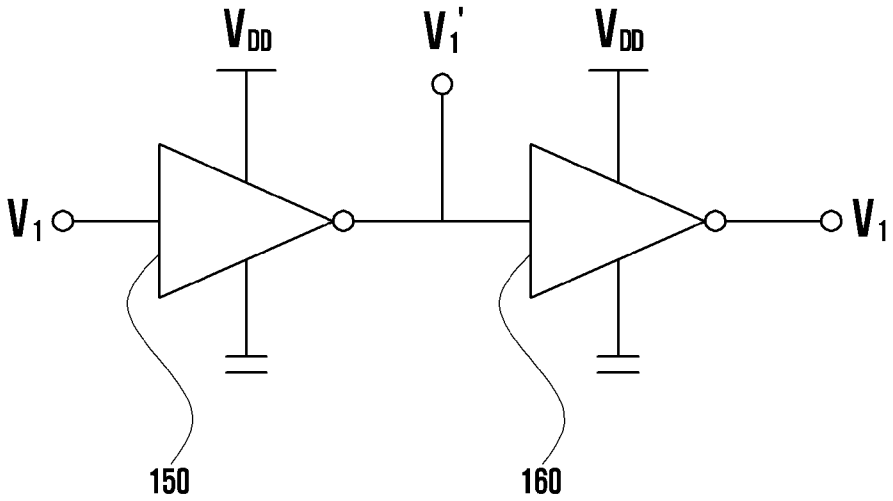
[Claim 14] The electronic device of claim 13,
wherein a bulk terminal of a PMOS constituting the first switch is electrically connected to the source terminal of the first PMOS or the source terminal of the second PMOS,
wherein a bulk terminal of an NMOS constituting the first switch is electrically connected to the source terminal of the first NMOS or the source terminal of the second NMOS,
wherein a bulk terminal of a PMOS constituting the second switch is electrically connected to the source terminal of the third PMOS or the source terminal of the fourth PMOS, and
wherein a bulk terminal of an NMOS constituting the second switch is electrically connected to the source terminal of the third NMOS or the source terminal of the fourth NMOS.

[Claim 15] The electronic device of claim 12,
wherein the amplifier further comprises a third switch having an impedance value lower than a preset second threshold between the first switch and the second switch, and
wherein the third switch comprises:
a fifth PMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the PMOS constituting the first switch and the PMOS constituting the second switch; and
a fifth NMOS having an impedance value lower than the second threshold and whose drain terminal is electrically connected between the NMOS constituting the first switch and the NMOS constituting the second switch.

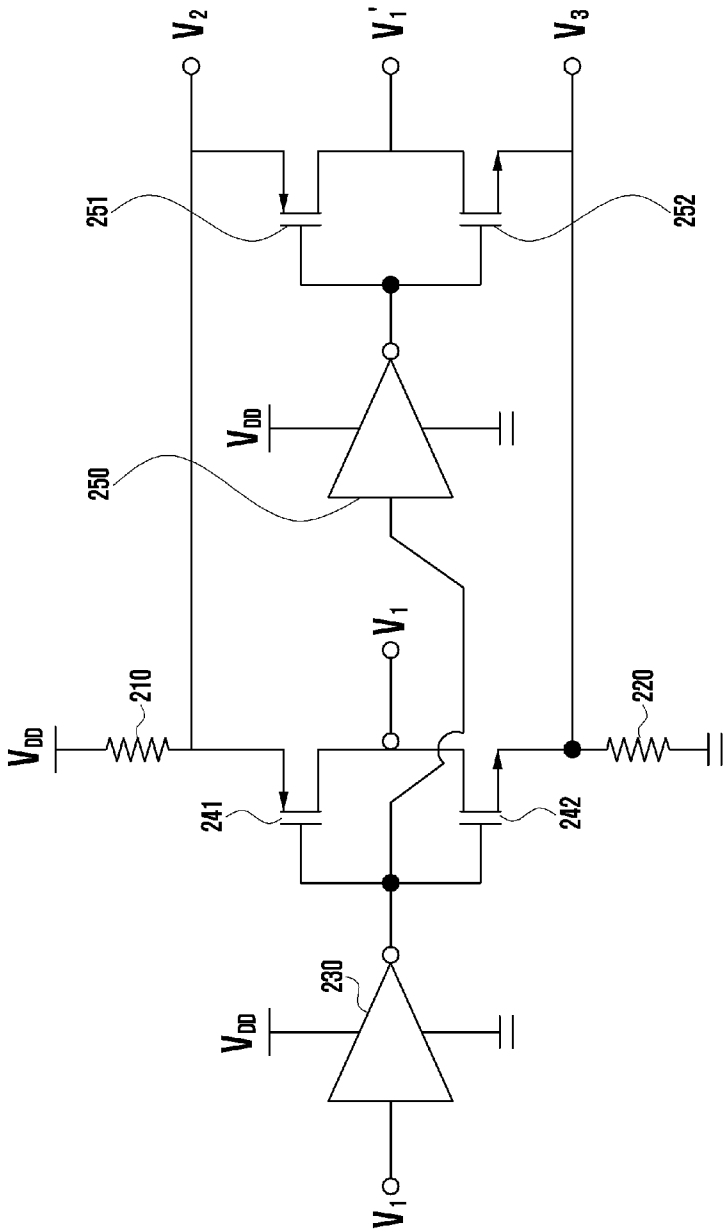
[Fig. 1a]



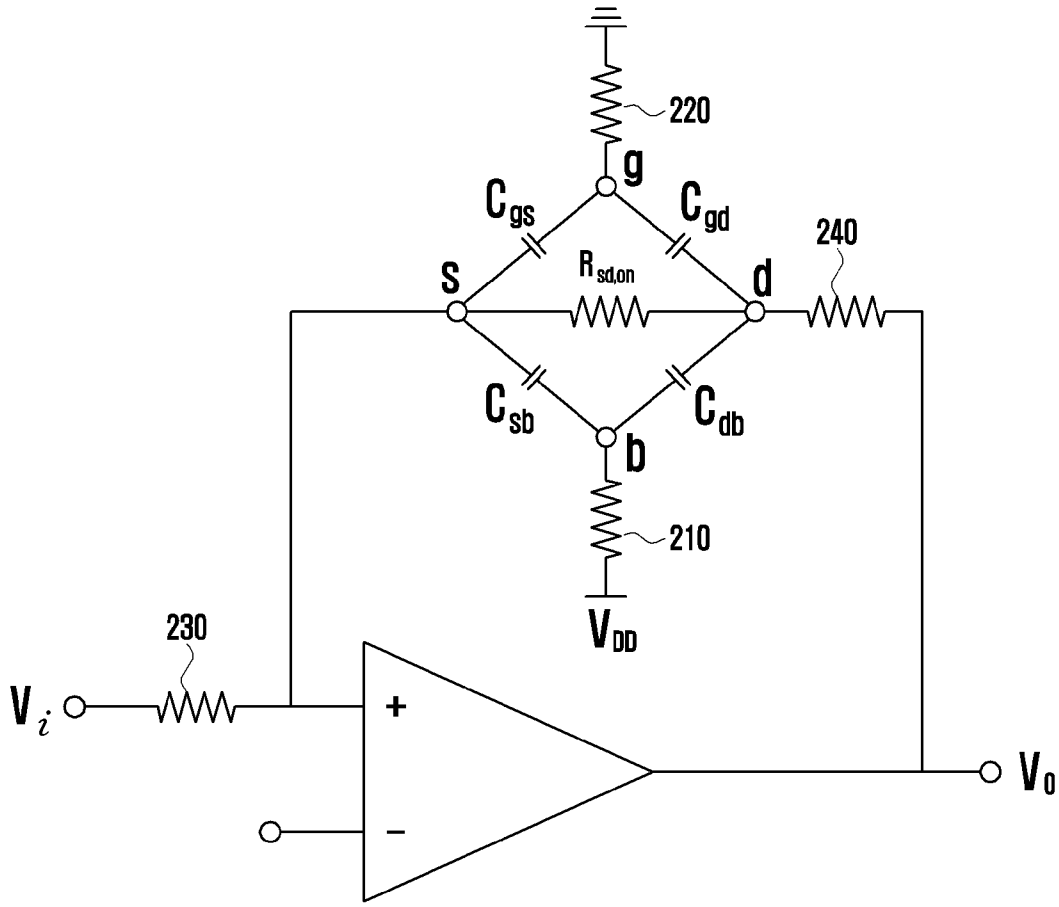
[Fig. 1b]



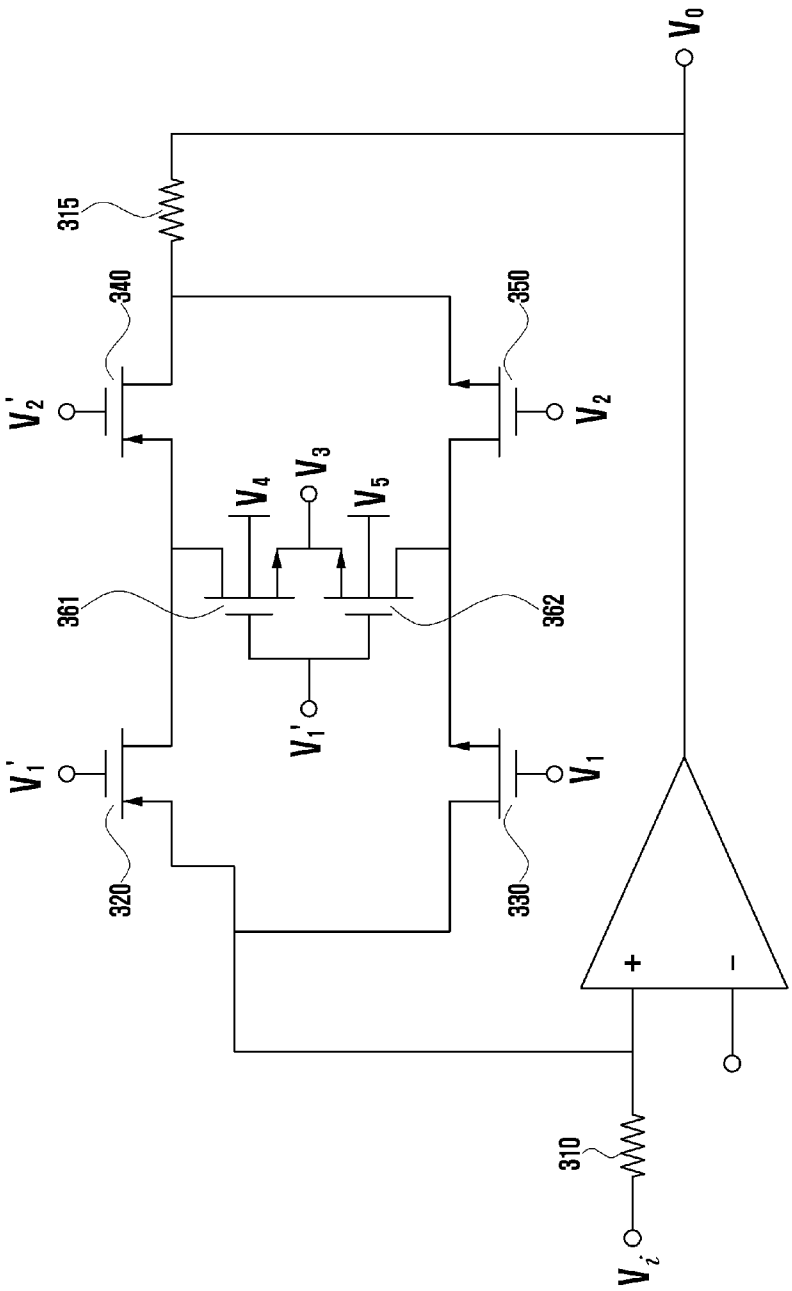
[Fig. 2a]



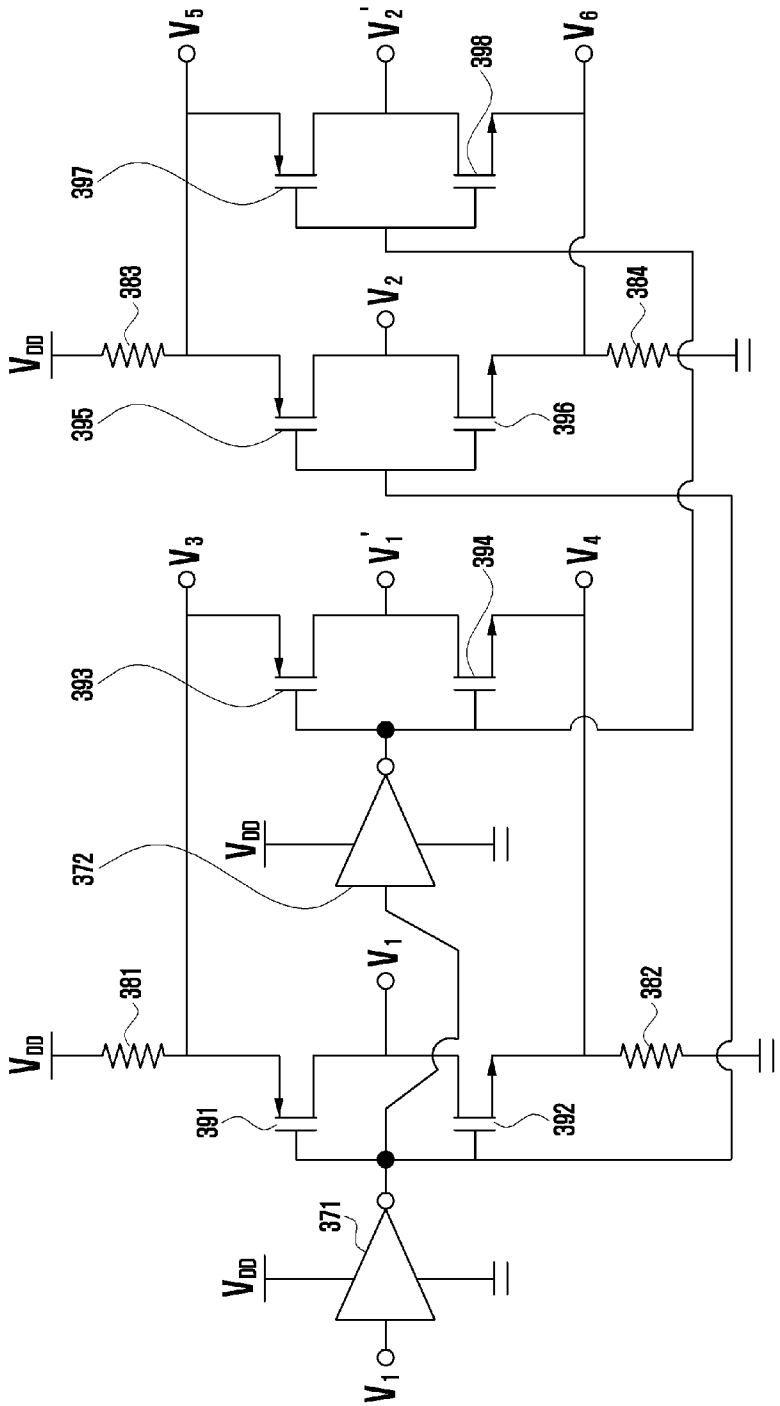
[Fig. 2b]



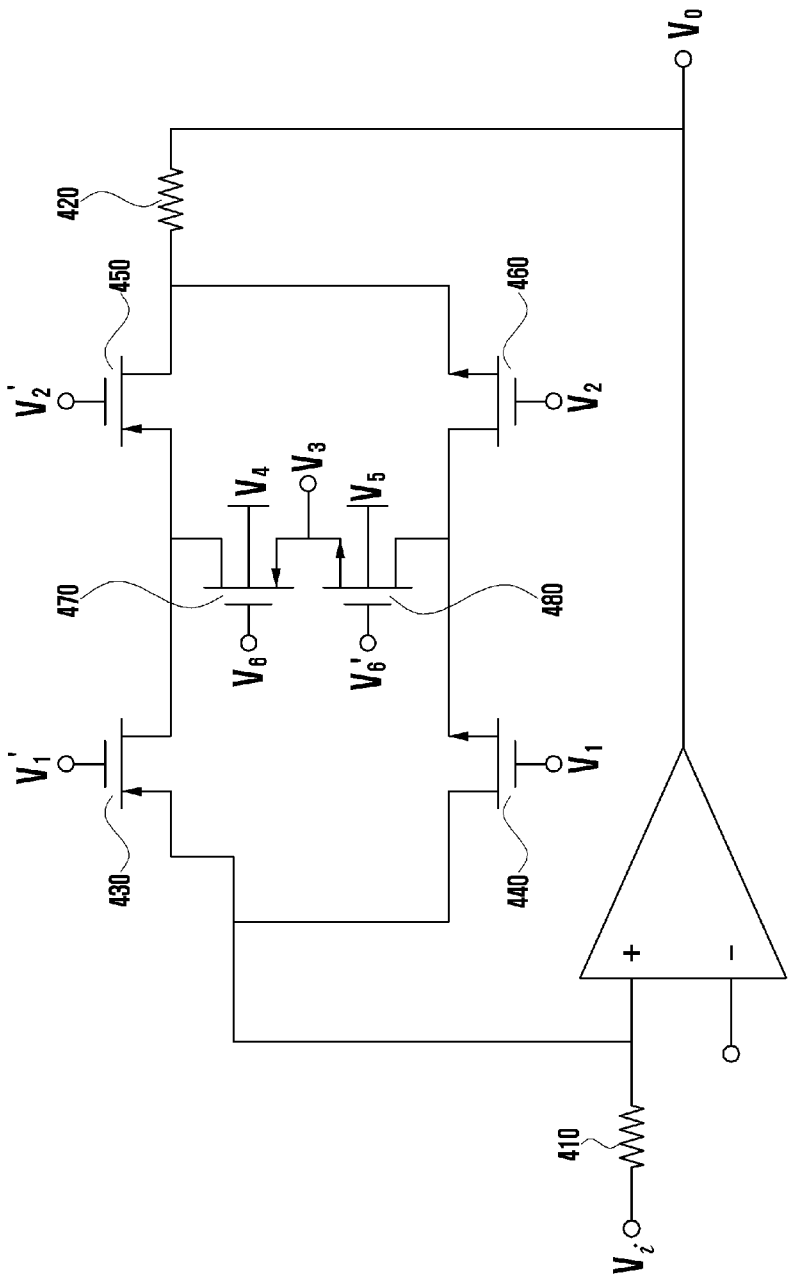
[Fig. 3a]



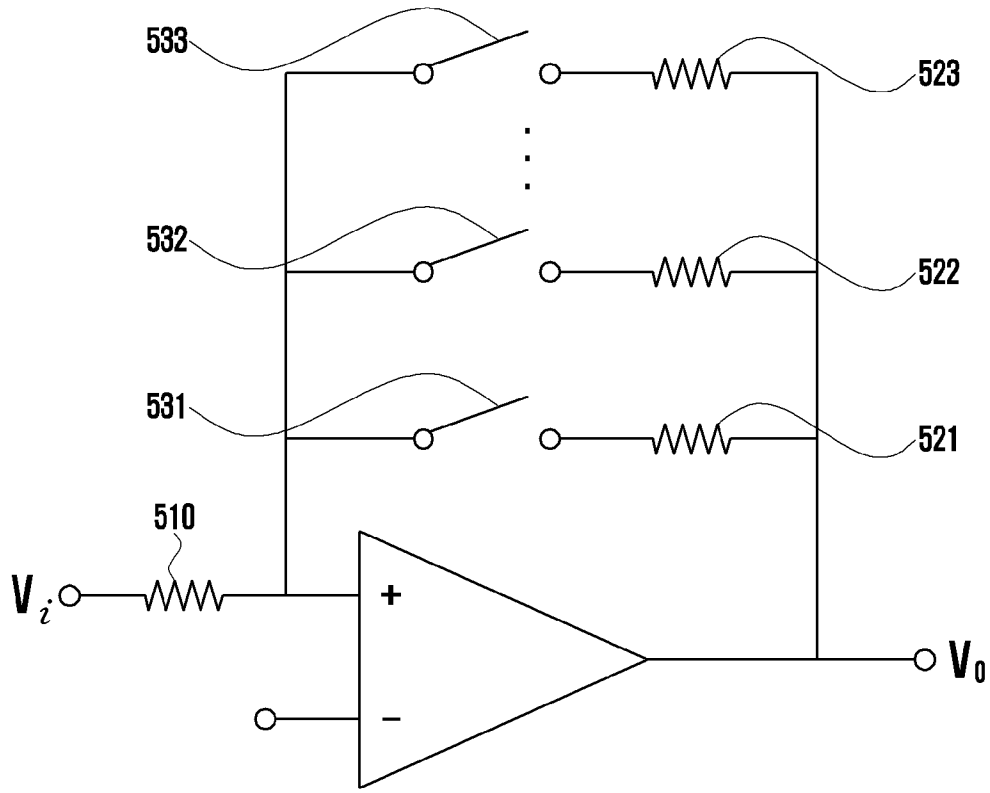
[Fig. 3b]


V5
V2'
398
V6
397
383
V2
384
VDD
395
396
V3
V1'
394
V4
393
372
VDD
V1
381
382
VDD
391
392
371
VDD
V1

[Fig. 4]



[Fig. 5]



INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR2020/001149

A. CLASSIFICATION OF SUBJECT MATTER

H03G 1/00(2006.01)i, H03G 3/30(2006.01)i, H03K 17/687(2006.01)i, H03K 17/693(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H03G 1/00; H03F 1/34; H03G 005/16; H03G 3/00; H03G 3/08; H03G 3/12; H03G 3/30; H03K 17/687; H03K 17/693

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: amplifier, resistor, switch, MOSFET, switch control processor, impedance

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5387879 A (NORITOSHI SATOH) 07 February 1995 See column 2, line 56 - column 4, line 33 and figure 1.	1,9,12
A		2-8,10-11,13-15
A	US 2004-0239421 A1 (WEN-CHI WANG et al.) 02 December 2004 See paragraphs [0018]-[0027] and figures 3-5.	1-15
A	JP 2008-187329 A (SONY CORP.) 14 August 2008 See paragraphs [0031]-[0042] and figure 1.	1-15
A	EP 0774834 B1 (FUJITSU LIMITED) 28 November 2001 See paragraphs [0017]-[0027] and figures 1-5.	1-15
A	US 5369711 A (WILLIAM A. WILLIAMSON, III) 29 November 1994 See column 5, line 40 - column 13, line 18 and figure 2.	1-15

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

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